Silicon based device for smart assessment of cellular stiffness

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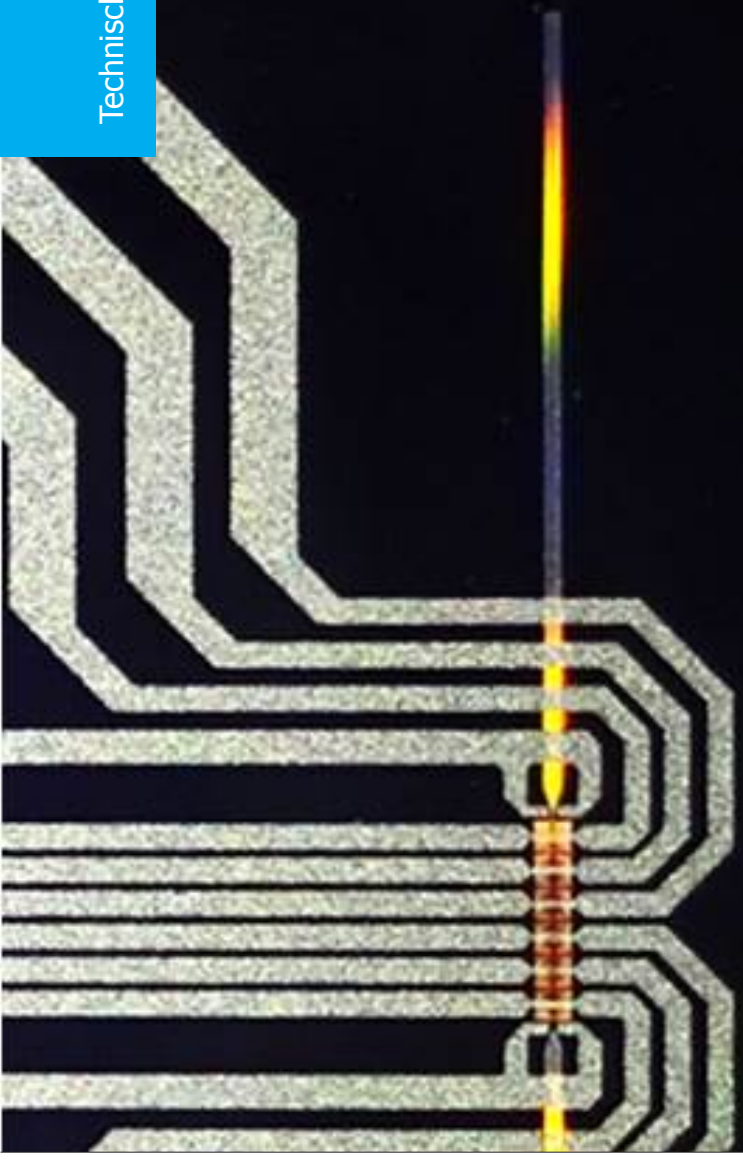

TU Delft Delft University of Technology

Challenge the future

Silicon based device for smart assessment of cellular stiffness

by

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Contents

1

Introduction

In section 1.1 the relation between mechanical deformability and diseases and how it can be used to create a new approach for personalized medicine is explained. In section 1.2 existing methods to measure the cellular stiffness are explained. In section 1.3 the importance of fabricating a device which is simple to used, high throughput and mass producible is described. In section 1.4 the structure of this thesis will be presented.

1.1. Cellular stiffness measurement for diagnostics and personalized medicine

The mechanical properties of a cell are inextricably related to the constituents of the cell, such as the cytoskeleton or the cell membrane and to some lesser degree to the nucleous or the organelles that are inside the cytoplasm [1]. Mechanical changes can occur to these constituents of the cell for various reasons such as, treatment by medicine, cancer and inflammatory response. Even for a healthy individual, cells can change the mechanical deformability. For example, white blood cells can change their mechanical deformability to a more compliant state for easier migration from the blood vessel through the endothelium into the interstitial space [2]. Therefore, measuring the mechanical properties of a cell such as cellular stiffness, is an effective approach to understanding the state of a cell.

Past studies have shown that diseases such as malaria can increase the

cellular stiffness by 10-folds [3]. As a result, red blood cells cannot deform enough when they travel through the capillary blood vessels, lowering the surface area in contact with the endothelial cells, causing less oxygen to be exchanged, leading to symptoms such as necrosis[1]. Other disease such as sepsis, sickle cell and diabetes are also known to alter the cellular stiffness of red blood cells [4]. Other cells have also been studied such as tumor cells. When tumor cells become malignant,[2] it is generally that they become more compliant [5]. By becoming more compliant, malignant cells can migrate through the endothelium into the blood stream more easily to spread into other locations of the body. In this case measuring the stiffness of malignant cells inside the blood stream can serve as a diagnostic technique to understand the stage of cancer.

Various chemicals are used to treat cancer that alters the deformability of the cell. However, some individuals have a higher resistance against these chemical treatments leading to less change in the mechanical deformability of the cells [1]. The efficacy of a drug can be correlated to how much deformation occurs before and after the treatment. In such a case, measuring the change in cellular stiffness for every individuals can lead to a new approach for personalized medicine. In addition, the test must be done for thousands of cells to detect the abnormal cells within a large population of cells. Consequently, a high-throughput system is required for this application.

1.2. Existing methods to measure cellular stiffness

Numerous methods to measure cellular stiffness have been investigated over the past few decades [6]. Table 1.1 summarizes the most common methods used to measure cellular stiffness. In micropipette aspiration (MA) technique, the cell is deformed by aspirating it inside a micropipette and measuring the time it takes to recover to its original shape after the cell is released. This process is modelled including the mechanical properties of the cell (size, youngs modulus, viscosity of the cell membrane) and then the cellular stiffness is derived by fitting a model to the results [7]. In atomic force microscope (AFM) technique, the cell is deformed by a cantilever and again the response is fitted with a particular model and the cellular stiffness is calculated. A major

[1] Form of cell injury which results in the premature death of cells
[2] The state in which the cells can grow uncontrollably. same meaning as cancerous cells

difference in these two methods is that they target different cell types. In the MA method the cell needs to be suspended in a solution, therefore non-adherent cells are favorable such as red blood cells and white blood cells. On the other hand in the AFM method the cell needs to adhere to a substrate. There are also some other methods such as microbead rheometry, optical tweezers which deform the cell by either a magnetic field or a high intensity light. The preferred method, depends on the targeted cell or the typical range of force that needs to be applied. However, the throughput of these methods are limited by the manual handling time.

Table 1.1: Comparison of existing methods to measure cellular stiffness. *Source: D. D. Carlo et al. [1]*

Technique	Cell restrictions	Mechanical properties	Typical applied force range	High-throughput
Atomic force microscopy	Adherent cells	Elastic and viscoelastic properties of a local region or a whole cell	pN–μN	Potentially
Micropipette aspiration	Nonadherent or detached, adherent cells	Elastic and viscoelastic properties of a local region or a whole cell	pN–nN	Potentially
Microbead rheometry	Adherent cells	Elastic and viscoelastic properties of a local region	pN	No
Optical tweezers and traps	Adherent or nonadherent cells	Membrane elasticity, whole-cell deformability	fN–pN	Potentially
Fluid-based deformation cytometry	Nonadherent or detached, adherent cells	Whole-cell deformability	pN	Yes

Increasing the throughput of the system has several benefits. Firstly, rare abnormal cells existing in a large population can be detected. This can be used as a technique to measure the effectiveness of chemotherapy. Secondly, it will open new applications such as cell sorting. If red blood cells can be sorted at a high throughput to distinguish healthy cells from diseased cells, this can be used as a dialysis-like technique [8]. Thus, reducing organ failures in sepsis patients or to remove malaria-infected cells from the blood stream.

A simple but effective way to measure the cellular stiffness is to use a flow-based deformation cytometry. In this method, the cell is squeezed through a confined microchannel[3] and the velocity of the cell travelling inside the constriction channel is measured. The deformation of the cell inside the constriction channel is modeled and the cellular stiffness is derived. According to a very simplified modeled by F. Arai [9], the velocity of the cell is inversely

[3]A channel that has a width less than the diameter of the cell

proportional to the stiffness of the cell.

In table 1.1 some methods are denoted as ”potentially” high throughput. This is due to the recent advancement in automation and image analysis techniques that can replace the manual work of the operator. Nonetheless fluid-based deformation cytometry poses a very promising method to evaluate cellular stiffness at a high-throughput. The cellular stiffness measurement proposed in this thesis is based on the flow-based deformation cytometry.

1.3. Confined microfluidic flow for cellular stiffness measurement

Depending on the measurement method, the cell is deformed in different ways. For example, in the micropipette aspiration technique the cells are squeezed into a glass tube so a pressure is applied from all of the surfaces that are in contact with the glass tube. In optical tweezer method, force is applied to both ends of the cell in the opposite directions. Therefore, for each measurement method a different model is used to assess the cellular stiffness.

For modeling the behavior of a cell inside a confined microfluidic flow, a one dimensional viscoelastic model called the Kelvin-Voigt model was used [9]. This model combines a damper and a spring in parallel as shown in figure 1.1. The cellular stiffness is analogous to the spring because it is the property of a material to be restored to its original state after deformation. Terms such as elasticity and rigidity are often used interchangeably with stiffness in literature [10]. Viscosity is analagous to the damper because it is the property of fluid to resist to the rate of deformation caused by shear stress. From this model the total force F that is exerted to the outer environment by the cell is,

$$F = \mathrm{k}\delta + \mathrm{c}\frac{d\delta}{dt} \tag{1.1}$$

where δ is the deformation of the cell, k is the spring constant and c is the damping coefficient. Since damping is proportional to the time derivative of δ, a long enough deformation will cause the cell to act solely as a spring ($\because \frac{d\delta}{dt} = 0$). Therefore, within the confined microfluidic flow, the cell must be deformed for a long enough time before the velocity is measured.

In previous research by R. Hendrikx et al. [11] a device was fabricated to measure the change in cellular stiffness before and after a chemical stimulus

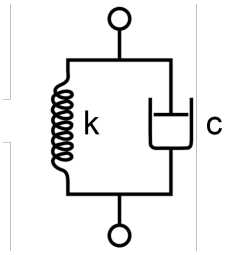


Figure 1.1: Kelvin-Voigt model of a cell. Stiffness of the cell k is in parallel with the damping component c of the cell.

was applied. In this device two channels where fabricated. One channel was injected with the solution including the cell, and the other channel was injected with the stimulus to alter the deformability of the cell. The two channel were separated by a porous membrane where the stimulus would diffuse into the other channel to alter the cellular stiffness. The channel injected with the solution with the cells has two constriction channel at the beginning and the end of the channel where the stiffness is measured. Figure 1.2 is a schematic overview of this method. Such method is promising to analyze the effect of drugs on cellular deformabilty in simple but effective manner.

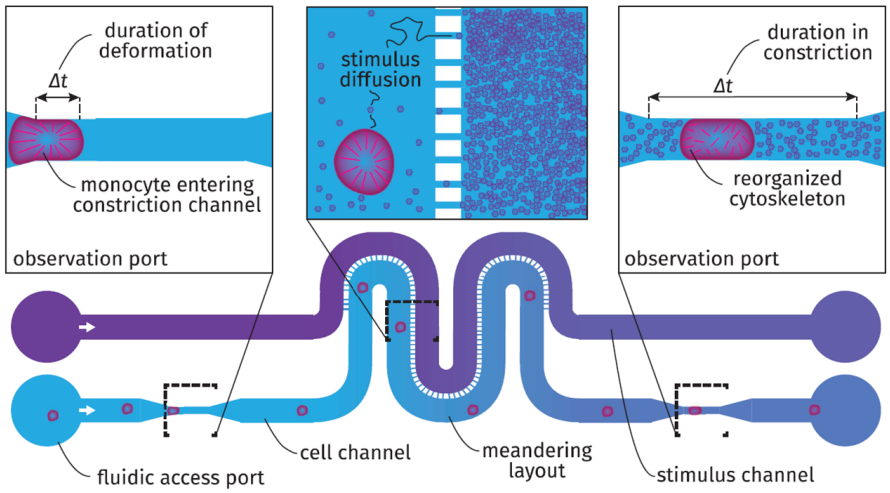


Figure 1.2: Schematic overview of the microfluidic proof-of-principle device. Cells in their solution enter the device through the fluidic access ports, where after the are flown through a constriction channel to measure the cell stiffness. Next, they reach a meandering structure with a porous membrane that allows diffusion of a chemical from the nearby stimulus channel. Finally, the cell reaches the second constriction where the stiffness is measured again. Observation ports were etched above the constriction channels to enable visual inspection of the flown cells. *Source: R. Stoute et al. [12]*

Innovative methods are constantly being developed to quantify the change in cellular stiffness. However, these methods have not yet left the research stage to be used in clinical practice or for standard diagnostic techniques. One reason is the fact that clinicians and cell biologists are not familiar with using cellular stiffness as a biomarker [1]. Yet this is gradually changing due to the recent attention in mechanotransduction[4] [13]. Another reason is the time consuming steps to measure the cellular stiffness such as focusing. This can be solved by using a plug-in-play like method to measure cellular stiffness. The final reason is the difficulty of scaling up the fabrication of these devices. Most research institutes base their fabrication techniques on materials such as PDMS or polymers which are not mass producible in a reliable manner [14, 15]. By replacing this with mass producible fabrication method such as IC based fabrication process, a standard platform for measuring cellular stiffness can be establish for researchers and clinician across the world.

The demand for a high-throughput, simple and mass producible device to measure cellular stiffness has never been so important. High-throughput can be achieved by using flow-based deformation cytometry as mentioned earlier. Expanding on this idea, a novel method for measuring cellular stiffness is proposed that will minimize the manual handling procedure of the operator while simultaneously being mass-producible. The realization of this device will accelerate the use of cellular stiffness measurement in the future.

1.4. Thesis Overview

In chapter 2 a new method to measure cellular stiffness measurement will be explained, followed by an electrical equivalent circuit model to assess the feasiblity of the method. In chapter 3 the fabrication of the embedded microchannel will be tested. Based on these results in chapter 4 additional test will be performed and the electrode integrated embedded microchannel (EIEMC) will be fabricated. In chapter 5 the results of the electrical characterization measurement of the device will be presented. Finally, the conclusion of this thesis will be summarized in chapter 6.

[4]The molecular mechanism how cells sense the mechanical stress and respond to it.

2

Measurement of cellular stiffness with Electrical Impedance

In section 2.1 the measurement method and fabrication technique chosen for this thesis is compared with previous devices seen in literature. In section 2.2 the design and concept of the device will be explained. In section 2.3 the channel where the detection of the cell occurs is modelled with a simplified equivalent circuit and simulated with a circuit simulation software. In section 2.4 the model is extended to the entire device to clarify some dominant parameters to reflect on the design of the device. In section 2.5 the goal is divided into individual task and summarized.

2.1. Electrical Impedance Measurement with Standard IC-based Fabrication

Cellular stiffness is related to the velocity of a cell that is being squeezed through a constriction channel. In most cases, the velocity inside this constriction channel is measured optically. In an optical measurement, the constriction channel is exposed with a light source (i.g. laser, optical microscope) and the difference in refractive index of the cell, in comparison to the surrounding medium, is detected with a sensor (i.g. photo diode, CCD camera) [14, 16, 17]. A disadvantage of the optical method is the manual step to focus the light at the constriction channel. This is a time consuming process that makes it difficult for clinicians to use.

In an electrical impedance measurement, a pair of electrodes is used instead. The impedance between a pair of electrode is measured to find the difference in conductivity of the medium with and without the cell. This will dramatically reduce the effort to manually adjust the focus during the measurement. Adamo et al. has demonstrated this concept by fabricating a microfluidic channel inside a silicon wafer by DRIE with thermally grown oxide of 0.3 µm [18] on the front side. This channel was sealed by anodic bonding of a borofloat glass wafer which had gold electrodes deposited by electron beam deposition and patterned by lift off. The electrodes were placed on each side of the constriction channel which measured the impedance across the entire channel (Fig. 2.1-top). The resistance increased when the position of the cell was between the electrode (Fig. 2.1-bottom). The diameter of the cell was also measured from the amplitude information during position B in the same figure. This is synonymous to the Coulter principle [19]. Although this method was successful to demonstrate the electrical impedance method, it can be improved since the fabrication process uses gold deposition and anodic bonding which are not standard IC-based process.

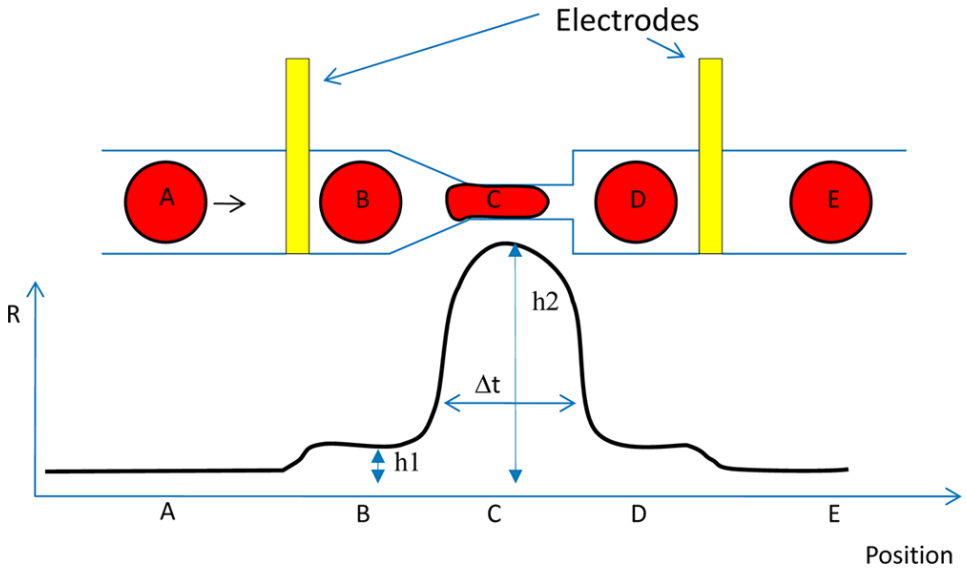


Figure 2.1: The impedance based measurement of cellular stiffness by A. Adamo et al [18].

The advantage of a standard IC-based process, is the mass producibility insured by the overwhelming success of the semiconductor industry and the potential to be integrated with further CMOS electronics. In this thesis a fabrication process completely compatible with standard IC based fabrication technique was developed.

2.2. Design and Concept

The concept of the device is to detect the cell at two different locations along the constriction channel to measure the velocity of the cell (Fig. 2.2). This will also lead to a higher signal to noise ratio than having the electrode only at the entrance and the exit of the channel [20].

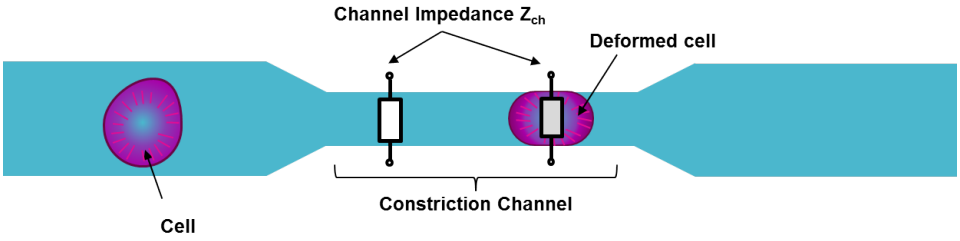


Figure 2.2: Channel impedance Z_{ch} is the impedance along the channel as shown. The channel impedance changes due to the presence of the cell.

The developed fabrication process was based on the Embedded Microchannel (EMC) fabrication process [12]. The EMC fabrication process is a method to fabricate microchannels with vertical sidewalls inside a silicon substrate which is subsequently sealed with an PECVD SiO_2 layer. The EMC fabrication process utilizes the BOX layer of an SOI wafer as an etch stop layer during the DRIE process. Here we exploit the BOX layer not only as an etch stop layer, but also as an insulating material to isolate parts of the device layer to use as electrodes. Figure 2.3 is an example of how an electrode can be integrated alongside the microchannel. The two silicon pieces shaped like a ”pin” are the electrodes. Since they are fabricated from highly boron doped silicon, they have a low resistivity and are effectively conductors. The electrodes are electrically isolated from the silicon substrate by the BOX layer and the void that is surrounding it. The tip of the pin facing the constriction channel is the location where the cell pass through and are detected. The electrodes can be excited via the aluminum interconnect that is connected from the top.

In the following section the modeling and simulation of the device is separated in two parts. In the first part the impedance of the channel is simulated. Next, the entire device including the bondpad, interconnect and leakage current is considered.

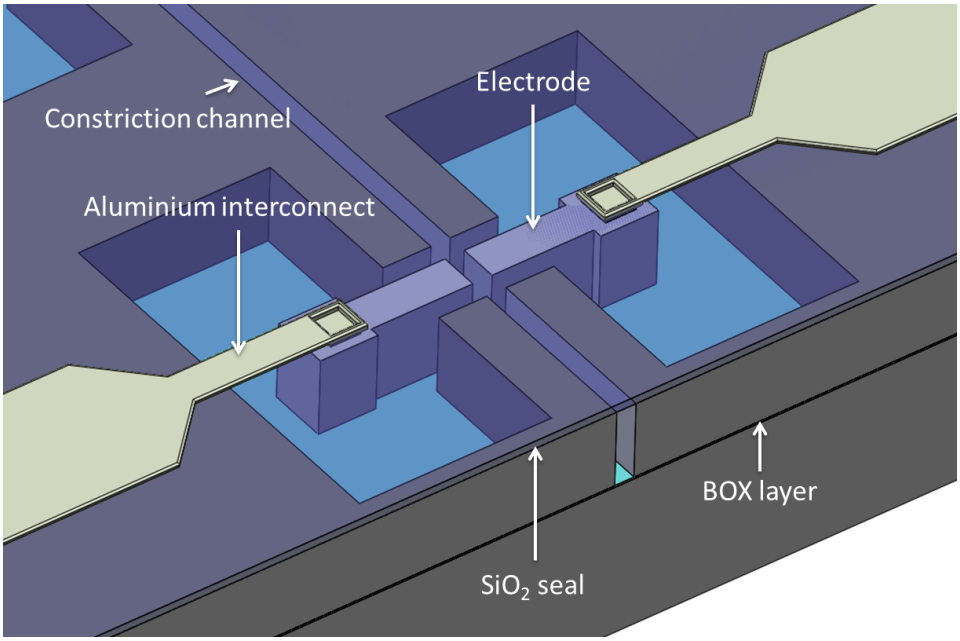


Figure 2.3: 3D model of the Electrode Intergrated Embedded Microchannel.

2.3. Modeling and Simulating the Channel Impedance

An equivalent circuit model translates a physical model (i.e. cell membrane, cytoplasm and etc.) into a combination of simplified electrical components such as resistors and capacitors. In this section, the equivalent circuit model of the channel impedance will be described and simulated.

2.3.1. Modeling of the Channel Impedance

When the cell is not present, the channel impedance (Z_{ch}) is due to the medium. Thus, Z_{ch} can be divided into the medium resistance (R_{med}) and medium capacitance (C_{med}) in parallel, connected to the double layer capacitance (C_{dl}) in series as shown in figure 2.4 (a). The double layer capacitance is a capacitance that forms at the interface of the electrode and the solution. When the cell is present, the cell and the medium will be in parallel to each other. Using the cell impedance model proposed by Foster and Schwan [21], the cell impedance is the membrane capacitance (C_{mem}) and cytoplasm resistance (C_{cyto})in series as shown in figure 2.4 (b).

A specific geometry of the electrodes, the constriction channel and the cell must be decided to model the channel impedance (Z_{ch}). For this analysis, the constriction channel is 40 µm deep and 10 µm wide. The electrode has the same height as the constriction channel (40 µm) and is 10 µm wide. Two elec-

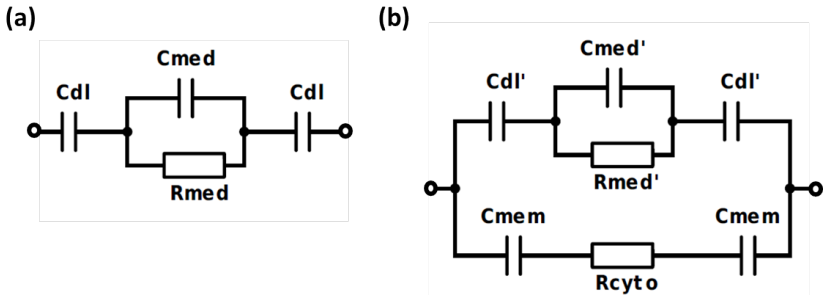


Figure 2.4: Channel impedance model based on Foster and Schwan [21]. The model consists of a double layer capacitance C_{dl}, medium capacitance C_{med}, medium resistance R_{med}, membrane capacitance C_{mem} and cytoplasm resistance R_{cyto}. R_{med}' and C_{med}' denotes the value when the cell is between the pair of electrodes. (a) Channel impedance without the cell (Z_{ch}) (b) Channel impedance with the cell (Z_{ch}')

trode are oriented in parallel facing each other with the constriction channel in between. Therefore, the spacing between the two electrode is equivalent to the width of the constriction channel. From the geometry and the orientation of the electrodes, the medium resistance (R_{med}) and capacitance (C_{med}) when the cell is not present between the electrode is,

$$R_{med} = \frac{1}{\sigma_{med}} \frac{W}{S} = 7.5\,\text{k}\Omega$$

$$C_{med} = \varepsilon_{med}\varepsilon_0 \frac{S}{W} = 30\,\text{fF}$$

where the S = 10×40 = 400 µm^2 is the surface area of the electrode, σ_{med} = 1.6 S m^{-1} is the conductivity of saline which is the medium. ε_{med} = 80 is the relative permittivity of saline and ε_0 is the vacuum permittivity [22].

The cell considered for this thesis is an HL-60 cell which has an average diameter of 12 µm. Normally the equivalent circuit analogue of a cell is simplified as a spherical shape in suspension. However, in our device the cell is squeezed in the constriction channel that is 10 µm wide and it would not be appropriate to directly use the equations developed for a spherical shape [21]. Instead, the cell will be modeled as a rectangular solid as shown in figure 2.5. The simplified cell model has a width, height and length which is W = 10 µm, H = 8 µm and L = 11 µm respectively. The membrane thickness is 5 nm [22]. The volume of the cell is V_{cell} = 880 µm^3.

The pink layer is the cell membrane and the blue area wrapped inside the pink layer is the cytoplasm. The cytoplasm resistance (R_{cyto}) is the resistance

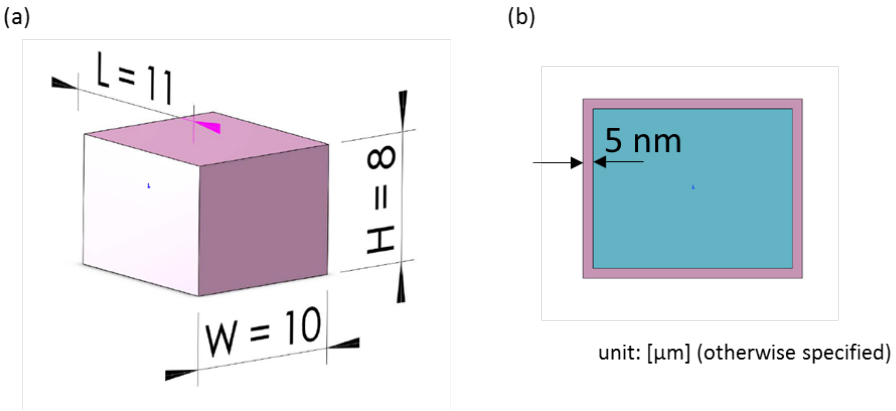


Figure 2.5: Simplified cell model pink layer represents the cell membrane and the blue part wrapped inside the pink layer represents the cytoplasm.(a) 3 dimensional view of the cell (b) A cross section of the cell

across the width of the simplified cell,

$$R_{cyto} = \frac{1}{\sigma_i}\frac{W}{LH} = 280\,k\Omega$$

where the conductivity of the cytoplasm is $\sigma_i = 0.4\,S\,m^{-1}$. The relative permittivity of the cell membrane is $\varepsilon_{mem} = 5$ [22]. The cell membrane capacitance (C_{mem}) is,

$$C_{mem} = \varepsilon_{mem}\varepsilon_0\frac{LH}{t_{mem}} = 0.4\,pF$$

When the cell is present between the electrode the surface area of the electrode decreases by the surface area that is covered by the cell. Taking into account that the simplified cell model has a slightly longer length than the electrode width, the surface area that is not covered by the cell is S' = S - 8 × 10 = 320 µm^2. In this case the medium resistance (R'_{med}) and capacitance (C'_{med}) becomes,

$$R'_{med} = \rho_{med}\frac{W}{S} = 9.4\,k\Omega$$

$$C'_{med} = \varepsilon_{med}\varepsilon_0\frac{S}{W} = 24\,fF$$

Lastly, the double layer capacitance is proportional to the surface area. The double layer capacitance will decrease if the cell covers the surface of the electrode. To our knowledge there is no information in literature which characterizes the double layer capacitance formed at the interface between highly boron doped silicon and saline solution. According to [23] capacitance per unit area (c_{dl}) for a double layer capacitance is typically in the range from

10 to 40 µF cm^{-2}. For our analysis we will use c_{dl} = 30 µF cm^{-2}. The double layer capacitance is,

$$C_{dl} = c_{dl} S = 120\,\text{pF}$$

$$C'_{dl} = c_{dl} S' = 96\,\text{pF}$$

where C_{dl} and C'_{dl} are the double layer capacitance without and with the cell between the electrodes.

To summarize the circuit parameters table 2.1 lists the values derived in this section.

Table 2.1: Paramter derived in this section for the circuit presented in figure 2.4

Circuit parameter	Explanation	With cell	Without cell	Unit
R_{med}	medium resistance	9.0	7.5	kΩ
R_{cyto}	cytoplasm resistance	280	x	kΩ
C_{mem}	cell membrane capacitance	0.4	x	pF
C_{med}	medium capacitance	24	30	fF
C_{dl}	double layer capacitance	96	120	pF

2.3.2. Simulating the Channel Impedance

The impedance of the channel was simulated using an AC analysis from 100 kHz to 10 GHz with a sinusoidal signal with a 1 V amplitude on LT-Spice. To calculate the channel impedance Z_{ch} the complex version of Ohm's law was used as shown below,

$$Z_{ch}(j\omega) = \frac{V(j\omega)}{I(j\omega)}$$

where j, V, I and ω are the imaginary unit, voltage, current and angular frequency respectively.

The result of the simulation is shown in figure 2.6. The difference in phase with and without the cell is negligible. In comparison, for the impedance, there is always a slight difference of a few kΩ over the entire frequency that was simulated. From 100 kHz to 1 MHz the impedance begins to decrease as the frequency increases. This is a typical characteristic of a capacitor because the impedance of a capacitor is inversely proportional to the frequency. At frequencies above 1 MHz the impedance hits a plateau and the value becomes constant. This transition to the plateau is a result of the dominant

impedance changing from a capacitive to a resistive characteristic. This can be confirmed by calculating the corner frequency for figure 2.4 (a); channel impedance without the cell. By neglecting the medium capacitance ($\because C_{dl} \gg C_{med}$) the circuit will simplify to one medium resistance and two double layer capacitance in series. Thus the corner frequency f_c can be calculated as,

$$f_c = \frac{1}{2\pi R_{med} C_{dl}/2} = 0.36\,\text{MHz}$$

This corner frequency aligns well with the result from figure 2.6. It also aligns well with theoretical calculation result that was achieved by S.Gawad et al.[24] who modeled the system with similar electrode size and distance between the electrode plates. At frequencies below f_c the impedance is capacitive due to the double layer capacitance C_{dl}, and at frequencies above f_c the impedance is resistive due to the medium resistance R_{med}. Another important thing to notice is the impedance value of the plateau region. For the situation with and without the cell, the simulated impedance is approximately 8.7 kΩ and 7.5 kΩ respectively. This is very close to R_{med} which is 9.0 kΩ and 7.5 kΩ for with and without the cell respectively. This similarity is caused by the transparency of the double layer capacitance at this frequency range.

When detecting the cells it is important to decide on a certain frequency range to operate in. The transit time of the cell to cross over the electrode defines the lower limit of the frequency. In previous research [12] the fluid velocity ranged from $1 \times 10^{-3}\,\text{m s}^{-1}$ to $1 \times 10^{-2}\,\text{m s}^{-1}$. Assuming the fastest velocity the lowest frequency f_o defined by the cell passing by the electrode is,

$$f_o = \left(\frac{W}{v_{max}}\right)^{-1} = 1\,\text{kHz}$$

where W is the width of the electrode and v_{max} is the maximum velocity of the cell. Thus, a frequency lower than f_o cannot be used to detect the cell because the transit time is less than one period of the signal. To summarize, a frequency higher than 1 k must be used to detect the cell. In addition to the channel impedance simulation, the detection mechanism is different depending on which frequency is used. If a frequency range from 1 kHz to 0.36 MHz is used, the difference in double layer capacitance will be detected. And if a frequency range higher than 0.36 MHz is used, the increase in medium resistance will be detected. In all cases the measurement of the cellular stiffness using the purposed electrode geometry is feasible.

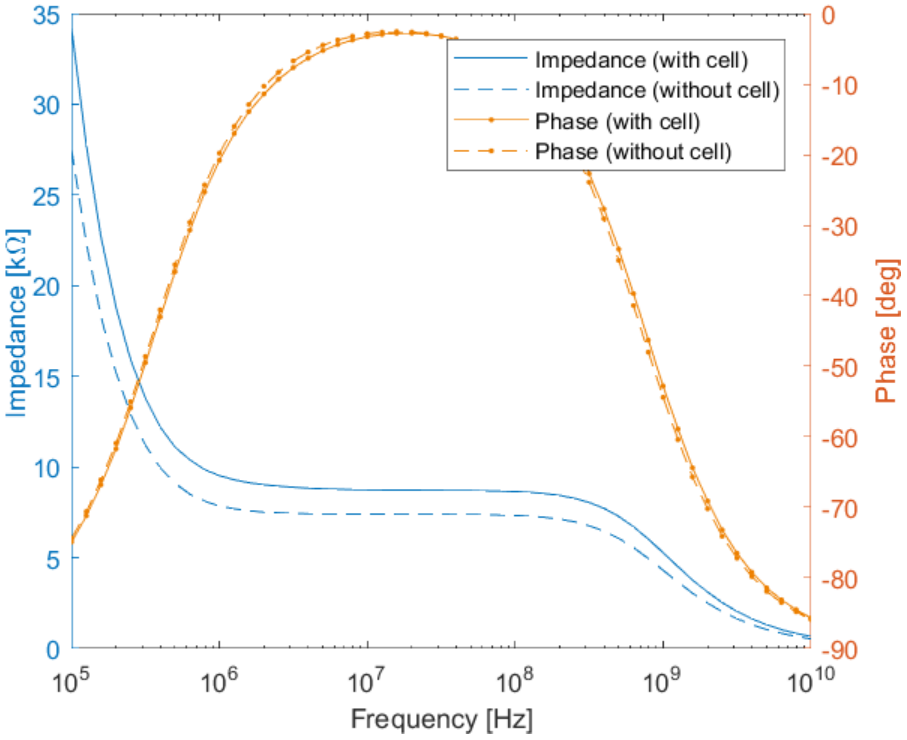


Figure 2.6: AC simulation result of the impedance and phase from 100 kHz to 10 GHz using LT-Spice when the cell is between the electrodes (with cell) and when the cell is not between the electrodes (without cell).

2.4. Modeling and Simulating the entire device

Now we will extend our equivalent circuit model to the entire device (Fig. 2.7-a). In addition to the constriction channel that was modelled previously (Fig. 2.7-b,c), the interconnect resistance ($R_{interconnect}$), the contact resistance ($R_{contact}$), bond pad capacitance (C_{bp}), bulk resistance (R_b) and leakage resistance and capacitance (R_{med_leak},C_{med_leak}) are taken into account. The location of these values is depicted in figure 2.7.

2.4.1. Modelling the entire device

To quantify the circuit parameter in figure 2.7 a particular design was specified (Fig. 2.8). The leakage resistance and capacitance correspond to the current that flows from the electrode to the surrounding silicon. It is impossible to derive an exact value of the leakage without a finite element analysis. For simplicity, in this model, the complex geometry of the leakage was divided into simple rectangles so we can apply our usual formula to calculate

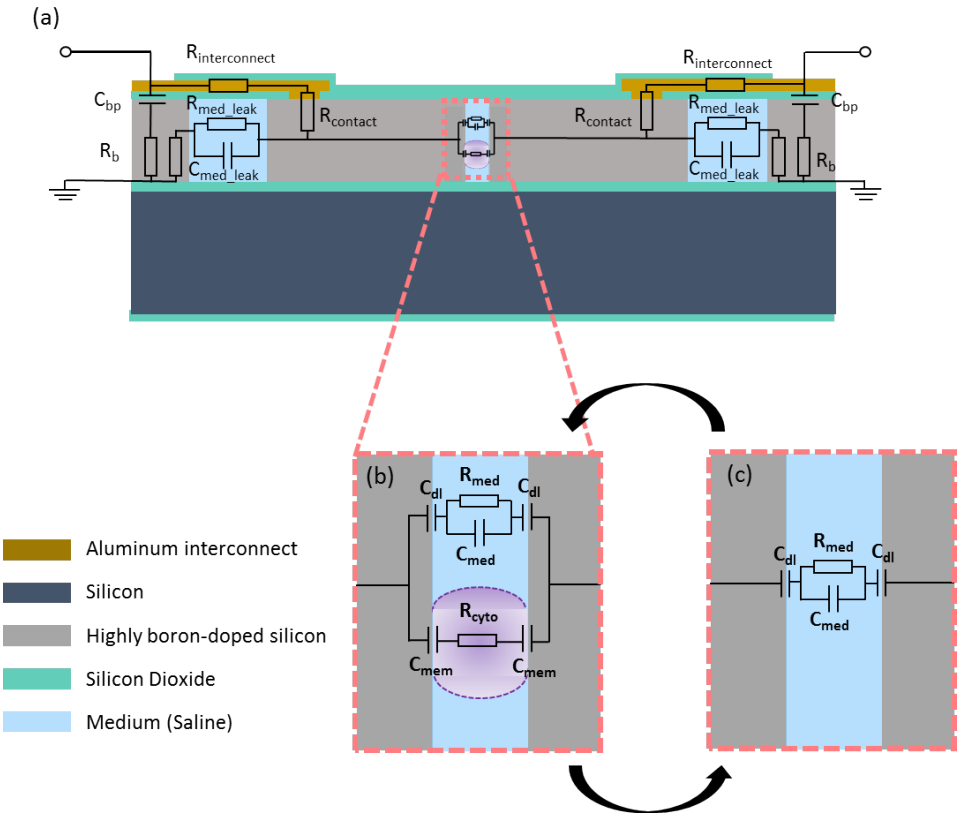


Figure 2.7: (a)Cross section of the channel with the corresponding circuit component. (b) Expanded view of the constriction channel when the cell is present. (c) Expanded view of the constriction channel when the cell is not present. The circuit values for this model are summarized in table 2.1

the resistance and capacitance of the leakage. Figure 2.9-a divides the leakage current from the electrode to the bulk into four rectangular areas. These areas are named Area I to Area IV (Fig. 2.9-b). As a result, figure 2.9-a can be recognized as a parallel connection of these area (Fig. 2.9-c).

The value of the resistance and the capacitance for each area is summarized in table 2.2

The total resistance and capacitance of the leakage can be calculated as,

$$R_{\text{med-leak}} = \frac{R_{\text{med-leak-1}}}{2} // \frac{R_{\text{med-leak-2}}}{2} // \frac{R_{\text{med-leak-3}}}{2} // R_{\text{med-leak-4}} = 1.1\,\text{k}\Omega$$

$$C_{\text{med-leak}} = 2C_{\text{med-leak-1}} + 2C_{\text{med-leak-2}} + 2C_{\text{med-leak-3}} + C_{\text{med-leak-4}} = 0.2\,\text{pF}$$

When resistors are in parallel the lowest resistance is dominant and when capacitors are in parallel the highest capacitance is dominant. Therefore, the dominant resistance and capacitance is from Area I and most of the current will flow through this area if a voltage is applied between the electrode and

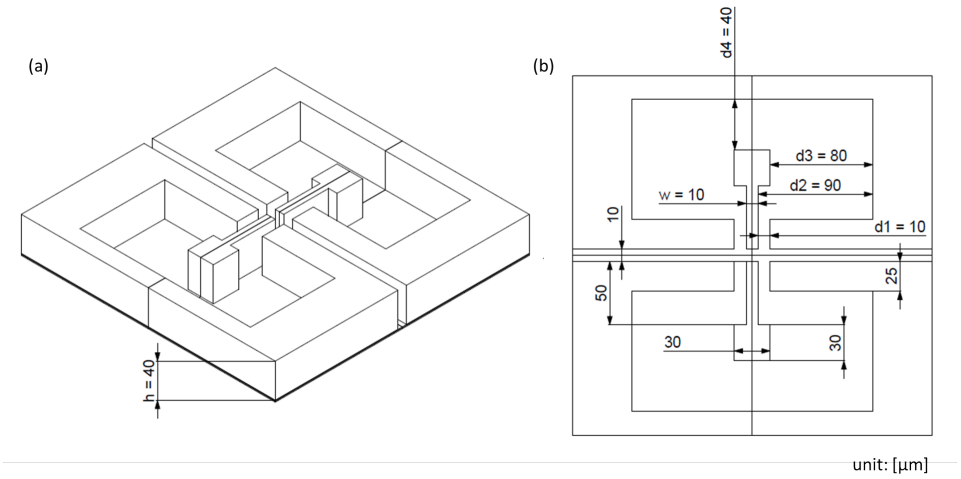


Figure 2.8: Geometry of the channel used in the model

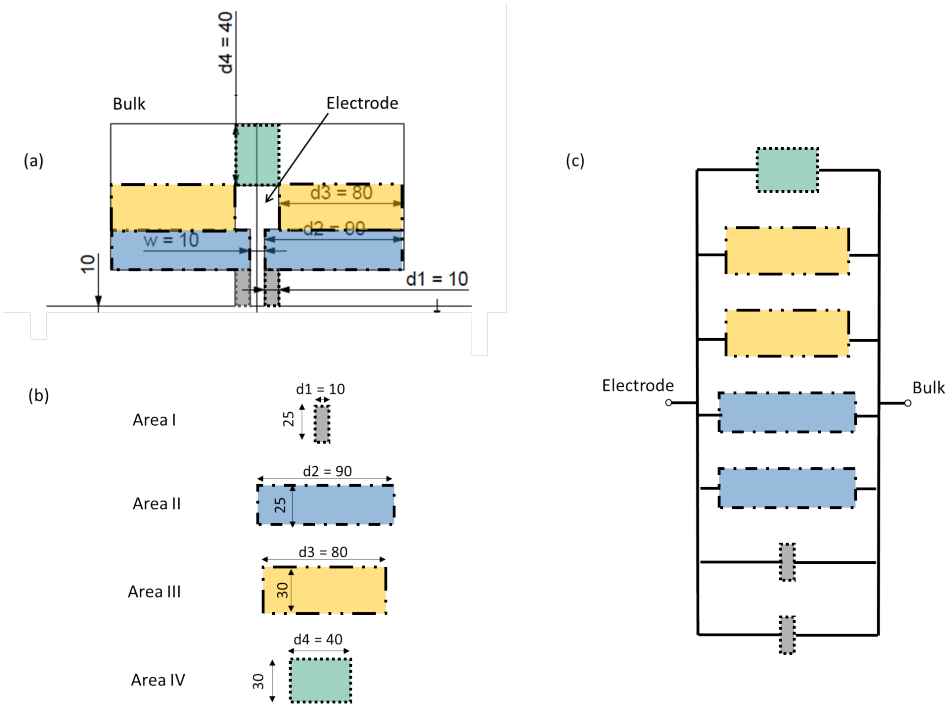


Figure 2.9: Area I to IV where the leakage occurs

Table 2.2: Summary of the resistance and capacitance value for Area I to IV in figure 2.9

	Leakage resistance Rmed_leak (kΩ)	Leakage capactiance Cmed_leak (fF)
Area I	1.5	138
Area II	13.5	15.4
Area III	10	20
Area IV	5	42
Total	1.1	200

the surrounding silicon. This is visually represented in table 2.2; the total is nearly the same as Area I.

Next, the aluminium interconnect was modelled with the length, thickness and width of 5 mm, 2 µm and 30 µm respectively. The resistivity of aluminum is $2.65 \times 10^{-8}\,\Omega\,\mathrm{m}$, thus the aluminium interconnect resistance is,

$$R_{\text{interconnect}} = 2\,\Omega$$

Ion implantation of boron was performed to increase the dopant concentration to $1 \times 10^{19}\,\text{atoms/cm}^3$ at the surface of the wafer. This creates an ohmic contact between the aluminum and silicon. For a good ohmic contact the contact resistance is around $10\,\mathrm{m\Omega\,cm^{-2}}$. Since the contact surface area is 30 µm by 30 µm, the resistance is 90 nΩ. The resistance caused by the contact is much less than the interconnect resistance in series, thus the contact resistance can be neglected,

$$R_{\text{contact}} = 0\,\Omega$$

The resistivity of the highly boron-doped silicon is given by the data sheet from Okmetic and it is in the range from 5 to 20 mΩ cm. The resitance of the surrounding silicon is difficult to estimate because the return path of the current is not well defined. For now let us assume that this value is,

$$R_b = 2\,\Omega$$

The surface area of the bondpad S_{bp} = 700 µm ×3800 µm = 2.7 mm^2 and the thickness of the silicon t_{ox} = 3 µm. Thus, the bondpad capacitance is,

$$C_{\text{bondpad}} = \varepsilon_{ox}\varepsilon_0 \frac{S_{bp}}{t_{ox}} = 31\,\text{pF}$$

Table 2.3 summarizes the circuit parameters derived in this section.

2.4.2. Simulating the entire device

A circuit simulation was performed on the complete device model that was developed. The entire equivalent circuit model was simulated by applying an external voltage to one of the electrodes while the bulk was grounded and the signal on the other electrode was read-out. The output voltage for with and without the cell between the electrodeds were simulated for a frequency range from 100 Hz to 100 MHz with a 1 V amplitude sine wave signal. In reality this

Table 2.3: Circuit parameters circuit in figure 2.7

Circuit parameter	Explanation	Value	Unit
$R_{interconnect}$	interconnect resistance	2	Ω
$R_{contact}$	contact resistance	0	Ω
$C_{bondpad}$	bond pad capacitance	31	pF
R_{med_leak}	leakage resistance	1.1	kΩ
C_{med_leak}	leakage capacitance	0.2	pF

is likely to change to a lower voltage, because an amplitude higher than 0.8 V would drive too much current into the solution to oxidize or reduce the water. However, the linearity of the circuit insures the scalability of the results that is obtained from the simulation. As long as the linearity of the model holds, it is sufficient to simulate for one input voltage and depending on the real input voltage the simulation results can be scaled proportionally.

The simulation result of the phase is shown in figure 2.10. There is hardly any difference with or without the cell because the V_{out}(without cell) and V_{out}(with cell) is overlapping completely. The amplitude against the frequency is plotted in figure 2.11. ΔV is the change in amplitude caused by the cell. From this figure if the cell passes between the electrodes the amplitude of the signal will decrease by a approximately five percent. Beyond the corner frequency (f_0) this difference will gradually decrease.

From this analysis, increasing ΔV is the key to design a higher signal to noise ratio. In order to achieve such a design, the leakage impedance should be designed so that it is equal to the channel impedance. Since the leakage resistance for this model was 1.1 kΩ and the channel resistance was 7.5 kΩ the leakage resistance should be increased. In order to increase this value the distance from the electrode to the surrounding silicon must be designed carefully. Especially, area I (Fig. 2.9) should be increase or the width of area I should be decreased. For the former option the distance in Area I cannot be increased arbitrarily because if this spacing increases too much, the cells would enter the void between the electrode and the bulk. For the latter option, the width of Area I cannot be too thin because this will cause the wall to mechanically break down. Therefore, several design for Area I should be tested to find the optimal geometry which maximizes the signal but does not cause any failures.

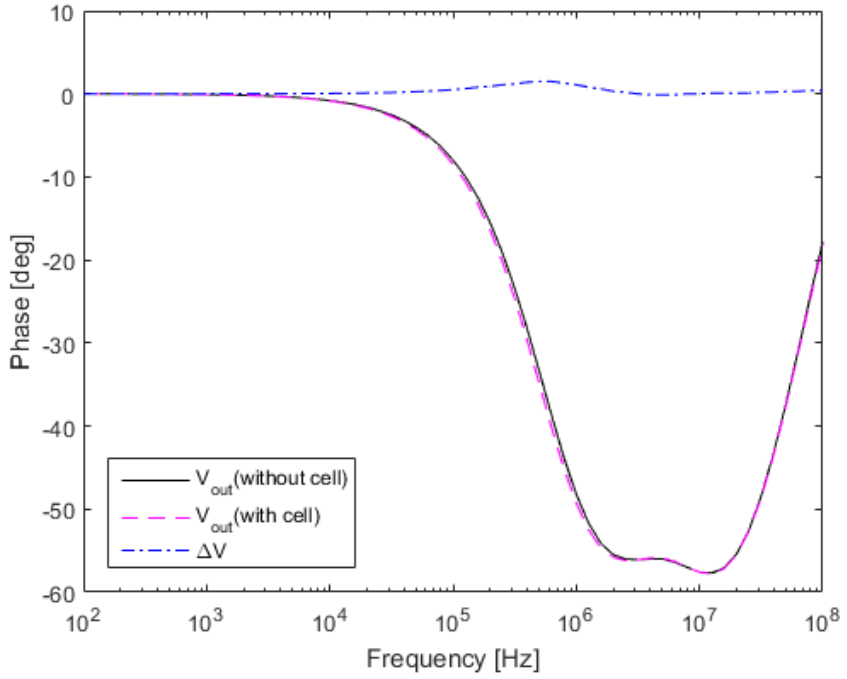


Figure 2.10: AC simulation result from 100 Hz to 100 MHz. The phase of the output voltage is plotted for two situation with and without the cell. $\Delta V = V_{out}(\text{without cell}) - V_{out}(\text{with cell})$ is the difference between the phase.

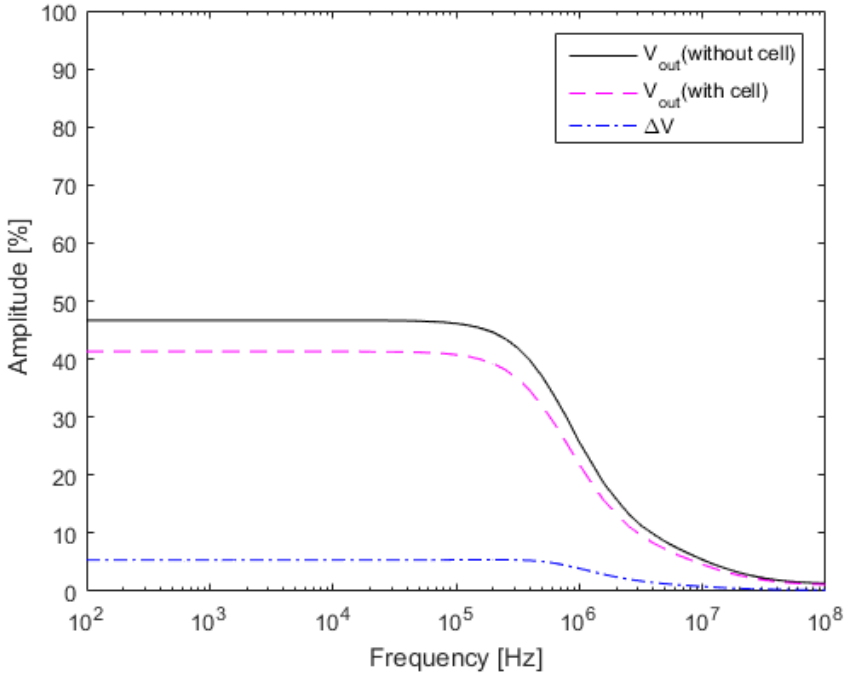


Figure 2.11: AC simulation result from 100 Hz to 100 MHz. The output voltage is plotted for two situation with and without the cell. $\Delta V = V_{out}(\text{without cell}) - V_{out}(\text{with cell})$ is the difference between the amplitude.

2.5. Design Goals

The goal must be divided into smaller task level goals for further progress. In order to fabricate the device there are mainly 5 aspects that need to be considered, (1) fabrication of the chip, (2) electrical analysis, (3) read-out electronics design, (4) packaging of the chip and (5) programming of the read-out system. Table 2.4 summarizes the tasks for this thesis.

Table 2.4: Summary of goal and method

Level			Goal	Method
High	Real time cell stiffness measurement through impedance sensing			
	Medium	Fabrication of the chip		
		Low	Mask fabrication	A mask design software (L-Edit) was used to design 5 masks aluminium interconnect, bond pad, channel with electrodes, inlet/outlet and contact hole.
		Low	EMC fabrication (Cleanroom)	Fabrication test was done using the channel mask and Rene Hendrikx's mask
		Low	EIEMC (Cleanroom)	The fabrication steps that can be tested separately was tested beforehand.
	Medium	Electrical analysis		
		Low	Equivalent Circuit modeling	The equivalent circuit model was made based on previous research.
		Low	Actual measurement of the device	Several measurement method were used. 1) Impedance spectroscopy 2) single frequency excitation 3) bode analysis
	Medium	The design of adapters to read out the signal and inject liquid into the channel		
		Low	PCB design	PCB to easily read out the signal from the chip.
		Low	3D printing of holder	A holder was designed and 3D printed.
		Low	Microfluidic packaging	PDMS was used to connect the chip to the microfluidic pump.
	Medium	Program to control Redpitaya (a credit card size microcontroller) to quantify the cell stiffness.		

3

Investigation of the fabrication process for Embedded Microchannel

Embedded Microchannel (EMC) is a method to fabricate microscale channels with vertical sidewalls inside silicon wafer without the need for a subsequent bonding process. It was developed to integrate CMOS technology and microfluidics with the same planar process.

In this chapter, the EMC process was studied for two reasons. First, the fabrication of the EMC was developed at Philips Innovation Center and it was necessary to transfer the technology to the Else Kooi Laboratory (EKL) at Delft University of Technology. Secondly, the fabrication process was modified to eliminate one etch step in the process and to achieve optimal depth and sidewall angles for Electrode Integrated Embedded Microchannel (EIEMC). The fabrication result of EIEMC will be described in the next chapter.

In section 3.1 the fabrication of the EMC previously developed at Philips Innovation Center is reviewed. In section 3.2 the modification to the recipe is explained followed by a detailed process flow. In section 3.3 the fabrication results are discussed. In section 3.5 another etch recipe was tested to clarify the mechanism of single step DRIE.

3.1. EMC fabrication at Philips Innovation Center

The fabrication steps of an EMC is shown in figure 3.1. For this process a silicon on insulator (SOI) wafer was prepared with 40 µm thick device layer,

1 µm thick buried SiO_2 (BOX) layer, 380 µm thick substrate. Using PECVD, 500 nm of SiO_2 was deposited on the front side and patterned into a mesh of rectangular holes of 0.8 µm by 4 µm (Fig. 3.1-a). On the backside of the SOI wafer 4 µm of PECVD SiO_2 was deposited and subsequently patterned with the observation port design. Deep reactive ion etching (DRIE) was used to etch deep holes through the mesh hard mask on the front until it landed on the BOX layer (Fig. 3.1-b). The silicon walls between neighboring holes were removed by an additional isotropic etch step (Fig. 3.1-c). Finally, the SiO_2 mesh was closed by TEOS layer of 2 µm and an observation port for the channel was etched from the backside using the DRIE (Fig. 3.1-d).

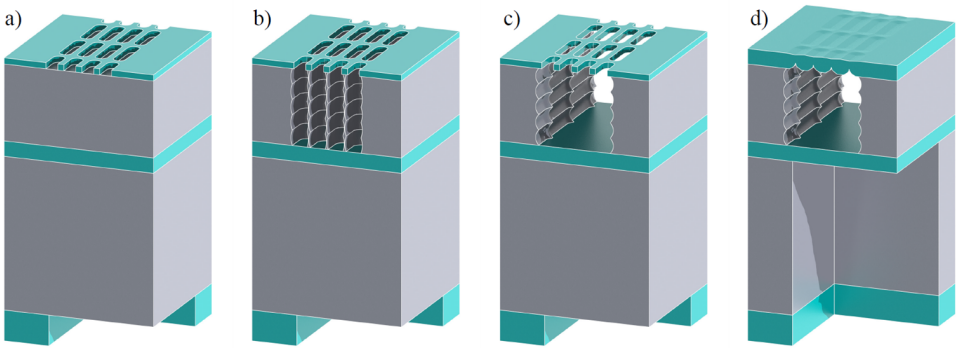


Figure 3.1: Process steps for the fabrication of embedded microchannels. a) Small holes are etched into a 500 nm SiO_2 layer. b) The silicon is deep reactive ion etched anisotropically until the BOX layer. c) The remaining silicon is removed from the channels with an CF_4 etch isotropically. d) The holes are closed with a 2.0 µm TEOS and the observation port is deep reactive ion etched from the back. *Source: reprinted from R.Stoute et al. [12].*

3.2. Single step EMC fabrication at Else Kooi Laboratory

Upon transfer of the EMC fabrication technology to EKL, most of the fabrication steps were kept the same. However, the DRIE step from (a) to (b) in figure 3.1 was tuned so that the sidewalls disappeared simultaneously when the holes were etched (≡ Single step DRIE [25]). The advantage of this method is that faster production can be achieved because the isotropic etch step is not necessary.

The process flow used at EKL for fabricating the EMC is schematically shown in Figure 3.2. The process was done on single side polished wafers.

This was preferable compared to an SOI wafer since the motive of this experiment was to characterize the channel depth for different etch recipes.

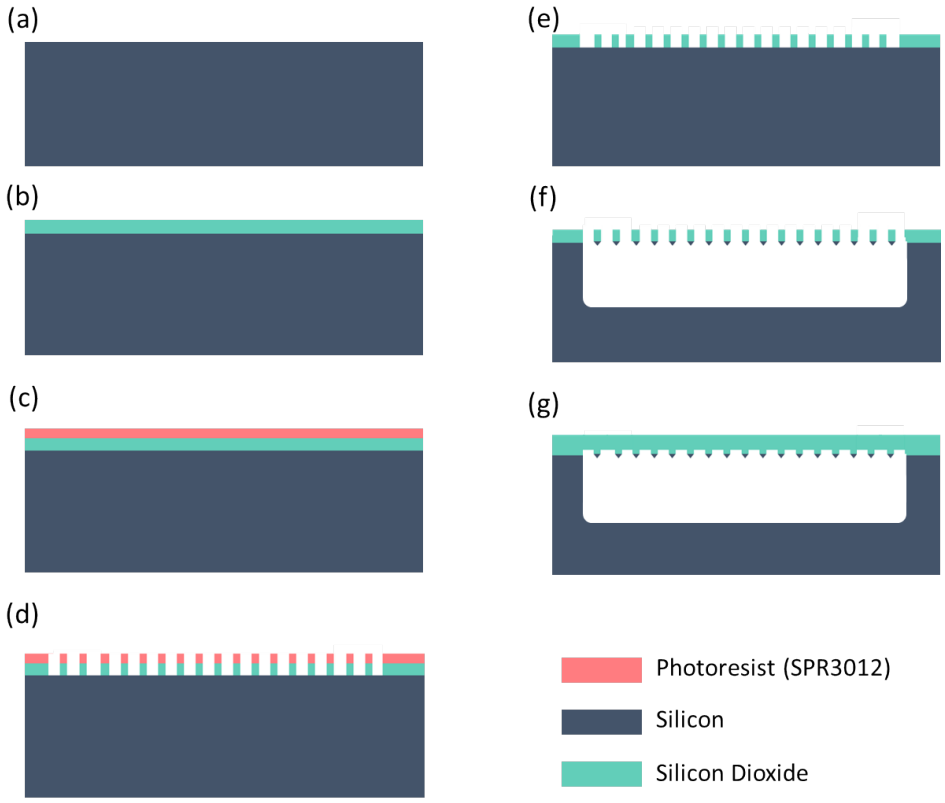


Figure 3.2: Process flow used in EKL for the fabrication of EMC with single side polished wafer. (a) Bare single side polished wafer. (b) 2 µm thick PECVD SiO_2 deposited on the front side of the wafer. (c) Photoresist (SPR3012) is coated on the front side of the wafer. (d) Photoresist is exposed and developed which is subsequently used as a mask to pattern the PECVD SiO_2. (e) Photoresist is stripped and the wafer is cleaned. (f) Single Step DRIE is performed to fabricated the EMC. (e) The EMC is closed with 2 µm of PECVD SiO_2

First, a single side polished silicon wafer was prepared a thickness of 525 µm thickness(Fig. 3.2-a). Novellus-Concept One was used to deposit 2 to 2.5 µm PECVD SiO_2 at 400 °C (Fig. 3.2-b). EVG 120 Coater-Developer was used to spin-coat positive photoresist (SPR3012) with 1.4 µm or 2.1 µm thickness (Fig. 3.2-c). Hexamethyldisilazane (HDMS) treatment was done prior to the coating. An ASML PAS 5500/80 waferstepper was used for the exposure of the photoresist. For the exposure, an exposure energy of 90 mJ cm^{-2} (for SPR3012 1.4 µm) or 150 mJ cm^{-2} (for SPR3012 2.1 µm) was used. Relatively low energy was used to prevent over development. After the post-exposure bake at 115 °C for 90 seconds, the exposed photoresist was developed for 57 seconds with the MF322 developer. Afterwards, the resist was hard baked

for 90 seconds at 100 °C (Fig. 3.1-d). A Drytek Triode etcher was used to dry etch the SiO_2 using the photoresist mask. The photoresist was stripped with oxygen plasma using endpoint detection and a 2 min over etch in Tepla (Fig. 3.2-e). In a DRIE process, first a passivation layer was deposited for 1.2 s. Next, a passivation breakthrough step of 1 s is followed by an 8 s of silicon etching step. These steps are performed in a cyclic manner to etch deep holes. During this process the holes coalesced beneath the SiO_2 mesh mask. The mesh was sealed using Novellus Concept by depositing 2 µm of PECVD SiO_2.

3.3. Results

The single step process is sensitive to the spacing between each holes. In section 3.3.1 an experiment was conducted to understand the influence of the spacing between each hole on the etch rate of Si. In section 3.3.2 the EMC was fabricated with different widths (i.e. 10 µm or 100 µm) and design (i.e. hexagonal or rectangular). Finally, the optimal parameter for fabricating EMC channel is discussed in section 3.4.

3.3.1. Fabrication of single slit trenches with various spacing

A mask design with rectangular slits of 1 µm by 6 µm aligned in a line with different spacing between the slits, was used (Fig. 3.3). On the same mask the distance between the holes (D) was varied from 0.6 µm to 2.0 µm with a step of 0.2 µm.

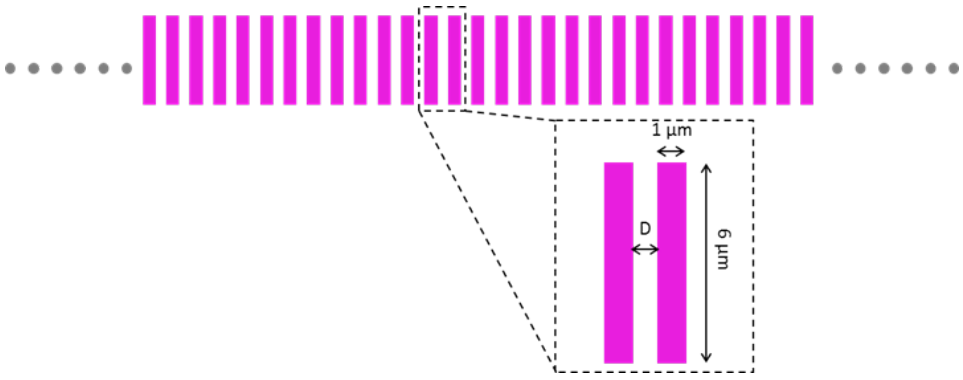


Figure 3.3: The mask design used for evaluating the influence of the distance between neighboring holes to the etch rate. The exposed region is the colored rectangular area. On the same mask spacing between the holes (D) was varied from 0.6 µm to 2.0 µm with a step of 0.2 µm.

By using the process steps explained in section 3.2, 7 wafers were pro-

cessed with different cycle numbers in the DRIE process - 10, 30, 60, 70, 80, 90, and 120 cycles. The result is shown in figure 3.4. The total etch time is plotted on the horizontal axis. The total etch time is the sum of the passivation breakthrough etch per cycle and the silicon etch per cycle multiplied by the number of cycles that was used in DRIE. Since each cycle has 1 s of passivation break through etch and 8 s of silicon etch, the total etch time is 9n [s] for n [cycles].

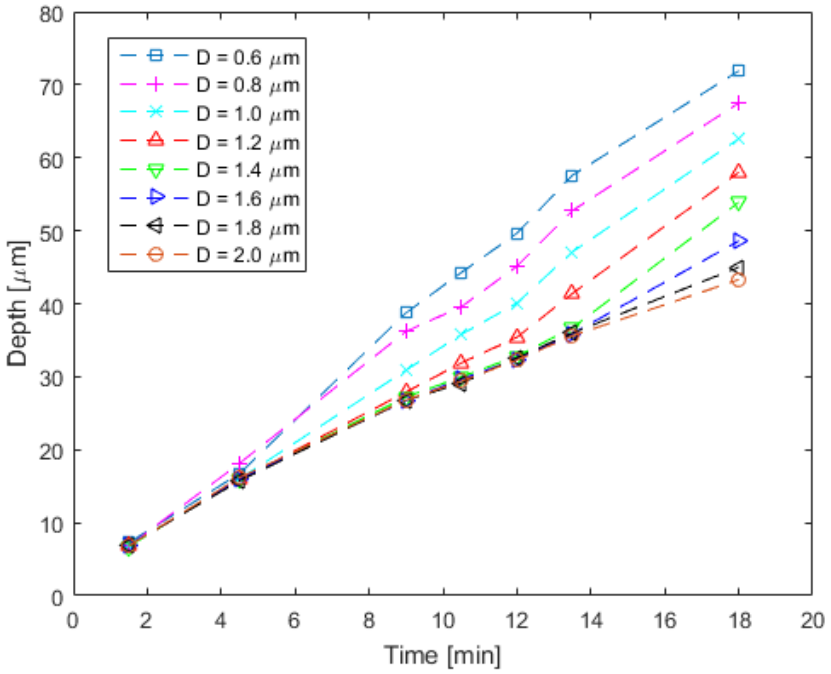


Figure 3.4: Depth of the channel during single step DRIE. The spacing between neighboring holes are varied from 0.6 µm to 2.0 µm in 0.2 µm steps.

The results show that the etch rate increases for smaller D. Although the detailed physics of this process is yet to be understood, it is likely that the merging of neighboring holes causes more gas to exchange inside the holes which results in a faster etch rate. The merging of the holes was confirmed by comparing SEM pictures. As an example, in figure 3.5 are the cross sections of the channels at 4.5 min for D = 0.8 µm and 1.8 µm. Figures (a) and (c) refer to the cross section that looks at the individual rectangular holes from the side and the figure with (b) and (d) refer to the cross section that look inside through the channel. In figure 3.5-a for D = 1.8 µm, the holes are not merged together, while in figure 3.5-c the holes are merged together. In figure 3.5-d the very thin vertical lines are the residues of the wall that used to be in

between each hole, which corresponds to the location shown with a red arrow in figure 3.5-b-2.

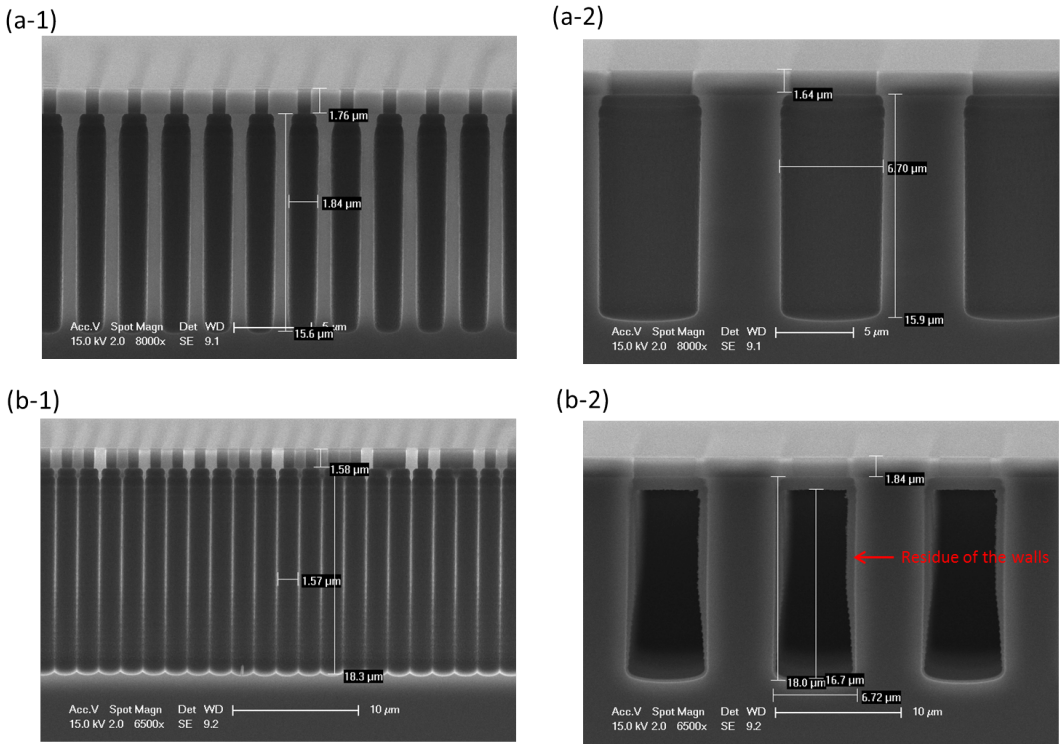


Figure 3.5: 4.5 min of etching with single step DRIE with the spacing between etch hole as (a) 1.8 µm and (b) 0.8 µm.

Based on the fact that the etch rate increases as the holes merge, conversely it is also possible to estimate when the holes merged by comparing it to the etch rate when the holes did not merge. For this purpose, Δ was defined as the difference between the etch rate when the holes merged to when the hole did not merge at all. In figure 3.6 Δ is plotted against the total etch time, and it is clear that Δ begins to increase, when the holes begin to merge. For instance, for sub-micron size D the holes are merged immediately within the first 2 to 3 min of the process.

The decrease in the thickness of SiO_2 hard mask during the single step DRIE was also measured (Fig. 3.7). This provides information on how much SiO_2 is necessary for etching to a certain depth in the DRIE process. The measured data was fitted with a 1st order polynomial, and the slope of the curve was $-0.09\,\mu m\,min^{-1}$ with a y-intercept at 2.1 µm. This is equivalent to an SiO_2 etch rate of 1.5 nm/ sec which is quite high for a DRIE process. Since there are no chemical reactions that etches SiO_2, this high etch rate of SiO_2

is purely due to the mechanical bombardment of the ions in plasma, caused by the high bias that is applied during the DRIE process.

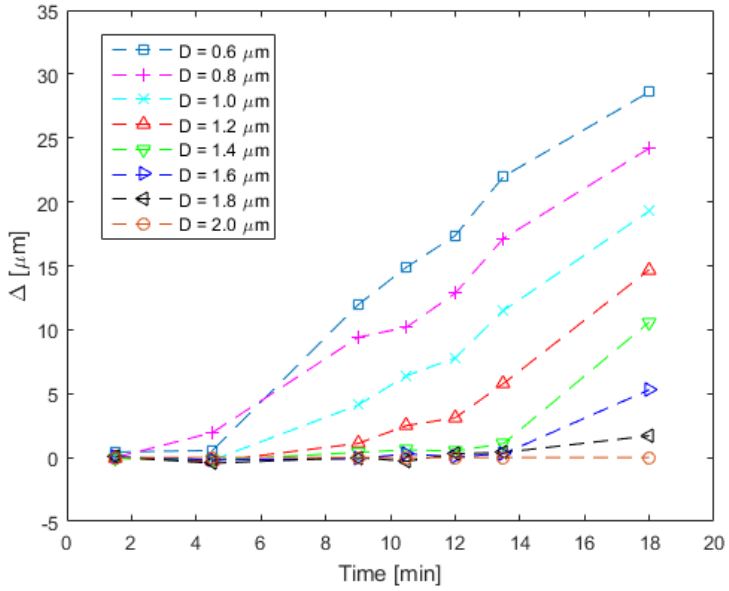


Figure 3.6: Δ is the depth of the channel subtracted from the the depth of the channel when D is 2.0 µm. $\Delta = \text{Depth}|_{\text{D=0.6,0.8,1.0,1.2,1.4,1.6,1.8,2.0 µm}} - \text{Depth}|_{\text{D=2.0 µm}}$

3.3.2. EMC fabrication results

The EMC were fabricated with two different widths - 10 µm and 100 µm. These channels were fabricated using two different designs of the mesh hard mask. One design consisted of hexagonal holes and the other design consisted rectangular holes. The detail of the dimension of the design are shown in figure 3.10.

The channels were fabricated with the same process flow given in section 3.2. The test was conducted with 12 wafers with different DRIE cycle numbers - 5, 10, 20, 40, 60, 70, 80, 90, 100, 110 and 120 cycles. Figure 3.9 shows the depth of the channel against the total etch time. The total etch time is defined in the same way as in the previous section. The average etch rate is summarized in table 3.1.

In table 3.1 to compare the result of the hexagonal pores to the rectangular pores a parameter called the open area ratio (OAR) was introduced. The OAR is a parameter that is often used for perforated sheets, and reflects how much of the sheet is occupied by holes [26]. The OAR of the hexagonal pores was 26.7 % (Fig. 3.10-left) and for rectangular pores the OAR was 46.5 % (Fig.

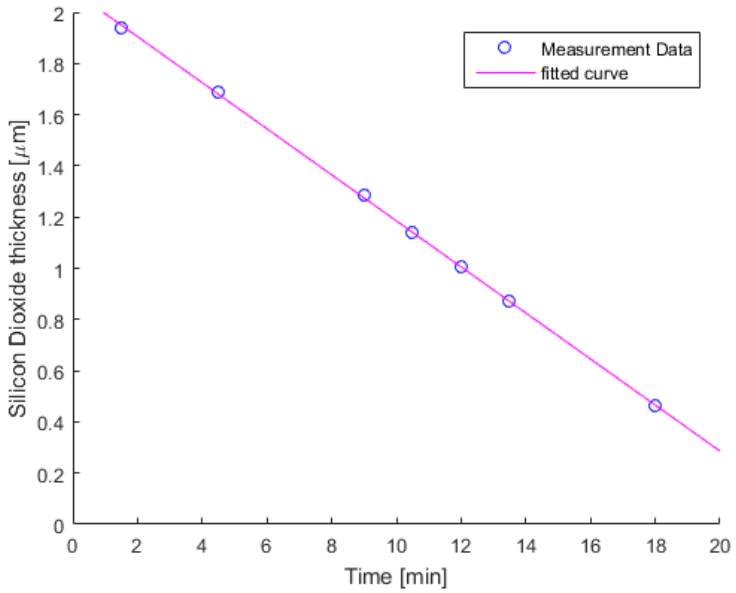


Figure 3.7: The decrease in the thickness of SiO_2 hard mask during the single step DRIE

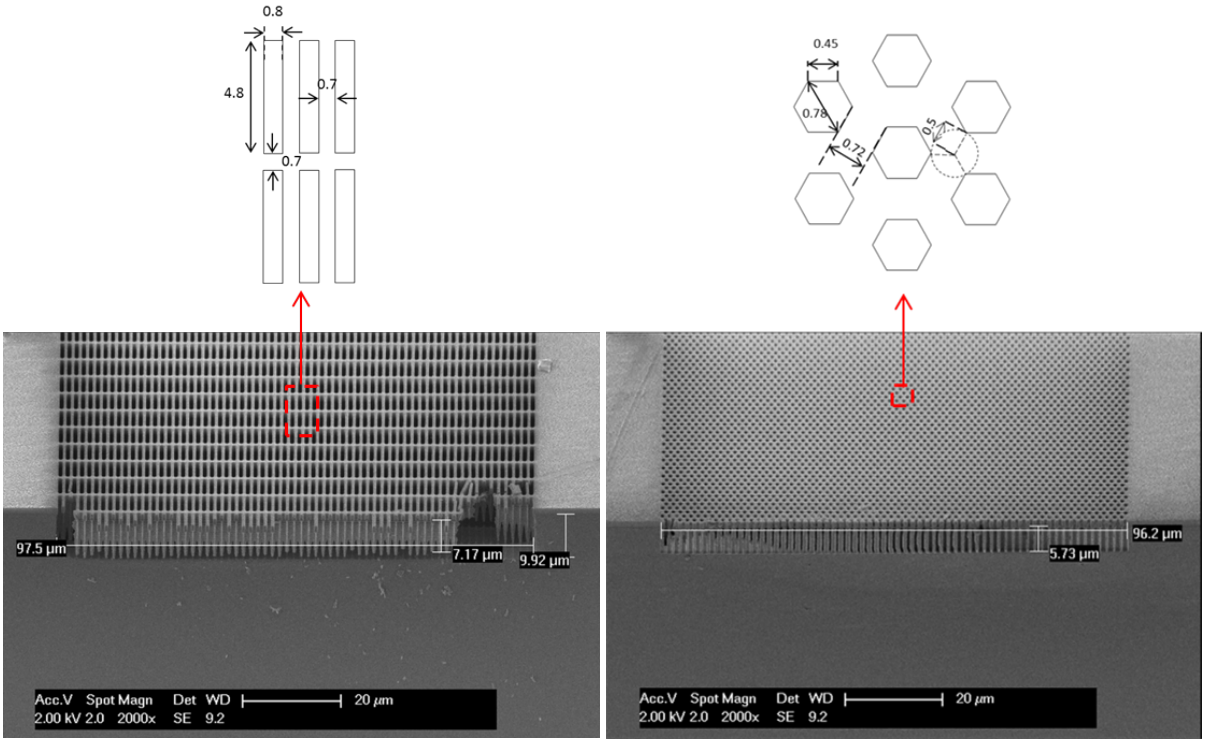
Table 3.1: Comparison of channel etch rate for different width and design for the mesh hard mask

Channel width	Hexagonal Pores (26.7 %)	Rectangular Pores (46.5 %)
10 µm	2.0 µm min^{-1}	4.1 µm min^{-1}
100 µm	2.3 µm min^{-1}	5.0 µm min^{-1}

3.10-right). When the channel width was changed from 10 µm to 100 µm, the etch rate did not increase as much. On the other hand, when the OAR of the channel increased the etch rate increased substantially. Accordingly, the OAR of the channel was found to have a larger influence on the etch rate compared to the channel width.

During the experiment, sharp thin pieces of silicon formed either at the top or the bottom of the channel during DRIE (Fig. 3.10). For convenience, this will be called ”icicle” from now on. These icicles are undesirable for the fabrication of EMC because it will distort the microfluidic flow and potentially rip the cells if they are left inside the channel. In order to completely remove the icicles, DRIE process must be done for a long enough time.

To investigate how long an etch time is needed to remove the icicles, the length of the icicle was measured (Fig. 3.11). The result showed that after 10 to 12 min of DRIE the length for both types of icicles became shorter than 2 µm. From this result, at least 10 min of etching is necessary in order to



(a) Rectangular holes (b) Hexagonal holes

Figure 3.8: The figures on the left is a SEM picture after 3 min (or 20 cycles) of single step DRIE was performed.

remove all of the icicles.

To investigate if the icicles can be removed earlier, a final experiment was conducted by varying the silicon etch per cycle as 8 s, 10 s and 12 s while the other parameters (passivation break through time (1 s) and the deposition time (1.2 s)) in each cycle were kept the same. The mask had the same rectangular mesh but the channel width was 50 µm. The DRIE cycle number was varied so that the total etch time would be approximately the same. By increasing the etch time per cycle while keeping the total etch time the same, the relative amount of passivation deposition would decrease and thus it was presumed that the icicles can be removed earlier. Thus, for a silicon etch of 8 s, 10 s and 12 s per cycle the total number of cycle was 60, 49 and 42 cycles respectively and the total etch time was 9 min. From this experiment the side wall etch rate was plotted against the silicon etch per cycle (Fig. 3.12). To calculate the side wall etch rate, the largest width of the EMC cross section was used and subtracted from the initial width (48 µm) and divided by 2. From figure 3.12 there is an increase in the sidewall etch rate when the silicon etch

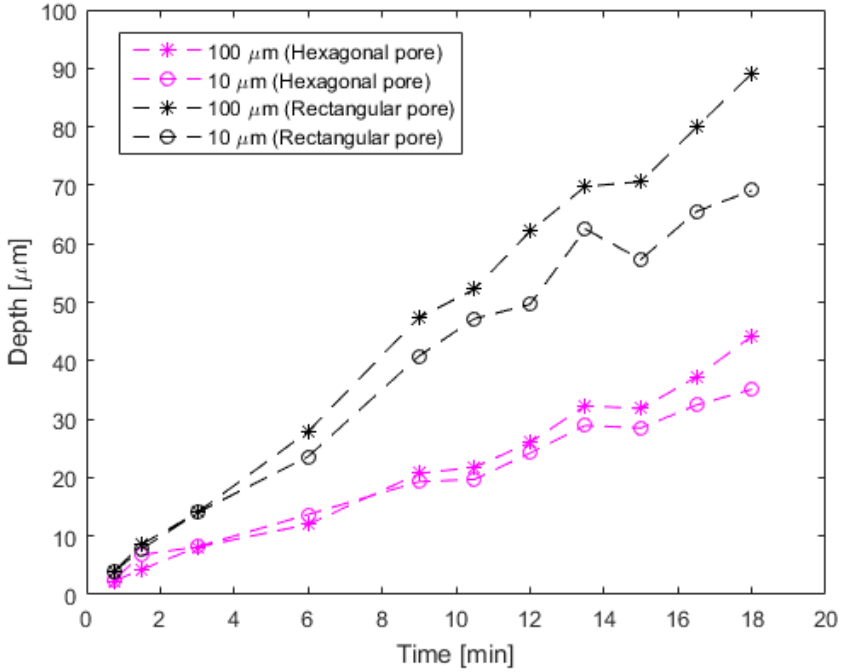
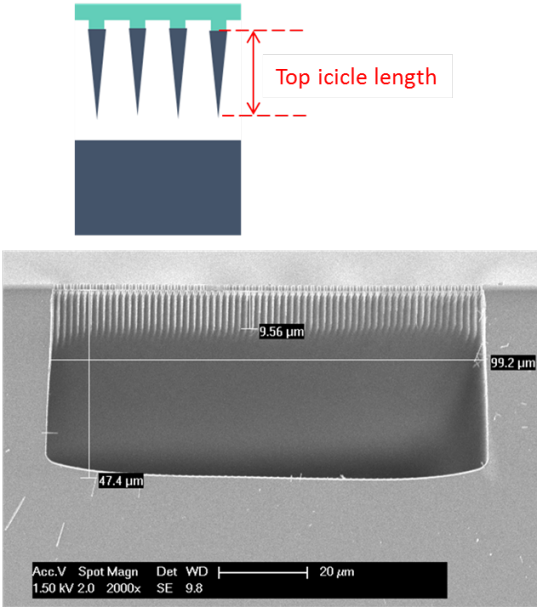
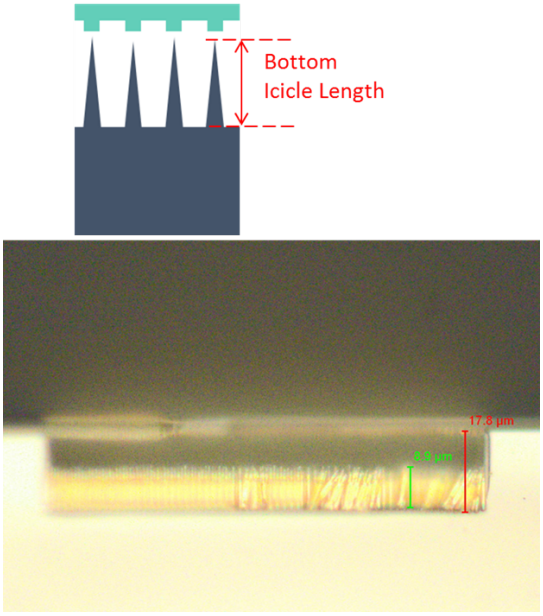


Figure 3.9: The EMC depth against total etch time for different width and design of the mesh hard mask

per cycle is increased. This is due to the decrease in the amount of passivation that was deposited. The higher the sidewall etch rate the easier it is to merge the channels beneath the mesh, however this results in a notched profile of the EMC as shown in figure 3.13. Considering this trade off, 8 s of silicon etch was used for the fabrication of the device.



(a) Top icicles that formed when rectangular pores were used for the mesh hard mask.



(b) Bottom icicles that formed when hexagonal pores were used for the mesh hard mask.

Figure 3.10: Two types of icicles. For both situation single step DRIE for 60 cycles were used.

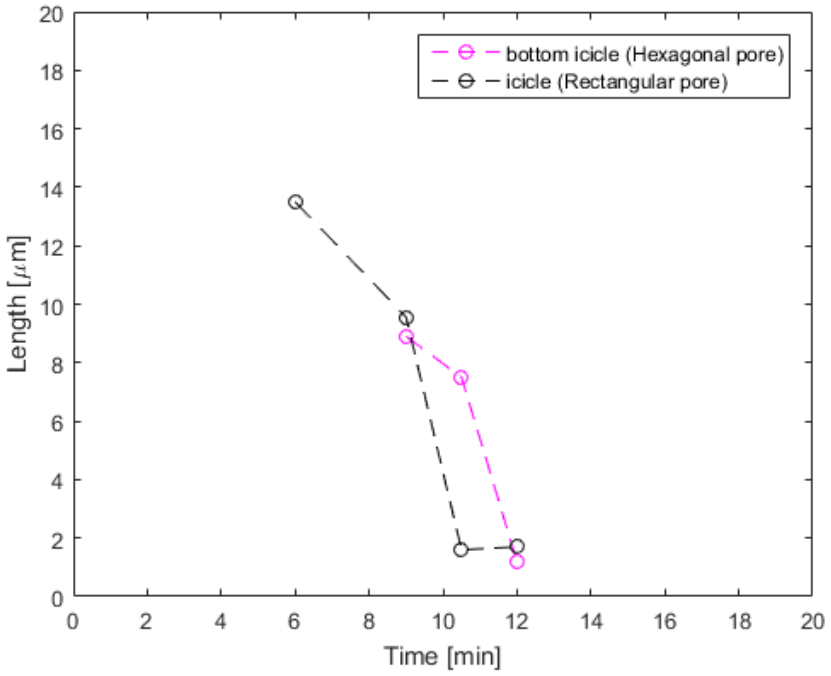


Figure 3.11: Icicle length for hexagon and rectangle

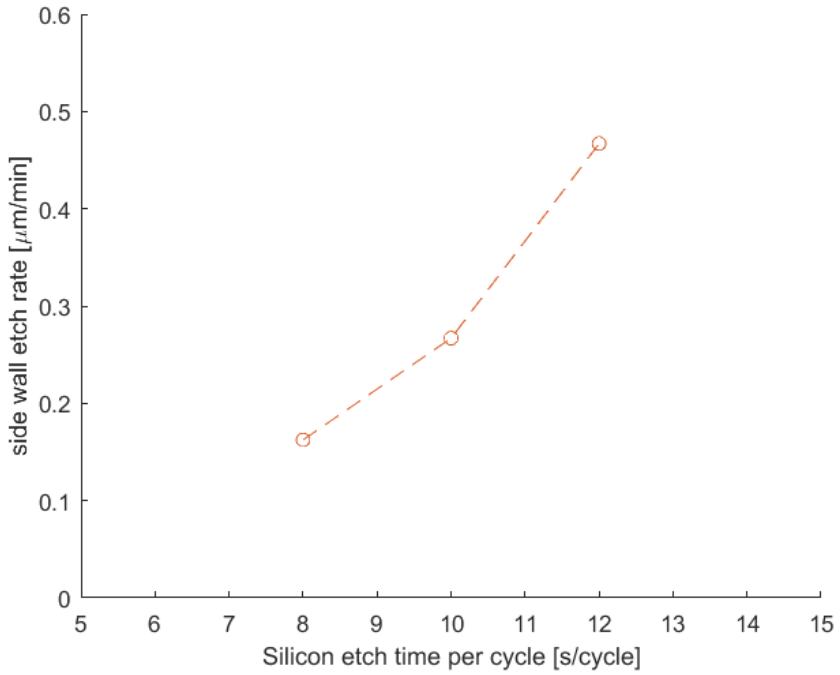


Figure 3.12: The side wall etch rate against the silicon etch rate per cycle

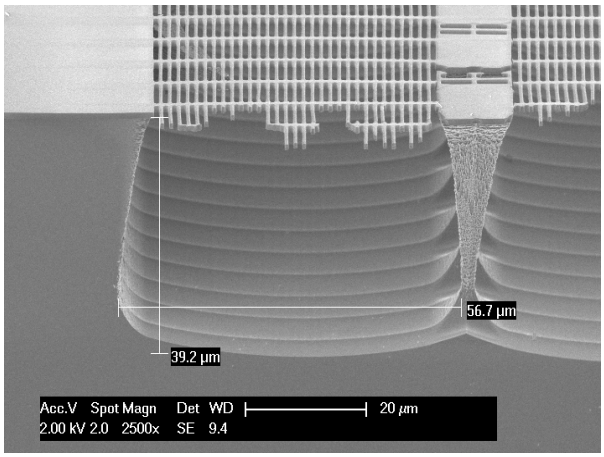


Figure 3.13: The total etch time was 9 min and the silicon etch per cycle was 12 s

3.4. Conclusion

For the fabrication of the EIEMC in the next chapter, the EMC must conform to the following requirements: (1) 40 µm deep, (2) vertical sidewalls and (3) no icicles. From these requirements the thickness for the SiO_2 hard mask and DRIE parameter (time, silicon etch per cycle) must be decided.

To fulfill the first requirement, at least 10 min for rectangular pores and 20 min for hexagonal pores is needed (Fig. 3.9). Assuming that a SiO_2 hard mask of 500 nm should remain after the DRIE, an initial thickness of 1.4 µm of SiO_2 hard mask is necessary for rectangular pores and 2.3 µm of SiO_2 hard mask is necessary for hexagonal pores.

For the second requirement a silicon etch equivalent or less than 8 s per cycle should be used to limit the tapering of the wall (Fig. 3.12). Since silicon etch time less than 8 s per cycle was not investigated, this was kept at 8 s per cycle.

For the third requirement, the DRIE must be at least 10 min (Fig. 3.11). This requirement is already achieved through the first requirement and does not have to be considered any further.

The parameters of DRIE process to fabricate the required EMC profile is summarized in table 3.2.

Table 3.2: General working range to fabricate the required EMC profile which is 40 µm deep with vertical sidewalls and has no icicles.

	DRIE parameter for depth of 40 µm		SiO_2 thickness
	total etch time	number of cycles	µm
Rectangular pores	>10 min	>70	>1.4
Hexagonal pores	>20 min	>140	>2.3

3.5. Mechanism of side wall etch

The selectivity of Si to SiO_2 in this particular recipe is approximately 30. For other recipes the DRIE can achieve much higher selectivity such as 100 to 200. In the application for this thesis this is not a problem. However, if deeper structure is needed this poses a problem because a thicker hard mask must be used and a thicker hard mask is more difficult to pattern with submicron feature size. In this section an experiment using a lower bias was conducted to clarify the reason why the high substrate bias was needed to fabricate the EMC in a single step.

From previous results from single step DRIE, it is known that the holes were merged after the first two to three minute of etching (Section 3.3.1). To replicate this effect an isotropic etch was used to merge the holes beneath the mesh hard mask. In addition, a low biased DRIE was used in the following step. Figure 3.14 is the result after 2 min of isotropic etch followed by a 13 min (or 100 cycle) of low biased DRIE through a mesh hard mask of hexagonal pores. Table 3.3 shows the DRIE parameter for the first isotropic etch and the second low biased DRIE along with the previously used single step DRIE. From figure 3.14 the depth of the channel was 37.6 µm [1] and this is equivalent to an etch rate that is 2.5 µm min^{-1}. This is approximately the same etch rate that was seen for single step DRIE (Table 3.1). However, it is clear that the icicles appeared along with an increase in passivation residue which was not the case when the single step DRIE recipe was used.

As one theory why the single step DRIE worked and was able to remove the icicle while etching deeply, in single step DRIE the high substrate bias increased the sputtering component of DRIE which helped to remove the passivation on the icicle. This is the reason why when low bias was used in figure 3.14, the area right beneath the hexagon where the passivation was removed was etched deeply.

It is worth noting that the substrate bias voltage is not the only parameter that was changed as shown in table 3.3. For a more accurate analysis, the DRIE parameter must be tuned individually to identify the main cause of the appearance of the icicle. Nonetheless, if we assume that the icicle disappears during single step DRIE because of the sputtering of silicon, the method pur-

[1] The value of the height (26.6 µm) in figure 3.14 is the length seen from a 45° angle without correction

Table 3.3: The detail of the recipe used in DRIE

Description		Two step etch						Single step DRIE		
		1st Isotropic etch			2nd low biased etch					
Program Name		DTC_IsoEtch_120sec			Toshi_flat_bottom			TMPHARtrench		
Platen Temperature	°C	20			0			0		
Step Name		Strike1	Strike2	IsoEtch1	Depo	Etch_1a	Etch_1b	Depo	Etch_1a	Etch_1b
Process Time	Secs	5	5	120	1.5	2	6	1.2	1	8
Process Pressure	mTorr	50	75	100	40	25	25	40	30	30
Platen HF Power	W	0	0	0	0	100	40	0	175	60
Primary Source Power	W	2500	2500	2500	2200	2200	2200	2500	2500	2500
Secondary Source Power	W	0	0	0	0	0	0	500	500	500
Inner current	Amps	10	10	10	10	10	10	0	0	0
SF6 Flow	sccm	0	250	500	1	350	350	1	400	400
C4F8 Flow	sccm	0	0	0	280	1	1	220	1	1
O2 Flow	sccm	0	0	0	0	0	0	0	0	0
Ar Flow	sccm	250	250	0	0	0	0	0	0	0

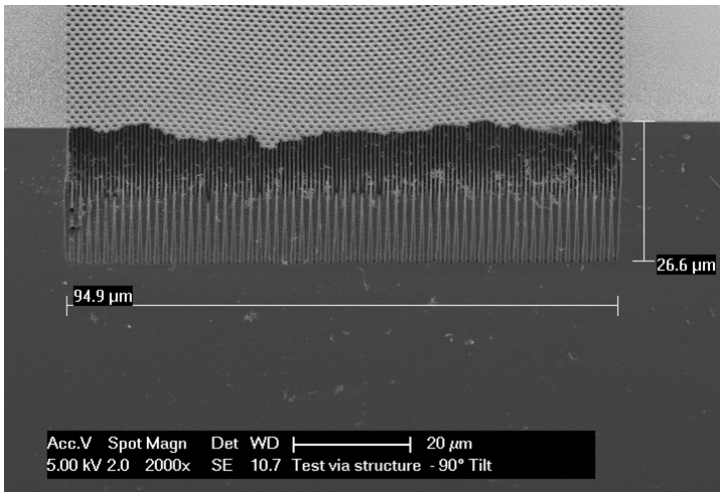


Figure 3.14: 2 min of isotropic etch followed by a DRIE with a lower substrate bias.

posed in this section of using an isotropic etch followed by a low biased etch would not work because the passivation on the icicle cannot be removed and the icicle will form.

4

Fabrication of Electrode Integrated Embedded Microchannel

To fabricate the EIEMC (Electrode Integrated Embedded Microchannel) aluminium interconnects, bond pads, etc. must be added after the EMC to connect the electrodes to external electronics. Various prefabrication tests were performed in section 4.1 to confirm if it is possible to integrate these additional steps. In section 4.2, a fabrication method was designed based on these tests. In section 4.3, the fabrication results are explained. In section 4.4, a conclusion is drawn from the fabrication results. The electrical measurement will be discussed in the next chapter (Chapter 5).

4.1. Prefabrication test

Prefabrication tests were performed to check if the EIEMC fabrication process is feasible or not. In other words, these tests will clarify potential failure modes in the EIEMC process before the actual process is started to prevent redesigning of the masks. These tests made the experiment cost effective by minimizing the redesign cost of masks.

4.1.1. Inlet/Outlet test

To read-out the signals from the electrodes, aluminium interconnects must be fabricated on top of the EMC to read-out the signals. This implies that additional lithography steps must be compatible with the EMC. The compat-

ibility of successive lithography steps were never considered in the previous research and is investigated in this section.

Here, three different methods to open the inlet/outlet were considered to see if it can withstand the successive steps. The first method was to fabricate the inlet/outlet simultaneously when the EMC was fabricated. The second method was to reopen the inlet/outlet after the mesh was once closed. The third method was to closed the mesh from the front side and open the inlet/outlet from the backside of the wafer. These three method are schematically represented in figure 4.1. Out of the three methods, method 1 is the same method which was used in previous research. The mask was readily available and did not cost any time or money to design the inlet/outlet. In this section, method 1 was tested if aluminium can be patterned after the EMC was fabricated.

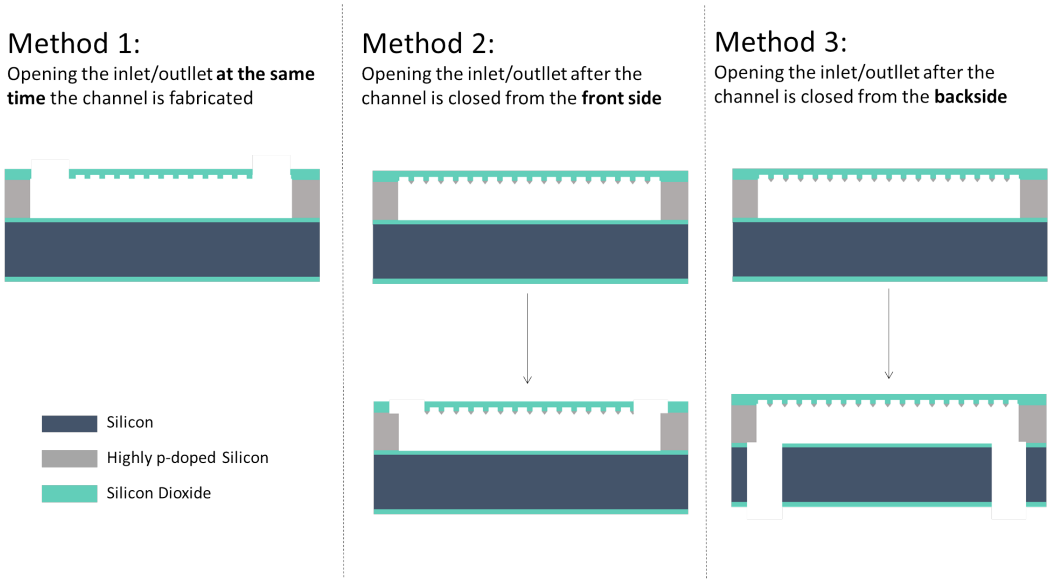


Figure 4.1: Inlet opened simultaneously when the channel was being fabricated.

Figure 4.2 is the reproduced result using method 1 on a single side polished wafer. The channel was sealed afterwards with 2 µm of PECVD SiO_2 and 2 µm of Al/Si (1 %) was deposited at 50 °C. Subsequently, photoresist SPR3012 1.4 µm was spin coated. As a result, the photoresist drooped inside the 150 µm diameter holes of the inlet/outlet and cause wide areas of the wafers to be uncovered with photoresist as shown in figure 4.3-a . As an alternative, spray coating was also tested and the result is shown in figure 4.3-b. In this case, photoresist uniformity was better than spin coating but there was still a non-uniform coating near the inlet/outlet of the channel.

The wafer that was spin coated with photoresist was cleaned with acetone, rinsed and spin dried. Figure 4.4 shows the same wafer after it had been stored inside the wafer box after a day. It was found that the aluminium corroded due to the residual water remaining inside the holes of the channel after the spin drying step.

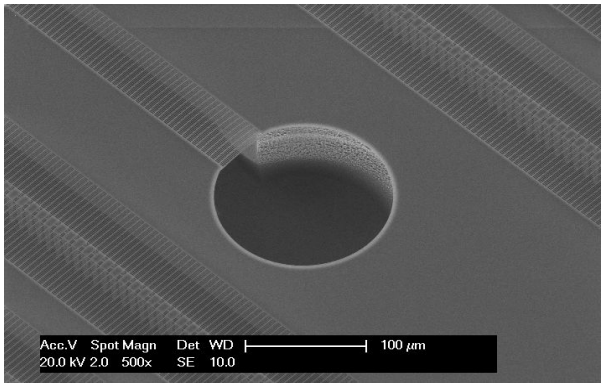
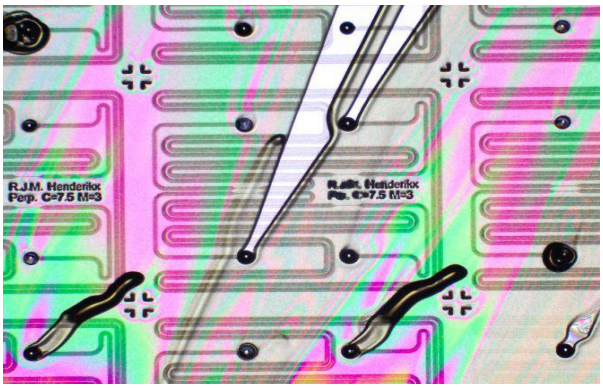
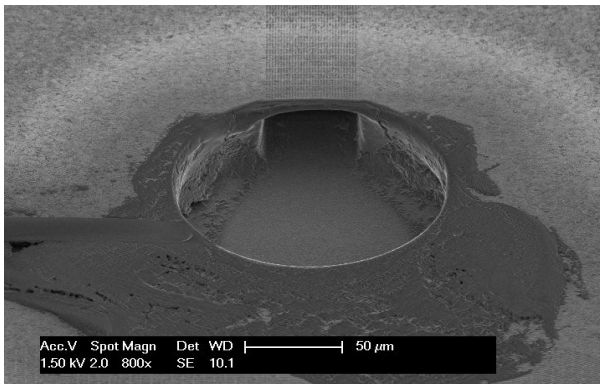


Figure 4.2: Inlet/Outlet opened with method 1; simultaneously etching the inlet/outlet along with the EMC.



(a) After spin coating 1.4 µm of SPR3012 photoresist.



(b) After spray coating negative photoresist.

Figure 4.3: Results after lithography steps used on wafers with channels fabricated using method 1 and subsequently sealed with PECVD silicon dioxide and covered with Al/Si(1 %)

In summary, using method 1 for the fabrication of the channel and subsequently fabricating the aluminium interconnect was possible if spray coating was used instead of spin coating. The non-uniform coating of photoresist will be not important if it does not occur near the aluminum interconnect. However, the spray coating procedure is manual and laborsome, thus for multiple lithography steps and numerous wafers method 1 should be avoided. It was

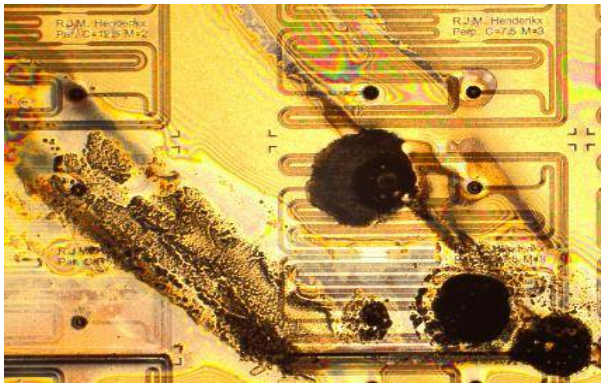


Figure 4.4: Inlet/Outlet opened with method 1.

also found that a heating step to evaporate the water trapped inside the channel was necessary for every rinsing step afterwards because it will corrode the aluminium.

In conclusion, method 2 or 3 should be investigated for the EIEMC fabrication. Referring back to figure 4.1, method 2 is clearly more simple to fabricate than method 3. Nonetheless, method 3 is advantageous because the microfluidic and electronics can be isolated to be on each side of the wafer. On the other hand, using method 3 will make it difficult to integrated an observation port to the device (Section 4.1.3). The fabrication result of the inlet/outlet using method 2 will be presented in section 4.3. Method 3 was also tested but due to the limitation in time it was not completed.

4.1.2. DRIE cycle number test using SOI wafers

In chapter 3 the detailed parameters for the DRIE was derived using a single side polished wafer and summarized in table 3.2. According to this table when a mesh hard mask with rectangular pores were used, more than 70 cycles was needed to fabricate the EMC. Here, two SOI wafers, the same ones which will be used for the fabrication of EIEMC, were treated with different DRIE cycle numbers to confirm if this was also valid for SOI wafers. This SOI wafer has 40 µm of device layer, 1 µm of BOX layer and 380 µm of backside handling wafer.

The cross section of the device was taken after the mesh hard mask was covered with PECVD SiO_2 followed by a step to etch the via. Figure 4.5-a,b are when 70 and 80 cycles of DRIE was performed, respectively. In both cases the EMC is landing on the BOX layer and no icicles were seen. However, notching occurred near the BOX layer that was not seen when single side

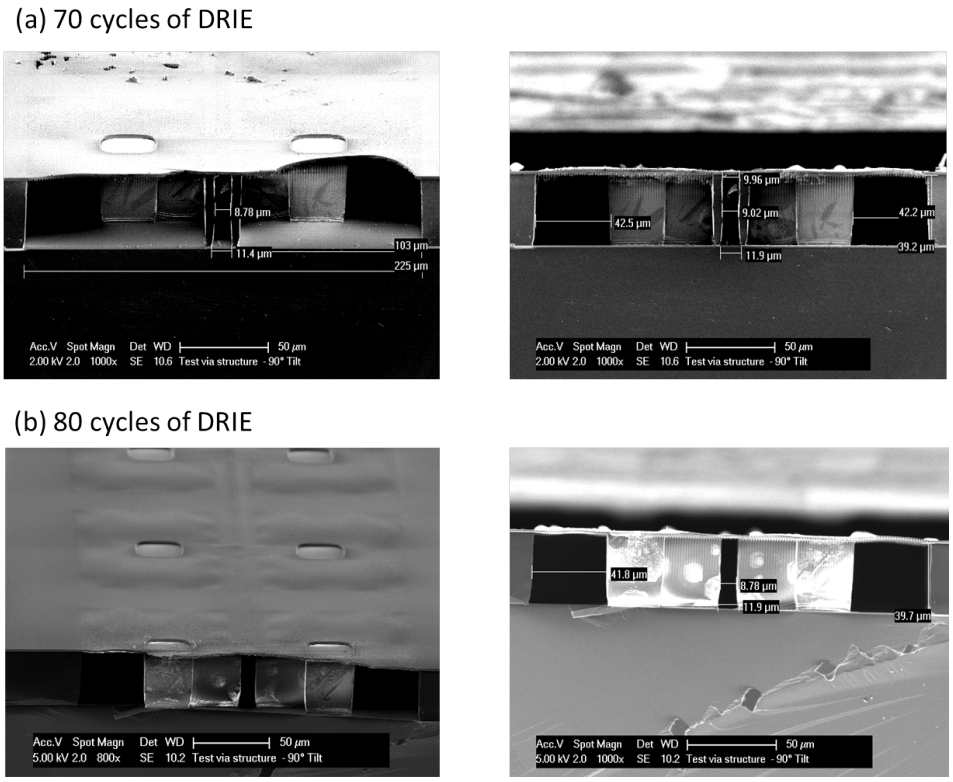


Figure 4.5: (a) After 70 cycle of DRIE seen from an angle -left and cross section - right. (b) After 80 cycle of DRIE seen from an angle - left and cross section - right

polished wafers were used. Notching is when the material being etched begins to charge so that the incoming are deflected from the original direction and etch the sidewalls [27]. This mainly occurs with non-conducting materials such as SiO_2. In this case, the BOX layer was positively charged and deflected the SF_5^+ ions to the sidewalls.

In the EIEMC fabrication 70 cycles was used instead of 80 cycles in order to minimize the effect caused by notching.

4.1.3. Observation port test

The observation port is an opening on the backside of the wafer to monitor the behavior of the cell in the squeezing channel. In figure 3.1-d a schematic representation of the observation port is presented. In previous research by R. Stoute et al.[12], the observation port was monitored with an inverted microscope in combination with a high speed camera to measure the cell velocity inside the channel. In this research fabricating the observation port will enable the cross referencing of the results obtained from the electrical measurement with the result obtained from the optical inspection. Here a test

was conducted to investigate the DRIE cycle number needed to fabricate the observation port for the EIEMC.

The test began with a 400 µm thick double sided polished wafer which was thermally oxidized to form 1 µm of thermal SiO_2 on the front and backside of the wafer. Additional 4 µm of PECVD SiO_2 was deposited on the backside of the wafer and was subsequently patterned with the observation port design. Using DRIE, 400 µm of silicon was etched with 120 cycles from the backside to land on thermal SiO_2.

Figure 4.6-left shows the result after the DRIE at wafer level and it is clear that some parts of the wafer are transparent. Figure 4.6-right is a magnified photograph of the observation port with a SEM. In the SEM image it is clear that there are some residues on the bottom of the hole. Since this was transparent in the optical image, this is the thermal SiO_2 layer that was formed during the initial thermal oxidation step.

From this result, the DRIE cycle number for the fabrication process of the observation port can be calculated. Assuming that the etch rate is constant, the number of cycles needed to etch 380 µm of silicon is 114 cycle.

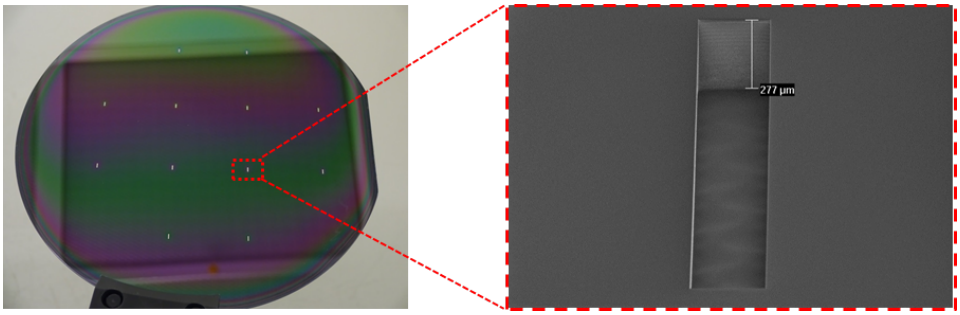


Figure 4.6: Backside window after DRIE. (a) Wafer level view (b) Zoomed view of the area shown in the box. The inner area of the rectangle was discolored and transparent.

4.2. Fabrication Method

The device fabrication starts with a double side polished SOI wafer with a 40 µm thick device layer that is doped with high boron concentration to a low resistivity < 20 mΩ cm, a 1 µm thick BOX layer and a 380 µm thick handling wafer with 1 µm of oxide. Ion implantation of boron was used on the device layer with an energy of 15 keV and a dosage of 5×10^{14} atoms/cm^2 which was subsequently annealed for 30 min at 950 °C. This was to form an ohmic contact to the aluminum interconnect at later stages of the processing (Fig 4.7-a).

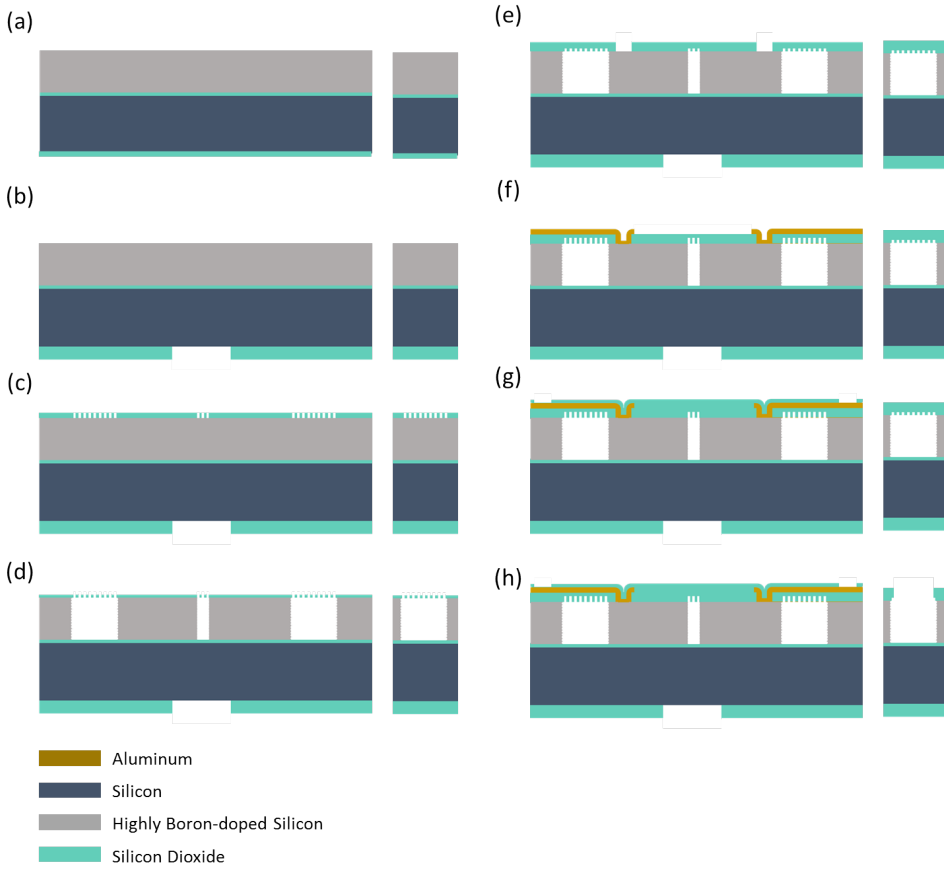


Figure 4.7: Process flow of the Electrode Integrated Embedded Microchannel (EIEMC)

First, a 4 µm thick layer of PECVD SiO_2 was deposited on the backside of the wafer and patterned with the mask for the channel observation window (Fig. 4.7-b). On the device layer, a PECVD SiO_2 layer with a thickness of 1.7 µm was deposited and patterned using a mask with a mesh of small rectangular openings of 0.8 by 4.8 µm at the location of the microchannel and around the electrodes (Fig. 4.7-c). PECVD SiO_2 is used to induce less stress

into the layer. This was to prevent the breakage of the SiO_2 layer when the membrane was suspended in the later stage of the process. Next, the single-step DRIE [25] was performed to etch trenches down to the BOX layer with 70 cycles (Fig. 4.7-d) which merged the individual holes beneath the mesh to form a single channel. The remaining SiO_2 mesh was sealed by a deposition of 2.0 µm thick PECVD SiO_2 layer. This was patterned with the via openings to expose the surface of the silicon-based electrodes (Fig. 4.7-e) which was subsequently covered with 2.0 µm thick Al/Si (1 %) layer and patterned to form the electrical interconnects and the bond pads (Fig. 4.7-f). Another deposition of 2.0 µm thick PECVD SiO_2 was performed and patterned to expose only the surface of the bond pad (Fig. 4.7-g). Finally, the microfluidic inlet/outlet were etched open (Fig. 4.7-h).

4.3. Fabrication Result

In this section, first the fabrication result of the device will be presented. Afterwards, the problems that occurred during the fabrication will be explained. The detailed fabrication process flow chart with all of the modifications is given in Appendix D.

4.3.1. Overview of EIEMC fabrication result

The fabricated device has a microfluidic channel near the center of the die and 14 bond pads for external electrical connections (Fig. 4.8-left). Six pairs of electrodes were fabricated along the channel and were spaced apart by 200 µm from each other (Fig. 4.8-right). Two ground connection were made on each end of the channel to ground the bulk. The design included three different electrode width - 5, 10 and 20 µm. The die size was fabricated to be 20 by 20 mm which was rather large for standard IC based fabrication process. This was to accommodate for the working space necessary to manually attach the microfluidic adapter (Appendix C). The sealing of the device was tested with a microfluidic flow using a microfluidic pump. The test was aborted after 2 hours since there was no leakage and it was likely that a longer stress test will not lead to any device failure.

The cross section of the device was taken with an optical microscope and an SEM (Fig.4.9, 4.10). In the optical image we clearly see a difference in the color of different materials. For example, the aluminium has a rough

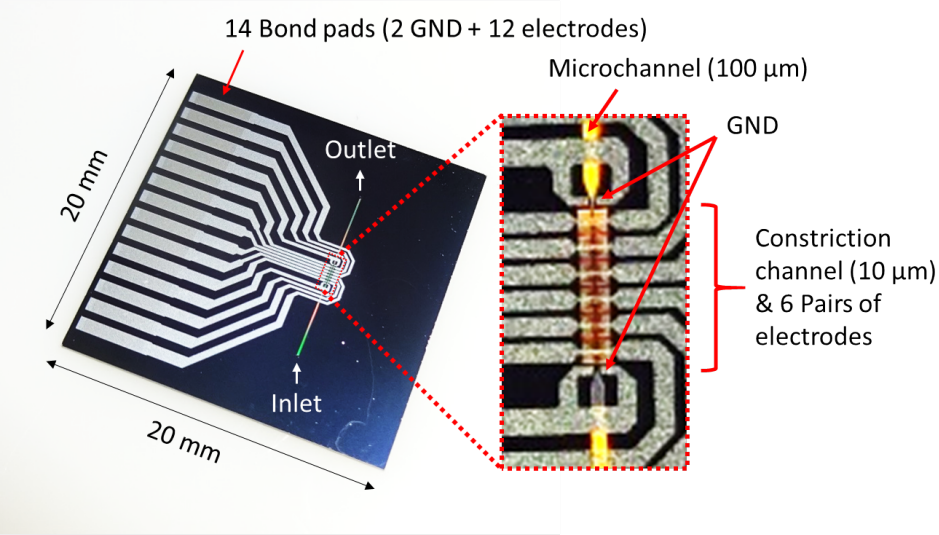


Figure 4.8: Fabricated device (Left). Close up image of the device (Right)

texture with a silver color and the silicon-based electrodes are brightly lit up in blue due to the reflection of the light on the BOX layer. These features are not obvious on the SEM image because the aluminium layer is actually cover by a 2 µm of SiO_2. On the other hand, the optical image is blurry due to the limited focus depth, whereas the SEM image clearly shows the void surrounding the electrodes and the clean landing on the BOX layer.

Another cross section is shown in figure 4.11. Icicles with a length of14 µm was observed that remained after the DRIE of 70 cycles which was not the case in previous tests as explained in section 4.1.2. On the other hand, notching which were previously seen did not appear. It is likely that the etch rate slowed down for DRIE compared to when the test was conducted. Additionaly, the preparation of the mesh hard mask for DRIE was different compared to the previous tests. Therefore, in future research it is advised that a test wafer with the same mesh hard mask as the processing wafers is used to check the DRIE recipe before the real device wafer is processed.

4.3.2. Stress issues caused by the deposition of Al/Si(1 %)

During the fabrication method mentioned in section 4.2 the process temperature for depositing Al/Si (1 %) on the SiO_2 membrane was compared for 350 °C and 50 °C. At 350 °C three wafers were processed and the SiO_2 membrane partially detached for 36 % of the die during this process. On the other hand, at 50 °C two wafers were processed and in average 10 % of the SiO_2 membrane

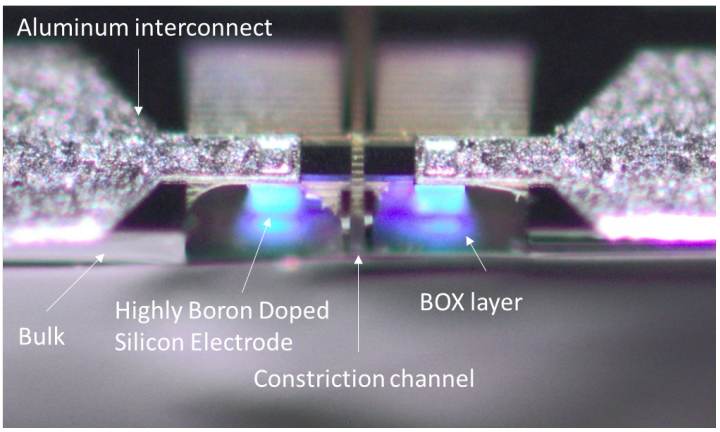


Figure 4.9: An optical microcope image of the cross section of the electrode and the constriction channel.

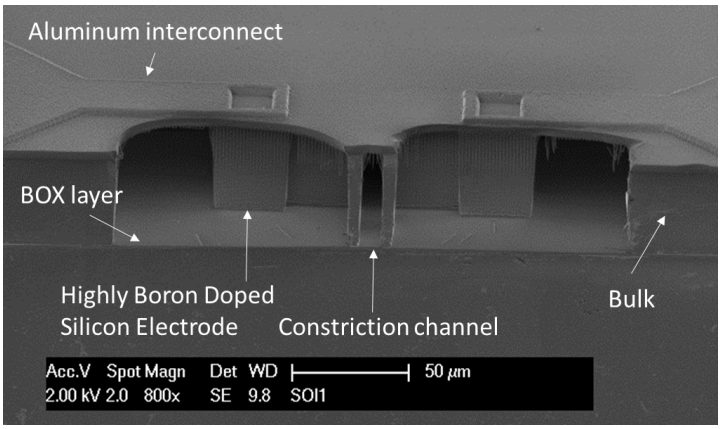


Figure 4.10: A SEM image of the cross section of the electrode and the constriction channel.

partially detached. Thus, it was clear that a lower temperature induced less stress to the wafer which increase the yield of the process.

The breakage of the membrane was only found nearby the inlet/outlet of the microfluidic channel for all cases. The design of the inlet/outlet may have an influence on the stress that is being induced. As a possible explanation, figure 4.12 is the inlet/outlet after it was opened with dry etch. When Al/Si (1 %) is deposited this part is closed with SiO_2 along with the other parts of the channel. From this figure we see that the design as a whole is circular, however since this was designed with a mesh hard mask of rectangular holes, it created multiple corners. These individual corners contributed to an increase in stress to the membrane and caused the membrane to break at this location more easily than other locations.

For future work the inlet/outlet should be designed with a rectangle if a mesh hard mask with rectangular pores are used. Moreover, if hexagonal

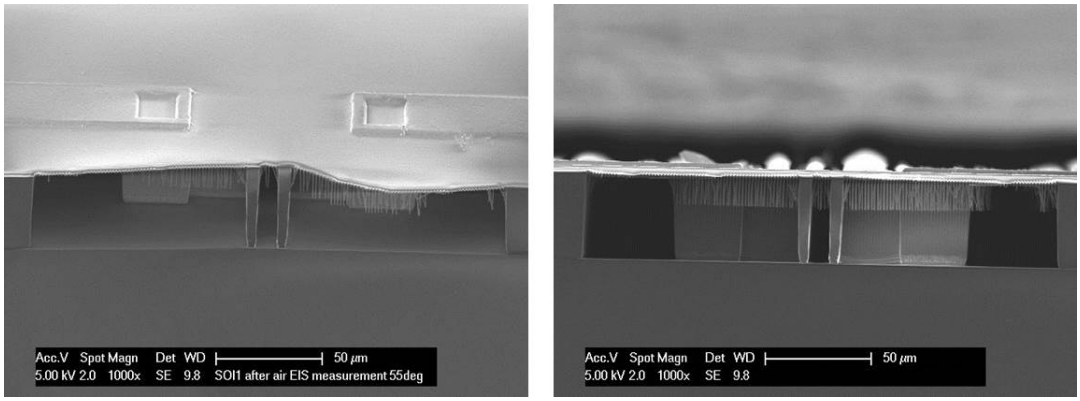


Figure 4.11: A SEM image of the cross section of the channel seen from an 55degree angle (Left) and the cross section seen from a 90 degree angle (Right). The icicle length was 14 µm.

pores are used this issue may not occur because hexagon has a symmetrical shape that can evenly distribute the stress to all directions.

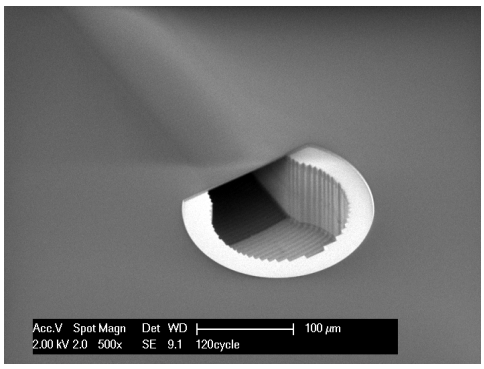


Figure 4.12: SEM image of the inlet/outlet after it was opened with dry etch. More stress is induced because there are many corners.

4.3.3. Oxide removal of the inner wall of the channel

After the device was completed an ac voltage was applied to one electrode and measured from the paired electrode. However, there was no measurable signal at the ouput whether the channel was filled with PBS, DI water or air. It was suspected that the PECVD SiO_2 to close the mesh went through the mesh and covered the electrode surface and insulated the electrodes. Here an experiment was conducted to confirm the existence of PECVD SiO_2 on the surface of the inner wall of the channel.

For this experiment, a device with a detached SiO_2 membrane was used. This device was broken in half and one side was dipped in buffered HF (BHF) 1:7 for 4 min, while the other was used as a control for comparison. It clearly

showed that the white blobs on the scallop that previously appeared (Fig. 4.13-a) were removed after the BHF 1:7 treatment (Fig. 4.13-b). Thus, the white blobs were identified as PECVD SiO_2.

In the actual fabrication process an additional wet etch step with BHF 1:7 to remove the PECVD SIO_2 on the inner walls of the channel was not used. The reason is that the BHF 1:7 has a fast etch rate and cannot be controlled well within the channel because the refreshment of the solution inside the channel is limited, while the the etch rate of PECVD SiO_2 on the surface of the die is constantly at a high rate because the solution can be easily refreshed.

As an alternative, vapor HF was used to etch the PECVD SiO_2 on the inner walls of the channel. During this treatment, vaporized HF would flow into the channel through the inlet/outlet and react with PECVD SiO_2 and the reaction would be stopped immediately by removing the HF vapor from the chamber. The result of vapor HF treatment for 3 min is shown in figure 4.13-c. The white blobs of PECVD SiO_2 that appeared previously is removed and the byproduct of the vapor HF which is SiF_4 can be seen. SiF_4 can be removed by heating the device on a hotplate at 200 °C for 3 min.

After the 3 min vapor HF treatment there was a measurable difference in the signal when PBS was inside the channel compared to air. Therefore, it was finally confirmed that the PECVD SiO_2 on the surface of the electrode was insulating the signals. Although this method works, this easily breaks or cracks the SiO_2 membrane covering the channel. Figure 4.14 is an image of the electrodes using an optical microscope before and after the treatment with 3 min of vapor HF. The device was dipped in solution and was found that these cracks did not cause any leakage. Therefor these cracks were not fatal for the operation of the device. Cracks were also found in the closing SiO_2 layer on top of the channels of the device as shown in figure 4.15. Interestingly the pattern of the cracks was always the same which was an arc of a length about 300 µm repeating one after another.

With regards to how long it is necessary to treat the structures with vapor HF, 2, 3, 5 and 10 min of vapor HF treatment was compared and 3 min was used because this had a high enough yield. Beyond this time, the membrane began to break and at 10 min the mesh hard mask reappeared. However it is still not clear if 3 min is enough to completely remove the PECVD SiO_2 from the inner walls of the channel.

Another experiment was conducted with a device with photoresist on the

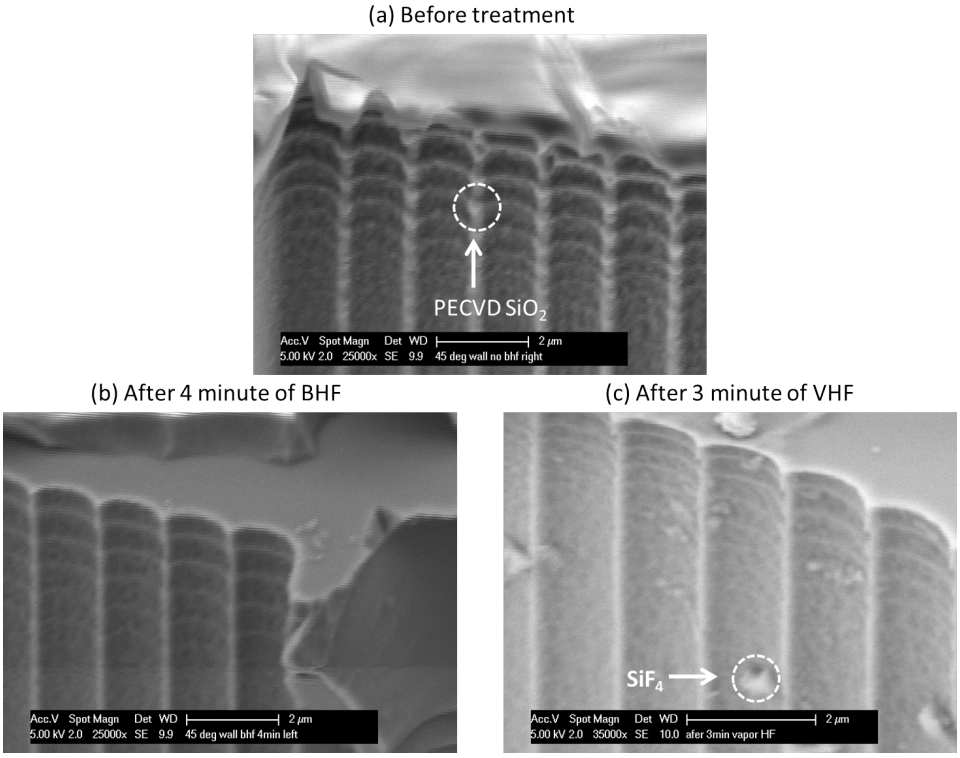


Figure 4.13: (a) Before treatment: PECVD SiO_2 is attached to the inner walls of the channel. (b) After buffered HF treatment for 4 min: PECVD SiO_2 is completely removed. (c) After 3 min vapor HF treatment for 3 min: The PECVD SiO_2 is removed but SiF_4; the residue of the vapor HF (VHF) treatment is attached to the surface of the channel.

surface with the inlet/outlet patterned on it and this was treated with vapor HF for 3 min . This did not show any significant improvement because the photoresist was permeable against vapor HF. The only difference was that the pattern of the PECVD SiO_2 on the surface was slightly different compared to when the photoresist was not there. This difference in the pattern is due to the vapor HF being trapped and accumulated between the photoresist and the surface of the die. It maybe possible that the amount of etching on the surface increased compared to when the photoresist was not there.

For future research, BHF 0.55 % should be investigated to etch the PECVD SiO_2 inside the channel. BHF 0.55 % has a lower etch rate than BHF 1:7 so this may be able to provide enough margin to control the etch rate of SiO_2 inside the channel. Another alternative would be to use low concentration HF and put the die on top of it with the inlet/outlet facing down and leave it for a long enough time (Fig. 4.16). The spontaneously evaporating HF will work alike the vapor HF treatment but with a more mild etch rate since catalysts such as alcohol is not present. However, there may be sever hazard

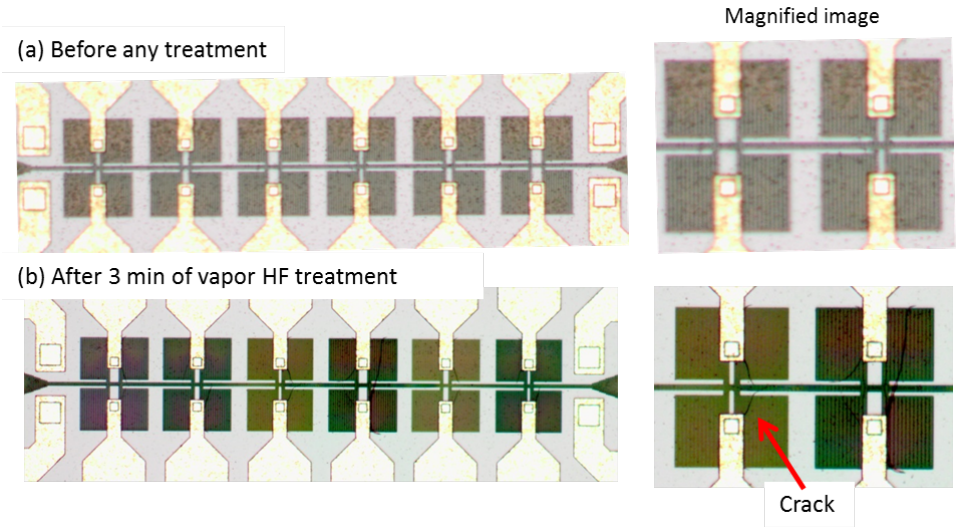


Figure 4.14: An image of the electrodes from above using a optical microscope before and after 3 min of vapor HF treatment. Cracks appear after the treatment as shown in the magnified image on the right with a red arrow.

issues to take into consideration, although theoretically it should work the same.

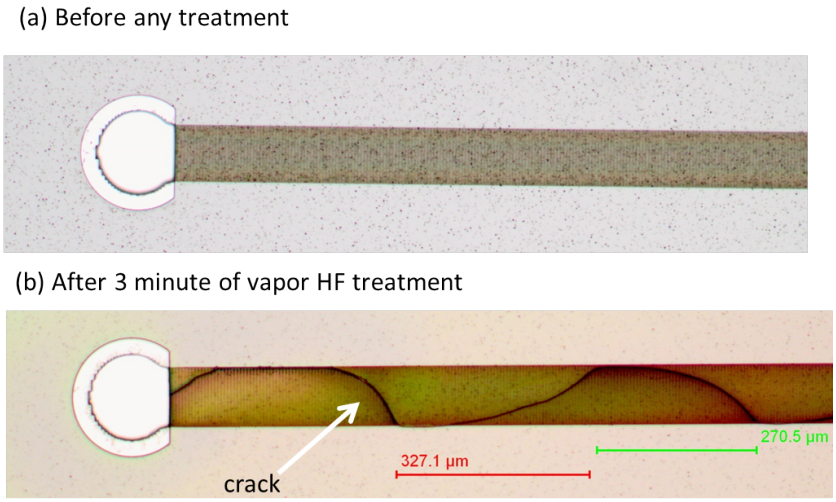


Figure 4.15: An image of the channel from above using a optical microscope before and after 3 min of vapor HF treatment.

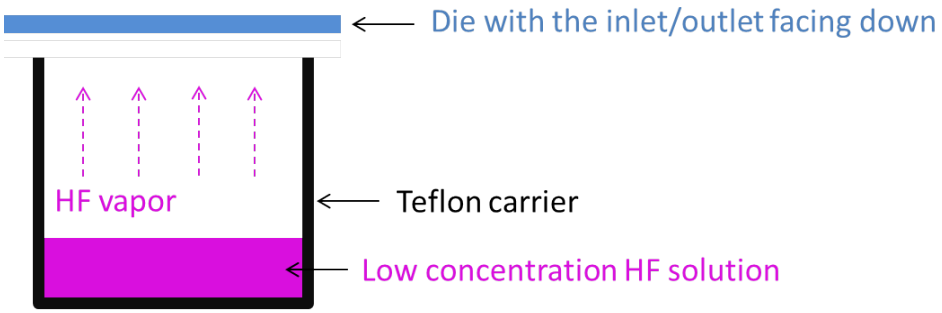


Figure 4.16: Use the evaporating HF from low concentration HF solution to etch the PECVD SiO_2 inside the channel at a mild rate.

4.4. Conclusion

In this chapter the EMC fabrication process was modified to incorporate steps such as via opening, aluminium interconnect patterning, bond pad patterning. This was executed by first conducting short loop tests to check the fabrication process in smaller parts. In this phase, it was found that the inlet/outlet should be fabricated in the last step.

From the results of short loop tests the EIEMC were fabricated. During the fabrication, there were two failure modes that were not anticipated initially; 1. High temperature stress during the deposition of Al/Si (1 %), 2. Insulation of the electrode caused by the PECVD SiO_2 on the surface of the electrode. The former issue was solved by using low temperature Al/Si (1 %) deposition. The latter issue was solved by using a final treatment of vapor HF to remove the oxide inside the channel.

5

Electrical characterization of EIEMC

In this chapter the EIEMC device was electrically characterized with various ways of stimulation and read out. Prior to all of the measurements, the device was always treated with 3 min of vapor HF and heated on the hotplate at 200 °C after the fabrication of the device. This was to remove the PECVD SiO_2 layer on the surface of the silicon electrode as explained in section 4.3.3.

In section 5.1 the impedance of the aluminium interconnect and channel impedance is determined. In section 5.2 an AC voltage stimulation at a single frequency is applied to the device and the output voltage is measured. In section 5.3 the characterization of the silicon electrode is discussed by using cyclic voltammetry and electrochemical impedance spectroscopy. In section 5.4 the conclusions from this chapter will be summarized.

5.1. Impedance measurement

For convenience, each bond pad is assigned to a port number from #1 to #14 as in figure 5.1. The corresponding electrode that the bond pad is connected to is shown on the expanded figure to the right. The bond pads that are paired together are represented by a line on the left of the figure. In this method two ports are selected and the impedance between the two ports was measured from 100 kHz to 100 MHz using an impedance analyzer (Agilent 4294A). The measurement was done by touching the bond pad with a needle that is connected to the impedance analyzer. Two needles were use where one was for applying the voltage and the other for the ground connection. Figure

5.2 is a reprint from the equivalent circuit model presented in chapter 2 when PBS was inside the channel. There are four ports in the equivalent circuit and the impedance between two ports will be measured in this section.

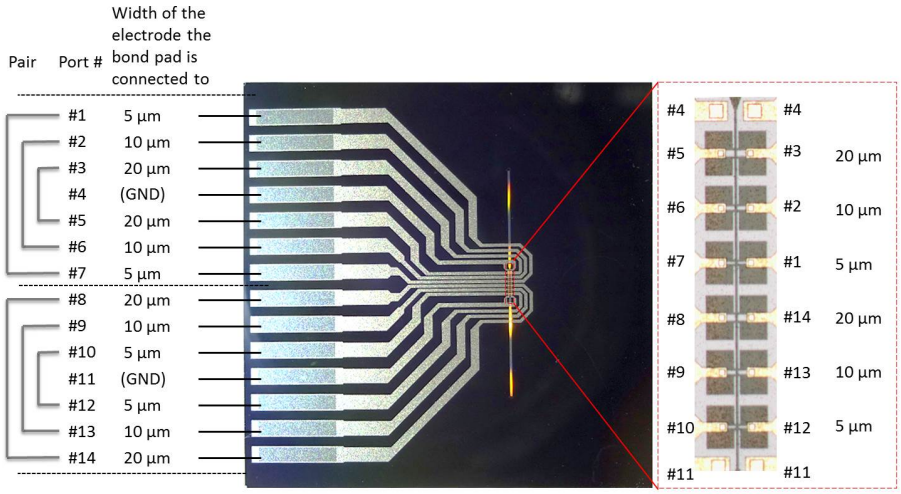


Figure 5.1: Details on the layout of the electrode and the bond pad. For convenience, each bond pad is assigned to a port number from #1 to #14 and the corresponding electrode that it is connected to is shown on the figure to the right.

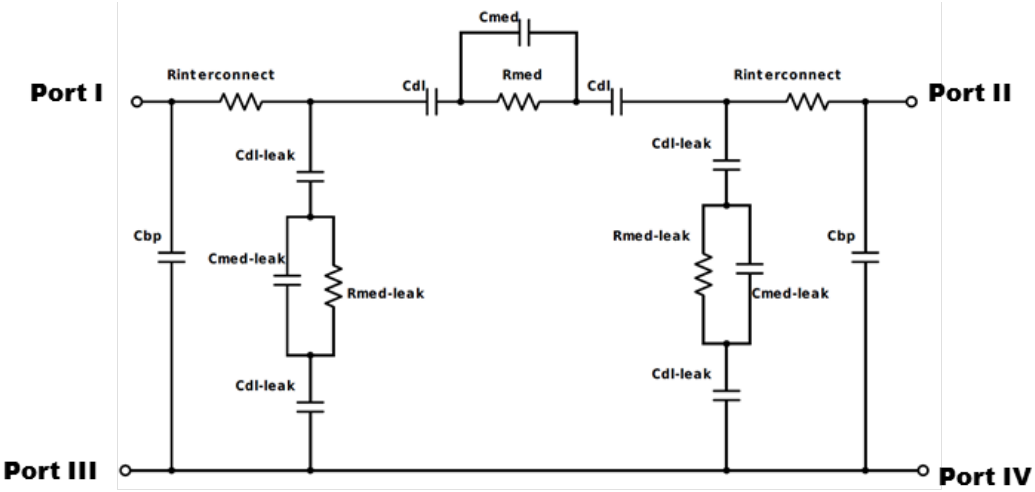


Figure 5.2: Equivalent circuit model with PBS inside the channel equivalent to the model that was presented in 2. For the values of the component refer to 2.

5.1.1. Aluminium Interconnect resistance

The impedance between two ground ports (#4 and #11) was measured. Using the equivalent circuit model in figure 5.2, this is equivalent to measuring the ground path which is from Port III to Port IV. In the equivalent circuit model

this was shorted but in reality the current will flow through the aluminium interconnect, the silicon surrounding the electrode and through the aluminium interconnect again. Therefore, this should be a very low resistive path.

The result was fitted with a circuit fitting software (i.e. ZVIEW2), modeled as an inductor and a resistor in series. The impedance and phase are shown in figure 5.3. It was found that the resistance was 7.39 Ω (±0.20 %) and the inductance was 34.8 nH (±0.45 %). This impedance can be associated to the two aluminium interconnect in series. Therefore, one aluminium interconnect will have 3.7 Ω and 17.4 nH; half of the measured value. The calculated resistance in section 2.4 which was 2 Ω is very close.

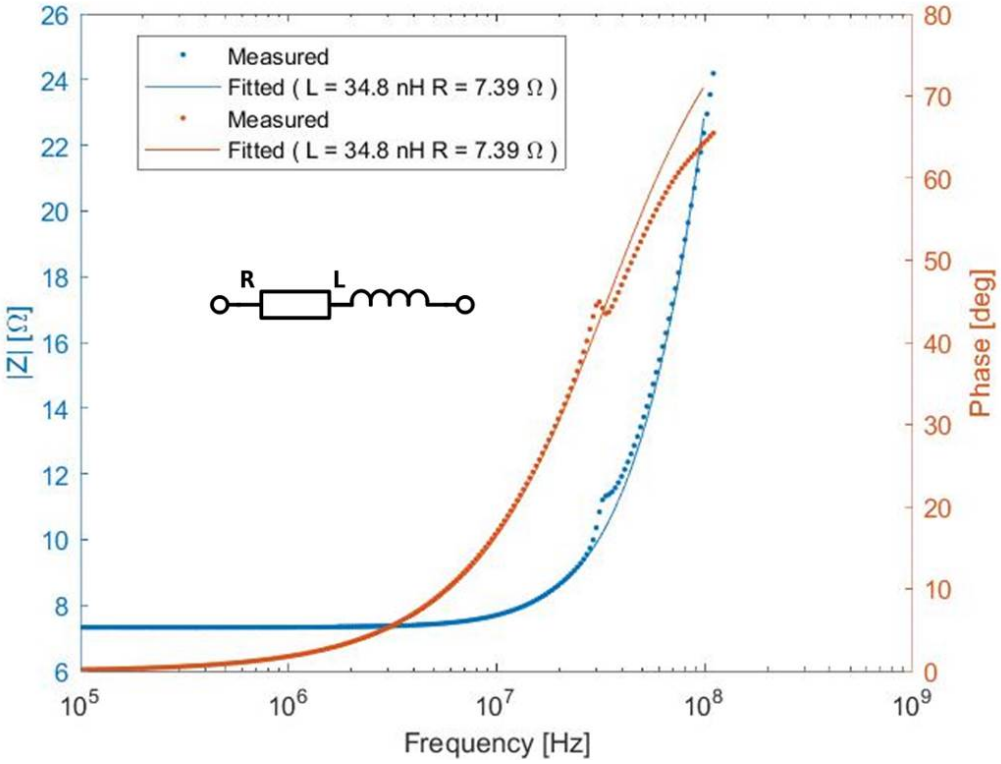


Figure 5.3: Impedance spectroscopy result of the ground connection.

5.1.2. Channel Impedance

The impedance spectrum between two electrodes (Port I to Port II in figure 5.2) with and without PBS inside the channel was compared.

First, the channel filled with air was measured. The measured impedance spectrum is shown in figure 5.4. The result was fitted with a capacitance from 100 kHz up to 10 MHz for 5, 10 and 20 µm wide electrodes. Frequen-

cies higher than 10 MHz were excluded from the fitting because there was an artifact from an unknown source that appeared around 20 MHz. The same artifact was seen in a different measurement and is probably from an external source. The fitted result for 10 µm and 20 µm are omitted from figure 5.4 because these curves were mostly the same as 5 µm. The fitted value for each electrode width is summarized in table 5.1. It is clear that all of the measurement value were similar.

Looking back at the equivalent circuit model in figure 5.2 when only air is inside the channel, the medium resistance will have a very high value because air is non-conductive. Only the medium capacitance will exist as shown in figure 5.5. Furthermore, the bond pad capacitance is several orders of magnitude larger than the medium capacitance so the measured capacitance is dominated by the bond pad capacitance. Since the bond pad capacitances are connected in series, one bond pad capacitance is twice as large as the measured capacitance. Therefore, the bondpad capacitance was found to be 88 pF.

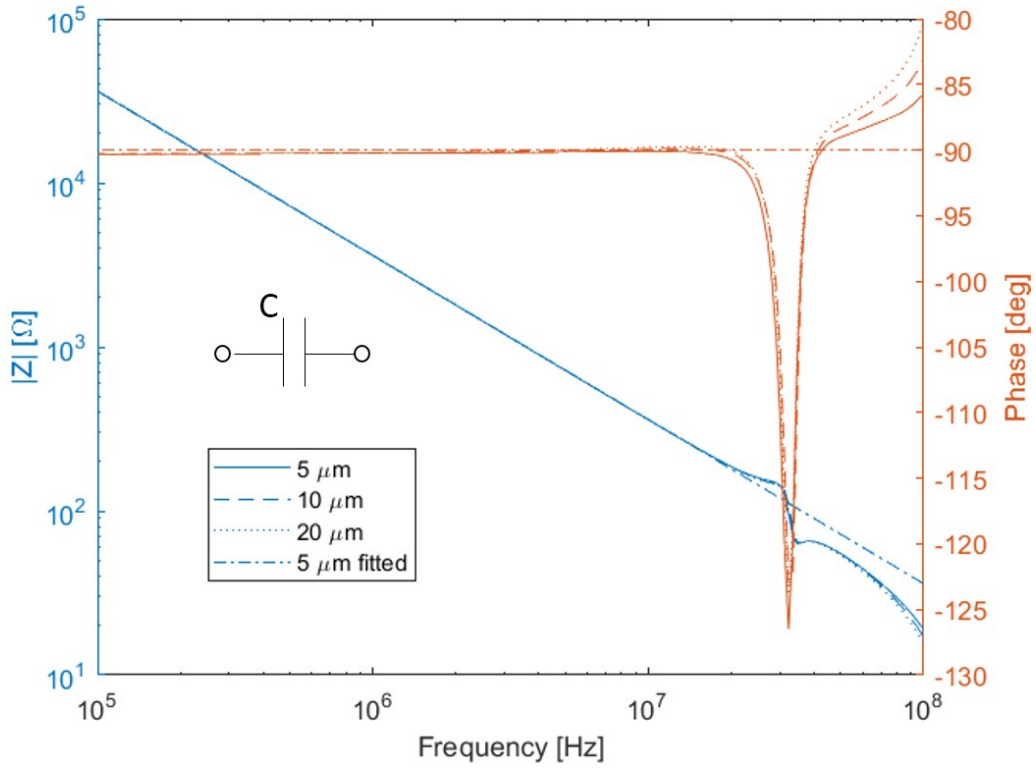


Figure 5.4: The impedance and phase for 5 µm, 10 µm and 20 µm was measured between two ports when the channel was filled with air.

Table 5.1: Fitted capacitance value and bond pad capacitance value.

Used ports	Electrode Width	C (fitted)	C_{bp} = 2C
#10 and #12	5 µm	44.1 pF ±0.03 %	88.2 pF
#9 and #13	10 µm	43.9 pF ±0.03 %	87.8 pF
#8 and #14	20 µm	44.2 pF ±0.03 %	88.4 pF

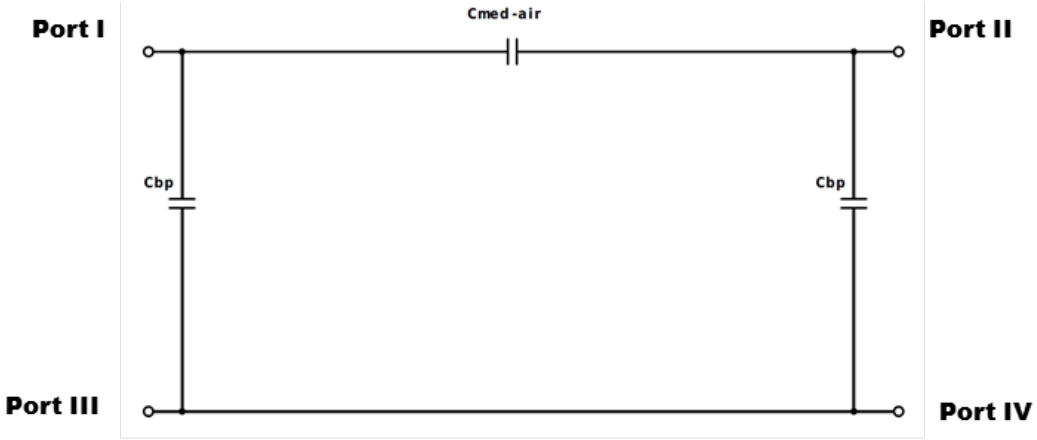


Figure 5.5: Equivalent circuit model with only air inside the channel

The impedance spectrum with PBS inside the channel was measured. First, the device was dipped into PBS. Then the device was vacuum pumped until it was seen under the microscope that bubbles were not trapped inside the channel or the voids surrounding the channel. Afterwards, the inlet/outlet was sealed with kapton tape to prevent the PBS from evaporating. After the measurement it was checked again if the channel was completely filled with PBS.

The measured result of the real and imaginary impedance as well as the modulus and the phase are shown in figure 5.6 and figure 5.7 for with PBS and without PBS inside the channel. From figure 5.7 the real component of the impedance has increased with the PBS inside the channel. The result was fitted with an RC parallel circuit. The fitted resistance is shown in table 5.2. It was found that the fitted resistance became lower as the width of the electrode increased. The physical implication of this result is not well understood because the model that was shown in figure 5.2 was more complex. Further research should be conducted to achieve a definitive conclusion. Although, it is likely that the fitted resistance value has some correlation to the medium resistance.

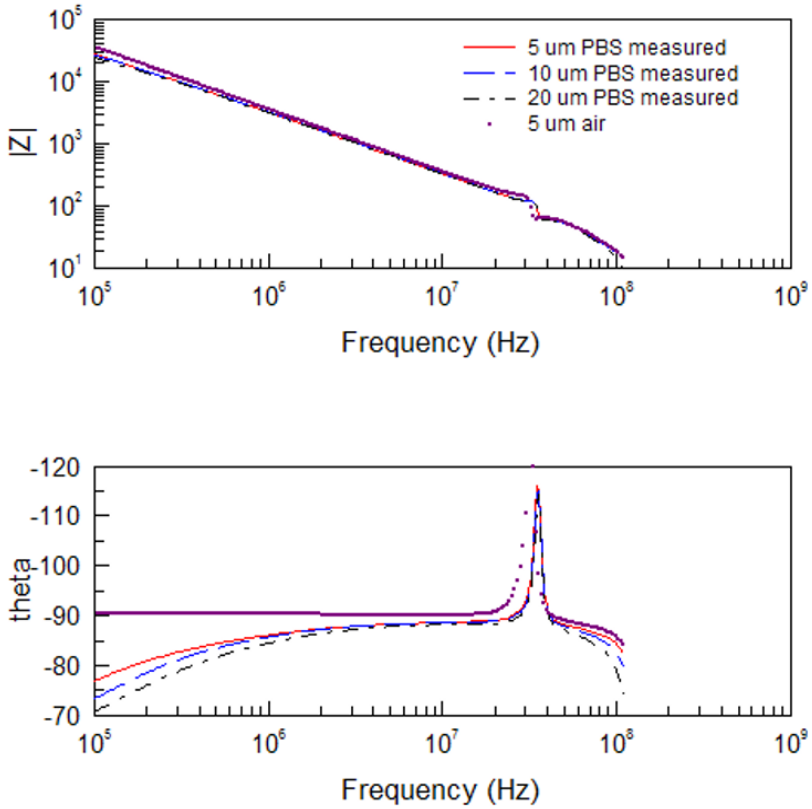


Figure 5.6: Measured modulus and phase of the impedance when PBS is inside the channel. For comparison, the impedance when air was inside the channel is also shown in the figure. The figure shows the measured result for 5 µm(10 and 12), 10 µm(9 and 13) and 20 µm(8 and 14). The numbers in parenthesis are the electrodes used for the measurement.

Table 5.2: Fitted value for the resistance from PBS. The capacitance was fixed with the value that was measured for the channel without PBS.

Used ports	Electrode Width	C (fixed)	R (fitted)
#10 and #12	5 µm	44.1 pF	94.4 kΩ ±6.0%
#9 and #13	10 µm	43.9 pF	75.8 kΩ ±4.6%
#8 and #14	20 µm	44.2 pF	57.3 kΩ ±4.5%

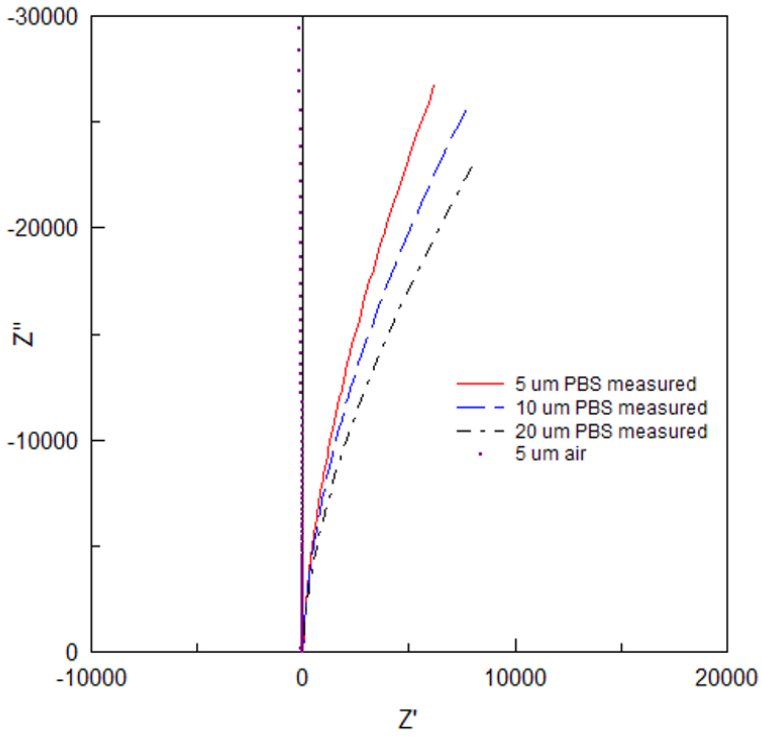


Figure 5.7: Measured real and imaginary impedance when PBS is inside the channel. For comparison, the impedance when air was inside the channel is also shown in the figure. The figure shows the measured result for 5 µm(10 and 12), 10 µm(9 and 13) and 20 µm(8 and 14). The numbers in parenthesis are the electrodes used for the measurement.

5.2. Single frequency stimulation measurement

The single frequency stimulation measurement was done by applying a voltage of 0.4 V amplitude at a frequency of 1 kHz between the surrounding silicon to one electrode while the voltage at the other electrode was measured against the surrounding silicon. This was done under a constant microfluidic flow through the channel. The channel was injected with the solution 30 min prior to the measurement so the bubbles inside the channel were removed.

The electrical setup to apply the voltage to the device is shown in figure 5.8. The voltage is applied from the redpitaya to Vin and measured from Vout. The PCB is used to connect the device to external electronics and manually switch between the electrodes. The PCB is held up vertically by the PCB holder which was 3D printed. Figure 5.9-a is a close up view from the backside of the PCB. Here the manual switch is connected to 20 µm wide electrodes. Figure 5.9-b is a view from the front side of the PCB where the device is placed inside the edge card slot. The transparent piece of block on the device is the PDMS seal that was used to connect the syringe tip to the inlet of the device. Although it is not shown in the figure the syringe tip is connected to a pressure controlled microfluidic pump. The output is not connected to a syringe because it was found that when the syringe is being filled with liquid, the pressure at the outlet increases. To compensate this, additional pressure must be applied to the inlet which causes the device to leak. Since the outlet is not connected to any syringe tip, in figure 5.9-b, by taking a closer look at the outlet of the device, there is some liquid coming out and forming a small droplet. During the experiment this droplet was constantly absorbed with tissues to keep the device clean.

First, DI water was injected through the channel and the output was measured. In this case, the measured voltage amplitude at the output was about 5 mV for all electrodes. When the switches were all turned off, the voltage was not measurable since the voltage was too low.

Next, using the same device, PBS was injected through the channel. The output voltage was measured for different electrode width as shown in figure 5.10. The amplitude at the output was found to change over time as well as the DC offset. The maximum amplitude recorded for 5 µm, 10 µm and 20 µm were 68 mV, 28 mV and 61 mV respectively. From this measurement, it was clear that there was a conductive path between the two electrode because the

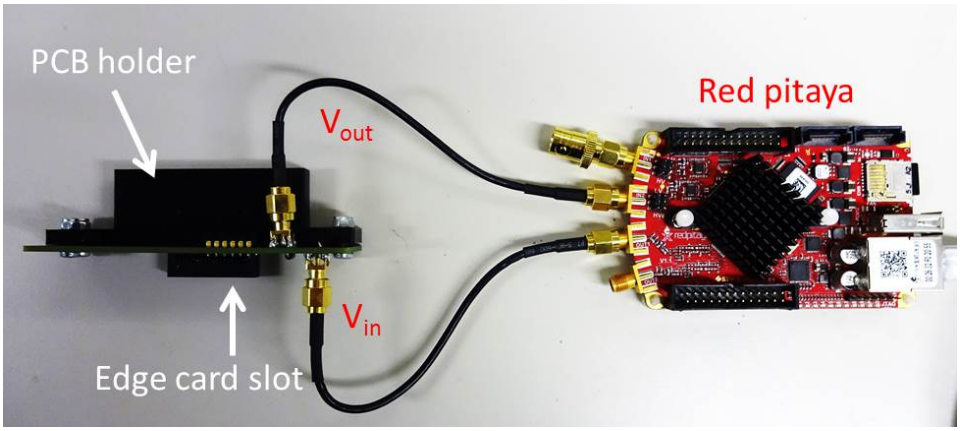
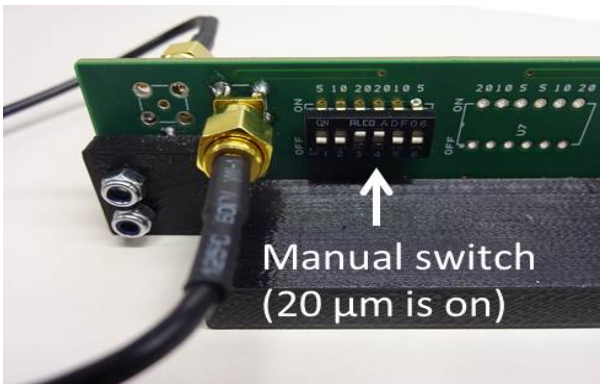
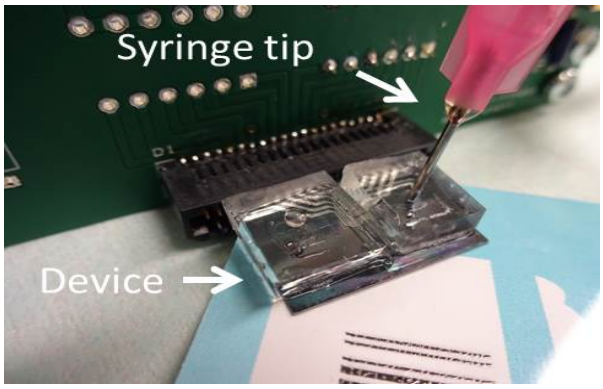


Figure 5.8: Overview of the experimental setup. Using redpitaya a voltage is applied to Vin and the output is monitored at Vout.



(a) Manual switch on the backside of the PCB. Electrodes 20 µm wide are on in this figure.



(b) Device inside the edge card slot with the microfluidic pump connected to the device via the syringe tip and the PDMS seal.

Figure 5.9: Closer image of the front and backside of the PCB.

amplitude was much higher compared to DI water. However, the amplitude did not increase as the width of the electrode increased, nor did it have a correlation between the electrode width and the amplitude.

The electrical circuit model when DI water is inside the channel is shown in figure 5.11. Compared to figure 5.2, the medium resistance is neglected because the resistance of DI water is very high. In addition, the series connection of double layer capacitance and medium capacitance is replaced with a parasitic capacitance C_p. This is because, according to the calculation performed next, the capacitance value was too high for it to be the medium capacitance and double layer capacitance in series.

If the equivalent circuit can be expressed by a network of capacitance the

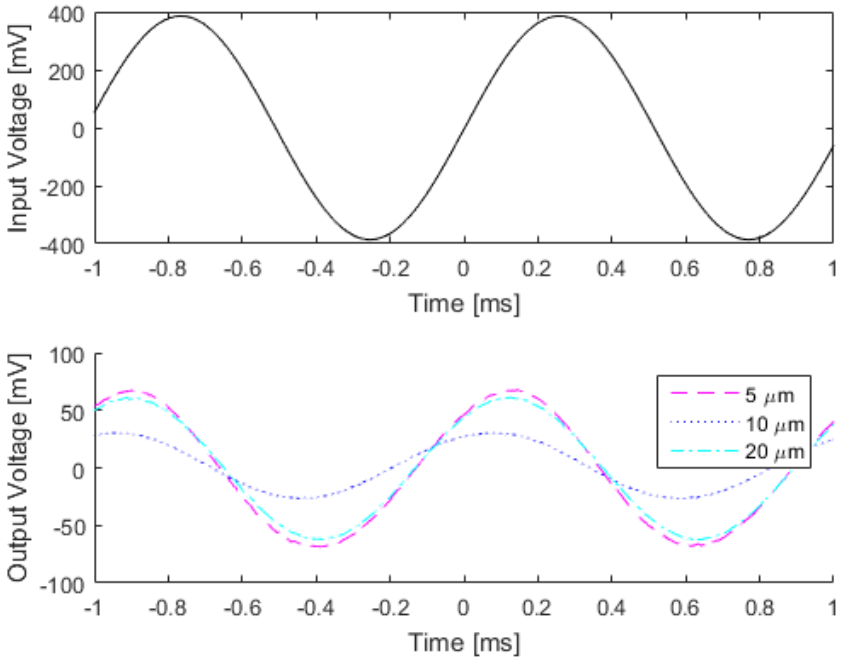


Figure 5.10: Input voltage (above) and the output voltage for different electrode width (bottom) when PBS solution was continuously injected through the channel.

voltage at the output can simply be expressed by a capacitive voltage divider as,

$$V_{out} = \frac{C_p}{C_{bp}} V_{in} \tag{5.1}$$

C_{bp} was measured in the section 5.1 to be 88 pF and by inserting the input (400 mV) and output (5 mV) voltage, C_p is 1.1 pF. The calculated medium capacitance in chapter 2 was about 30 fF, and the capitance values is much larger, therefore a parasitic capacitance must be in parallel with the channel impedance.

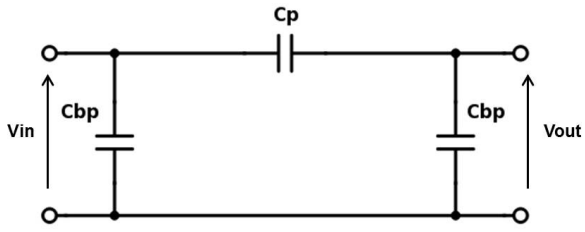


Figure 5.11: Electrical equivalent circuit when DI water is inside the channel.

When PBS is inside the channel, the amplitude based on the model was 200 mV at the output. In reality, the voltage was much lower from 20 mV

to 70 mV. This discrepancy in the data was not understood and must be analyzed further.

In summary, when DI water was inside the channel the two electrodes were connected by a parasitic capacitance of 1.1 pF. But when PBS was inside the channel, there was a conduction path between the two electrodes. When PBS was inside the channel, no correlation was seen between the width of the electrode to the output voltage. It was also found that the DC offset of the output signal as well as the amplitude changed over time. The DC offset can be cancelled with a high pass filter but the change in amplitude is not understood. It might be caused by the unstable impedance at the silicon electrode to electrolyte interface. In the next section preliminary experiments were done to investigate this interface.

5.3. Characterization of silicon electrode

From the previous electrical measurements it became clear that more investigation must be done on the silicon electrode to electrolyte interface. In this section, preliminary experiments were conducted to understand the properties of the silicon electrode using two methods. The first method is the cyclic voltammetry method and the second method is the electrochemical impedance spectroscopy measurement.

5.3.1. Experimental setup

The silicon electrode is trapped beneath the SiO_2 membrane so a pretreatment was done to remove the SiO_2 membrane. The device was treated with an additional 3 min of vapor HF to make the SiO_2 membrane fragile. Subsequently, kapton tape was used to peal off the SiO_2 membrane. Figure 5.13 are the electrodes after the kapton tape was used to remove the membrane. In the figure, the silicon electrodes are exposed while still connected to the aluminium interconnect. The total surface area of the electrode is 7840 μm^2 for all electrodes.

A three electrode measurement setup was used for the experiment where the counter electrode was Pt, the reference electrode Ag/AgCl and the working electrode is the silicon electrode. Figure 5.12 is a schematic of the three electrode setup. Figure 5.14-a is the front view of the experimental setup. The silicon electrode is immersed inside PBS solution. The working electrode

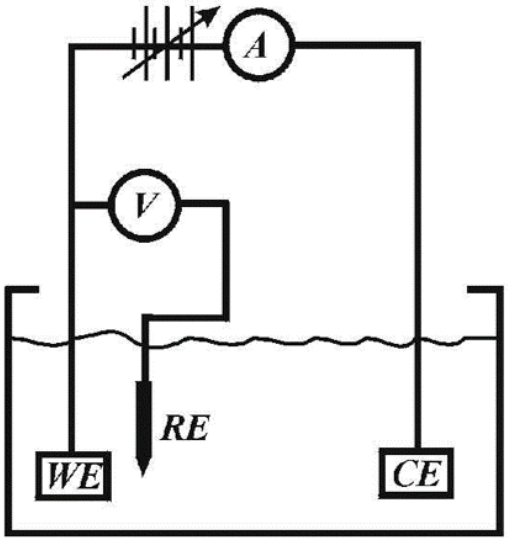


Figure 5.12: Schematic diagram of a 3 electrode schematic. A voltage is applied to the working electrode (Si) against the reference electrode (Ag/AgCl) and the current going through the counter electrode (Pt) is measured.

connection (red alligator clip) is connected to the aluminium bond pad which is then connected to the selected silicon electrode. The other aluminium bond pads that are not used are covered with kapton tape so they do not touch the red alligator clip. The location of the three electrodes used for the experiment are shown in figure 5.14-b.

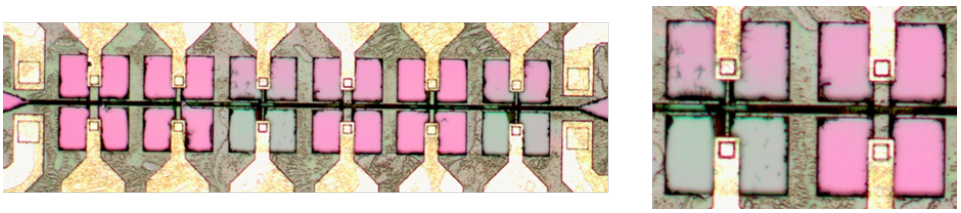
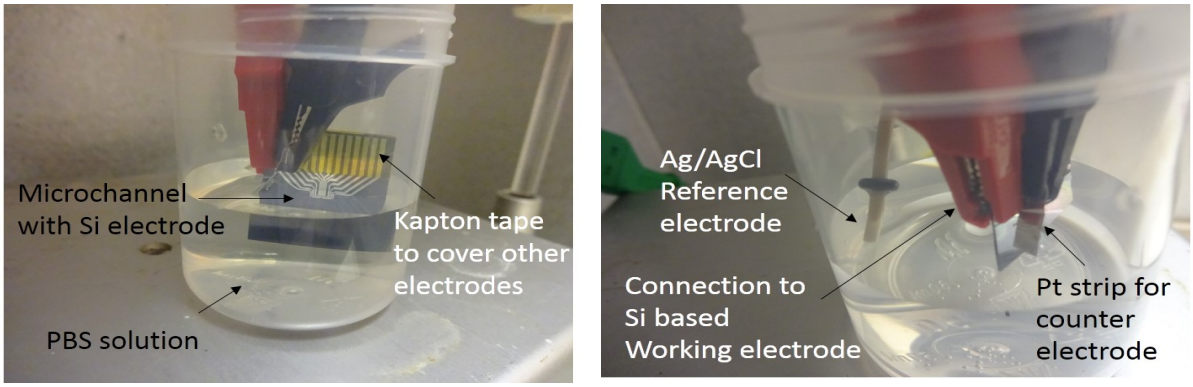


Figure 5.13: 3 min of vapor HF treatment followed by a kapton tape attached to the mesh and removed along with the SiO_2 membrane. (There is also a 3 min vapor HF performed beforehand so in total it will be 6 min of vapor HF)

5.3.2. Cyclic voltammetry measurement

Figure 5.15 shows the result of the cyclic voltammetry measurement at a scan rate of 10 mV s^{-1} for two scans. At positive voltages the silicon electrode behaves as a resistance since the current is proportional to the voltage being applied. When a negative voltage was applied to the working electrode a re-



(a) Front view (b) Side view

Figure 5.14: Cyclic voltammetry experiment setup.

duction peak was seen around -0.5 V. The redox reaction of water is as follows [23],

$$2\,H_2O + 2\,e^- = H_2 + 2\,OH^- \,(-0.605\,V\,\text{vs}\,Ag/AgCl) \tag{5.2}$$

Since -0.5 V and -0.605 V are relatively close it is likely that the reaction in equation 5.2 is causing the formation of H_2 on the surface of the electrode.

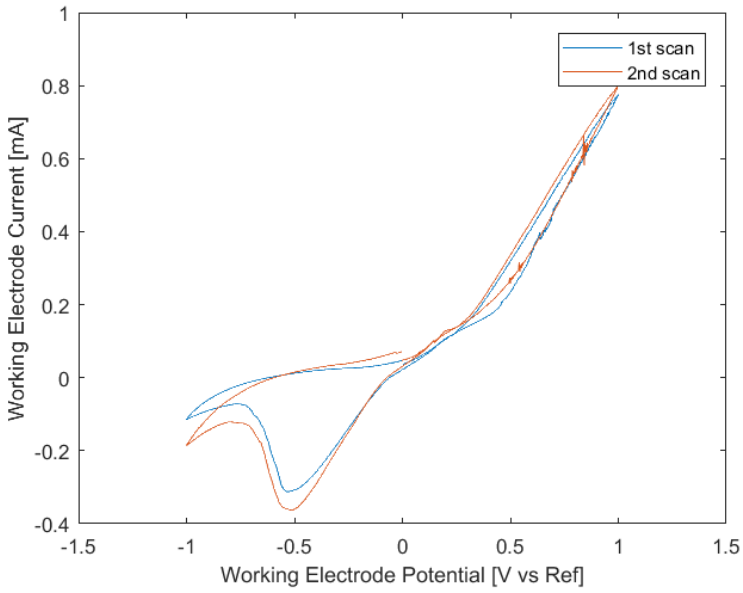


Figure 5.15: Cyclic voltammetry result for silicon electrode using a Ag/AgCl reference electrode and Pt counter electrode.

5.3.3. Electrochemical impedance spectroscopy

An electrochemical impedance spectroscopy measurement uses the same three electrode setup as explained previously. This measurement can characterize the interface impedance between silicon electrode and the PBS. In this setup an AC voltage of 140 mV was applied to the working electrode in reference to the Ag/AgCl electrode. The current that flows through the working electrode is collected at the counter electrode and measured to calculate the impedance. The measured bandwidth was from 0.1 Hz to 10 kHz. From this measurement the impedance is plotted in figure 5.16 and 5.17.

At low frequencies such as 0.1 Hz the impedance is resistive since the phase is near 0°. At higher frequencies the impedance gradually becomes capacitive. In chapter 2 the silicon to PBS interface was modeled as a double layer capacitance. It became clear that this was not sufficient to model the interface. Further research must be done to create a precise model of the interface. This is most likely the reason why the measurement result for the single frequency stimulation at 1 kHz did not follow the theoretical value in section 5.2.

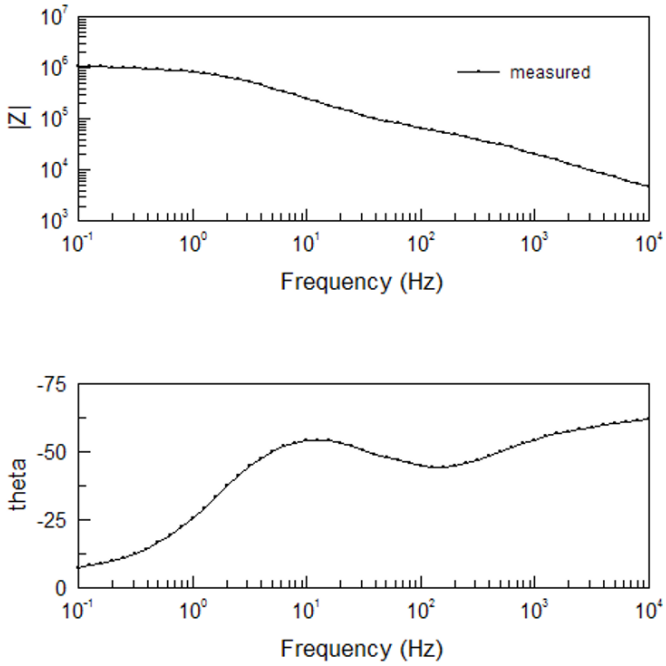


Figure 5.16: EIS amplitude and phase for measured result.

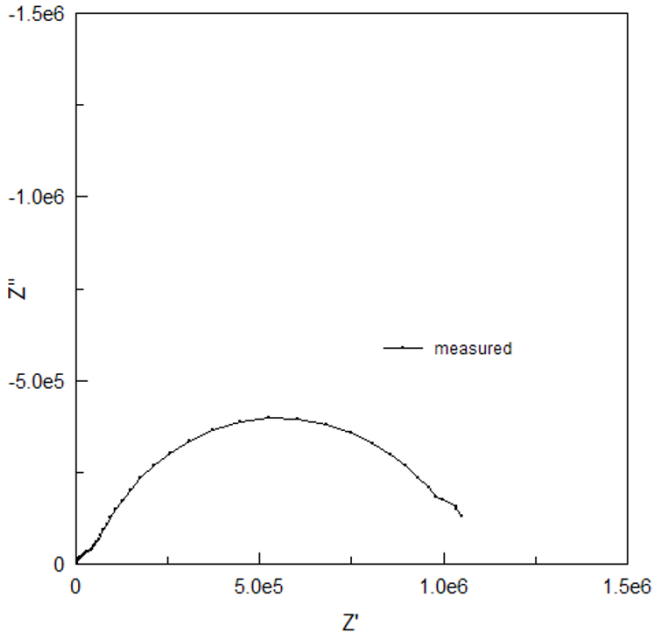
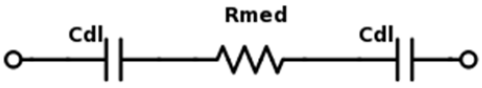


Figure 5.17: EIS real and imaginary impedance for measured result.

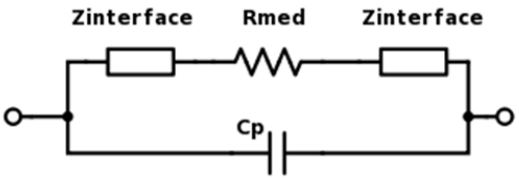
5.4. Conclusion

From the impedance spectroscopy the bond pad capacitance and the aluminium interconnect resistance was measured to be 88 pF and 3.9 Ω respectively. From the single frequency stimulation, when the channel was filled with PBS, there was a conductive path that formed between the two electrodes. It was also found that a parasitic capacitance existed from the input to the output which was about 1.1 pF. From the electrochemical impedance spectroscopy measurement, the silicon electrode to electrolyte interface was found to be more complicated than a simple double layer capacitance.

Therefore, the channel impedance model must be revised. Figure 5.18-a is the channel impedance that was previously proposed. Figure 5.18-b is the channel model that should be used, where the double layer capacitance is replaced by a complex impedance and a parasitic capacitance of 1.1 pF is shorting the input and output. That being said, in figure 5.16 the impedance is decreasing as the frequency is increasing. It may be possible to operate at a higher frequency to avoid the unwanted effect of the interface impedance if the interface impedance becomes lower than the medium resistance. However, since there is a parasitic capacitance of 1.1 pF there is also a limitation to how high the frequency can be raised. Further detail on the which frequency range to operate in, can only be decided after the silicon electrode to electrolyte interface is analyzed in more detail.



(a) Equivalent circuit model of the channel with the interface impedance modeled as only a double layer capacitance.



(b) Equivalent circuit model of the channel with the interface impedance and a parasitic capacitance 1.1 pF.

Figure 5.18: Two equivalent circuit model for the channel impedance. The medium capacitance is abbreviated for both figures because it was too small.

The electrical measurement result presented in this chapter are preliminary results. This is why the operating frequency is not aligned for all mea-

surement and the stability of the measurement is not perfect. The measurement method has been revised multiple times before achieving these results. Therefore, the main achievement in this chapter may be the configuration of the measurement method itself. For example, the method to detach the SiO_2 membrane for 3 electrode setup or combining microfluidic pump, redpitaya, pcb and etc. to read out the signal. These methods will be valuable for the successors who will work on this project.

There are still insufficient aspects in these measurement methods. For example, the DC offset varied over time. This is because a high pass filter was not implemented on the PCB to remove low frequency signal. Once these improvements are implemented, it will be possible to measure signals at a higher frequency or to create a bode plot of V_{out}/V_{in}. These measurements will further clarify the equivalent circuit model and provide information on how to design the device in a better way.

6

Conclusion

The primary goal of this thesis was to detect a cell at two different locations using silicon based electrodes and measure the velocity of the cell inside the constriction channel. Since this thesis was the first step to realize this device, the focus was placed on the fabrication.

The fabrication began with reproducing the results of EMC fabricated at Philips Innovation Services. The process was extensively studied and optimized to fabricate the EIEMC. Parameters were derived to fabricate 40 µm deep, vertical channels with no icicles. During this process the mechanism of EMC fabrication, especially the sidewall etch was understood in detail. This result is not only useful for the fabrication of EIEMC but can be extended for similar structures or EMC with different depths or widths. For example, if a channel with 20 µm depth is necessary, a mesh hard mask with hexagonal pores are more suitable compared to rectangular pores because the etch rate is slower and the icicles can be removed simultaneously when the depth reaches 20 µm. Therefore this research can be a starting point for other researchers who will work on EMC.

The key to fabricating EIEMC was the patterning of multiple layers after the EMC was closed with PECVD SiO_2. It was found that the stress induced by high temperature process deposition such as Al/Si (1%) deposition at 350° had a high possibility to detach the seal on the EMC. The design of the mesh hard mask (hole type, channel width, number of corners) also influenced the integrity of the SiO_2 membrane. Therefore, these results can be used to design

a better mesh hard mask that can withstand higher temperature process. The successful fabrication of EIEMC also opened a wide range of applications such as the integration of microfluidics and CMOS electronics on the same wafer.

After the EIEMC was fabricated some electrical measurements were carried out. The channel was filled with either PBS, air or DI water. Several circuit components were de-embedded from these result such as bond pad capacitance, parasitic capacitance and aluminium interconnect resistance. The measurement with PBS inside the channel did not fit the theoretical model and revealed some potential challenges on how to detect the cell. This is because silicon was used for the electrode material which has not yet been studied extensively for the application of cell detection.

Finally, the main results of these thesis is summarized in table 6.1.

Table 6.1: Summary of Results

Level			Goal	Method	Result
High	Real time cell stiffness measurement through impedance sensing				Incomplete
	Medium	Fabrication of the chip			Complete
		Low	Mask fabrication	A mask design software (L-Edit) was used to design 5 masks aluminium interconnect, bond pad, channel with electrodes, inlet/outlet and contact hole.	5 masks were designed. The inlet/outlet and channel were combined so 4 physical masks were ordered in total.
		Low	EMC fabrication (Cleanroom)	Fabrication test was done using the channel mask and Rene Hendrikx's mask	Reproduction of EMC has been verified.
		Low	EIEMC (Cleanroom)	The fabrication steps that can be tested separately was tested beforehand.	EIEMC was fabricated.
	Medium	Electrical analysis			Partially complete
		Low	Equivalent Circuit modeling	The equivalent circuit model was made based on previous research.	More investigation must be done on the interface between silicon and PBS.
		Low	Actual measurement of the device	Several measurement method were used. 1) Impedance spectroscopy 2) single frequency excitation 3) bode analysis	Impedance spectroscopy, single frequency was done. Bode analysis was not done.
	Medium	The design of adapters to read out the signal and inject liquid into the channel			Partially complete
		Low	PCB design	PCB to easily read out the signal from the chip.	The PCB to easily measure out the signal was a success, however high pass filters should be implemented
		Low	3D printing of PCB holder	A holder was designed and 3D printed.	3D printed holder held the PCB vertically.
		Low	Microfluidic packaging	PDMS was used to connect the chip to the microfluidic pump.	The method of using PDMS to seal the inlet/outlet was established.
	Medium	Program to control Redpitaya (a credit card size microcontroller) to quantify the cell stiffness.			Incomplete

A

Mask design

There are 5 mask designs that were used for the fabrication of the device. For all of the designs positive photoresist was used. Figure A.1 is a figure when all of the masks are overlayed on top of each other. Figure A.2 is the aluminium interconnect pattern. When the mask was ordered the design was inverted. Figure A.3 is the bondpad opening the colored area is the exposed region. Figure A.4 is the channel mask. On this mask 7 design for the design was fabricated. This mask is multilevel and the inlet/outlet design was also fabricated. Figure A.5 is the mask for the contact hole opening.

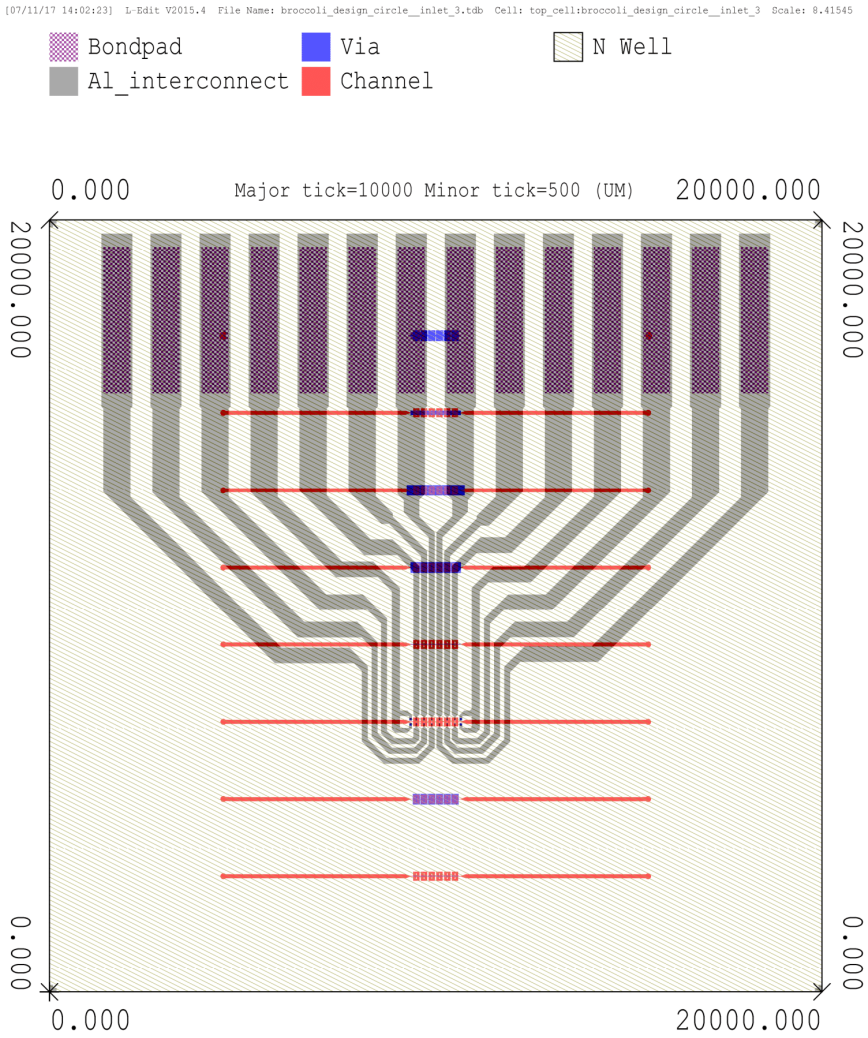


Figure A.1: Mask design with all layers

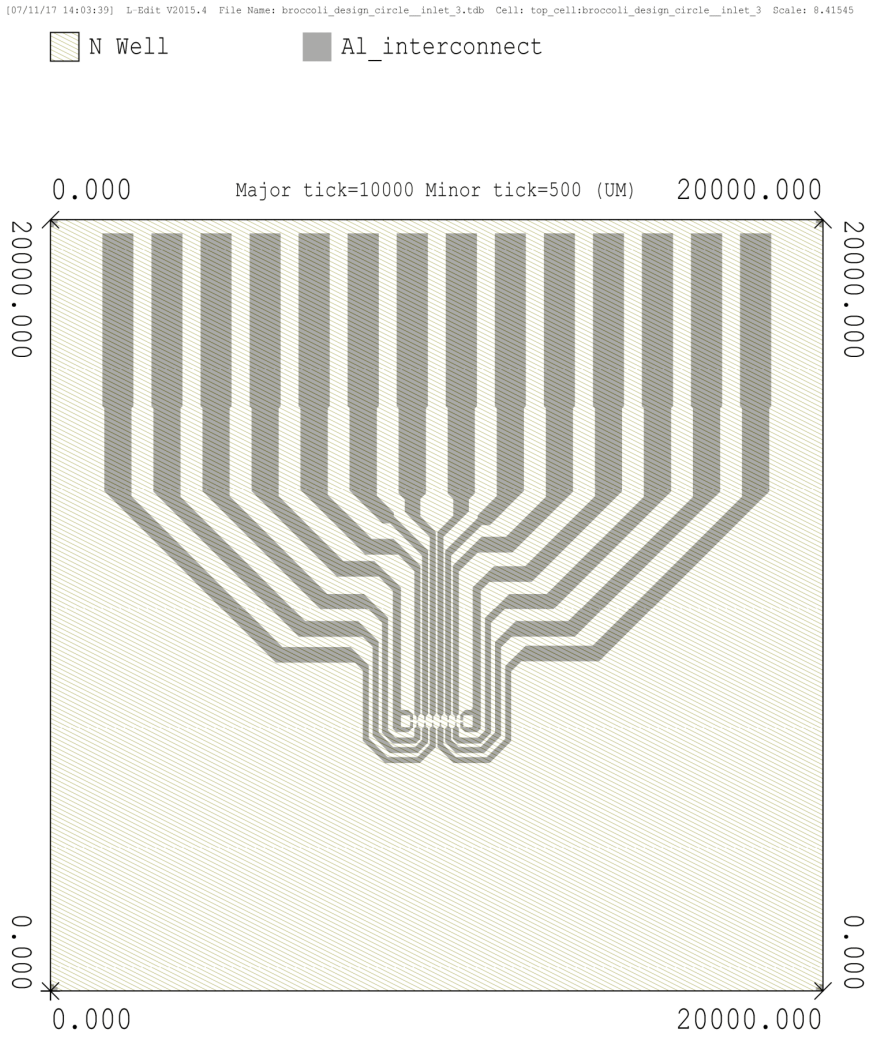


Figure A.2: Mask design of the aluminum interconnect. For this mask we use the inverted version of the mask.

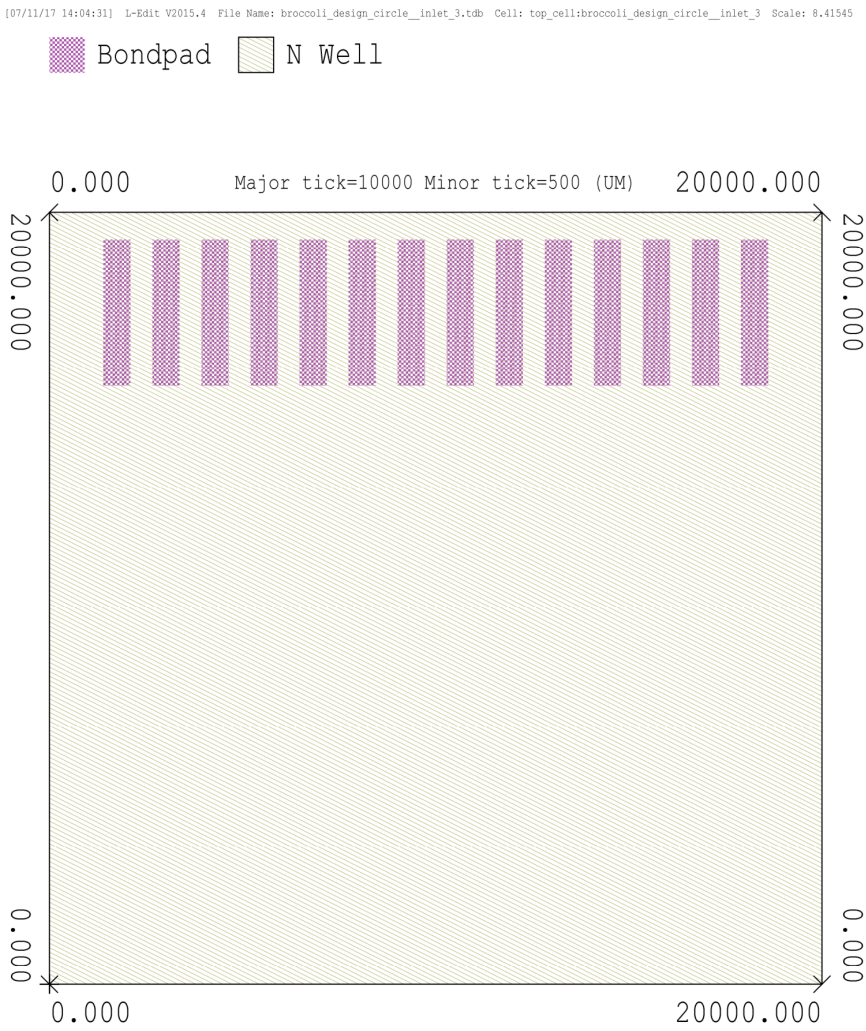


Figure A.3: Mask design of the bondpad

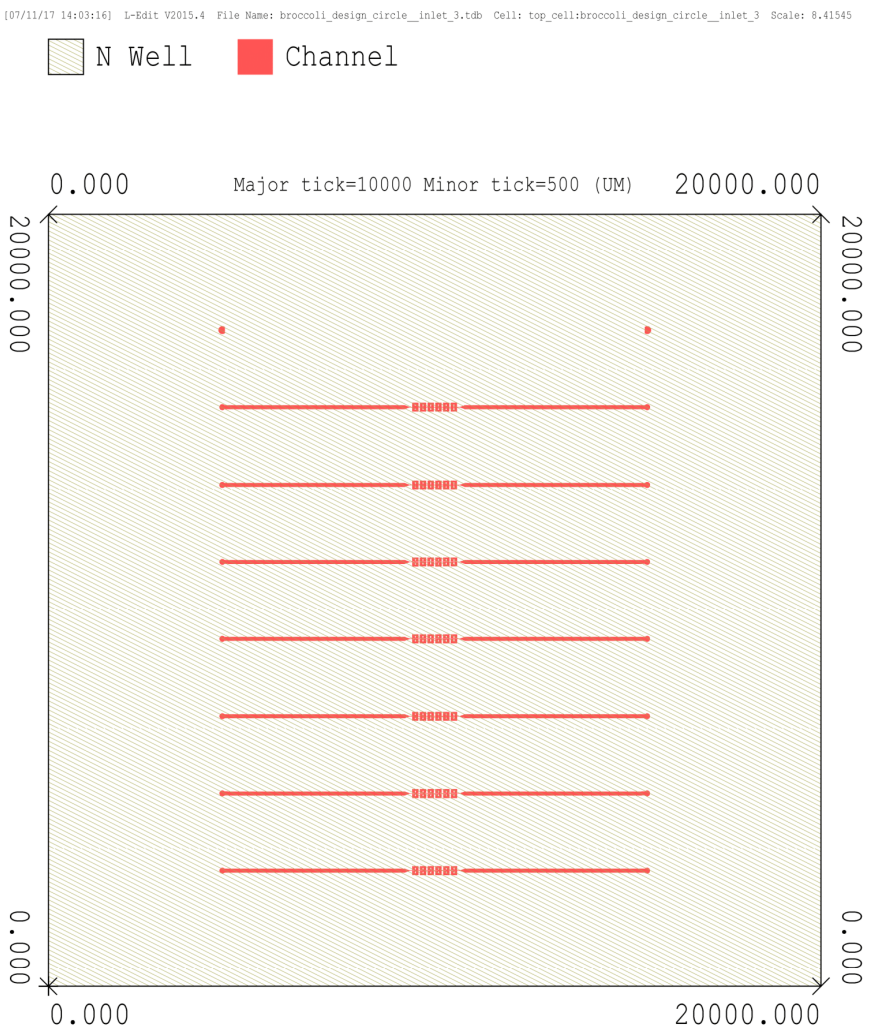


Figure A.4: Mask design of the channel

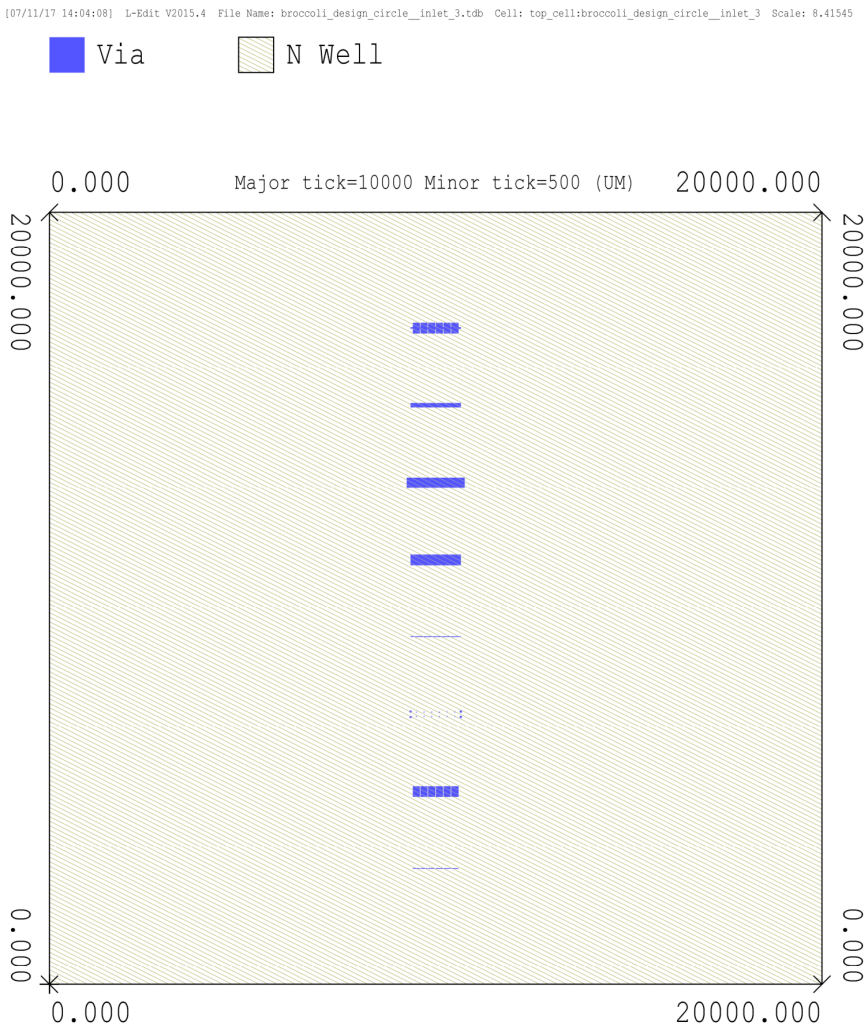


Figure A.5: Mask design of the contact hole opening

B

Multi-level mask exposure method

The multi-level mask exposure method was used to decrease the fabrication cost of the mask by effectively utilizing the area of the mask. This was especially useful when we wanted to test the channel because the method proposed uses 1 mask for the channel and 1 mask for the microfluidic access port. By programming the wafer stepper one mask to exposed to designs. In this section the method of multi-level mask exposure used in this research will be explained schematically.

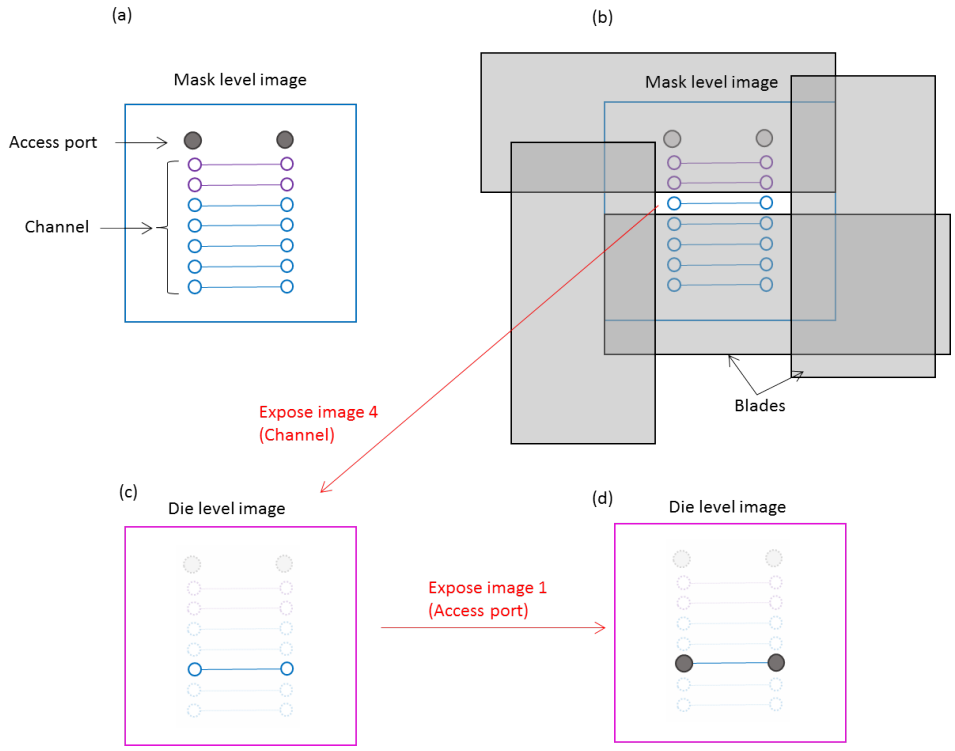


Figure B.1: Multilevel exposure method 1

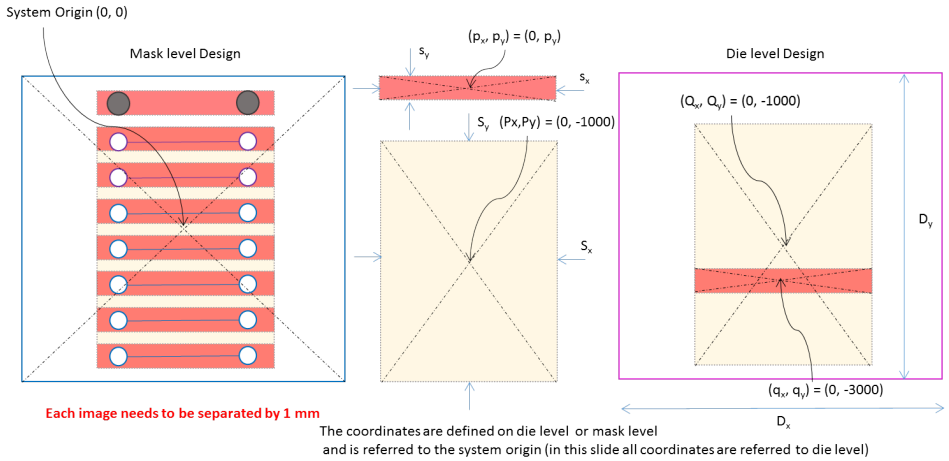


Figure B.2: Design guide for multi-level exposure

C

World to chip connection

The chip in micro-scale must be connected to the external peripheral devices for both microfluidics and electronics. Here the fabrication method of the microfluidic seal will be explained.

C.1. Microfluidic connection using PDMS seal

A printed mask on a transparent film was used and a design as shown in figure C.1 was printed with a commercial lazer printer. Using this mask the process flow shown in figure C.2 was followed.

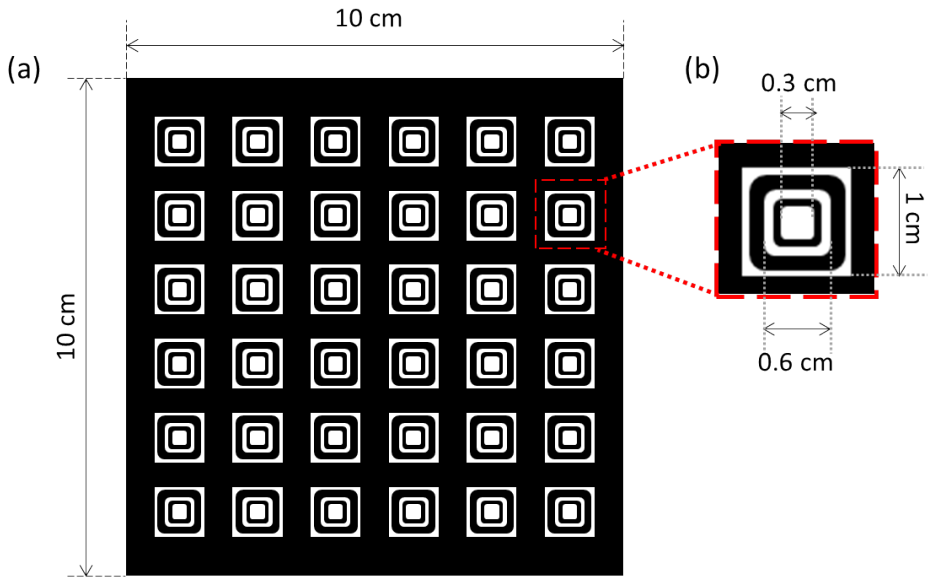


Figure C.1: the printable mask design used for the PDMS seal

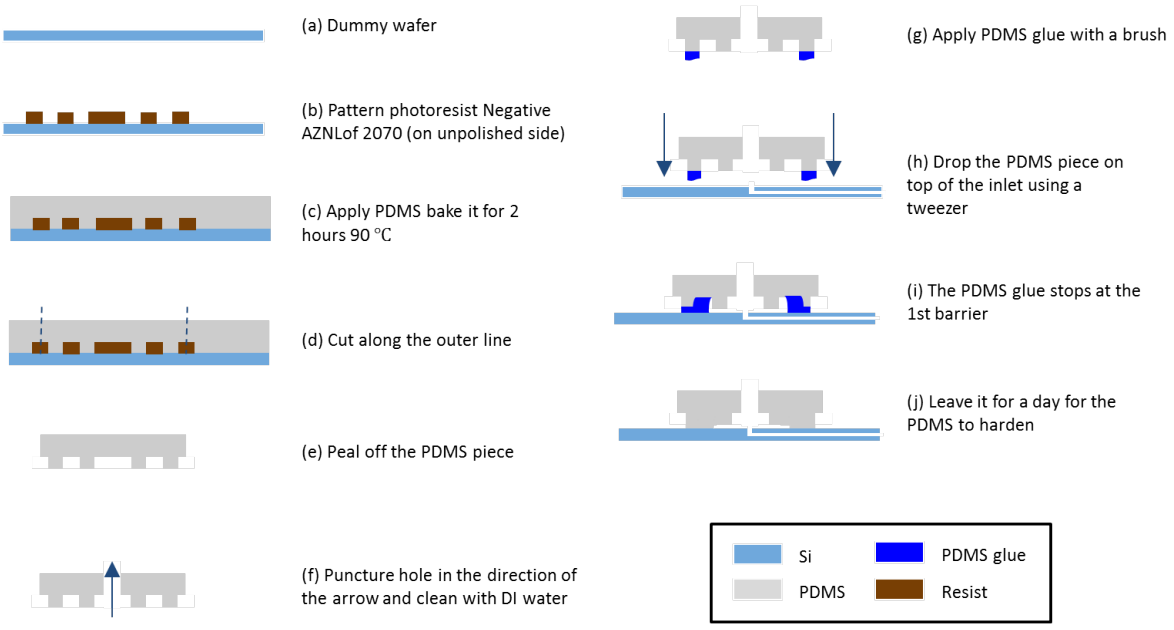


Figure C.2: flow chart PDMS seal

D

Detailed flowchart

D.1. EIEMC fabrication process

If not differently specified, the process was performed in cleanroom class 100. As a disclaimer it is worth noting that the observation port was **not fabricated** in the batch that was made for this thesis due to the limited time. However these steps are included in this process flow chart for completeness. These steps which were not tested are shown in gray text.

The process begins with an SOI wafer with 40 µm thick highly boron doped silicon, 1 µm thick BOX layer, 380 µm thick backside silcon layer with 1 µm of additional thermal oxide. The resistivity of the device layer was within 5 to 20 mΩ cm and was ordered through Okmetics.

1. Boron ion implantation (15 keV, 5×10^{14} atoms/cm^2)

   Ion implantation of boron was done on the front side with an energy of 15 keV and a dosage of 5×10^{14} atoms/cm^2. No dip etch or pre-baking is necessary. The simulated result of this ion implantation has a ion implantation depth of .

2. Cleaning procedure: Tepla + HNO3 99 % and 65 %

   (a) Plasma strip: Use Tepla plasma system to remove the photoresist that may have attracted from the chuck of the ion implanter using oxygen plasma. Follow the instructions specified for Tepla and use

the quartz carrier. Use program 4: 1000 W power and abort the process after 2 to 3 min.

(b) Cleaning: Use wet bench " HNO3 (99 %)" (Silicon) for 10 min.

(c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

(d) Cleaning: Use wet bench " HNO3 (65 %)" (Silicon) for 10 min.

(e) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

(f) Drying: Use the Semitool "rinser/dryer"(Silicon) with the standard program.

3. Annealing C2 furnace 950 °C for 30 min

   Using C2 furnace anneal at 950 °C for 30 min in nitrogen ambience using a process named "ANN950".

4. Coating and baking

   Use the EVG120 coater/developer to coat the wafers with resist and follow the instruction specified for the equipment. The process consists of a treatment with HDMS (hexamethyldisilazane) vapor with nitrogen carrier gas, spin coating with Shipley SPR3012 positive photoresist (spin velocity 3450 RPM; spin time 30 s) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3012-zero layer (resist thickness: 1.4 µm).

5. Alignment and exposure

   Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask "COMURK" with job "20x20COMURK" at an exposure energy of 150 mJ cm^{-2}.

6. Development

   Use EVG 120 coater/developer to develop the wafers by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe "Dev-SP" for this procedure.

7. Photoresist inspection

   Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

8. Plasma etching of alignment markers

   Use Trikon Omega 201 plasma etcher and follow the instruction manual. Use the sequence ”URK_NPD” (with a platen temperature of 20 °C) to etch 120 nm deep alignment markers in silicon.

9. Cleaning procedure: Tepla + HNO3 99 % and 65 %

   (a) Plasma strip: Use Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for Tepla and use the quartz carrier. Use program 4: 1000 W power and abort the process 2 to 3 min after the endpoint curve has gone down.

   (b) Cleaning: Use wet bench ” HNO3 (99 %)” (Silicon) for 10 min.

   (c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

   (d) Cleaning: Use wet bench ” HNO3 (65 %)” (Silicon) for 10 min.

   (e) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

   (f) Drying: Use the Semitool ”rinser/dryer”(Silicon) with the standard program.

10. Deposit 4 µm of PECVD SiO_2 on backside

    Use Novellus PECVD reactor to deposit 4 µm thick PECVD SiO_2 on the backside of the wafer. Follow the instruction of the machine and use recipe ”zerostressox” at 400 °C. Change the deposition time according to the log-book or use a test wafer to measure the deposition rate beforehand.

11. Measuring thickness

    Use Leitz MPV-SP and program ”Novellus SiO_2 > 50 nm auto 5 points” to measure the PECVD SiO_2 thickness. If Leitz MPV-SP is not available use an ellipsometer, however in this case a test wafer needs to be made

because the ellipsometer cannot measure the thickness of SiO_2 on a SOI wafer.

12. Coating and baking

    Use EVG120 coater/developer to coat the wafers with resist on the back side and follow the instruction specified for the equipment. The process consists of a treatment with HDMS (hexamethyldisilazane) vapor with nitrogen carrier gas, spin coating with Shipley SPR3027 positive photoresist (spin velocity ???? RPM; spin time) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3027-4 µm-noEBR for this procedure.

13. Alignment and exposure

    Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask "EC2157-via" with job "EC2157" at an exposure energy of 500 mJ cm^{-2} on the backside. On the mask there are 6 different designs for the observation port to be selected from, so choose the one that is suitable for the process (Fig. **??**). Furthermore the alignment markers on the front side needs to be selected manually through the system or since the observation windows are quite large "no alignment marker" option can also be used since the alignment restrictions are not that stringent.

14. Development

    Use EVG 120 coater/developer to develop the exposed area on the backside by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe "Dev-SP" for this procedure.

15. Photoresist inspection

    Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

16. BHF 1:7 (Silicon) wet etch of SiO_2

    Average etch rate for PECVD SiO_2 is from 200 to 300 nm min^{-1} and for thermal SiO_2 is around 50 nm min^{-1}. It is better to check the etch rate for PECVD SiO_2 using a dummy wafer before doing this process.

    (a) Surface tension treatment: Dip wafers in Triton (Silicon) for 1 min to change the surface tension so that the BHF can easily come in contact with the SiO_2 in the next step.

    (b) Wet etch: Use BHF 1:7 (Silicon) to etch 4 µm thick PECVD SiO_2 + 1 µm thick thermal SiO_2. During the procedure agitate the carrier once in 5 min to remove the bubbles formed from the etch reaction.

    (c) Rinse and dry: Rinse the wafer until it reaches 5 MΩ and rinse dry inside Avengers (Metal).

17. Cleaning procedure: Tepla + HNO3 99 % and 65 %

    (a) Plasma strip: Use Tepla plasma system to remove the photoresist in an oxygen plasma. The photoresist are attracted from the ion implanter's chuck. Follow the instructions specified for Tepla and use the quartz carrier. Use program 4: 1000 W power and abort the process 2 to 3 min after the endpoint curve has gone down.

    (b) Cleaning: Use wet bench " HNO3 (99 %)" (Silicon) for 10 min.

    (c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

    (d) Cleaning: Use wet bench " HNO3 (65 %)" (Silicon) for 10 min.

    (e) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

    (f) Drying: Use the Semitool "rinser/dryer"(Silicon) with the standard program.

18. Deposit 1.7 µm of PECVD SiO_2 on front side

    Use Novellus PECVD reactor to deposit 1 µm thick PECVD SiO_2 on the front side of the wafer. Follow the instruction of the machine and use recipe "zerostresox" at 400 °C. Change the deposition time according to the log-book or use a test wafer to measure the deposition rate beforehand.

19. Measuring thickness

    Use Leitz MPV-SP and program ”Novellus SiO_2 > 50 nm auto 5 points” to measure the oxide thickness. If Leitz MPV-SP is not available use an ellipsometer, however in this case a test wafer needs to be made because the ellipsometer cannot measure the thickness of SiO_2 on a SOI wafer.

20. Coating and baking

    Use EVG120 coater/developer to coat the wafers with resist on the back side and follow the instruction specified for the equipment. The process consists of a treatment with HDMS (hexamethyldisilazane) vapor with nitrogen carrier gas, spin coating with Shipley SPR3012 positive photoresist (spin velocity ???? RPM; spin time) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3012-1.4 µm-noEBR for this procedure.

21. Alignment and exposure

    Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask ”EC2157-channel” with job ”EC2157” (under the file ”special/kawasaki”) at an exposure energy of 90 mJ cm^{-2} on the front side. On the mask there are 7 different designs for the channel to be selected from so choose the one that is suitable for the process (Fig. A.4).

22. Development

    Use EVG 120 coater/developer to develop the exposed area on the backside by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe ”Dev-SP” for this procedure

23. Photoresist inspection

    Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

24. Plasma etching of SiO_2

    Use Drytek Triode 384T plasma etcher. Following the instruction manual of the copy the program ”STDOX” to ”MAGWEGSK” and change the maximum He flow to 30 sccm. Use this program to etch SiO_2. Normally, 3 min 30 s should be sufficient to land on Silicon. Check if it is properly etched using the SEM if not etch additionally using Drytek.

25. Cleaning procedure: Tepla + HNO3 99 % and 65 %

    (a) Plasma strip: Use Tepla plasma system to remove the photoresist in an oxygen plasma. The photoresist are attracted from the ion implanter’s chuck. Follow the instructions specified for Tepla and use the quartz carrier. Use program 4: 1000 W power and abort the process 2 to 3 min after the endpoint curve has gone down.

    (b) Cleaning: Use wet bench ” HNO3 (99 %)” (Silicon) for 10 min.

    (c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

    (d) Cleaning: Use wet bench ” HNO3 (65 %)” (Silicon) for 10 min.

    (e) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

    (f) Drying: Use the Semitool ”rinser/dryer”(Silicon) with the standard program.

26. Deep Reactive Ion Etching of Silicon

    Use Rapier Omega i2L plasma etcher. Select ”wafer view” as the cassette recipe and ”TMP_HAR_TRENCH” for the wafer recipe. The cycle number to etch 40 µm deep is 70 cycle to 80 cycle. A test wafer should be made to check the icicle size and the depth of the channel. The details of this recipe is given in **??**.

27. Deposit 2.0 µm of PECVD SiO_2 on front side

    Use Novellus PECVD reactor to deposit 2.0 µm thick PECVD SiO_2 on the front side of the wafer. This step should be done as soon as possible after the previous step because we noticed that the channel with the mesh begin to swollen and break due tot the water that is absorbed through the atmosphere. Follow the instruction of the machine and use recipe

"zerostresox" at 400 °C. Change the deposition time according to the log-book or use a test wafer to measure the deposition rate beforehand.

28. Measuring thickness

    Use Leitz MPV-SP and program "Novellus SiO_2 > 50 nm auto 5 points" to measure the oxide thickness. If Leitz MPV-SP is not available use an ellipsometer, however in this case a test wafer needs to be made because the ellipsometer cannot measure the thickness of SiO_2 on a SOI wafer.

29. Coating and baking

    Use EVG120 coater/developer to coat the wafers with resist on the front side and follow the instruction specified for the equipment. The process consists of a treatment with HDMS (hexamethyldisilazane) vapor with nitrogen carrier gas, spin coating with Shipley SPR3012 positive photoresist (spin velocity ???? RPM; spin time) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3012-2.1 µm-noEBR for this procedure.

30. Alignment and exposure

    Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask "EC2157-via" with job "EC2157" (under the file "special/kawasaki") at an exposure energy of 200 mJ cm^{-2} on the front side. layer 6 should be selected for this process process (Fig. A.4).

31. Development

    Use EVG 120 coater/developer to develop the exposed area on the front side by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe "Dev-SP" for this procedure

32. Photoresist inspection

    Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

33. Plasma etching of SiO_2

    Use Drytek Triode 384T plasma etcherto etch SiO_2. Following the instruction manual copy the program "STDOX" to "MAGWEGSK" and change the maximum He flow to 30. Use this program to etch SiO_2 and leave a 100 to 200 nm of SiO_2.

34. BHF 1:7 (Silicon) wet etch of SiO_2

    Wet etch the remaining oxide for soft landing.

    (a) Surface tension treatment: Dip wafers in Triton (Silicon) for 1 min to change the surface tension so that the BHF can easily come in contact with the SiO_2 in the next step.

    (b) Wet etch: Use BHF 1:7 (Silicon) to etch the remaining SiO_2.

    (c) Rinse and dry: Rinse the wafer until it reaches 5 MΩ and rinse dry inside Avengers (Metal).

35. Check landing

    Use an optical microscope to check if the openings to the silcon substrate are exposed.

36. Dip etch BHF 0.55 %

    Right before next step a dip etch in BHF 0.55 % was done to remove the native oxide layer that forms at the surface of Silicon.

37. Al/Si(1 %) deposition

    Use the TRIKON SIGMA sputter coater to deposit 2 µm of Al/Si(1 %). The deposition temperature should be 50 °C or lower for less stress. Before the deposition perform target cleaning with dummy wafer at the same temperature if necessary. **If there are ruptures of the seal on the channels, after every spin drying step in the successive steps leave the wafers inside an oven at** 100 °C **for** 5 min **to evaporate the water trapped inside the channel to avoid corrosion.**

38. Coating and baking

    Use EVG120 coater/developer to coat the wafers with resist on the front side and follow the instruction specified for the equipment. The process

consists of a treatment with HDMS (hexamethyldisilazane) vapor with nitrogen carrier gas, spin coating with Shipley SPR3012 positive photoresist (spin velocity ???? RPM; spin time) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3012-2.1 µm-noEBR for this procedure.

39. Alignment and exposure

    Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask "EC2157-interconnect" (rename the mask to A1) with job "20x20 (layer ID: 1)" at an exposure energy of 150 mJ cm^{-2} on the front side. (Fig. A.2).

40. Development

    Use EVG 120 coater/developer to develop the exposed area on the front side by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe "Dev-SP" for this procedure

41. Photoresist inspection

    Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

42. Plasma etching of interconnect and bond pads

    Use Trikon Omega 201 plasma etcher and follow the instruction manual. Use the sequence "AL675TMP" (with a platen temperature of) to etch 2 µm of Al/Si. The etch time in the recipe needs to be changed to 00:15 03:40 02:20 and after using the equipment put the etch time back to its orginal values. After this step visually inspect if the aluminum is etched.

43. Cleaning procedure: Tepla + HNO3 99 %(Green Metal)

    (a) Plasma strip: Use Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for Tepla and

use the quartz carrier. Use program 4: 1000 W power and abort the process 2 to 3 min after the endpoint curve has gone down.

(b) Cleaning: Use wet bench " HNO3 (99 %)" (Green Metal) for 10 min.

(c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

(d) Drying: Use the Semitool "rinser/dryer"(Green Metal) with the standard program or spin dry it and use the oven to evaporate the water inside the channel if necessary.

44. Deposit 2.0 µm of PECVD SiO_2 on front side

Use Novellus PECVD reactor to deposit 2.0 µm thick PECVD SiO_2 on the front side of the wafer. Follow the instruction of the machine and use recipe "zerostresox" at 400 °C. Change the deposition time according to the log-book or use a test wafer to measure the deposition rate beforehand.

45. Measuring thickness

Use Leitz MPV-SP and program "Novellus SiO_2 > 50 nm auto 5 points" to measure the oxide thickness. If Leitz MPV-SP is not available use an ellipsometer, however in this case a test wafer needs to be made because the ellipsometer cannot measure the thickness of SiO_2 on a SOI wafer.

46. Coating and baking

Use EVG120 coater/developer to coat the wafers with resist on the back side and follow the instruction specified for the equipment. The process consists of a treatment with HDMS (hexamethyldisilazane) vapor with nitrogen carrier gas, spin coating with Shipley SPR3012 positive photoresist (spin velocity ???? RPM; spin time) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3027-4.0 µm-noEBR for this procedure.

47. Alignment and exposure

Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask "EC2157-bondpad" with job "20x20" at an exposure energy of 500 mJ cm^{-2} on the front side (Fig. A.3).

48. Development

    Use EVG 120 coater/developer to develop the exposed area on the backside by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe ”Dev-SP” for this procedure

49. Photoresist inspection

    Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

50. Plasma etching of SiO_2

    Use Drytek Triode 384T plasma etcher. Following the instruction manual of the copy the program ”STDOX” to ”MAGWEGSK” and change the maximum He flow to 30 sccm. Use this program to etch 2 µm of SiO_2. Normally, 4 min should be sufficient to land on the aluminium.

51. Cleaning procedure: Tepla + HNO3 99 %(Green Metal)

    (a) Plasma strip: Use Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for Tepla and use the quartz carrier. Use program 4: 1000 W power and abort the process 2 to 3 min after the endpoint curve has gone down.

    (b) Cleaning: Use wet bench ” HNO3 (99 %)” (Green Metal) for 10 min.

    (c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

    (d) Drying: Use the Semitool ”rinser/dryer”(Green Metal) with the standard program or spin dry it and use the oven to evaporate the water inside the channel if necessary.

52. Coating and baking

    Use EVG120 coater/developer to coat the wafers with resist on the back side and follow the instruction specified for the equipment. The process consists of a treatment with HDMS (hexamethyldisilazane) vapor with

nitrogen carrier gas, spin coating with Shipley SPR3012 positive photoresist (spin velocity ???? RPM; spin time) and a soft bake at 95 °C for 1.5 s. Always check the temperature of the hotplates and the relative humidity (48±2 %) in the room first. Use recipe Co-3027-4.0 µm-noEBR for this procedure.

53. Alignment and exposure

    Use ASML PAS550/80 automatic wafer stepper. Following the instruction manual of the machine, expose mask "EC2157-channel" with job "EC2157" (under the file special/kawasaki) with layer ID 1 at an exposure energy of 500 mJ cm^{-2} on the front side (Fig. A.4).

54. Development

    Use EVG 120 coater/developer to develop the exposed area on the backside by following the instruction of the equipment. The process consists of a post-exposure bake at 115 °C for 1.5 min, followed by a development step using Shipley MF322 developer (single puddle process) and a hard bake at 100 °C for 1.5 min. Use development recipe "Dev-SP" for this procedure

55. Photoresist inspection

    Visually inspect the wafers through a microscope that uses filtered light so the photoresist does not get further exposed. Check if there are any photoresist residue or unexposed/undeveloped areas.

56. Plasma etching of SiO_2

    Use Drytek Triode 384T plasma etcher. Following the instruction manual of the copy the program "STDOX" to "MAGWEGSK" and change the maximum He flow to 30. Use this program to etch 4 µm of SiO_2. Normally, 8 min should be sufficient to open the inlet/outlet ports. To avoid resist burning it maybe better to divide the step in two steps.

57. Vapor HF to remove the PECVD SiO_2 in the inside

    Use vapor HF for 3 min to remove 100 to 300 nm of PECVD SiO_2 that formed inside the channel.

58. Cleaning procedure: Tepla + HNO3 99 %(Green Metal)

(a) Plasma strip: Use Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for Tepla and use the quartz carrier. Use program 4: 1000 W power and abort the process 2 to 3 min after the endpoint curve has gone down.

(b) Cleaning: Use wet bench " HNO3 (99 %)" (Green Metal) for 10 min.

(c) Rinsing: Rinse with the standard program until the resistivity is 5 MΩ.

(d) Drying: Use the Semitool "rinser/dryer"(Green Metal) with the standard program or spin dry it and use the oven to evaporate the water inside the channel if necessary.

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