A Glimpse of the History of Analog ICs: A Tale of Amplifiers, Data Converters, and Sensor Interfaces

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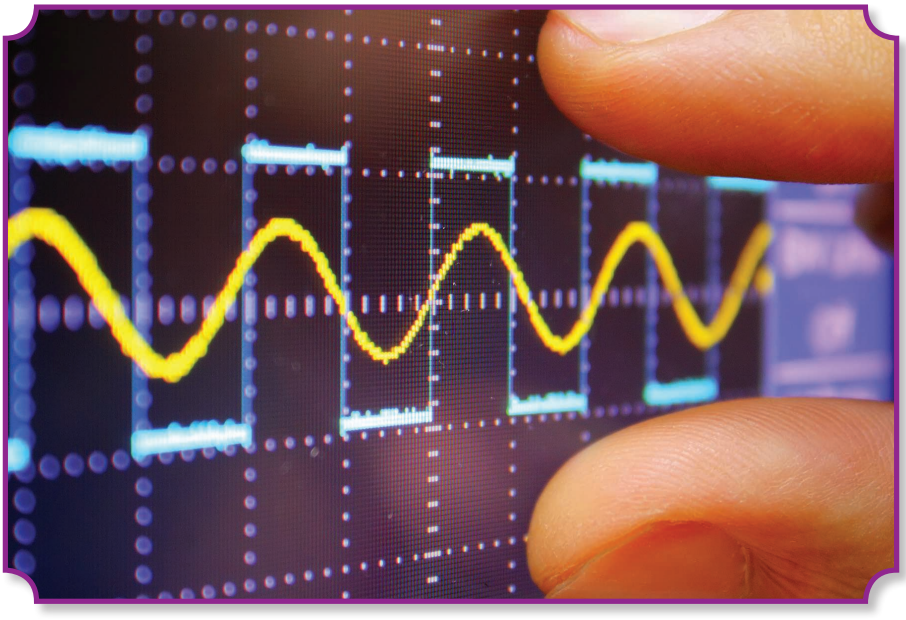

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Probably the most distinct divide in electronic circuits is that between digital and linear (analog) circuits. Using vacuum tubes; later, transistors; and then ICs, circuits based on switching (binary and digital signals) and amplification (analog signals) have always been at the heart of electronic systems. Even though electronics are making our world more digital, the real world remains stubbornly analog. Circuits for interfacing sensors and driving actuators, amplifying (weak) analog signals, manipulating these signals through analog signal processing, and, finally, converting them into the digital domain and vice versa were, are, and will remain fundamental research and development fields in circuit design. Due to the wide scope of the field, ranging from RF circuits, power management, reference generation, filter design, and oscillators to comparators and other nonlinear circuits, just to name a few, it is clear that a short review article cannot possibly mention all topics, let alone cover them all. So, choices were made. We begin this article with amplifiers, which are one of the critical analog building blocks that often determine system performance. We briefly review the early days of IC-based amplifiers and some outstanding circuit innovations for amplifier design. Thereafter, we highlight the history and state of the art of ADCs, their architectures, and efficiency improvements over four decades. Finally, we review sensor interfaces, first with a general focus on their history and

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the state of the art of various sensor modalities and, second, with a special focus on biomedical interface circuits for biopotential recording in the context of neural amplifiers. With this variety of topics, we intend to highlight the importance of the transistor and analog ICs to the world as we know it today.

Amplifiers

Amplifiers are the cornerstone of all analog circuits, as they are used in signal conditioning and processing, low-noise applications, ADCs, and so on. While the first IC-based operational amplifier (OA), Widlar's µA702, already had two stages, it was the ubiquitous µA741 that established itself as the workhorse of early PCB-based designs. It had two stages, a differential input stage and a class AB output stage. Its CMOS equivalent is still in use but often with CMOS inverters replacing the single transistors in its signal path, as shown in Figure 1.

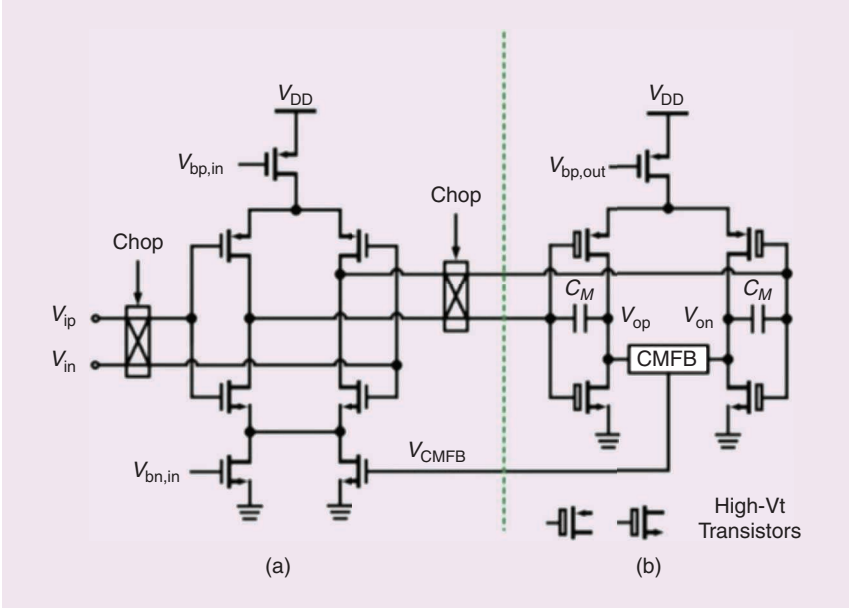

FIGURE 1: A Miller CMOS OTA with CMOS inverters [1]. The (a) input stage and (b) output stage. CMFB: common-mode feedback.

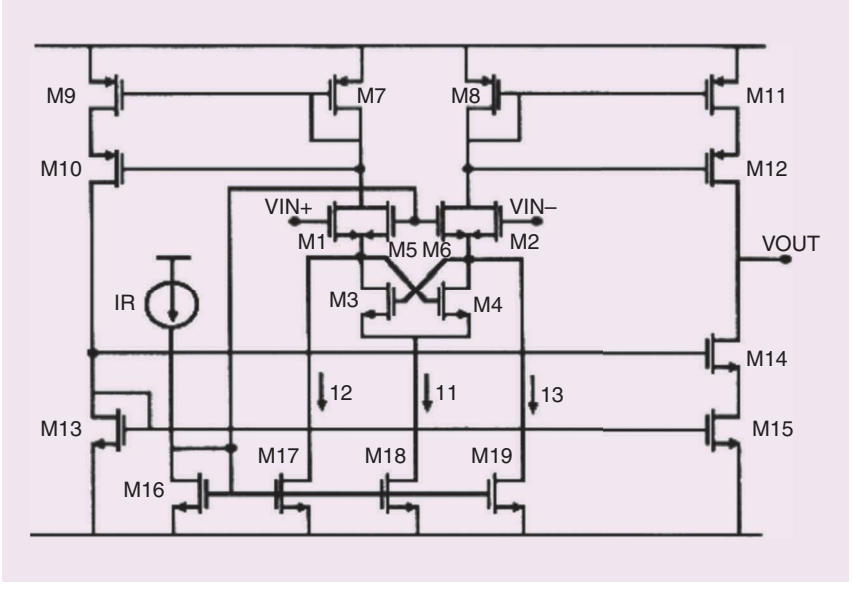

FIGURE 2: The increased input transconductance by negative resistance [4].

The amplifier is fully differential and so requires a common-mode feedback circuit. The Miller compensation capacitor (C_M) sets the amplifier's GBW product and ensures the phase margin. Chopping is used to mitigate offset and $1/f$ noise. However, the power efficiency of this classic design is only moderate. Consequently, many other designs have been proposed over the past decades to reduce the power needed to achieve a given speed, such as feedforward, multistage, positive feedback, and dynamic architectures [2].

The use of a single stage to bypass a two-stage amplifier is called *feedforward*, while the use of a two-stage amplifier to bypass a single-stage amplifier is called *gain enhancement*. However, these two terms both describe essentially the same circuit! Feedforward introduces a left-plane zero that ensures stability by canceling a nondominant pole [3]. Compared to Miller compensation, the efficiency of a feedforward amplifier can easily be better by factor of two to three.

Even better efficiency can be achieved by using negative impedances or positive feedback. Negative capacitances have been used for a long time to extend the bandwidth of RF amplifiers, while negative resistances have been used in OAs. As demonstrated in Figure 2, connecting a negative resistance (M_3, M_4) to the sources of the input pair (M_1, M_2) increases the transconductance and GBW for the same power consumption [5]. Negative resistances can also be connected to the loads of the input stage of a symmetric or load-compensated amplifier [5]. They can also be used to cancel offset and lack of gain [6] and so are a recommended building block in high-performance amplifiers.

Multistage amplifiers also enable considerable power reduction. In three-stage amplifiers, the second stage is used to create zeros, which compensate the nondominant poles. Second-order pole-zero compensation is realized in the three-stage amplifier [7] in Figure 3: the value of the transconductance gm_t

will usually be about two to three times larger than gm_2. As a result, the power consumption of the second stage can be lowered while still yielding a GBW of about 40× larger than for the conventional nested-Miller three-stage amplifier, leading to an amplifier FOM ≈ 20,000 MHz · pF/mA. More complex active filters in the intermediate stages of a four-stage amplifier give rise to an even more stunning FOM = 96,000 MHz · pF/mA [8].

In sampled data systems, dynamic amplifiers can be advantageously used because they allow only the required bandwidth to be used, thus minimizing the power consumption for a given noise requirement. Dynamic inverter-based amplifiers have already been reported in [9]. The same circuit configurations are often used, also with switches in all biasing branches, as described in Figure 4. Another type is the floating inverter dynamic amplifier [11], where the supply voltage is switched rather than the amplifiers. This provides proper biasing with limited power consumption.

Considerable further power savings have been realized by using more efficient (like class AB) amplifier topologies [12]. Also, class C and ring oscillator amplifiers provide superior power savings [13], [14]. In particular, class D amplifiers, in which the output devices are switched at a high frequency, can provide close to 100% power efficiency at very low levels of distortion and are often used in audio applications [15].

Data Converters

Such innovations in amplifiers blur the boundary between digital and analog circuit implementation, which leads us to the second topic of this brief review, the analog–digital interface, i.e., the data converter. It is the last—or the first, depending on the signal flow—part in the analog signal chain. Even though DACs also play an important role in electronic systems, we limit this brief historic review to ADCs because of their wider variety and much greater visibility and

In sampled data systems, dynamic amplifiers can be advantageously used because they allow only the required bandwidth to be used, thus minimizing the power consumption.

because almost all ADCs also employ an internal DAC. We thereby glimpse architectural innovations and performance evolution over more than 40 years since the first appearance of integrated ADCs. A very complete handbook, including a huge historical overview of data converters, has been written by Walt Kester, and the interested reader is referred to [16].

The basic principles of quantization and ADCs were explored, invented, patented, and published long before ICs emerged. Some of the best-known works are Howard's proposal of a tracking ADC [17], Inose's proposal of the delta–sigma modulator (DSM) [18], and Kaiser's work on the SAR ADC [19]. However, flash, subranging, pipeline, counting, slope, voltage-to-frequency conversion, and other ADC architectures were proposed one to two decades before the first ICs appeared. These early implementations were based on vacuum tubes (e.g.,

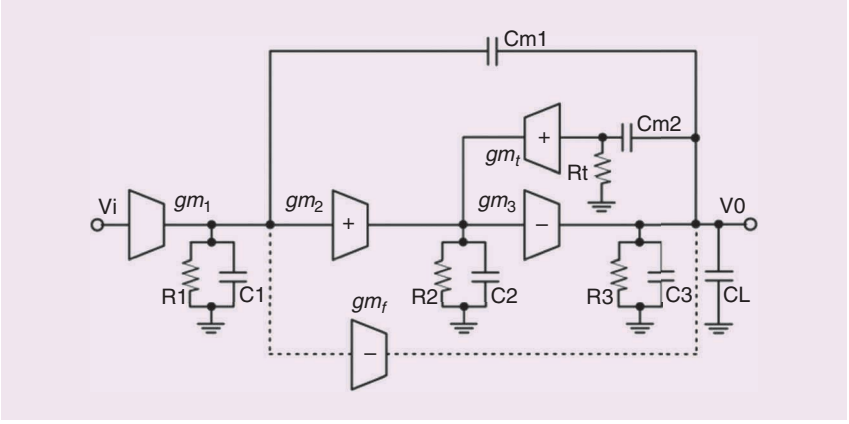

FIGURE 3: Capacitive feedback compensation [7].

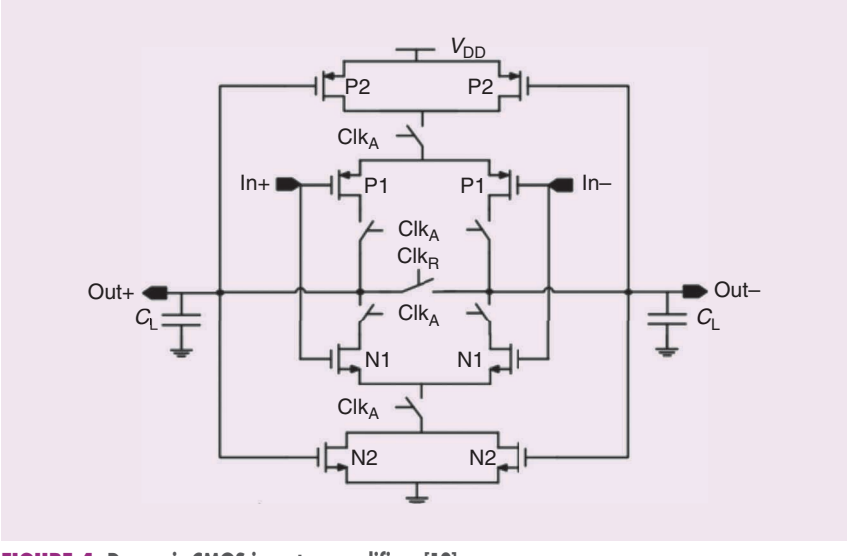

FIGURE 4: Dynamic CMOS inverter amplifiers [10].

Due to technology scaling and circuit innovation, the best reported ADC efficiencies have improved by almost six orders of magnitude over 40 years.

the first commercial SAR ADC, released in 1954), and, after the IC's invention, they were based on discrete transistors. But it was not until the early 1970s that hybrid and modular ADCs based on IC building blocks, as well as fully integrated data converters, appeared. Two are notable: Paul Brokaw's design of the first complete monolithic SAR ADC, including reference generation, achieving 10 b with 40 MS/s, introduced in 1978 [21], and van der Plassche's first-order DSM, achieving 6 b at a 200-kHz clock frequency and including autozeroing, introduced in 1977 [20], both in bipolar technologies.

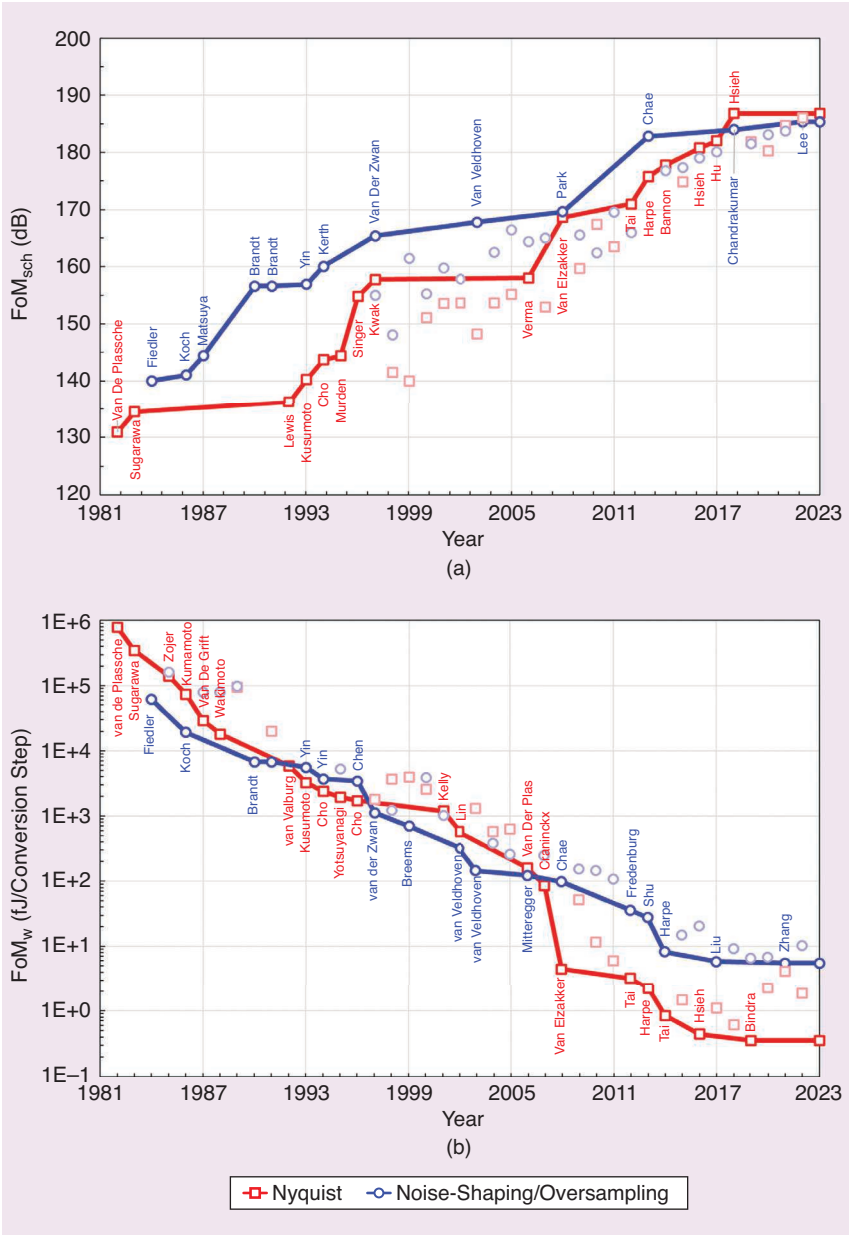

FIGURE 5: The evolution of the yearly best reported (a) Schreier and (b) Walden FOM for Nyquist and noise-shaping ADCs, including front line, based on [30] and extended with [29].

The 1980s represented an era of high growth in many applications, with the first commercial monolithic 16-b DSM appearing in 1988. More detailed specifications, such as the SNR, SNDR, ENOB, SFDR, aperture jitter, and so on, began to appear on data sheets. While improvements in IC technology, together with circuit and system research, mainly dictated progress, distinctively new principles were still being discovered. For example, the concept of time-interleaved ADCs was proposed in 1980 [22], while the incremental, MASH, and bandpass DSMs were published in the late 1980s. The combination of different ADC principles into innovative hybrid forms still drives innovation today, such as the use of SAR in pipeline ADCs or DSMs [23] or the use of VCO-based quantizers and their inclusion into DSMs [24]. Furthermore, the use of DSP to correct for the nonidealities of analog circuitry is now ubiquitous [25].

Over time, thousands of ADC designs have been made, and so comparing their performance has become a subject of great interest. ADCs are probably the most well specified of all circuit building blocks, with their FOM being the most important. The two most commonly used are the Walden FOM_W, proposed in 1994 [26], and the Schreier FOM_S, described by Richard Schreier in 2005 [27] but proposed as early as 1997 [28]. Today, Boris Murmann's performance survey [29] covering all IEEE International Solid-State Circuits Conference (ISSCC) and IEEE Symposium on VLSI Technology and Circuits results since 1998 is universally cited in almost all data converter publications. A chart showing the best reported FOM_W over the past 40 years is in Figure 5, based on the database of [30] and extended using [29].

Amazingly, due to technology scaling and circuit innovation, the best reported ADC efficiencies have

improved by almost six orders of magnitude over 40 years. However, the best reported FOM_W appears to have saturated, and one can also expect that the record FOM_S will soon follow. A closer look at the data shows that the best FOM_S is obtained for a limited class of architectures: medium-resolution/speed SAR obtains the best FOM_W, while high-resolution low-bandwidth noise-shaping SAR and hybrid SAR + DSM ADCs achieve the best FOM_S. This emphasizes the fact that a single number does not tell the whole story, and so FOM comparisons should be made between ADCs that are intended for the same applications. Furthermore, the power consumed by calibration engines, decimation filters, and input and reference buffers are often neglected in reporting FOM_S. Fortunately, this is well understood by the data converter community, and so there is an increasing focus on converters with easier drivability, implicit filtering, better calibration-free linearity, and so on, rather than just a new record FOM.

In the past decade, a few megatrends in ADCs can be observed. First, the SAR ADC, mainly driven by its superior efficiency in scaled CMOS, has become omnipresent and can be found from the highest energy efficiency to the fastest speed time-interleaved ADCs; the use of noise and mismatch error shaping blurs the difference with DSMs, and they are often used as the quantizer of a DSM loop in the latest state of the art. Second, DSMs covering incredible bandwidths can be found, especially based on CT loop filters, with their intrinsic filtering, easier drivability, hundreds of megahertz of bandwidth, and linearity even in excess of 100 dB. With the same trend toward wider bandwidth and significant improvement in aperture uncertainty, Nyquist ADCs are available with multigigahertz bandwidth and resolutions greater than 10 b. With wider bandwidth and easier drivability, hybrid (CT + DT) ADCs are a successful alternative to classical structures. Finally, time-based quantization benefits from technology scaling and is now the most area-efficient solution for low- (or medium-) resolution ADCs or as part of high-resolution ADCs.

For the past two decades, the development of smart sensors has been mainly driven by the requirements of mobile devices and automotive applications.

Smart Sensor Interfaces

ADCs directly interfacing with transducers and sensors have received increasing attention over the past decades. This leads us to the field of smart sensor interfaces. Today, sensors surround us in our homes, our cars, and our phones. Most of these sensors are "smart" in the sense that they are cointegrated with all the interface circuitry needed to amplify, linearize, and convert their weak analog outputs into robust digital data. By cleverly exploiting the properties of silicon, smart sensors can be designed to measure a wide variety of physical phenomena, such as light, force, heat, and magnetic fields, to name but a few.

The invention of the transistor and, subsequently, the IC spurred extensive research into the properties of semiconductors. It was soon discovered that they could be used to make sensors as well as circuits. In the 1960s, sensors for pressure, stress, temperature [31], and magnetic fields [32] were reported at ISSCC. These were followed by image sensors, beginning with the CCD [33] and followed by the CMOS image sensor [34], which, because of its lower manufacturing cost, became the dominant technology. It was also discovered that the well-defined characteristics of BJTs could be used to realize accurate voltage references [35] and temperature sensors [36]. Another significant development was the use of micromachining to create MEMSs [37]. This rapidly led to the realization of sensors with moving parts, such as pressure sensors, accelerometers, and gyroscopes.

Early silicon sensors typically output small analog signals, which were then amplified, processed, and digitized by external electronics. By the 1970s, however, the availability of monolithic amplifiers meant that amplification and filtering could be done on chip. Initially, trimmed BJT amplifiers were used to achieve low offset and $1/f$ noise. Soon, the use of dynamic error reduction techniques, such as chopping and autozeroing, made it possible for CMOS amplifiers to achieve similar performance [38]. Furthermore, by using DEM [39], [40], gain (or ratio) errors could be reduced to the ppm level. Various combinations of these techniques, e.g., autozeroing and chopping [41], nested chopping [42], and DEM and chopping [43], have led to amplifiers with a nanovolt-level offset and ppm-level gain error/linearity.

The next step in the evolution of smart sensors was the development of robust interfaces to the outside world. In the 1980s, sensors often employed frequency and duty cycle modulators [44]. By encoding analog information in the timing of the transitions of two-level signals, such modulators could output microprocessor-compatible signals without limiting sensor resolution. However, the subsequent conversion to

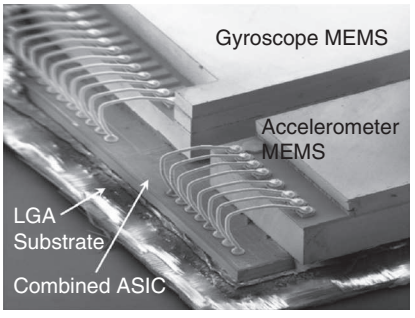

FIGURE 6: Inside a multidie inertial sensor. LGA: land grid array. (Source: Bosch; used with permission.)

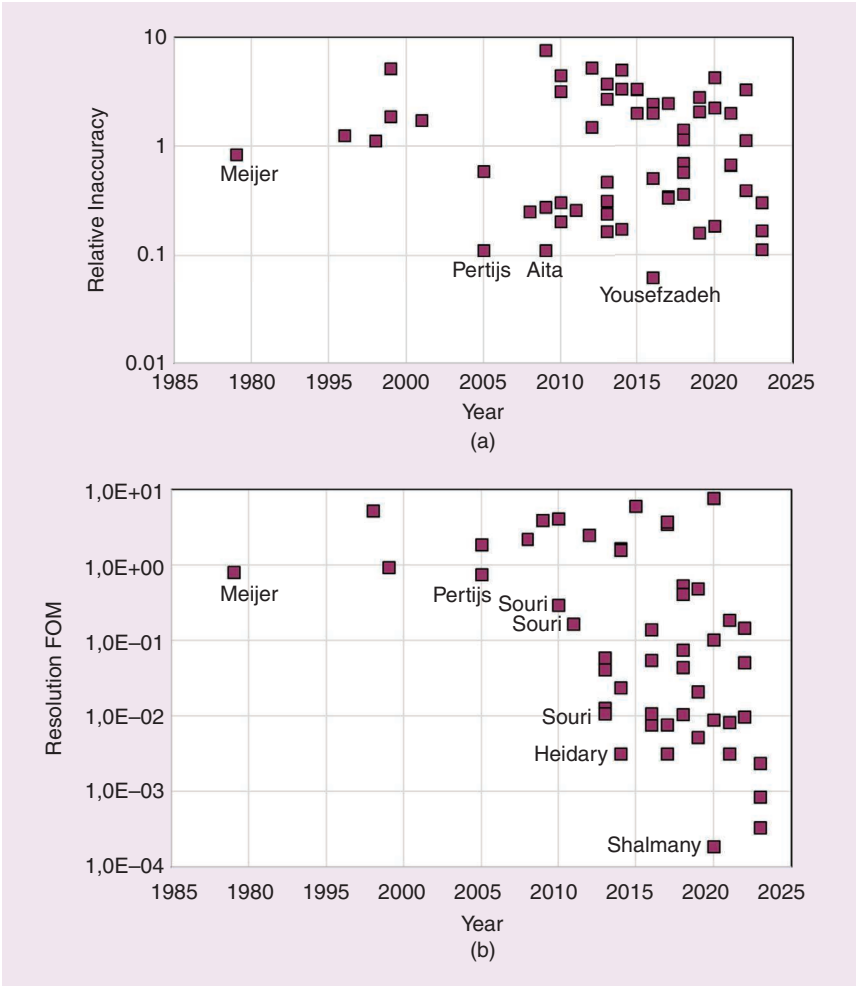

FIGURE 7: The evolution of the (a) relative inaccuracy and (b) resolution FOM (energy efficiency) of BJT-based temperature sensors (based on [46]).

high-resolution digital data then required a low-jitter high-frequency reference clock. Furthermore, there was no standardization, and so each sensor required its own specific signal chain.

This all changed with the development of monolithic ADCs and, in particular, the DSM [45]. The latter's ability to trade speed for resolution meant that the relatively slow outputs of sensors could be digitized on chip without limiting their resolution. In turn, on-chip digitization allowed smart sensors to communicate with the outside world via standard digital buses and protocols. This made them much easier to use and allowed them to be marketed as stand-alone building blocks with well-defined specifications. Furthermore, it allowed much of the required on-chip signal processing (filtering, trimming, and linearization) to be done flexibly and precisely in the digital domain.

In an attempt to reduce cost, much effort was devoted to the development of CMOS-compatible sensors, which could then be integrated on the same die with their interface electronics. However, with some exceptions (thermal and magnetic field sensors), this approach imposes too many constraints on sensor performance. Today, most smart sensors employ a two-die approach, with the sensor being implemented on one die (or substrate) with an optimized manufacturing process while the CMOS interface is implemented on the other. This approach also facilitates the cointegration of multiple sensors in a single package (see Figure 6).

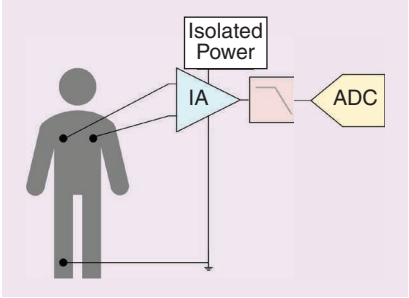

FIGURE 8: A typical wearable biopotential readout system. IA: instrumentation amplifier.

Spurred by sensor and circuit innovations, smart sensors have come a long way since the 1980s. BJT-based temperature sensors are a case in point. The evolution of their accuracy and energy efficiency is plotted in Figure 7 using data from Kofi Makinwa's online survey [46]. Although their accuracy now appears to have plateaued, reflecting the limits imposed by process spread and calibration cost, their energy efficiency has improved by nearly four orders of magnitude, reflecting improvements in their interface electronics. Similar trends can be seen for other types of smart sensors.

For the past two decades, the development of smart sensors has been mainly driven by the requirements of mobile devices and automotive applications. The current trend toward an IoT, however, has spurred research into the development of autonomous smart sensors, i.e., energy-harvesting sensors that can be powered by ambient energy and thus do not need batteries [47]. Sensor fusion, where a design combines multiple sensors and local intelligence to achieve better performance, is another major trend.

Biomedical Sensor Interfaces

While the sensor interfaces discussed in the preceding have in common that they are cointegrated with a sensor, biomedical sensor interfaces are connected to a biological signal source. Those are covered in the final section of this review, as the invention of the transistor, the IC, and technology scaling have enabled erstwhile unseen applications of electronics. Electrophysiology studies the electrical properties of

biological cells and tissues, and it plays a crucial role in understanding the functioning of the human body. It involves not only the measurements of voltage changes, electric currents, and bioimpedances but also the manipulation of biological tissues at different scales. The roots of electrophysiology can be traced back to the groundbreaking research of Luigi Galvani, who discovered, in 1791, that the muscles of dead frogs could be activated by the application of electrical currents. This inspired research into the concept of "bioelectricity" and eventually led to the development of instrumentation for recording the small electrical currents and potentials of tissue and even individual cells.

After the invention of transistors and ICs, the emerging analog circuit design techniques were adopted for the development of more advanced, miniaturized, and implantable biomedical interfaces. A highly impactful early result was the invention of the first implantable cardiac pacemaker, in 1958 (by Ake Senning). In the 1970s, this was greatly improved by the introduction of IC sensing amplifiers, digital logic, and noninvasive electronic control [48]. In the same decade, groundbreaking work on the use of implantable microelectrodes for the recording of brain biopotentials was reported by Kensall Wise [49]. These developments laid the foundations for modern silicon neural probes.

Today, modern electrophysiology techniques allow the accurate measurement of biopotentials originating from the heart, brain, nerves, and muscles. In particular, wearable cardiac monitoring has become increasingly popular, especially for the long-term monitoring of patients with cardiovascular conditions. ICs and technology scaling enable a broad range of biomedical devices, including implants for sensory prostheses (e.g., cochlear and retinal implants), motor prostheses (e.g., to control robotic arms), brain pacemakers (i.e., deep brain stimulators), glucose sensing, and insulin delivery, among many others.

The invention of the transistor and the IC and the ensuing technology scaling have changed our world more than most inventions in human history.

Many of these biomedical applications require specialized readout electronics to acquire biopotentials with high signal quality. As illustrated in Figure 8, low noise, high input impedance, a high common-mode rejection ratio, and a large differential input range to avoid saturation caused by motion artifacts [38] are critical for reliable and accurate wearable readout systems [50]. In addition, very low power consumption is required to achieve reasonable battery life. Typically, a fully differential high-input-impedance instrumentation amplifier (IA) is used to amplify biopotential signals. Since the IA characteristics dominate the

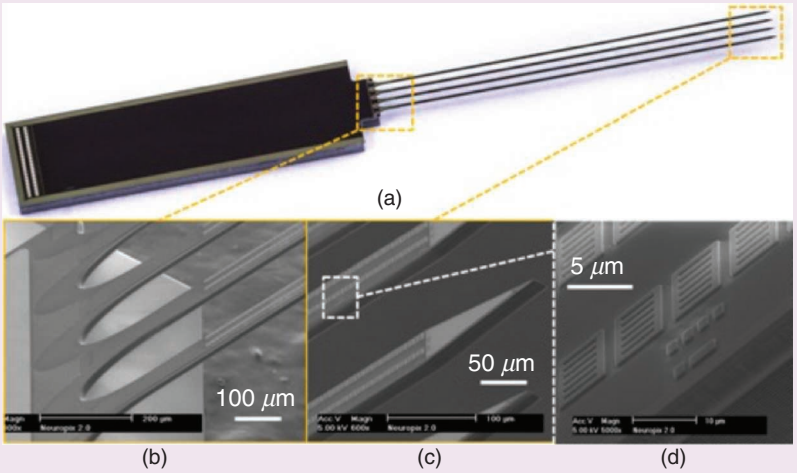

FIGURE 9: (a) A fully fabricated Neuropixels 2.0 CMOS probe, with details of the probe (b) neck, (c) tip, and (d) electrodes [53].

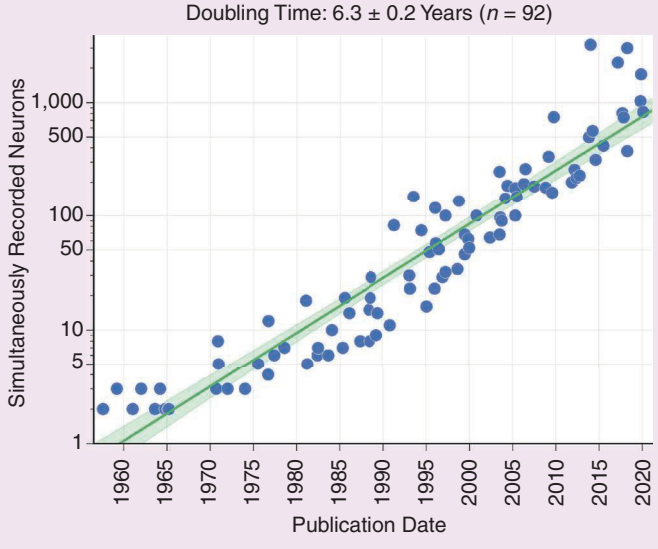

FIGURE 10: The 2020 version of the Moore's law of neuroscience plot reported in [56].

While technology scaling has given us tremendous improvements in transistor operating speed and integration density, it has also exacerbated transistor nonidealities.

overall performance of the readout chain, many circuit techniques have been proposed to achieve the aforementioned requirements, even in the presence of large dc offsets and low frequency drifts originating from the polarization voltage of the electrodes. To reduce common-mode interference, a third electrode that biases the body to a dc voltage through an active feedback loop called "right-leg drive" is commonly used [51].

Neural recording using implantable probes has become a popular method for measuring electrical neural activity at the single-cell level [52]. Silicon probes have advantages, such as precise shank shapes, accurate fabrication processes, automation capabilities, and integration with CMOS circuits. An example of a fully integrated CMOS probe is presented in Figure 9. Neural recording circuits must tackle several challenges, including a small neural signal amplitude, low signal frequency, electrode offset, high electrode impedance, and need for high-density neural interfaces. Two neural readout architectures are commonly used: a conventional architecture consisting of an ac-coupled IA and an ADC and a direct digitization approach with an input transconductance stage merged within the ADC loop.

In the conventional architecture, first proposed in [54], ac coupling effectively blocks the electrode offsets, while high-impedance pseudoresistors are used to set the dc bias of the IA's input nodes. The ac coupling capacitor must be large enough to provide sufficient gain but not too large so as to avoid excessive deterioration of the ac input impedance. Different amplifier architectures can be used in the IA, with folded-cascode and inverter-based OTAs being popular choices [55]. The multiplexing ratio needs to be optimized to solve the tradeoff between the power and area required for the ADC and its preceding driver [53]. A SAR ADC is commonly used due to its good power efficiency in the moderate-resolution and low-frequency ranges. Since conventional ac-coupled readouts have limited scalability, limited input dynamic range, and undesirable sensitivity to process variation, direct-to-digital readout architectures have been recently explored as a solution. For this, oversampling ADCs can be employed to develop recording-only or artifact-tolerant architectures for bidirectional neural interfaces. Different readouts based on delta–sigma modulation, delta modulation, and a combination of both have been proposed; these can be very compact and scalable.

Overall, the field of wearable and implantable bioelectronics continues to evolve and improve, with new sensor technologies and circuit techniques being developed to provide more accurate and comfortable monitoring. In the neuroscience field, silicon neural probes are getting denser and, as shown in Figure 10, allow the recording of more and more neurons simultaneously. However, designing neural interfaces with increased parallel recording capabilities presents a new challenge: the data bottleneck. To address this challenge, ongoing research focuses on implementing on-chip data analytics. This brings exciting design challenges and opportunities for analog and mixed-signal front-end designers.

Conclusion

Analog circuits interface the real world with the world of electronics. The invention of the transistor 75 years ago gave us a tiny robust device that could switch and amplify. Analog circuits use both these functions of the transistor in many varied and ever-changing ways. The invention of the transistor and the IC and the ensuing technology scaling have changed our world more than most inventions in human history. While technology scaling has given us tremendous improvements in transistor operating speed and integration density, it has also exacerbated transistor nonidealities, which have resulted in architectural and circuit innovations as well as in extensive digitally assisted analog circuit design. This review gave an insight into a tiny fraction of the contributions of analog circuits, from circuit innovation of amplifiers to architectural innovations of data converters and system innovations in the field of sensor interfaces. As long as we live in an analog world, many more contributions and innovations will come in the future.

References

[1] S. Pan et al., "A 0.12mm^2 wien-bridge temperature sensor with 0.1°C (3σ) inaccuracy from -40°C to 180°C," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2019, pp. 184–186, doi: 10.1109/ISSCC.2019.8662457.

[2] W. Sansen, *Analog Design Essentials*. New York, NY, USA: Springer-Verlag, 2006.

[3] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested G/sub m/-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997, doi: 10.1109/4.643658.

[4] R. Castello, A. G. Grassi, and S. Donati, "A 500-nA sixth-order bandpass SC filter," *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp. 669–676, Jun. 1990, doi: 10.1109/4.102659.

[5] K. B. Ohri and M. J. Callahan, "Integrated PCM codec," *IEEE J. Solid-State Circuits*, vol. 14, no. 1, pp. 38–46, Feb. 1979, doi: 10.1109/JSSC.1979.1051139.

[6] M. Jang, C. Lee, and Y. Chae, "Analysis and design of low-power continuous-time delta-sigma modulator using negative-R assisted integrator," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 277–287, Jan. 2019, doi: 10.1109/JSSC.2018.2871111.

[7] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1514–1520, Jul. 2005, doi: 10.1109/JSSC.2005.847216.

[8] W. Qu et al., "Design-oriented analysis for miller compensation and its application to multistage amplifier design," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 517–527, Feb. 2017, doi: 10.1109/JSSC.2016.2619677.

[9] J. A. Archer, F. A. Petz, and H. P. Weidlich, "GaAs FET distributed amplifier," *Electron. Lett.*, vol. 17, no. 13, pp. 433–434, Jun. 1981, doi: 10.1049/el:19810303.

[10] B. Verbruggen et al., "A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28nm digital CMOS," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, 2014, pp. 1–2, doi: 10.1109/VLSIC.2014.6858451.

[11] M. S. Akter, K. A. A. Makinwa, and K. Bult, "A capacitively degenerated 100-dB linear 20–150 MS/s dynamic amplifier," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1115–1126, Apr. 2018, doi: 10.1109/JSSC.2017.2778277.

[12] F. Krummenacher, E. Vittoz, and M. Degrauwe, "Class AB CMOS amplifier micropower SC filters," *Electron. Lett.*, vol. 17, no. 13, pp. 433–434, Jun. 1981, doi: 10.1049/el:19810304.

[13] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009, doi: 10.1109/JSSC.2008.2010973.

[14] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, and U.-K. Moon, "Ring amplifiers for switched capacitor circuits," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2928–2942, Dec. 2012, doi: 10.1109/JSSC.2012.2217865.

[15] R. A. R. van der Zee and E. A. J. M. van Tuijl, "A power-efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, Jul. 1999, doi: 10.1109/4.772414.

[16] W. Kester, Ed., *The Data Conversion Handbook*. Oxford, U.K.: Analog Devices, 2004.

[17] B. K. Howard, "Binary quantizer," U.S. Patent 2 715 678, 1955.

[18] H. Inose, Y. Yasuda, and J. Murakami, "A telemetering system by code modulation: Δ-Σ modulation," *IRE Trans. Space Electron. Telemetry*, vol. SET-8, no. 3, pp. 204–209, Sep. 1962, doi: 10.1109/IRETSET.1962.5008839.

[19] H. R. Kaiser et al., "High-speed electronic analogue-to-digital converter system," U.S. Patent 2 784 396, Mar. 1957.

[20] R. van de Plassche and R. E. J. van Der Grift, "A five-digit analog-digital converter," *IEEE J. Solid-State Circuits*, vol. 12, no. 6, pp. 656–662, Dec. 1977, doi: 10.1109/JSSC.1977.1050975.

[21] P. Brokaw, "A monolithic 10-bit A/D using I^2L and LWT thin-film resistors," *IEEE J. Solid-State Circuits*, vol. 13, no. 6, pp. 736–745, Dec. 1978, doi: 10.1109/JSSC.1978.1052044.

[22] W. C. Black and D. A. Hodges, "Time-interleaved converter arrays," *IEEE J. Solid-State Circuits*, vol. 15, no. 6, pp. 1022–1029, Dec. 1980, doi: 10.1109/JSSC.1980.1051512.

[23] L. Samid, M. Ortmanns, Y. Manoli, and F. Gerfers, "A new kind of low-power multibit third order continuous-time lowpass ΣΔ modulator," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2002, p. III, doi: 10.1109/ISCAS.2002.1010218.

[24] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "An architecture of Delta-Sigma A-to-D converters using a voltage controlled oscillator as a multi-bit quantizer," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 1998, pp. 389–392, doi: 10.1109/ISCAS.1998.704448.

[25] B. Murmann and B. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003, doi: 10.1109/JSSC.2003.819167.

[26] R. H. Walden, "Analog-to-digital converter technology comparison," in *Proc. IEEE GaAs IC Symp.*, 1994, pp. 217–219, doi: 10.1109/GAAS.1994.636970.

[27] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2005.

[28] S. Rabii and B. A. Wooley, "A 1.8-V digital-audio sigma–delta modulator in 0.8-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783–796, Jun. 1997, doi: 10.1109/4.585245.

[29] B. Murmann. "ADC performance survey 1997–2022." GitHub. Accessed: Apr. 15, 2023. [Online]. Available: https://github.com/bmurmann/ADC-survey

[30] B. E. Jonsson, "A/D-converter performance evolution," Converter Passion, Aug. 2012. [Online]. Available: https://converterpassion.wordpress.com/2012/08/26/adc-performance-evolution-thermal-figure-of-merit-fom/

[31] E. Stern, "Solid-state sensors for process control," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1963, pp. 60–61, doi: 10.1109/ISSCC.1963.1157466.

[32] P. W. Fry, "A silicon MOS magnetic-field transducer of high sensitivity," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1968, pp. 94–95, doi: 10.1109/ISSCC.1968.1154603.

[33] R. Melen and J. Meindl, "A transparent-electrode CCD image sensor," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1973, pp. 130–131, doi: 10.1109/ISSCC.1973.1155215.

[34] P. B. Denyer, D. S. Renshaw, G. Wang, M. Y. Lu, and S. Anderson, "On-chip CMOS sensors for VLSI imaging systems," in *Proc. IFIP Trans. VLSI*, 1991, p. 10.

[35] R. J. Widlar, "New developments in IC voltage regulators," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1970, pp. 158–159, doi: 10.1109/ISSCC.1970.1154790.

[36] R. Dobkin, "Monolithic temperature transducer," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 1974, pp. 126–127, doi: 10.1109/ISSCC.1974.1155303.

[37] K. E. Peterson, "Silicon as a mechanical material," *Proc. IEEE*, vol. 70, no. 5, pp. 420–457, May 1982, doi: 10.1109/PROC.1982.12331.

[38] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996, doi: 10.1109/5.542410.

[39] K. B. Klaassen, "Digitally controlled absolute voltage division," *IEEE Trans. Instrum. Meas.*, vol. 24, no. 2, pp. 106–112, Jun. 1975, doi: 10.1109/TIM.1975.4314388.

[40] R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. 11, no. 6, pp. 795–800, Dec. 1976, doi: 10.1109/JSSC.1976.1050820.

[41] R. Poujois and J. Borel, "A low drift fully integrated MOSFET operational amplifier," *IEEE J. Solid-State Circuits*, vol. 13, no. 4, pp. 499–503, Aug. 1978, doi: 10.1109/JSSC.1978.1051084.

[42] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000, doi: 10.1109/4.890300.

[43] R. Wu, J. H. Huijsing, and K. A. A. Makinwa, "A current-feedback instrumentation amplifier with a gain error reduction loop and 0.06% untrimmed gain error," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2794–2806, Dec. 2011, doi: 10.1109/JSSC.2011.2162923.

[44] G. C. M. Meijer, R. van Gelder, V. Nooder, J. van Drecht, and H. M. M. Kerkvliet, "A three-terminal intergrated temperature transducer with microcomputer interfacing," *Sens. Actuators*, vol. 18, no. 2, pp. 195–206, Jun. 1989, doi: 10.1016/0250-6874(89)87018-0.

[45] B. Boser and B. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, Dec. 1988, doi: 10.1109/4.90025.

[46] K. A. A. Makinwa. "Smart temperature sensor survey." Accessed: May 1, 2023. [Online]. Available: https://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[47] G. Chen et al., "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2010, pp. 288–289, doi: 10.1109/ISSCC.2010.5433921.

[48] K. Jeffrey and V. Parsonnet, "Cardiac pacing, 1960-1985: A quarter century of medical and industrial innovation," *Circulation*, vol. 97, no. 19, pp. 1978–1991, May 1998, doi: 10.1161/01.CIR.97.19.1978.

[49] K. D. Wise, J. B. Angell, and A. Starr, "An integrated-circuit approach to extracellular microelectrodes," *IEEE Trans. Biomed. Eng.*, vol. BME-17, no. 3, pp. 238–247, Jul. 1970, doi: 10.1109/TBME.1970.4502738.

[50] J. Xu, S. Mitra, C. Van Hoof, R. F. Yazicioglu, and K. A. A. Makinwa, "Active electrodes for wearable EEG acquisition: Review and electronics design methodology," *IEEE Rev. Biomed. Eng.*, vol. 10, pp. 187–198, Jan. 2017, doi: 10.1109/RBME.2017.2656388.

[51] B. B. Winter and J. G. Webster, "Driven-right-leg circuit design," *IEEE Trans. Biomed. Eng.*, vol. BME-30, no. 1, pp. 62–66, Jan. 1983, doi: 10.1109/TBME.1983.325168.

[52] C. Mora Lopez, "Unraveling the brain with high-density CMOS neural probes: Tackling the challenges of neural interfacing," *IEEE Solid-State Circuits Mag.*, vol. 11, no. 4, pp. 43–50, Fall 2019, doi: 10.1109/MSSC.2019.2939338.

[53] S. Wang et al., "A compact quad-shank CMOS neural probe with 5,120 addressable recording sites and 384 fully differential parallel channels," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1625–1634, Dec. 2019, doi: 10.1109/TBCAS.2019.2942450.

[54] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003, doi: 10.1109/JSSC.2003.811979.

[55] K. A. Ng et al., "Implantable neurotechnologies: A review of integrated circuit neural amplifiers," *Med. Biol. Eng. Comput.*, vol. 54, no. 1, pp. 45–62, 2016, doi: 10.1007/s11517-015-1431-3.

[56] "Tracking advances in neural recording," University of Connecticut, Storrs, CT, USA. 2023. Accessed: Apr. 27, 2023. [Online]. Available: https://stevenson.lab.uconn.edu/scaling/

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