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Bond Wire Damage Detection Method on Discrete MOSFETs Based on Two-Port Network Measurement

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Abstract: Bond wire damage is one of the most common failure modes of metal-oxide semiconductor field-effect transistor (MOSFET) power devices in wire-welded packaging. This paper proposes a novel bond wire damage detection approach based on two-port network measurement by identifying the MOSFET source parasitic inductance (L_S). Numerical calculation shows that the number of bond wire liftoffs will change the L_S, which can be used as an effective bond wire damage precursor. Considering a power MOSFET as a two-port network, L_S is accurately extracted from frequency domain impedance ($Z-$parameter) using a vector network analyzer under zero biasing conditions. Bond wire cutoff experiments are employed to validate the proposed approach for bond wire damage detection. The result shows that L_S increases with the rising severity of bond wire faults, and even the slight fault shows a high sensitivity, which can be effectively used to quantify the number of bond wire liftoffs of discrete MOSFETs. Meanwhile, the source parasitic resistance (R_S) extracted from the proposed two-port network measurement can be used for the bond wire damage detection of high switching frequency silicon carbide MOSFETs. This approach offers an effective quality screening technology for discrete MOSFETs without power on treatment.

Keywords: MOSFET; bond wire fault; two-port network; source parasitic inductance

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1. Introduction

Power electronic devices are widely used in mission-critical applications, such as locomotive traction, high-speed railway, electric vehicles, industrial frequency conversion, and renewable energy generation [1,2]. Literature studies indicated that the failure rate of power electronic devices among all converter failure types is 31%, accounting for the largest proportion among all failure types [3,4]. High-power metal-oxide semiconductor field-effect transistor (MOSFET) is one of the most critical and fragile elements in power electronic devices operating in harsh and uncertain conditions. MOSFETs will suffer from continuous excessive electrical–thermal–mechanical stresses and damage the bond wires and the solder layer. The reliability of MOSFETs has been attracting increasing research interest. In practical applications, the fatigue failure of power semiconductor devices in wire welding packaging is mostly manifested as the bond wires completely liftoff [1,5–8]. Therefore, the quality detection of MOSFET bond wire is of considerable importance to avoid the catastrophic failure of power electronic converters in the lifecycle.

Middle- and high-power MOSFETs are generally based on wire-welded packaging, which uses some parallel aluminum bond wires to improve the current carrying capacity for electrical interconnections between drain and source terminals. This condition introduces a problem that cannot be ignored; that is, the slight fault of bond wires will not immediately affect the performance of MOSFETs, which increases the difficulty of bond wire damage detection. Numerous research papers indicated that the commonly used bond wire reliability detection methods can be classified into two: degradation precursor- and

morphology characteristic-based methods. Degradation precursor-based methods usually predict bond wire damage by measuring different types of signals and comparing them with the healthy device. These methods can be classified into the following three classes according to the type of signals used: voltage, current, and other signal precursor-based approaches. The first class is the voltage precursor-based approach. On-state drain-source (V_{DS}) [8], collector–emitter saturated voltage ($V_{CE(sat)}$) [9], gate threshold voltage (V_{th}) [10], and turn-on gate voltage overshoot [5] are selected as bond wire fault indicators. Measuring the voltage signal is usually easy, and the sensitivity is minimal when the bond wire faults are minor. Moreover, the accuracy of the measurement is easily affected by the changes in bus voltage, current, and chip junction temperature; thus, strictly ensuring the high consistency of test conditions in each measurement is necessary. The second class is the current precursor-based approach. Gate current (I_G) [11] and short-circuit current (I_{SC}) [12,13] are usually selected as bond wire fault indicators. Reference [14] indicates that I_{SC} is sensitive to bond wire failures but requires accurate control of gate-drive voltage and junction temperature (T_j) in measurement, which adds complexity to applications. Reference [15] found that the bond wire liftoff has minimal influence on the dynamic differences of I_G. A high-precision A/D converter with a high sampling rate is needed to improve sampling precision, however using such a converter in the gate driver is too expensive. The third class is the other signal precursor-based approaches, including junction temperature (T_j) [16], thermal resistance from junction to case (R_{th}) [17], on-resistance ($R_{DS(on)}$) [18], Miller plateau duration (V_{GP}) [19], and others. $R_{DS(on)}$ and R_{th} belong to temperature-dependent parameters, and the measurement accuracy is affected by the junction temperature, T_j. Unfortunately, T_j cannot be measured directly, and the stable control of T_j is also a technical problem. Miller plateau duration has minimal sensitivity when one or two bond wires liftoff. Morphology characteristic-based methods mainly include thermal imaging [20–23] (eddy current pulse thermal imaging, infrared imaging) and structural imaging [24–26] (X-ray imaging, ultra-sound imaging, and industrial computerized tomography). Thermal imaging can identify the location of potential damage by observing the surface temperature distribution of the power devices, which is mainly used to detect solder-layer defects. Structural imaging is a non-destructive testing technology and can directly detect inner defects of devices by identifying the phase and amplitude of the reflected signals. However, the key to obtaining the ideal imaging quality lies in the accurate height estimation of the bond wire in the Z-axis direction in advance by the users, which is a remarkably difficult and time-consuming task. If delamination exists between the epoxy molding compound (EMC) layer and the upper surface of the die, then penetrating the EMC for effective bond wire imaging is difficult for the pulse ray, resulting in a limited application.

A novel bond wire damage detection approach based on two-port network measurement by identifying the MOSFET source parasitic inductance (L_S) is proposed in this study. Based on frequency domain impedance analysis, MOSFET is equivalent to some second-order *RLC* circuits comprising independent inductances, capacitances, and resistances in series, whereas the high-frequency impedance of MOSFET is dominated by the inductive components. Therefore, the bond wire is equivalent to the pure inductance model at a frequency much higher than the self-resonant frequency (f_{SRF}). The liftoff of the bond wire will increase the total parasitic inductance of the parallel bond wires, resulting in increasing high-frequency impedance. This notion provides a new idea that the physical failure of the bond wire can be mapped to the change in high-frequency impedance. Considering a power MOSFET as a two-port network, L_S is accurately extracted from vector network analyzer (VNA) measurement under zero basing conditions. The positive correlation between the L_S and the number of bond wire faults is then determined. The experimental results reveal that even a slight bond wire fault can be detected with high resolution. This method offers an effective bond wire damage detection technology for power-discrete devices without power on treatment.

2. Methodologies

2.1. MOSFET Small-Signal Equivalent Circuit

The schematic of a cross-section of a half-vertical-diffused MOSFET with a package structure is illustrated in Figure 1a. An ideal MOSFET chip can be equivalent to the constant and variable active devices, which comprise the voltage-controlled current source, internal parasitic capacitances, and anti-parallel body diode. The internal parasitic capacitances include drain–source capacitance (C_{DS}), gate–source capacitance (C_{GS}), and gate–drain capacitance (C_{GD}). The chip and external terminals are electrically interconnected through the aluminum bond wire packaging technology. Additional parasitic parameters are inevitably introduced: (1) $L_{S\text{-ter}}$ and $L_{G\text{-ter}}$, $L_{D\text{-ter}}$ and $R_{S\text{-ter}}$, and $R_{G\text{-ter}}$ and $R_{D\text{-ter}}$ are generated from the gate, source, and drain terminals, respectively. (2) $L_{S\text{-BW}}$, $L_{G\text{-BW}}$, and $R_{S\text{-BW}}$, $R_{G\text{-BW}}$ are generated from bond wires. (3) $R_{D\text{-solder}}$ and $R_{D\text{-base}}$ are generated from the solder and baseplate layers, respectively. The small-signal equivalent circuit model is simplified. The parasitic inductances are combined into L_G, L_S, and L_D and the parasitic resistors into R_S, R_G, and R_D to facilitate the analysis, as shown in Figure 1b. Figure 2 depicts a typical power MOSFET in a TO−247 discrete package, which is encapsulated by a chip, copper substrate, bond wires, lead terminals, solder layer, and an EMC. The equivalent circuit of the MOSFET power device is decomposed in sequence according to the drain-to-source current loop.

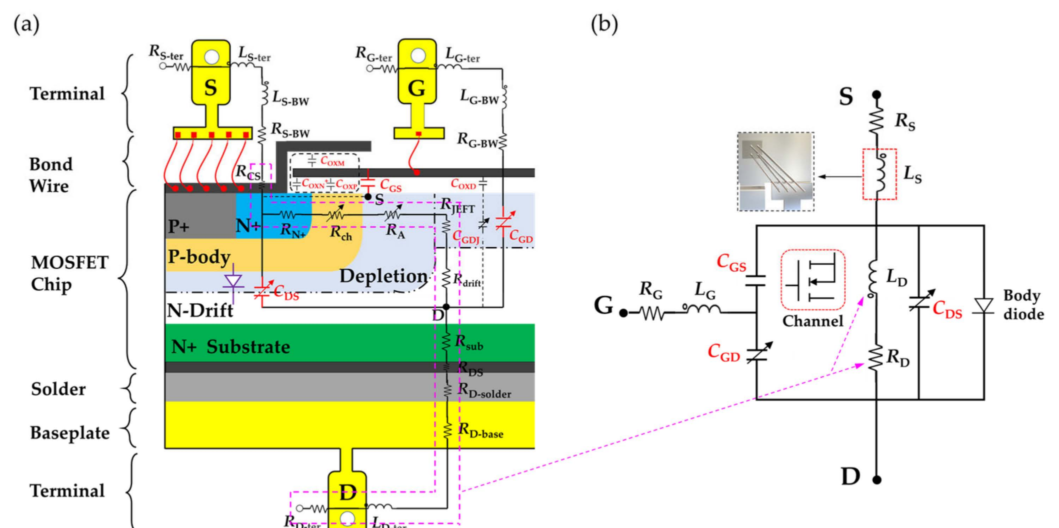

Figure 1. (**a**) Cross-section of a power MOSFET, and (**b**) small-signal equivalent circuit.

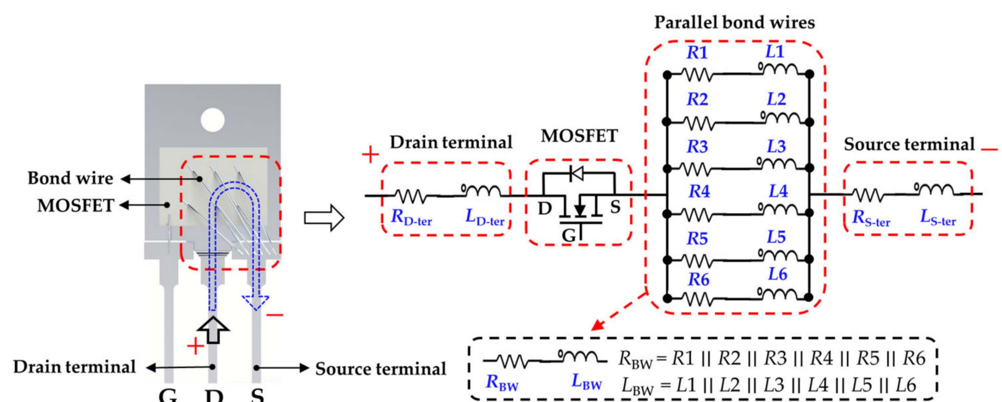

Figure 2. Simplified *RL* equivalent of a MOSFET in TO−247 package.

2.2. Bond Wire Parasitic Inductance

MOSFETs in wire-welding packaging comprise multilayered materials with different coefficients of thermal expansion (CTE). Long-term thermal stress causes the expansion of different materials at various rates, specifically in the weak points of the wire bond root, resulting in bond wire fatigue and degradation. Figure 3 shows a 3D structural diagram of the four parallel bond wires, wherein each bond wire can be equivalent to a set of *RL* series circuits. The partial inductance, L_{Bond}, of a bond wire comprises partial self and mutual inductances. According to [27], the self-inductance, *L* (in nH), of a single bond wire can be extracted by the simplified Equation (1), and the parasitic mutual-inductance, *M* (in nH), of a single bond wire can be determined by the simplified Equation (2).

$$L = 5l \times \left[(\text{In}(4l/d) - 0.75) \right], \tag{1}$$

$$M = 5 \times \left[\text{In}\left(\frac{2l}{s}\right) - 1 + \frac{s}{l} - \left(\frac{s}{2l}\right)^2 \right], \tag{2}$$

where *l* stands for the length of the bond wire (in inches), *d* stands for the diameter of the bond wire (in inches), and *s* stands for the distance between two bond wire centers (in inches). The mutual inductance for multiple bond wires is caused by the magnetic coupling of multiple bond wires. The internal structure and bond wire dimension of IXFK32N100P (IXYS Corporation, Milpitas, CA, USA and Leiden, The Netherlands) and C2M0160120D (Wolfspeed Corporation, Durham, NC, USA) are shown in Figure 4 and Table 1. Each bond wire is marked with a serial number for easy identification.

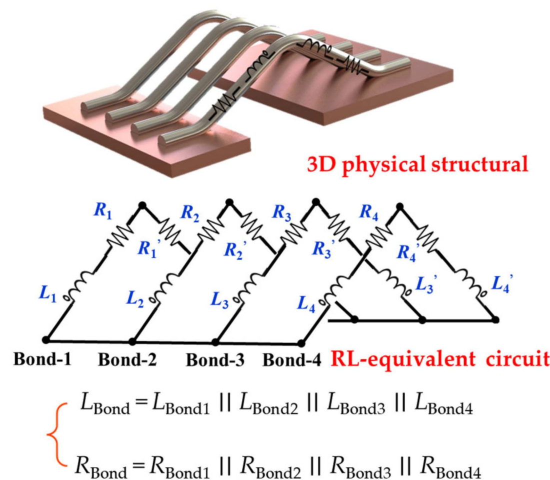

Figure 3. 3D structural diagram and *RL*-equivalent circuit of parallel bond wires.

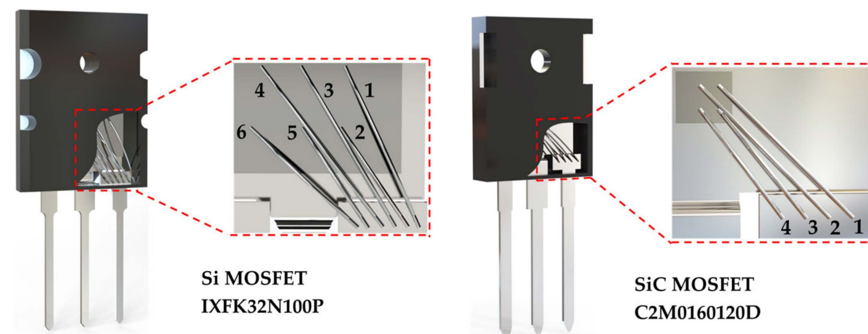

Figure 4. Internal structure of IXFK32N100P and C2M0160120D in TO−247, and the serial number marked on each bond wire.

Table 1. Bond wire dimension for MOSFETs.

Bond Wire No.		**1**	**2**	**3**	**4**	**5**	**6**
IXFK32N100P	l (mm)	13.54	8.76	14.16	15.50	8.94	11.35
	d (mm)	0.279					
C2M0160120D	l (mm)	5.78	5.90	7.85	8.00		
	d (mm)	0.178					

For IXFK32N100P, the parasitic inductance of bond wire No. 1, $L_{\text{Bond_1}}$, lies in the addition of bond wire self-inductance L_1 and mutual inductances M_{12}, M_{13}, M_{14}, M_{15}, and M_{16}. Similarly, the parasitic inductance of bond wire No. 2, $L_{\text{Bond_2}}$, lies in the addition of bond wire self-inductance L_2 and mutual inductances M_{21}, M_{23}, M_{24}, M_{25}, and M_{26}. The parasitic inductance of other bond wires is calculated by the same method. Therefore, the bond wire parasitic inductance, $L_{\text{Bond_}m}$, of No. m is the sum of bond wire self-inductance L_m of No. m (calculated by Equation (1)) and bond wire mutual inductances M_{mn} between No. m and No. n (calculated by Equation (2)), which can be described as follows:

$$L_{\text{Bond_}m} = L_m + \sum_{n=1}^{n} M_{mn} \; (m \neq n) \tag{3}$$

Figure 4 shows that the multiple bond wires of discrete MOSFETs are not strictly parallel to each other. To simplify the calculation, the non-parallel distribution of the parallel connection bond wires between the source and source terminal is ignored, and the average spacing between the two bond wires and the length of the short bond wire is selected for mutual inductance estimation. The parasitic inductance, L_{Bond}, is calculated and shown in Table 2. The total parasitic inductances of IXFK32N100P, $L_{\text{Bond_IX}}$, and C2M0160120D, $L_{\text{Bond_C2}}$, are correspondingly 4.33 and 3.75 nH, which are the results of parallel connections of six and four inductances, respectively.

Table 2. Parasitic inductance for IXFK32N100P and C2M0160120D discrete MOSFETs.

Bond Wire No.		**1**	**2**	**3**	**4**	**5**	**6**	$L_{\text{Bond_No}}$. **nH**
Si MOSFET IXFK32N100P	1	12.04	3.4	4.66	3.76	2.16	2.08	28.1
	2	3.40	7.04	3.66	3.40	2.39	1.86	21.75
	3	4.66	3.66	12.72	4.98	3.51	2.58	32.11
	4	3.76	3.4	4.98	14.19	3.76	3.57	33.66
	5	2.16	2.39	3.51	3.76	7.22	3.22	22.26
	6	2.08	1.86	2.58	3.57	3.22	9.7	23.01
				$L_{\text{Bond_IX}}$				4.33
SiC MOSFET C2M0160120D	1	5.63	3.11	3.11	1.85			13.70
	2	3.11	5.83	3.24	2.40			14.59
	3	3.11	3.24	6.78	3.84			16.99
	4	1.85	2.40	3.84	7.00			15.08
				$L_{\text{Bond_C2}}$				3.75

2.3. Two-Port Parasitic Inductance Extraction Approach

The two-port scattering (S) parameter measurement with VNA is used in this study to extract the parasitic parameters of MOSFET [28,29]. The MOSFET small-signal equivalent circuit under zero biasing conditions, which is a two-port network with S–G and D–G as Ports 1 and 2, respectively, is shown in Figure 5. Each of the two-port network Z−parameters, Z_{11}, Z_{12}, Z_{21}, and Z_{22}, can be equivalent to some second-order RLC circuits comprising independent inductances, capacitances, and resistances in series. Z_{11} is equivalent to the L_S–R_S–C_S–C_G–R_G–L_G series circuit, Z_{12} and Z_{21} are equivalent to the same G_G–R_G–L_G series circuit, and Z_{22} is equivalent to the L_G–R_G–C_G–C_D–R_D–L_D series circuit. Notably, as a standard form of the two-port network, the equivalent capacitances

(C_G, C_D, and C_S) demonstrate a star connection in Figure 5, which is different from the delta connection of parasitic capacitances (C_{GS}, C_{DS}, and C_{GD}) in Figure 1b. Therefore, the star connection should be converted into a delta connection by using Equations (4)–(6) to extract the parasitic capacitances.

$$C_{GS} = C_G C_S / (C_G + C_D + C_S), \quad (4)$$

$$C_{GD} = C_G C_D / (C_G + C_D + C_S), \quad (5)$$

$$C_{DS} = C_D C_S / (C_G + C_D + C_S). \quad (6)$$

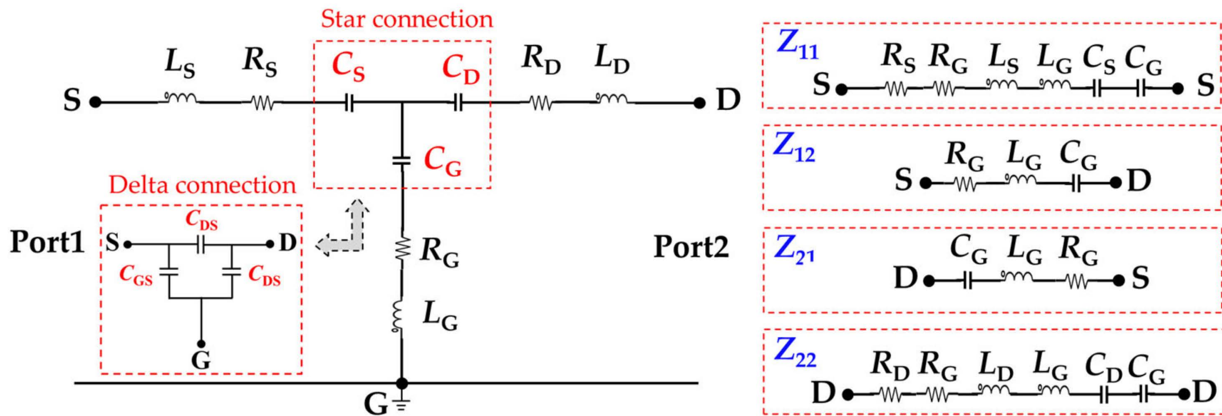

Figure 5. Two-port network of a MOSFET small-signal circuit model under zero biasing condition.

Figure 6 shows a typical impedance plot of a MOSFET small-signal equivalent circuit with predetermined parameters. A set of typical values for the parasitic inductances (L_G = 15 nH, L_D = 20 nH, and L_S = 30 nH), parasitic capacitances (C_S = 5 nF, C_D = 10 nF, and C_G = 15 nF), and resistances (R_G = 1.5 Ω, R_D = 0.5 Ω, and R_S = 0.5 Ω) is presented in the Advanced Design System (ADS) simulation setup with a frequency sweep from 1 to 300 MHz. The ADS simulated magnitude and phase angle of impedance (Z) parameters are shown in Figure 6a. Z_{11}, Z_{12}, Z_{21}, and Z_{22} of the series RLC circuit can be calculated using Equations (7)–(9). The effect of capacitive reactance and resistance can be neglected at high frequency, f_{High} (endpoint of the frequency range). Therefore, the two-port network representation of the MOSFET equivalent circuit can be simplified as shown in Figure 6d. The high-frequency impedance is dominated by the inductive reactance, and the parasitic inductances L_S, L_G, and L_D can be calculated through Equations (10)–(12). At the f_{SRF}, inductive and capacitive reactance cancel each other, and the impedance magnitude has its minimum value. The two-port network representation of the MOSFET equivalent circuit can be simplified as shown in Figure 6c. The parasitic resistances R_S, R_G, and R_D can be determined at the f_{SRF} through Equations (13)–(15). Meanwhile, the effect of inductive reactance and resistance can be neglected at low frequency, f_{Low} (starting point of the frequency range). Therefore, the two-port network representation of the MOSFET equivalent circuit can be simplified as shown in Figure 6b. The equivalent capacitances C_G, C_S, and C_D are respectively determined by plugging the extracted L_S, L_G, and L_D into Equations (16)–(18). Finally, the capacitor star connection is converted to a delta connection through Equations (4)–(6) to extract parasitic capacitances C_{GS}, C_{GD}, and C_{DS}.

$$Z_{11} = X_{L_S} + X_{L_G} + X_{R_S} + X_{R_G} + X_{C_S} + X_{C_G}, \quad (7)$$

$$Z_{12} = Z_{21} = X_{L_G} + X_{R_G} + X_{C_G}, \quad (8)$$

$$Z_{22} = X_{L_D} + X_{L_G} + X_{R_D} + X_{R_G} + X_{C_D} + X_{C_G}, \quad (9)$$

$$L_S + L_G = imag\,(Z_{11_High}) / w_{11_High}, \quad (10)$$

$$L_G = imag\,(Z_{12_High})\,/\,w_{12_High}\,, \tag{11}$$

$$L_D + L_G = imag\,(Z_{22_High})\,/\,w_{22_High}\,, \tag{12}$$

$$R_S + R_G = Z_{11_min}\,, \tag{13}$$

$$R_G = Z_{12_min}\,, \tag{14}$$

$$R_D + R_G = Z_{22_min}\,, \tag{15}$$

$$\frac{C_S C_G}{C_S + C_G} = 1\,/\,[w_{11_SRF}^2 \cdot (L_S + L_G)]\,, \tag{16}$$

$$C_G = 1\,/\,(w_{12_SRF}^2 \cdot L_G)\,, \tag{17}$$

$$\frac{C_D C_G}{C_D + C_G} = 1\,/\,[w_{22_SRF}^2 \cdot (L_D + L_G)]\,. \tag{18}$$

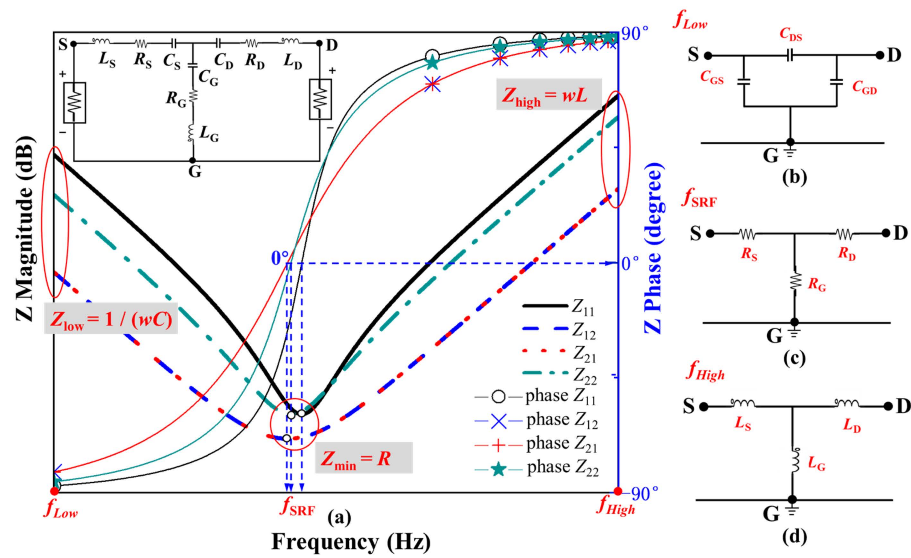

Figure 6. MOSFET parasitic parameter extraction theory. (**a**) Impedance magnitude and phase curves of a typical MOSFET. (**b**) Two-port network representation for the MOSFET at low frequency. (**c**) Two-port network representation for the MOSFET at the f_{SRF}. (**d**) Two-port network representation for the MOSFET at high frequency.

3. Experimental Results and Discussion

3.1. Validation Parasitic Inductance Extraction Approach for MOSFET

A 1000 V Si MOSFET (IXFK32N100P in TO−247 package) and a 1200 V SiC MOSFET (C2M0160120D in TO−247 package) were used in this paper to verify the two-port network measurement technique. Figure 7 shows the schematic of the two-port network model and the VNA measurement system. An additional test fixture [30], which reserves three connection positions and ensures the low-inductance connections between VNA and terminals, must be designed to ensure the effective connection between MOSFET and VNA. The test fixture shall have a negligible loss, good impedance match (50 Ω), and high isolation between input and output. The printed circuit board (PCB) test fixture comprises two 50 Ω SMA adaptors, two 50 Ω microstrip lines, and a through-hole, as shown in Figure 7a. The top copper layer of the PCB is graphically processed into two 50 Ω microstrip lines. The bottom copper layer of the PCB is reserved for interconnection with the VNA ground. The MOSFET was installed on the PCB test fixture and connected with VNA through SMA. The MOSFET source terminal is interconnected with VNA port 1, the MOSFET drain terminal is interconnected with VNA port 2, and the gate terminal is interconnected with the VNA ground through a PCB through-hole. De-embedding calibration [31] was performed to remove the systematic errors caused by test cables, adapters, and fixtures before VNA

measurement. The 80502D calibration kit (Keysight, Santa Rosa, CA, USA) provided by Keysight was used in this study to perform the short-open-load VNA calibration. A new "through" calibration element based on a PCB test fixture was designed to replace the "through" calibration element in the 80502D kit to extend the measurement plane from SAM coaxial connected to the interface of the device plane.

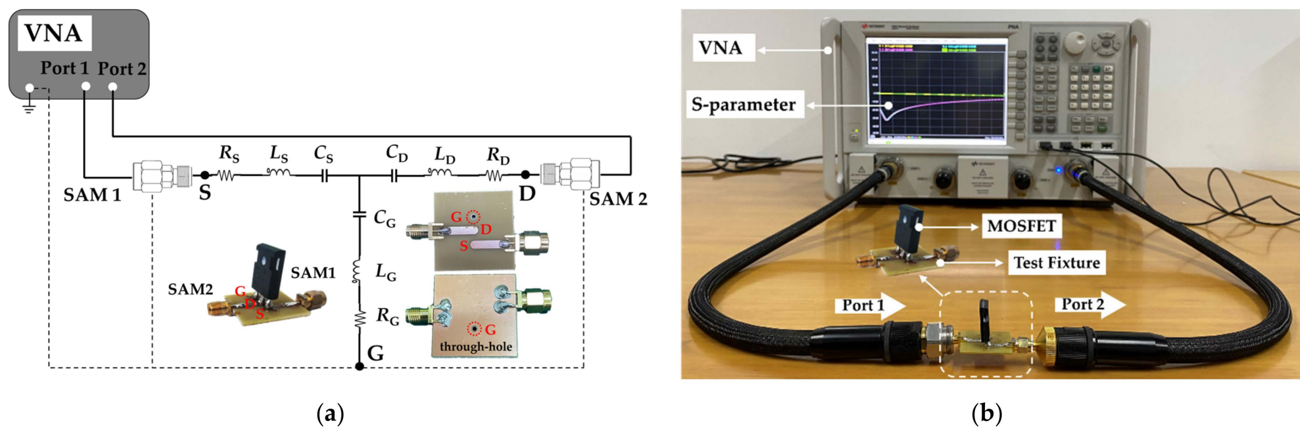

Figure 7. Two-port VNA measurement setup for MOSFET parasitic inductance extraction. (**a**) Schematic of proposed two-port network extraction approach. (**b**) VNA measurement setup including the PCB fixture.

ADS circuit simulation was used to validate the proposed two-port parasitic inductance extraction methodology. First, the S−parameter of the MOSFET was obtained from VNA measurement and converted into Z−parameters. Then, the parasitic inductances, capacitances, and resistances were accurately calculated from Z−parameters through Equations (10)–(18). Finally, the extracted parasitic parameters were plugged back into the small-signal equivalent circuit of the power MOSFET for ADS simulation over a frequency range of 100 kHz to 400 MHz (the frequency range is not strictly fixed and can be adjusted according to different MOSFETs). Figure 8 shows the frequency response curves of the Z−parameters obtained from ADS simulation and VNA experimental measurement. The ADS simulation curve (red dashed line) was found to be in good agreement with the experimental value (black solid line) in Si and SiC MOSFETs, which indicates that the derived parasitic parameter extraction mathematical formulas (Equations (10)–(18)) and extraction methodology mentioned in Section 2.3 are effective and correct. A through-hole must be set on the PCB test fixture to connect the MOSFET gate terminal to the VNA ground. Unfortunately, through-hole will cause unwanted signal reflection on the transmission path, resulting in a slight impedance mismatch between the simulation and measurement of Z_{12} and Z_{21} at frequencies above the f_{SRF}. L_S is calculated by subtracting Equation (10) from Equation (11). Thus, the gate parasitic inductance, L_G, and the impedance mismatch introduced by through-hole can be excluded from the calculation. In addition, the secondary validation approach was realized by comparing the parasitic capacitances extracted from the proposed approach with the device datasheet values. The parasitic capacitances of the SiC MOSFET (C2M0160120D) obtained from the proposed two-port extraction technique were 0.49, 0.27, and 0.55 nF. Considering the unavoidable measurement error, the extracted capacitances were consistent with the datasheet values reported in [29] (C_{GS} = 0.47 nF, C_{GD} = 0.28 nF, and C_{DS} = 0.51 nF, f = 1 MHz), and the mismatch was 4.25%, 3.57%, and 7.84%. The experimental results show that the proposed two-port extraction methodology is suitable for accurately extracting the parasitic inductance of discrete-power MOSFETs.

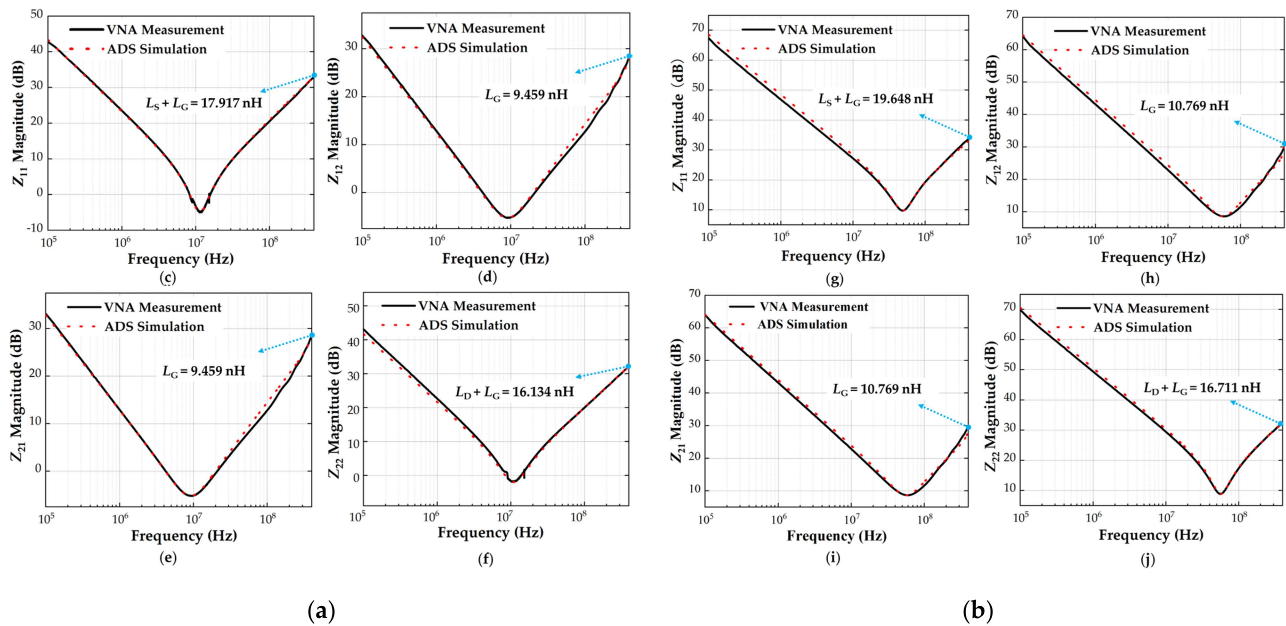

Figure 8. Z−parameters obtained from experimental measurement and ADS simulation. (**a**) Si MOSFET IXFK32N100P in TO−247 package ((**c**) Z_{11}, (**d**) Z_{12}, (**e**) Z_{21}, (**f**) Z_{22}). (**b**) SiC MOSFET C2M0160120D in TO−247 package ((**g**) Z_{11}, (**h**) Z_{12}, (**i**) Z_{21}, (**j**) Z_{22}).

3.2. Analysis of Parasitic Inductance with Bond Wire Fault

This paper aims to provide a precursor for bond wires' degradation. The current study used the approach of cutting off bond wires to simulate their faults to shorten the duration of experimental tests. Laser equipment was used to remove the epoxy layer of the power device to expose the bond wires completely. The bond wire damage models were then established by manually cutting off the bond wires individually. The damage models of IXFK32N100P and C2M0160120D are shown in Figure 9.

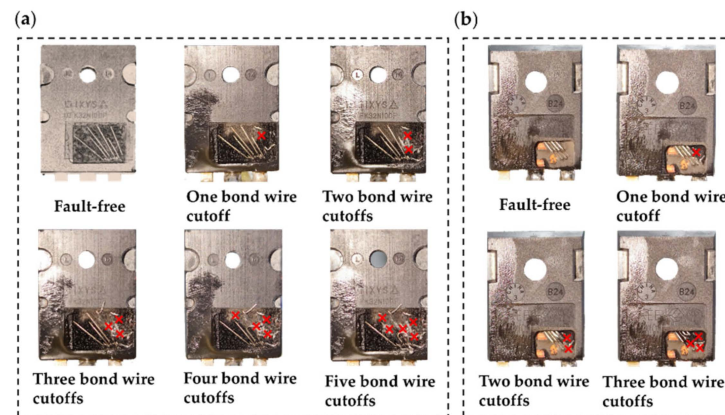

Figure 9. Bond wire damage models. (**a**) TO−247 Si MOSFET (its source has six aluminum bond wires connected in parallel). (**b**) TO−247 SiC MOSFET (its source has four aluminum bond wires connected in parallel).

When one bond wire is cut off (for instance, No. 1), the bond wire self-inductance L_1 and mutual inductances M_{1n} and M_{m1} (M_{12}, M_{13}, M_{14}, M_{15}, and M_{16}, and M_{21}, M_{31}, M_{41}, M_{51}, and M_{61}, are generated by the magnetic coupling between bond wire No. 1 and other bond wires Nos. 2–6, respectively) no longer exist. The parasitic inductances of other valid bond wires (Nos. 2–6) are calculated by Equations (1)–(3), described in Section 2.2, and summarized in Table 3. The total parasitic inductance of IXFK32N100P is

4.51 nH, which is attributed to the result of the parallel connection of the five remaining bond wires. The total parasitic inductance of C2M0160120D is 4.26 nH, which is the result of the parallel connection of the three remaining bond wires. Similarly, for other bond wire damage models, such as cutting off two bond wires (Nos. 1 and 2), cutting off three bond wires (Nos. 1, 2, and 3), cutting off four bond wires (Nos. 1, 2, 3, and 4), and cutting off five bond wires (Nos. 1, 2, 3, 4, and 5), the parasitic inductances are calculated from Equations (1)–(3), and listed in Appendix A, Tables A1–A4. The corresponding relationship between parasitic inductance, L_{Bond}, and the number of cutoff bond wires is shown in Figure 10. For ease of description, the liftoff of one or two bond wires is defined as "slight fault" and that of three or more bond wires is "serious fault." Each of the total bond wire parasitic inductances of IXFK32N100P and C2M0160120D are positively correlated with the number of the bond wire cutoff. For slight fault, the percentage changes of L_{Bond_IX} in IXFK32N100P were 4.16% and 22.40%, while those of L_{Bond_C2} in C2M0160120D were 13.60% and 43.20%, showing high sensitivity. These results indicate that the proposed bond wire damage detection approach is reasonable. Figure 10 indicates that the parasitic inductance, L_{Bond}, rises with the increase in the number of bond wire cutoffs, which can be potentially used as a precursor of bond wire damage. However, the parasitic inductance generated by the source terminal is not considered in the numerical analysis. The source parasitic inductance extracted from the two-port network measurement includes the bond wire parasitic inductance and the source terminal parasitic inductance. The sensitivity of MOSFET source parasitic inductance with various bond wire cutoffs is discussed in the following.

Table 3. Parasitic inductance, L_{Bond}, with one bond wire cutoff.

Bond Wire No.		**1**	**2**	**3**	**4**	**5**	**6**	**L_{Bond_No}, nH**
Si MOSFET IXFK32N100P	1				/			
	2		7.04	3.66	3.4	2.39	1.86	18.35
	3		3.66	12.72	4.98	3.51	2.58	27.45
	4	/	3.4	4.98	14.19	3.76	3.57	29.9
	5		2.39	3.51	3.76	7.22	3.22	20.1
	6		1.86	2.58	3.57	3.22	9.7	20.93
				L_{Bond_IX}				4.51
SiC MOSFET C2M0160120D	1				/			
	2		5.83	3.24	2.40			11.47
	3	/	3.24	6.78	3.84			13.87
	4		2.40	3.84	7.00			13.24
				L_{Bond_C2}				4.26

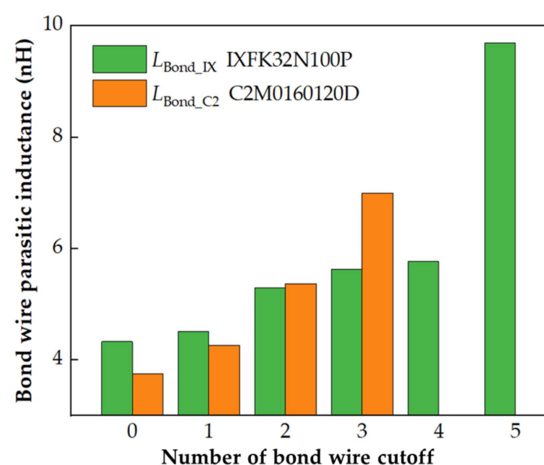

Figure 10. Parasitic inductance with different cutoff numbers of bond wires.

3.3. Bond Wire Experimental Results

The S−parameters of the bond wire damage models were measured with the VNA over a frequency range of 100 kHz to 400 MHz and then converted to Z−parameters. Figure 11 shows the Z−parameter frequency response curves of IXFK32N100P Si MOSFET with various bond wire faults. At frequencies above the f_{SRF}, Z_{11} ($Z_{11_High} = L_S + L_G$) increased with the number of bond wire cutoffs, whereas Z_{12} ($Z_{12_High} = L_G$), Z_{21} ($Z_{21_High} = L_G$), and Z_{22} ($Z_{22_High} = L_G + L_D$) changed by less than 1 Ω when five bond wires were cutoff. This finding indicates a strong positive correlation between the damage of bond wires and the increase in source parasitic inductance, which is consistent with the presented theoretical expectation. The ratios expressed as percentage changes were calculated to define the degree of bond wire degradation. Percentage changes in Z_{11} and L_S are the different ratios of the measured value with the actual device compared with the initial value of the fault-free device under testing. For IXFK32N100P, the percentage changes in Z_{11} parameters of each bond wire damage model were 0.51%, 3.52%, 6.46%, 8.46%, and 28.95% at 400 MHz. For C2M0160120D, the Z−parameter frequency response curves are shown in Figure 12. This finding has a similar change trend as in Figure 11 with the increase in the number of bond wire cutoffs. The percentage changes of Z_{11} at 400 MHz were 2.46%, 5.60%, and 14.72%.

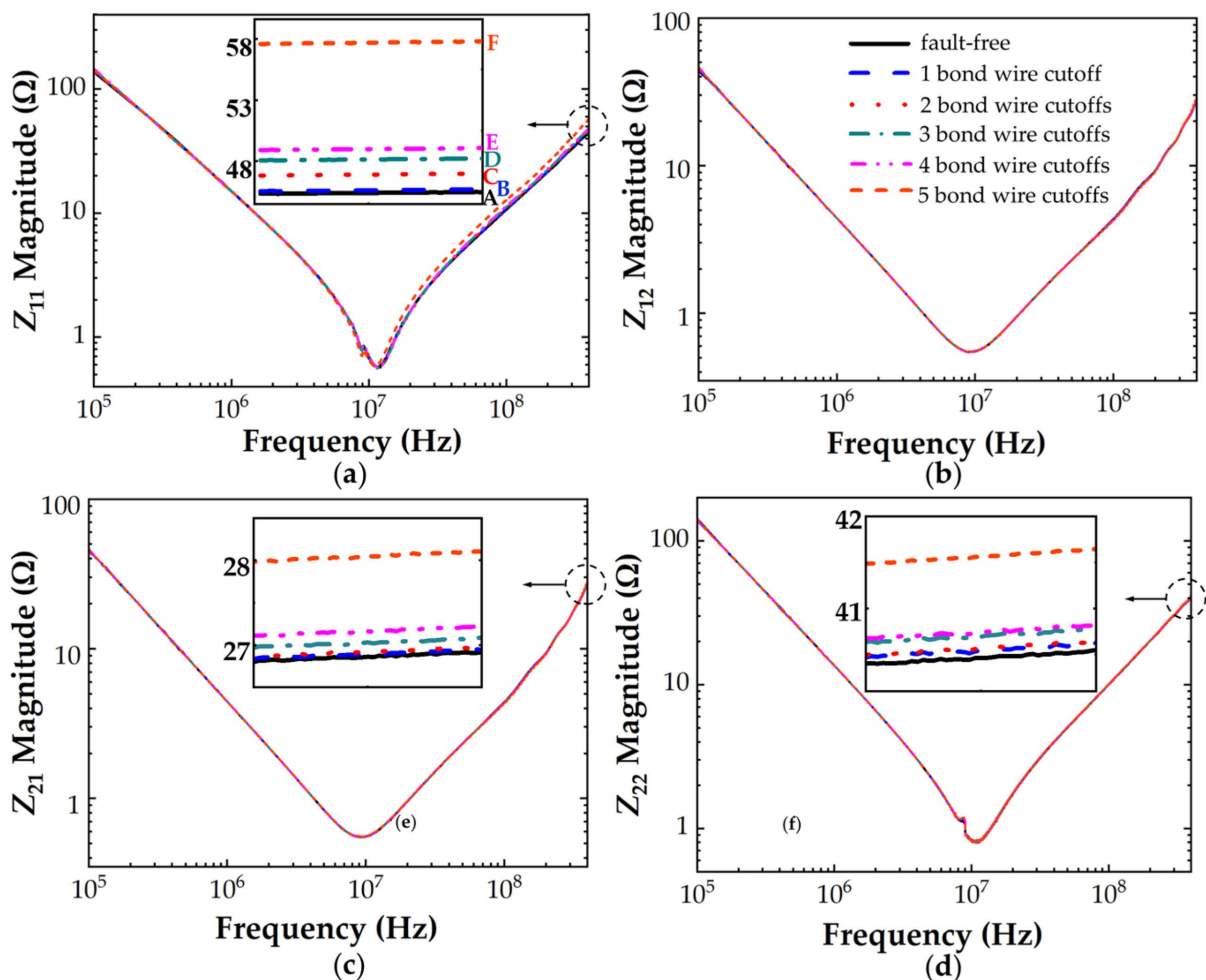

Figure 11. Z−parameters of IXFK32N100P with different cutoff numbers of bond wires (A = 45.03 Ω, B = 45.30 Ω, C = 46.62 Ω, D = 47.94 Ω, E = 48.84 Ω, F = 58.07 Ω). (**a**) Z_{11}, (**b**) Z_{12}, (**c**) Z_{21}, (**d**) Z_{22}.

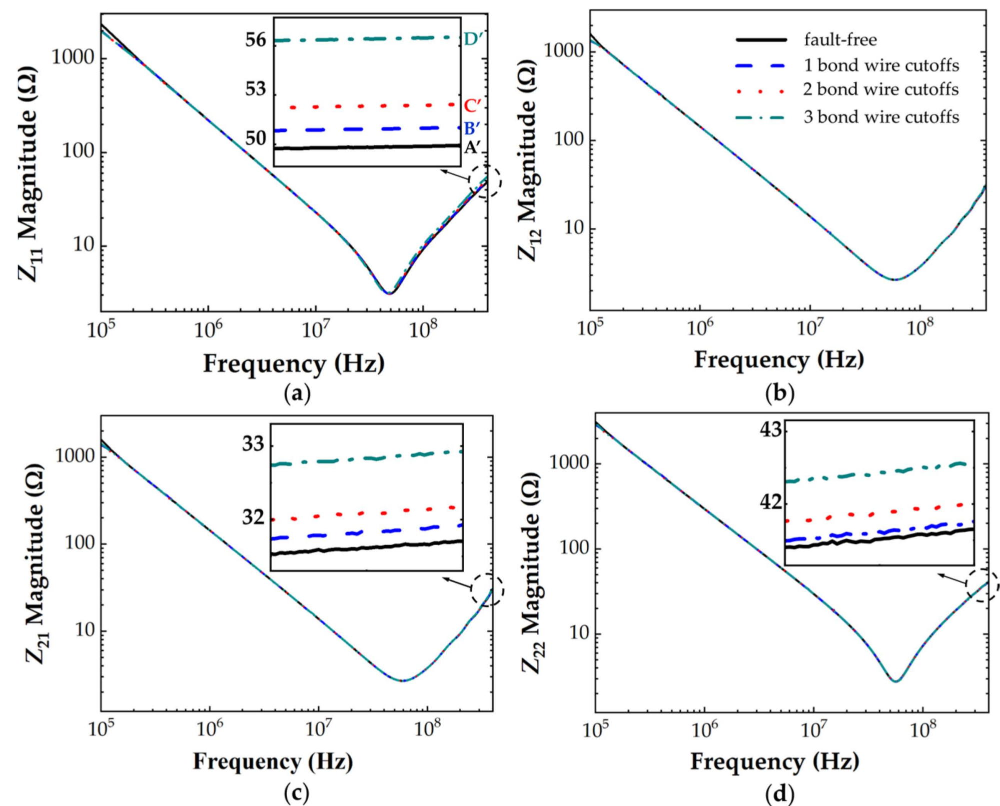

Figure 12. $Z-$parameters of C2M0160120D with different cutoff numbers of bond wires (A′ = 49.38 Ω, B′ = 50.60 Ω, C′ = 52.15 Ω, D′ = 56.66 Ω). (**a**) Z_{11}, (**b**) Z_{12}, (**c**) Z_{21}, (**d**) Z_{22}.

Figures 13 and 14 show that the source parasitic inductance increased with the increment of the number of the bond wire cutoffs, which is consistent with the change in L_{Bond} obtained by numerical calculation (Appendix A, Tables A1–A4). The parasitic inductance and resistance with various bond wire cutoffs are shown in Table 4. MOSFET is equivalent to the inductive element when the frequency is larger than the f_{SRF}. With the increase in frequency, the skin effect forces the increase in parasitic resistance of the conductors (such as bond wire and terminal) and the reduction in parasitic inductance. For IXFK32N100P, the percentage change in the source parasitic inductance L_{S_IX} significantly increased with the increment of the number of bond wire cutoffs, and the difference reached the maximum at 400 MHz. With bond wire cutoffs varying from 1 to 5, the L_{S_IX} at 400 MHz increased from 8.52 to 8.61, 9.20, 9.71, 10.03, and 13.46 nH, and the percentage changes were 1.12%, 7.96%, 13.98%, 17.75%, and 58.02%, respectively. However, the extracted source parasitic resistance R_{S_IX} did not show the expected regular increase with the rising severity of bond wire faults. This phenomenon is due to the excessively low f_{SRF} of IXFK32N100P (≈9 MHz) to identify the R_{S_IX} (<0.015 Ω) effectively. Similarly, for C2M0160120D, the percentage change of source parasitic inductance L_{S_C2} has the maximum difference at 400 MHz. With bond wire cutoffs varying from 1 to 3, the L_{S_C2} at 400 MHz increased from 8.88 to 9.30, 9.85, and 11.43 nH, and the percentage changes were 4.71%, 10.97%, and 28.79%, respectively. SiC MOSFET has a higher switching frequency than traditional Si-based power semiconductor devices. The f_{SRF} of C2M0160120D is close to 58 MHz. Thus, the skin effect induced the increment of source parasitic resistance R_{S_C2} to more than 0.400 Ω, which reduced the identification accuracy requirements of R_{S_C2} by an order of magnitude, facilitating its accurate identification. The measurement results of the percentage change of R_{S_C2} with various bond wire cutoffs were 1.35%, 4.24%, and 17.21%, indicating that R_{S_C2} can be used as another precursor for bond wire fault detection. However, Table 4 shows that the resolution of R_{S_C2} was lower than that of L_{S_C2} in a two-port VNA measurement. If the f_{SRF} of MOSFET is low, then the influence of the skin effect on the conductor is not observed.

Thus, the source parasitic resistance is too small to be accurately identified. Therefore, the source parasitic resistance can only be used to identify the bond wire damage of high switching frequency MOSFETs, especially in emerging wide-bandgap SiC MOSFETs.

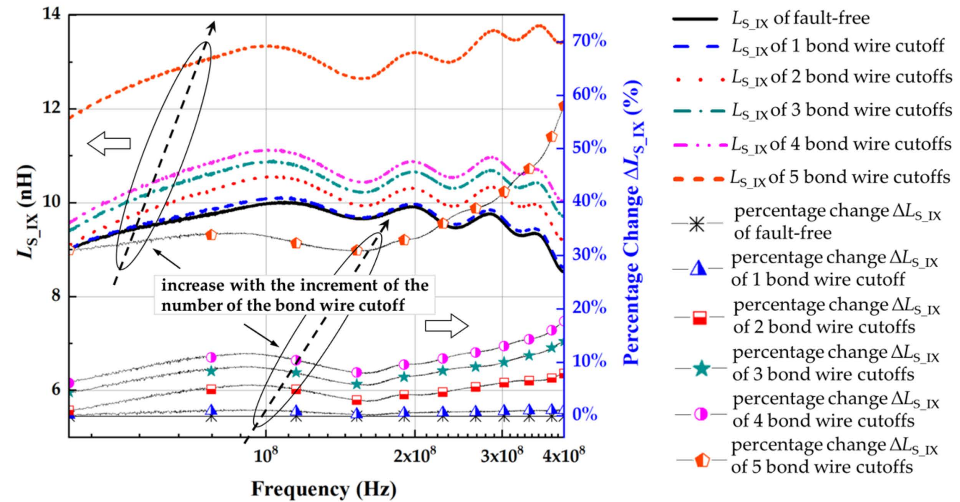

Figure 13. L_{S_IX} of IXFK-32N100P with different cutoff numbers of bond wires.

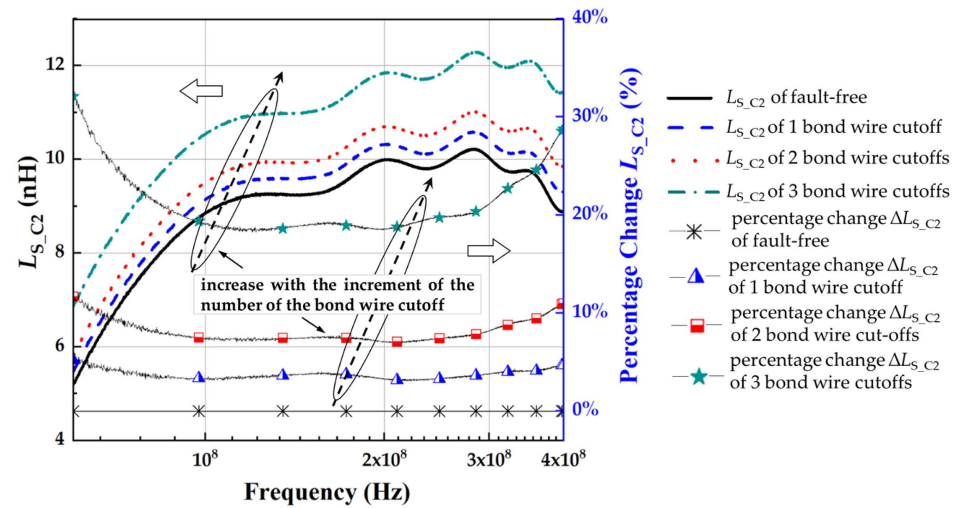

Figure 14. L_{S_C2} of C2M0160120D with different cutoff numbers of bond wires.

Table 4. Parasitic inductance and resistance with different cutoff numbers of bond wires.

Bond Wire Cutoff Model	**Si MOSFET**				**SiC MOSFET**			
	400 MHz		f_{SRF}		**400 MHz**		f_{SRF}	
	L_S **nH**	**Percentage Change %**	R_S **Ω**	**Percentage Change %**	L_S **nH**	**Percentage Change %**	R_S **Ω**	**Percentage Change %**
0	8.52	0	0.012	0	8.88	0	0.401	0
1	8.62	1.12	0.014	16.67%	9.30	4.71	0.406	1.25%
2	9.20	7.96	0.013	8.33%	9.85	10.97	0.418	4.24%
3	9.71	13.98	0.014	−8.33%	11.43	28.79	0.470	17.21%
4	10.03	17.75	0.006	−50.00%				
5	13.46	58.02	0.029	141.67%				

The bond wire parasitic inductances obtained by numerical calculation and the source parasitic inductance extracted from VNA measurement are compared in Figure 15. The parasitic inductances obtained by the two approaches have a similar trend with the increase of the number of bond wire cutoffs. For the two MOSFETs, the difference in parasitic inductance between numerical calculation and VNA measurement was maintained at ΔL_{C2} = 4.1 ± 0.3 nH and ΔL_{IX} = 4.7 ± 0.3 nH, respectively. This difference can be attributed to the following two reasons: (1) VNA-measured Z−parameters include source terminal parasitic inductance, which is the main reason for the difference, as shown in Figure 15. (2) The spacing between two bond wires is taken as the average value to simplify the mutual inductance numerical calculation. Therefore, the VNA measurement extracted values are consistent with the numerically calculated values considering the fixed difference (ΔL_{C2} and ΔL_{IX}). The comparison results further verify the effectiveness of the proposed method of extracting the parasitic inductance from VNA measurement by considering a power MOSFET as a two-port network.

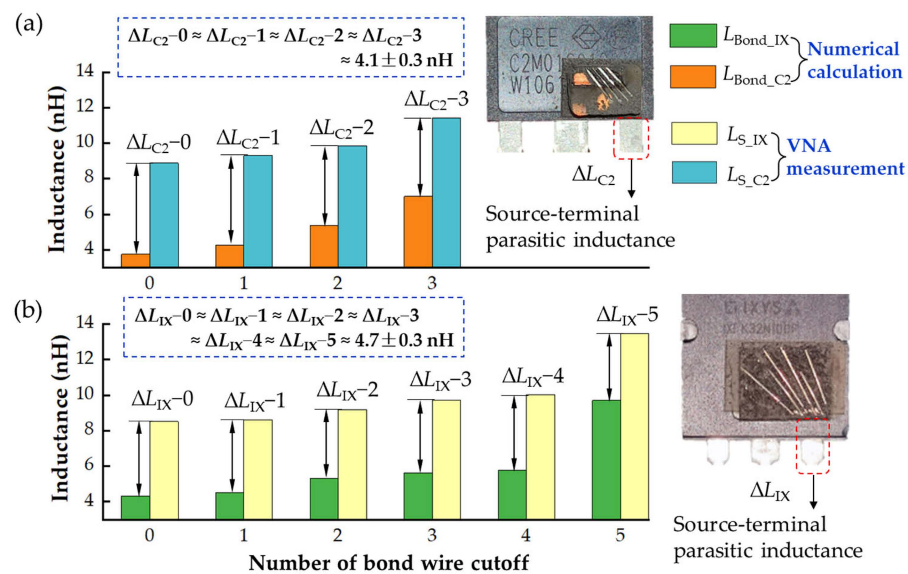

Figure 15. Numerical calculation and VNA measurement of parasitic inductance with different cutoff numbers of bond wires. (**a**) Comparison results of C2M0160120D. (**b**) Comparison results of IXFK32N100P.

The change in source parasitic inductance can be accurately distinguished regardless of a "slight fault" or "serious fault." Thus, the proposed bond wire damage detection approach in this paper has high discrimination. In addition, the parasitic parameters were extracted under zero DC biasing voltage (off-state) based on the two-port network VNA measurement, which can effectively avoid the design of additional test circuits, demonstrating its advantages compared with the traditional double-pulse power test. This approach offers an effective bond wire quality screening technology for power-discrete devices without power on treatment.

4. Conclusions

A novel bond wire damage detection approach on a MOSFET power device based on two-port network measurement by detecting parasitic inductance was proposed with theoretical analysis and experimental validation. The numerical calculation showed that the source parasitic inductance of discrete MOSFETs increased with the rising severity of bond wire faults, which can be used as a fault indicator to effectively determine bond wire liftoff faults. By considering a power device as a two-port network, MOSFET is equivalent to a pure inductance element at high frequency, and the parasitic inductances are accurately extracted from the Z−parameters without turning on MOSFETs. The experimental

results indicated that the source parasitic inductance, L_S, increased with the fault number of bond wires, and even the slight fault showed high sensitivity, which can effectively quantify the number of bond wire liftoffs of discrete MOSFETs under zero biasing conditions. Meanwhile, the feasibility and applicability of using source parasitic resistance, R_S, to identify the bond wire fault were discussed. The skin effect forced the increase in bond wire parasitic resistance to an effective detection scale due to the higher f_{SRF}, which was significantly positively correlated with the severity of bond wire faults. However, as a failure precursor, parasitic resistance is suitable for the detection of high switching frequency MOSFETs, especially in emerging wide-bandgap SiC MOSFETs, and the recognition resolution of low-frequency power MOSFETs was insufficient. The proposed two-port network VNA measurement approach was impressively achieved without turning on the MOSFET. Thus, designing additional test circuits and controlling the junction temperature is unnecessary. This approach offers an effective bond wire fault detection technology for power devices and can be extended by establishing online quality monitoring technology in future research.

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Appendix A

Table A1. Parasitic inductance, L_{Bond}, with two bond wire cutoffs.

Bond Wire No.		**1**	**2**	**3**	**4**	**5**	**6**	**$L_{Bond_No.}$ nH**
Si MOSFET IXFK32N100P	1	/						
	2	/						
	3	/		12.72	4.98	3.51	2.58	23.79
	4	/		4.98	14.19	3.76	3.57	26.5
	5	/		3.51	3.76	7.22	3.22	17.71
	6	/		2.58	3.57	3.22	9.7	19.07
				L_{Bond_IX}				5.30
SiC MOSFET C2M0160120D	1	/						
	2	/						
	3	/		6.78	3.84			10.63
	4	/		3.84	7.00			10.84
				L_{Bond_C2}				5.37

Table A2. Parasitic inductance, L_{Bond}, with three bond wire cutoffs.

Bond Wire No.		1	2	3	4	5	6	$L_{Bond_No.}$ nH
Si MOSFET IXFK32N100P	1							
	2					/		
	3							
	4				14.19	3.76	3.57	21.52
	5		/		3.76	7.22	3.22	14.2
	6				3.57	3.22	9.7	16.49
				L_{Bond_IX}				5.63
SiC MOSFET C2M0160120D	1							
	2					/		
	3							
	4		/		7.00			7.00
				L_{Bond_C2}				7.00

Table A3. Parasitic inductance, L_{Bond}, with four bond wire cutoffs.

Bond Wire No.		1	2	3	4	5	6	$L_{Bond_No.}$
Si MOSFET IXFK32N100P	1							
	2					/		
	3							
	4							
	5			/		7.22	3.22	10.44
	6					3.22	9.7	12.92
				L_{Bond_IX}				5.77

Table A4. Parasitic inductance, L_{Bond}, with five bond wire cutoffs.

Bond Wire No.		1	2	3	4	5	6	$L_{Bond_No.}$
Si MOSFET IXFK32N100P	1							
	2					/		
	3							
	4							
	5			/				
	6						9.7	9.7
				L_{Bond_IX}				9.7

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