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DOI
10.1109/ISSCC42613.2021.9365790

Publication date
2021

Document Version
Final published version

Published in
2021 IEEE International Solid-State Circuits Conference, ISSCC 2021 - Digest of Technical Papers

31.4 A Chopper-Stabilized Amplifier with -107dB IMD and 28dB Suppression of Chopper-Induced IMD

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2021 IEEE International Solid- State Circuits Conference (ISSCC) | 978-1-7281-9549-0/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISSCC42613.2021.9365790

Amplifiers often employ chopping to achieve low offset and low-frequency noise. However, the interaction between the input signal and the chopper clock can cause chopper-induced intermodulation distortion (IMD) [1-5]. This is especially problematic for input frequencies (F_{in}) near even multiples of the chopping frequency (F_{CH}), as the resulting IMD tones fold-back to low frequencies and so cannot be filtered out. In [2-4], spread-spectrum clocks are used to convert such tones into noise-like signals. However, this increases the noise floor and does not address the underlying problem. This paper shows that chopper-induced IMD is mainly due to amplifier delay, which results in large chopping spikes. A novel fill-in technique is proposed that mitigates these spikes, and so reduces the chopper-induced IMD. In a prototype chopper-stabilized amplifier, it reduces the chopper-induced IMD by 28dB, resulting in an IMD of -126dB for input frequencies near $4F_{CH}$ (=80kHz). Similarly, it improves the chopped amplifier's two-tone IMD (79 and 80kHz) from -97dB to -107dB, thus maintaining the same IMD as the un-chopped amplifier.

A simplified block diagram of the proposed amplifier is shown in Fig. 31.4.1. It consists of a two-stage main amplifier (folded-cascode 1st stage and Class-AB 2nd stage), whose offset and 1/*f* noise are suppressed by a three-stage auxiliary amplifier. To minimize its own offset (V_{os1}) and 1/*f* noise, the auxiliary amplifier employs a chopped OTA (G_{m1}, folded-cascode), followed by an integrator (G_{mINT}, folded-cascode, and $C_{int1\text{-}int2}$, each 36pF), and a correction OTA (G_{mCOR}, telescopic). When used in a negative feedback configuration, the offset of the main amplifier (V_{osMAIN}) appears at the input of the chopped G_{m1}, whose output current is integrated (G_{mINT}) to generate, via G_{mCOR}, an offset-correcting signal for the main amplifier (G_{mMAIN}).

As shown in Fig. 31.4.2, chopping an OTA with a non-zero delay (T_{delay}) causes large output spikes. This is because the transitions of the output chopper are no longer aligned with the OTA's delayed output signal (I_1), causing spikes in the demodulated output current (I_{out}). Even though these spikes are short (a few nanoseconds), their amplitude is proportional to the input signal, and therefore causes significant distortion. The OTA's input amplitude depends on F_{in}/GBW, and so its IMD increases with input frequency. In the frequency domain, the effect of these spikes can be understood by considering the simplified model shown in Fig. 31.4.2, bottom-left, in which the OTA's finite BW is modelled as a pure delay. It shows that the spikes can then be modelled by multiplying the input signal by a sequence of rectangular pulses (p) whose width is equal to the OTA's delay, and whose frequency is equal to $2F_{CH}$. This multiplication causes input signals close to multiples of $2F_{CH}$ to fold back to near DC, thereby causing IMD tones. These can be minimized by increasing the OTA BW, but at the expense of a very significant increase in power (about 25× for 28dB of IMD reduction, according to simulations). In reality, the OTA's finite BW causes exponentially settling spikes, resulting in somewhat lower IMD tones.

Alternatively, chopper-induced IMD can be eliminated by ensuring that there are no spikes in the input current of G_{mINT} (I_{int}). This is the goal of the proposed fill-in technique. As shown in Fig. 31.4.3, it employs two nominally identical auxiliary OTAs (G_{m1} and G_{m2}), which are chopped by quadrature clocks (CH_1 and CH_2) such that chopping transitions, and the associated spikes, will only be experienced by one OTA at a time. The OTAs' output currents ($I_{out1,2}$) are nominally identical, and so, via multiplexers ($S_{3\&5}$), the spikes of one OTA can be *filled in* with the output current of the other. The key insight is that the multiplexers can switch the OTA's output currents much faster than the OTAs themselves.

To reduce the ripple caused by their chopped offset (V_{os1} and V_{os2}), G_{m1} and G_{m2} are auto-zeroed whenever they are not driving G_{mINT}. During the auto-zero (AZ) phase, the OTA inputs are shorted to one of the input pins via S_1, instead of being shorted to a fixed common-mode voltage. This prevents input CM transients, which would cause extra IMD. Dummy always-closed and always-open switches (in grey) ensure that the input network formed by the switch resistances and the parasitic capacitance is symmetric. This mitigates switching spikes due to clock feedthrough and charge injection. During the AZ phase, C_{AZ} (25pF) acts as a passive integrator whose output drives G_{mAZ1} (Telescopic) to cancel the OTA's offset. The resulting voltage is held by $C_{1,2}$ (1.8pF each) during the amplification phase. To minimize noise folding, the noise BW during the AZ phase should be limited by minimizing G_{mAZ1}, but this increases the OTA's worst-case output swing. As a compromise, G_{mAZ1} is chosen to be ~50× smaller than G_{m1}. Furthermore, the AZ phase is ended roughly 100ns before the next chopping phase, allowing $G_{m1,2}$ to settle before it is connected to G_{mINT}.

When the OTA outputs are not connected to either G_{mINT} or to G_{mAZ1}, a shorting switch (S_4) maintains them at a well-defined voltage. Its resistance is set to ~$1/G_{mINT}$ (6.8kΩ), which minimizes the voltage transient (and switching spikes) that occurs when the OTA is re-connected to G_{mINT}. At the start of the AZ phase, the OTA's output must switch from a signal-dependent current to an offset-dependent current, and so for fast settling its output is shorted for about 100ns [6]. This also mitigates additional output spikes. To avoid disturbing the state of C_{AZ}, it is disconnected by switch $S_{6\&7}$ while the OTA is shorted ($Short_{1,2}$).

The opamp was realized in a 0.18µm CMOS BCD process (Fig. 31.4.7). It draws 550µA from a 5V supply and has an active area of 0.54mm². When it is configured as a buffer, a single $1V_{rms}$ 79kHz input tone results in the output amplitude spectrum shown in Fig. 31.4.4 (top). Without the fill-in technique (left) a large -97.7dB IMD tone is present at 1kHz ($4F_{CH}$-F_{in}). With fill-in enabled, this drops by 28dB, to -125.9dB (right). When two input tones are applied (79 and 80kHz, $0.5V_{rms}$ each) the resulting amplitude spectrum is shown in Fig. 31.4.4 (bottom). Without chopping, the IMD at 1kHz is -107dB, which increases to -97dB with chopping and with fill-in disabled. Enabling fill-in restores the IMD to -107dB, demonstrating that it effectively suppresses chopper-induced IMD.

The opamp has a 0-to-4.5V input CM range, a 124dB PSRR (DC) and 15.4 NEF. It also has a 4.2MHz GBW and a 1.7V/µs slew-rate (Fig. 31.4.5 bottom Left). With a 2.5V input CM voltage and an F_{CH} of 20kHz, measurements on 15 samples show that its offset does not exceed 0.8µV and its input current stays below 600pA (Fig. 31.4.5 top right). The opamp's voltage noise density is shown in Fig. 31.4.5 (top left). Without chopping, 1/*f* noise can be seen together with a white-noise level of 16nV√Hz. With chopping, auto-zeroing and fill-in enabled, the 1/*f* noise is suppressed and the white-noise level is extended to low frequencies. The noise bump around 20kHz is due to the low-frequency noise caused by auto-zeroing each OTA at 20kHz, which is then up-modulated to 20kHz by chopping. Some tones can be seen at the chopping/auto-zeroing frequencies, which was traced to PCB-related coupling between the chip and the 5V reference clock (80kHz). The input current vs F_{CH} (Fig. 31.4.5 bottom) shows a linear relationship, showing that the input current comes from the charge injection mismatch of the switches. The power breakdown (Fig. 31.4.5 bottom left) shows that each fill-in channel uses 24% of the power and 10% of the total active area.

Figure 31.4.6 shows the performance summary and a comparison with the state of the art. This design achieves the lowest chopper-induced IMD (-125.9dB) at a much higher input frequency (79kHz). This is enabled by the fill-in technique, which reduces the chopper-induced IMD by 28dB, without a significant increase in power. In addition, the opamp also achieves competitive offset (< 0.8µV) and noise (16nV√Hz).

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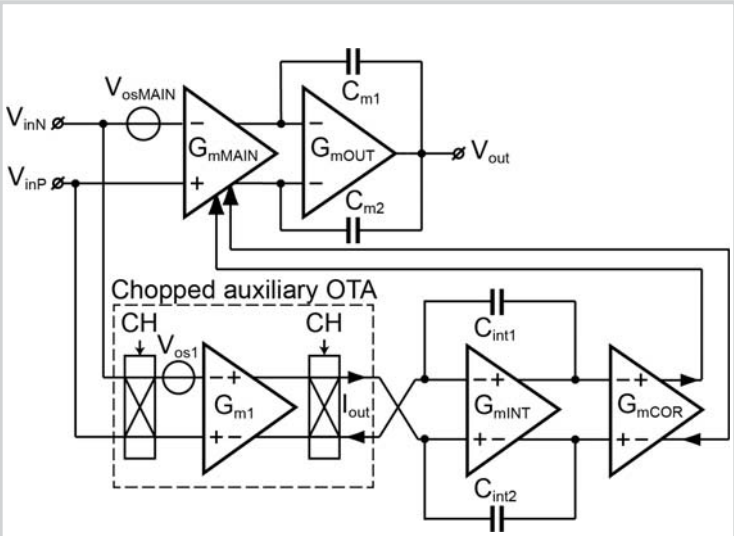

Figure 31.4.1: Simplified block diagram of the proposed Chopper-Stabilized Operational Amplifier.

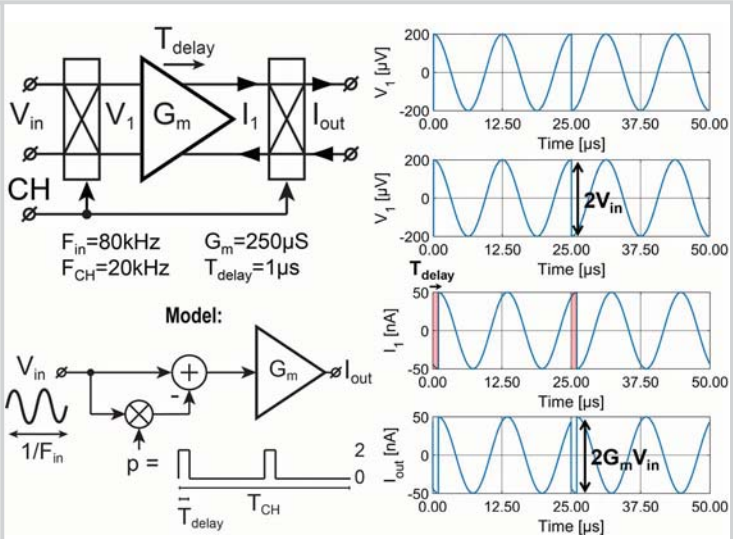

Figure 31.4.2: Chopped OTA with a delay (top left), and the resulting signals (right) when an input signal (V_{in}) is applied, showing large spikes at the output (I_{out}), and a model for the resulting waveform (bottom left).

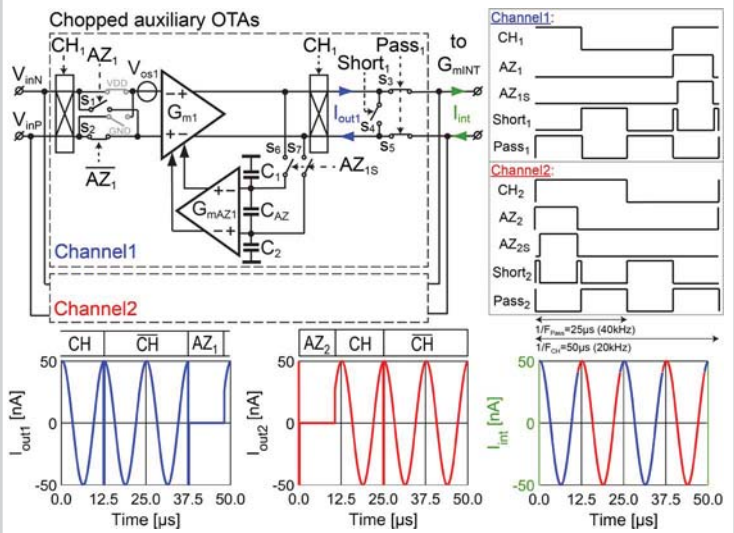

Figure 31.4.3: Block diagram of the proposed two channels in the stabilization loop that are auto-zeroed and are used for the fill-in technique (top left), the timing diagram (top right) and the resulting waveforms (bottom).

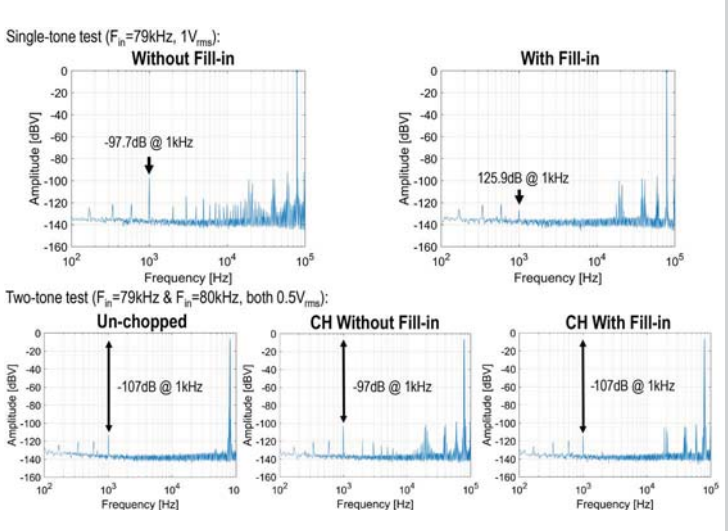

Figure 31.4.4: Measured amplitude spectrum (10 Averages) with a single-tone test (top) for F_{in}-4F_{CH}=1kHz without and with Fill-in (left & right respectively) and a two-tones test (bottom) all in a non-inverting buffer configuration.

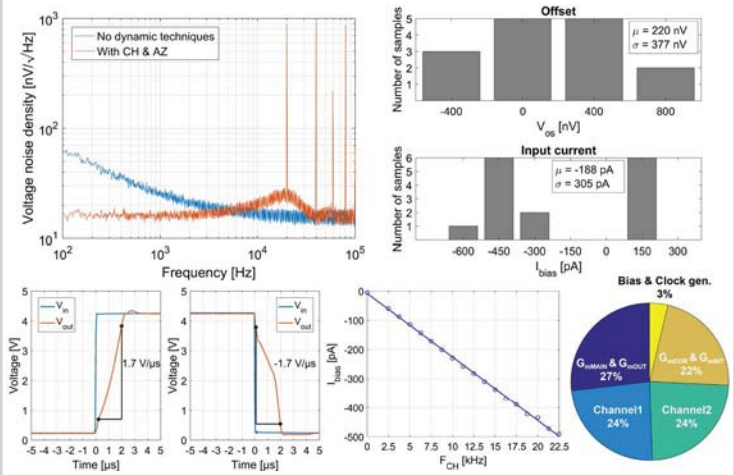

Figure 31.4.5: Voltage noise density vs frequency. Histogram of the offset voltage and input current for 15 Samples. Slew rate with a 4V input voltage step (0.2 to 4.2V) in a buffer configuration. Input current vs chopping frequency. Power breakdown.

	This work	[1] AD8551	[3] AD8571	[4] Ivanov	[5] Rooijers
Dynamic technique(s)	**Chopper Stabilized with Auto-zeroing**	Auto-zero Stabilized	Auto-zero Stabilized	Chopper Stabilized with ripple-reduction	Auto-zeroing and Chopped Stabilization
IMD tone (dB)	**f_{in}=79kHz -97.7 (No Fill-in) -125.9 (Fill-in)**	f_{in}=0.5kHz -80 (Single)* -	f_{in}=0.5kHz - -90 (Spread)*	f_{in}=1kHz -103 (Single)** -122.7 (Spread)**	f_{in}=16kHz -44 (Single) -
Offset (Max)	**0.8 µV*** **	5 µV	5 µV	3.5 µV	0.6 µV
Input current (Max)	**600pA*** **	50pA	50pA	200pA	0.2pA
Voltage Noise Density (nV/√Hz)	**16**	42	51	6.5	20
CH/AZ Frequency (kHz)	**20**	4	2-4	50-150	15
GBW (MHz)	**4.2**	1.5	1.5	10	1.45
Slew rate (V/µs)	**1.7**	0.4	0.4	5	-
PSRR (dB)	**124**	130	130	135	125
Supply voltage	**5V**	5V	5V	1.8-5.5V	1.8V
Supply current	**0.55 mA**	0.85 mA	0.85 mA	1.65 mA	0.21 mA
Technology	**0.18 µm**	-	-	0.6µm	0.18 µm
Die Area (mm²)	**1.25**	-	-	1.626	1.4

*V_{out}=1V_{rms}@500Hz (A=40dB) [2] **V_{out}=1V_{rms}@1kHz (A=1) ***Maximum value of 15 samples

Figure 31.4.6: Performance summary and comparison with previous works.

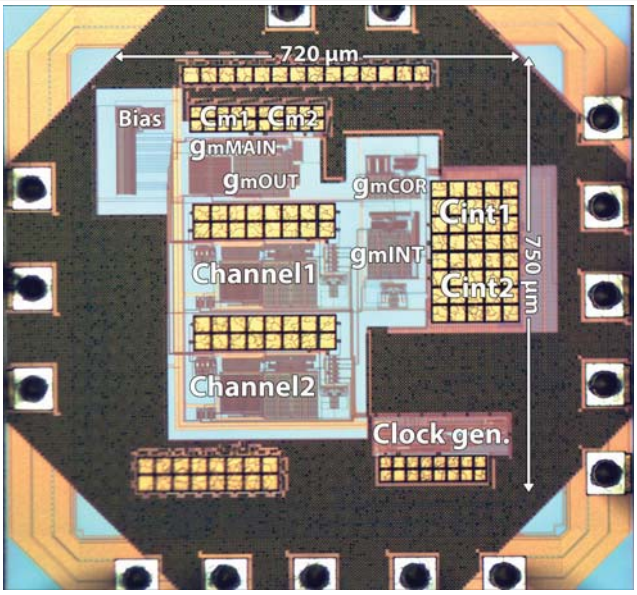

Figure 31.4.7: Die micrograph of the fabricated chip.

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