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A Pitch-Matched Transceiver ASIC for 3D Ultrasonography with Micro-Beamforming ADCs based on Passive Boxcar Integration and a Multi-Level Datalink

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Abstract

This paper presents a pitch-matched transceiver ASIC integrated with a 2-D transducer array for a wearable ultrasound device for transfontanelle ultrasonography. The ASIC combines 8-fold multiplexing, 4-channel micro-beamforming (μBF) and sub-array-level digitization to achieve a 128-fold channel-count reduction. The μBF is based on passive boxcar integration and interfaces with a 10-bit 40 MS/s SAR ADC in the charge domain, thus obviating the need for explicit anti-alias filtering and power-hungry ADC drivers. A compact and low-power reference generator employs an area-efficient MOS capacitor as a reservoir to quickly set a reference for the ADC in the charge domain. A low-power multi-level data link concatenates outputs of four ADCs, leading to an aggregate 3.84 Gb/s data rate. Per channel, the RX circuit consumes 2.06 mW and occupies 0.05 mm^2.

Introduction

Inadequate brain perfusion regularly shown in preterm infants exposes the developing brain to injury that could have severe consequences in later life. A wearable ultrasound device (Fig 1a) enables bedside monitoring of the neonatal brain via transfontanelle ultrasonography (TFUS), and thus facilitates a timely treatment for neonates. To match fontanel size and generate high-resolution 3-D images, a 2-D array of 10,000+ transducer elements, featuring small pitch and high central frequency, is required, leading to challenges in chip interconnection, packaging, and power dissipation.

Here, we present a pitch-matched ASIC prototype that is directly integrated with a 16×16 transducer array with 125-μm pitch and 9-MHz central frequency, in which a novel low-power architecture is implemented to reduce the number of transducer channel by a factor of 128, making it a promising solution to these major challenges. The ASIC is partitioned into a pitch-matched region containing element-level high-voltage (HV) pulsers and receive (RX) circuits, and a peripheral region containing 16-level pulse amplitude modulation (PAM16) data links and miscellaneous blocks such as a clock buffer (Fig. 1b). During transmission (TX), each transducer element is isolated from the low-voltage RX circuitry by a Transmit/Receive (T/R) switch and pulsed by a unipolar square-wave pulser. During the following RX, the transducer array is divided into 64 sub-arrays of 2×2 elements, eight of which are selected by 8:1 multiplexers and connected to single-ended analog front ends (AFEs) [1] via the T/R switches. The AFEs operate in current mode with built-in continuous time-gain compensation function (TGC) and provide high-impedance outputs for the following μBF ADCs, each incorporating boxcar-integration μBF [2] and a SAR ADC in the charge domain. The output data of the ADCs are concatenated into two data streams of 4-bit width, fed to two PAM16 transmitters with differential outputs, thus finally achieving a 128-fold channel-count reduction.

Circuit Implementation

Fig. 2 depicts a time-interleaved channel (e.g., TI_1) of the μBF, which, in contrast with [2], employs passive boxcar integration to save area and power. It cyclically integrates 4 current outputs of the AFEs on a capacitor C_{INT1}, controlled by clock signals D_1<1:4> that set the needed μBF delay (e.g., τ_1). C_{INT1} is then connected to the capacitive DAC (CDAC) array of the following charge-sharing SAR ADC during read phase R_1 [3]. Meanwhile, an input common mode feedback (ICMFB) circuit cancels out the CM signals on C_{INT1} and a dummy capacitor C_{DMY1}, thus converting the single-ended signal to a differential input for the ADC. After digitization, the residual charge on the capacitors is nulled (S_1). The integration, read and reset time are all orchestrated by an 80-MHz clock (CK_{RX}). To accommodate a maximum delay (τ_{max}) of 62.5 ns, five TI channels are used.

At the beginning of each read phase (Φ_{REF}), the CDAC array is quickly charged to V_{REF} by sharing charge with a pre-charged reservoir capacitor C_{RSV}. Afterward, a dynamic comparator successively decides the voltage polarity appearing at the common nodes (V_{CP}, V_{CN}) of the CDAC array for 10 bit cycles. Finally, the CDAC array is reset (Φ_{RST}). Asynchronous SAR logic is employed to avoid distributing a high-frequency clock over the whole chip.

During TX, a servo loop consisting of a comparator and a charge pump calibrates the current (I_{CHG}) charging the parallel-connected CDAC and the reservoir NMOS capacitor (C_{RSV}), until the voltage on top of these capacitors equals V_{REF} (Fig. 2). The overdrive required to generate I_{CHG} is sampled and held on a PMOS capacitor (C_{SH}) throughout the RX, delivering the same amount of charge to C_{RSV} in Φ_{CHG} that will be redistributed with the CDAC in the next read phase. The active blocks in the servo loop are all deactivated during RX, leading to a very low-power and area-efficient reference scheme.

The differential outputs of the ADC are transmitted to the chip's periphery where a clock data recovery (CDR) circuit recovers the clock, followed by a first-in, first-out buffer (FIFO) that synchronizes the data with a 480-MHz clock (CK_{PAM}) before concatenating four of such bitstreams into a 4-bit data stream. By using a structure similar to a 4-bit current-steering DAC [4] built from complementary unit cells (Fig. 2), the PAM16 transmitter converts the 4-bit data into a 16-level continuous signal, allowing for an external PAM16 receiver to recover the 4-bit data. In contrast with LVDS [5,6], this effectively reduces the clock frequency by a factor of 4 and reduces the associated power consumed by internal digital circuitry and external parasitic capacitors.

Measurement Results

Fig. 5 shows a micrograph of the ASIC and the prototype chip with transducer array built on top. Fig. 3a shows the output spectrum of the RX channel measured at the maximum AFE gain. It shows a maximum 50.7-dB SNR achieved in the

bandwidth from 5 MHz to 13 MHz. The two tones, associated with the mismatch and intermodulation of the µBF, have negligible impact on image quality. The measured eye diagram of the PAM16 transmitter (Fig. 3b) shows a > 0.9-ns width and > 20-mV height, allowing data recovery with a bit-error rate < 10^{-10}. The HV pulsers successfully generate 8-cycle pulses with up to 20-V amplitude and a delay resolution of 13.9 ns (Fig. 3c). The RX µBF directivity was measured by applying four time-shifted sinusoidal inputs to the chip to emulate an acoustic wave arriving at different angles (Fig. 3d), showing a good agreement with the ideal directivity. Fig. 4a shows the setup for acoustic measurements, in which a small water tank was mounted on top of the protype, with 3 needles positioned from 5 to 9 mm above the transducer array. A B-mode image and the rendered 3-D image (Fig. 3b,c) clearly distinguish the needle heads from the background. Table I gives a performance summary and comparison with the prior art.

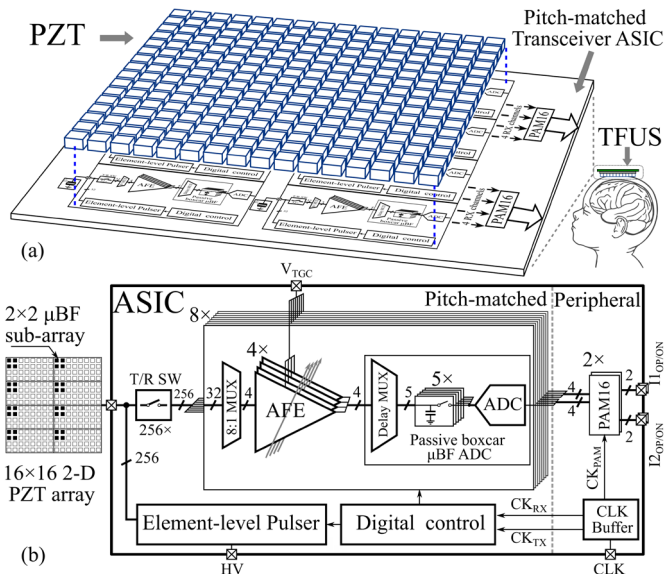

Fig. 1 Overview of (a) a wearable device for TFUS; (b) the ASIC architecture.

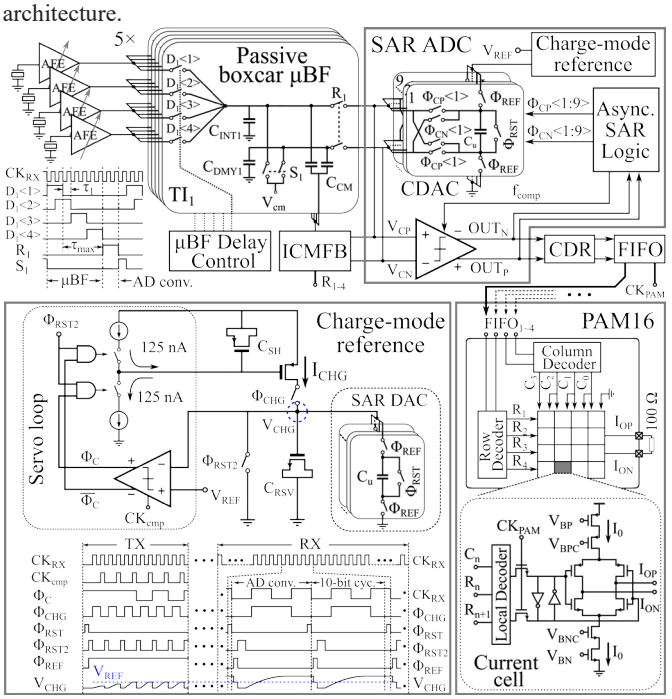

Fig. 2 Circuit diagram of the passive-boxcar-integration µBF, the charge-sharing SAR ADC with charge-mode reference generator, the PAM16 transmitter and their timing details.

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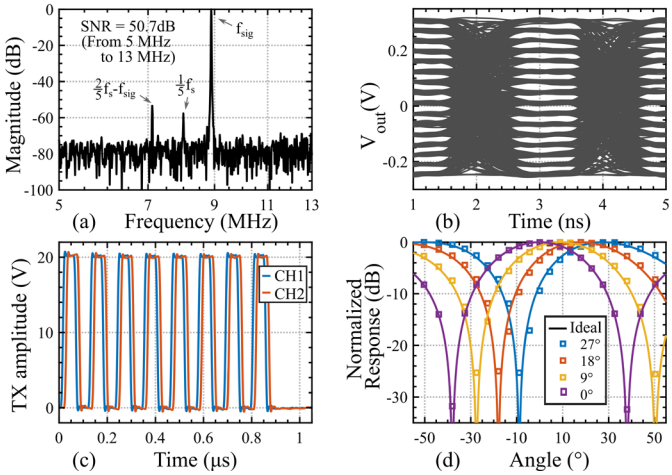


Fig. 3 Measured (a) output spectrum of RX, (b) eye diagram of PAM 16 TX, (c) output waveforms of high-voltage pulser, and (d) µ-beamforming directivity.

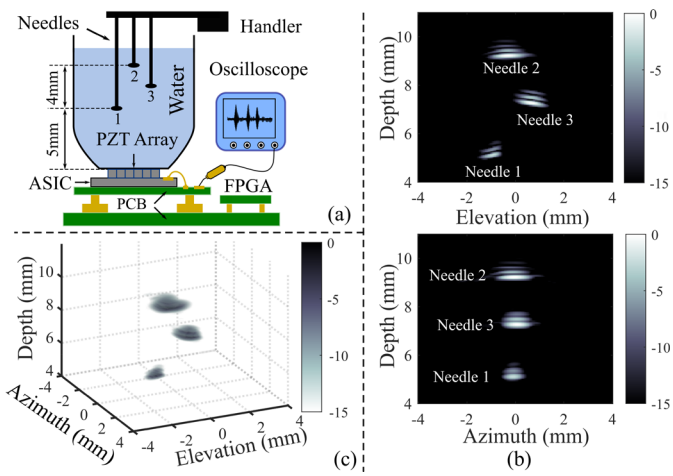
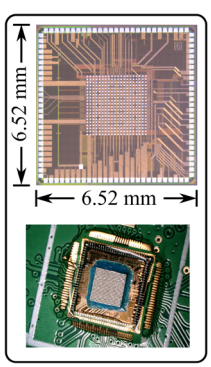


Fig. 4 (a) Imaging experiment setup; (b) B-mode image showing the position of the needles; (c) Rendered 3-D image.



† Divided by 16, 8:1 MUX not included.
* Include sub-array ADC.
§ Include ADC and datalink.

Table I
Performance summary and comparsion with the prior art

	This work	[5]	[6]	[7]
Process	180nm BCD	180nm	180nm BCD	180nm SOI
Center Freq.	9 MHz	5 MHz	6 MHz	< 5 MHz
Sub-array size	2 × 2	3 × 3	3 × 2	4 × 6
Pitch-matched	Y	Y	Y	Y
Pitch	125 µm	150 µm	160 µm	300 µm
Digitization	Y	Y	Y	N
Sampling rate	40 MS/s	30 MS/s	24 MS/s	40 MS/s
Datalink type	PAM16	LVDS	LVDS	–
Data rate	1.92 GHz	1.5 GHz	1.2 GHz	–
Datalink power	6.4 mW	15.4 mW	7 mW	–
Ch. Reduction	128-fold	36-fold	12-fold	24-fold
AFE type	LNA with TGC	LNA + PGA	LNA + PGA	LNA + PGA
AFE bandwidth	14.2 MHz	11.9 MHz	8.1 MHz	5.9 MHz
µBF resolution	12.5 ns	33 ns	20.8 ns	25 ns
µBF area/ch.	†*0.01 mm²	*0.011 mm²	*0.006 mm²	0.03 mm²
RX area/ch.	†*0.05 mm²	*0.026 mm²	*0.017 mm²	0.09 mm²
RX power/ch.	†§2.06 mW	§0.91 mW	§1.23 mW	0.43 mW
Input DR	83 dB	85 dB	91 dB	85 dB
Peak SNR	54 dB	52 dB	52 dB	N/A
TX Voltage	20 V	–	65 V	138 V

Fig. 5 Micrograph of the ASIC and prototype with transducer built on top, performance summary and comparison with prior art.