Design and Benchmark of Front-end Voltage Control for Wireless Power Transfer

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by

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to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday 12, 2022 at 14:30 PM.

Student number:	5261287	
Project duration:	January 1, 2022 – September 12, 2022	
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Preface

It is an unforgettable experience to do my thesis project in the DCE&S group. The courses and training here help me enhance my professional skills and prepare me for my career.

First and foremost, I would like to express my gratitude and respect to Dr. Jianning Dong. He gives me valuable suggestions on the framework of my thesis project and insightful comments when I meet problems.

Then I would sincerely thank my PhD supervisor Guangyao Yu for his all-along support during the process. He not only gives me many wise and professional academic guidances but also helps me improve my abilities to solve problems. I have benefited tremendously from his insightful thinking and rigorous attitude.

Zian Huang
Delft, September 2022

Abstract

In recent years, the Wireless Power Transfer (WPT) system has become more and more popular due to its prominent advantages, especially for Electrical Vehicle (EV) charging. The WPT systems are required to follow the EV battery charging profiles, thus more and more voltage control methods with distinctive characteristics are proposed and studied. The goal of this thesis report is to conduct a comprehensive benchmark of the front-end voltage control solutions.

This thesis report focuses on the front-end voltage control solutions including the front-end buck converter and the phase shift control based on the primary inverter. Six different front-end voltage control scenarios are designed and compared in terms of system efficiency. There are four scenarios of the front-end buck converters including the single-phase buck converter working in Continuous Conduction Mode (CCM), the single-phase buck converter working in Triangular Current Mode (TCM), the two-phase interleaved buck converter working in CCM and the two-phase interleaved buck converter working in TCM. There are also two scenarios of primary inverter-based phase shift controls including phase shift with and without phase delay. The single-phase buck converter working in TCM has the highest efficiency reaching 95.5% at a light load. The phase shift control scenario with phase delay has the highest efficiency exceeding 96.5% at a heavy load.

Different from previous research on phase shift control, this thesis report conducts an in-depth harmonic analysis and compares the accuracy of harmonics analysis with the accuracy of fundamental wave analysis. The conclusion not only proves that fundamental wave analysis is reliable and accurate enough to calculate the phase shift parameters for the S-S compensation but also improves the calculation accuracy at a light load by harmonics calibration.

Contents

1 Introduction

Wireless Power Transfer (WPT) has been introduced decades ago, and more recently, it has been used for industrial and commercial cases. WPT is widely used because of features like charging without cables and charging through the air. WPT technology finds application in factory automation, instrumentation and electronic systems, biomedical implants, insecurity systems, and many other applications where its unique features can be exploited according to the research from Z. Zhang et al., 2018. Electrical vehicle charging, as the main topic, has growing popularity in WPT systems due to its specific benefits like aesthetics, safety, and convenience. For EV charging, disordered cables bring inconvenient and unpleasant charging experiences. The replacement of charging cables also enables a completely waterproof design. WPT also increases the reliability level of EV charging by reducing the process of plugging in and out cables. The implementation of the WPT charging system in EV charging stations brings many challenges like foreign object disturbances and efficiency issues. Thus, there is an increasing need to study and improve the technologies of WPT systems.

1.1. Structure of WPT

In a Wireless Power Transfer system, a transmitter device, driven by electric power from a power source, generates a time-varying electromagnetic field, which transmits power across space to a receiver device, which extracts power from the field and supplies it to an electrical load. Wireless power techniques mainly fall into two categories, near-field and far-field. In the near field or non-radiative techniques, power is transferred over short distances by magnetic fields using inductive coupling between coils of wire, or by electric fields using capacitive coupling between metal electrodes according to the research from Garnica et al., 2013. Inductive coupling is the most widely used wireless technology. Its applications include charging handheld devices like phones and electric toothbrushes, RFID tags, induction cooking, and wirelessly charging or continuous wireless power transfer in implantable medical devices like artificial cardiac pacemakers or electric vehicles. In far-field or radiative techniques, also called power beaming, power is transferred by beams of electromagnetic radiation, like microwaves or laser beams. These techniques can transport energy longer distances but must be aimed at the receiver. Proposed applications for this type are solar power satellites, and wireless-powered drone aircraft as Lu et al., 2017 mentioned. These are the different wireless power technologies as Table.1.1.

In this thesis, the application of EV charging belongs to the resonant inductive coupling. In inductive coupling, power is transferred between coils of wire by a magnetic field. The transmitter and receiver coils together form an air-gap transformer. An alternating current through the transmitter coil creates

Table 1.1: Different WPT technologies

Technology	Range	Frequency	Antenna devices	Applications
Inductive coupling	Short	kHz	Wire coils	Industrial heaters
Resonant inductive coupling	Mid	kHz	Tuned wire coils	Qi products, EVs
Microwaves	Long	GHz	Rectennas	Solar power satellite

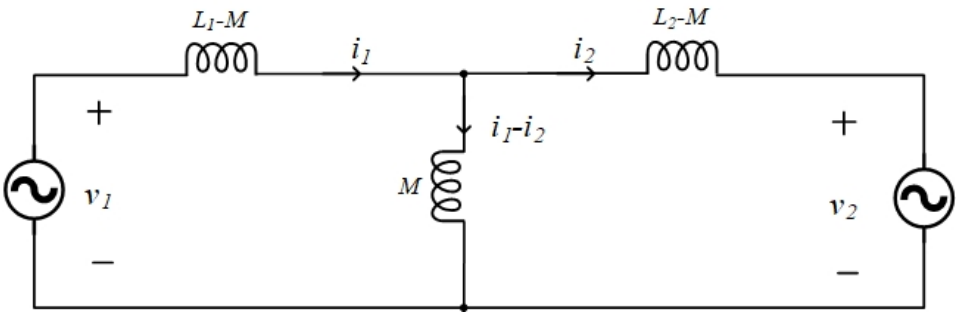

Figure 1.1: Mutual inductor model of WPT

an oscillating magnetic field by Ampere's law. The magnetic field passes through the receiving coil, where it induces an alternating EMF by Faraday's law of induction, which creates an alternating current in the receiver. The induced alternating current may either drive the load directly or be rectified to direct current by a rectifier in the receiver, which drives the load. Inductive coupling is the oldest and most widely used wireless power technology and virtually the only one so far which is used in commercial products based on the conclusion from Covic and Boys, 2013.

1.1.1. Magnetic coupling of WPT

The magnetic coupling of an inductive power transfer model could be regarded as an ideal air-gap transformer model. According to Ampere's law, a current flowing in a coil produces a magnetic field and, from Faraday's law, part of this field links to a second coil inducing a voltage at its terminals. This induced voltage causes a current to flow in the second coil.

Mizuno et al., 2011 concluded that IPT has two coils separated by a large air gap. The coils are placed around a magnetic material to improve coupling and minimize proximity losses. The primary coil is energized by a high-frequency ac current which generates a time-varying magnetic field in accordance with Ampere's law. A portion of the generated time-varying magnetic field is linked with a secondary coil to induce a voltage in the secondary side according to Faraday's law.

Based on the magnetic theory, the air-gap transformer could be represented by a mutual inductor model shown in Fig.1.1. And the network equation of the magnetic coil coupling can be written as Eq.(1.1) and Eq.(1.2).

$$v_1(t) = L_1 \frac{di_1(t)}{dt} - M \frac{di_2(t)}{dt} \tag{1.1}$$

$$v_2(t) = M \frac{di_1(t)}{dt} - L_2 \frac{di_2(t)}{dt} \tag{1.2}$$

where the v_1 is the primary coil voltage, v_2 is the secondary coil voltage, i_1 is the primary coil current and i_2 is the secondary coil current. L_1 is the primary coil inductance, L_2 is the secondary coil inductance and M is the mutual inductance between primary and secondary coils. The coupling coefficient or coupling factor k is a common dimensionless variable to describe mutually coupled coils as Eq.(1.3)

$$k = \frac{M}{\sqrt{L_1 \cdot L_2}} \tag{1.3}$$

The coupling coefficient is equal to the fraction of the flux generated by the first coil that flows through the second coil so it can reflect the strength of the coupling between the two coils. The coupling factor can be influenced by the distance, alignment and foreign object between coils.

1.1.2. Main circuit of WPT

A WPT charging system for electrical vehicles is composed of two main subsystems, the transmitter and the receiver. The transmitter is the primary circuit located under the ground of a charging station. The receiver is the secondary circuit implemented in the EVs. The power will be delivered from the transmitter to the receiver via the WPT system, charging the EVs' batteries. In order to transform the power from the primary coil to the secondary coil via magnetic coupling of coils, a circuit including a

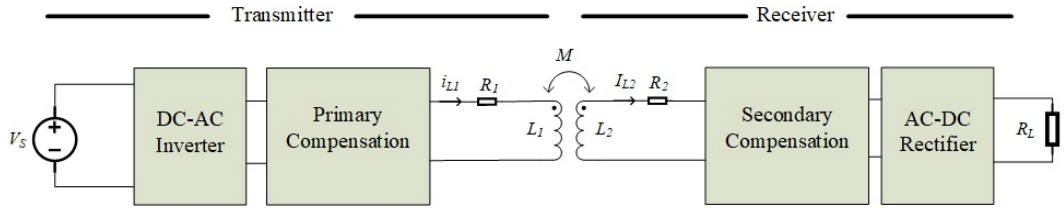

Figure 1.2: Main circuits of WPT

compensation network, inverter and rectifier is needed as Figure.1.2.

The first part is the primary and secondary compensation network. The WPT system has to transfer real power from the primary to the secondary circuit for charging the EV battery. According to the magnetic coupling analysis in the above section, a large primary coil current is required to produce a sufficient magnetic field to link secondary coils. Then the actual power transfer happens through two loosely coupled ferromagnetic coils. For a purely inductive circuit, the system can only deliver a low real power due to the low power factor. In practical WPT systems, it is necessary to cancel the inductive component in the circuit using a capacitor connected such that it resonates with the primary inductance to reduce the power rating of the input. The secondary side is also tuned to approximately the same resonant frequency to cancel the secondary leakage inductance and to maximize the power transfer efficiency according to the research of Grazian et al., 2020.

The second part is the power electronics needed for AC DC transformation and control. The system is powered by the 50 Hz AC power grid. The AC grid voltage is transformed to the DC voltage source V_S after a rectifier and a grid filter, which are not included in this research. A common maximum output DC voltage of the grid-connected rectifier is 500 V according to the reference design from the SAE J2954 standard. Thus the DC voltage source V_S is stabilized to 500 V in this thesis, which enables the designed voltage control circuits to cover most WPT EV charging systems. In order to supply high-frequency AC currents to the coils, an H-bridge inverter is needed on the primary side. For the secondary side, a rectifier is needed to transform the AC voltage to DC voltage in order to supply the DC loads such as batteries. A diode H-bridge rectifier is a common application for its simple structure.

For the converters, there are conduction losses and switching losses influencing the efficiency of the system. As for conduction losses, an increase in current will cause significant conduction losses in the system. As for switching losses, the switching frequency and the soft or hard switching methods will influence the system efficiency significantly according to the research from Yu et al., 2021. In the following chapters, the semiconductor losses will be analyzed in detail for different WPT system designs.

1.2. Additional requirement for voltage control

For the EV wireless charging application, the output power is flowing to the batteries in the charging stage. When charging an EV battery, the output voltage and current will not be a constant value due to the certain battery charging profile. The first stage is the bulk charge stage, also named the constant current stage. In this first stage, the charging current is held constant and the charging voltage increases. Then the battery charging enters the second stage, which is the absorption charge stage. At this point, most chargers will maintain a steady voltage, while the amperage declines. The lower current going into the battery safely brings up the charge on the battery without overheating it. The third stage of battery charging is the float charge stage. The current continuously declines until the battery almost reaches full capacity while the voltage keeps constant.

For EV battery charging, 80% of the capacity will be charged in the constant current stage and the remained capacity will be charged in the constant voltage stage according to the result from Gautam et al., 2012. In the constant current stage, the WPT system should supply a controllable and variable output voltage to follow the battery charging profile. An additional voltage control circuit will be important to meet the EV battery charging requirement.

Applying DC-DC converters to the original WPT structure is one of the most efficient and convenient solutions. Yu et al., 2021 has studied the application of a back-end boost converter to regulate the output voltage. A synchronous boost converter is designed to increase the constant output voltage of the original WPT system to follow the battery charging profile in this research. High efficiency and a wide voltage regulation range were achieved in this study. However, the implementation of an additional boost converter on the electric vehicle side will make it difficult to build the system highly integrated. Thus, a front-end buck converter implemented on the transmitter side will solve this problem and enable the WPT system to follow the battery charging profile efficiently.

Another possible solution to regulate the output voltage is to apply the phase-shift control method to the inverters on the transmitter side or the rectifiers on the receiver side. Vinod et al., 2021 has introduced two methods to control the H-bridge inverter to regulate the output voltage. By controlling the pulse modulation signal of the H-bridge switches, the generated phase shift will regulate the primary coil voltage, which will control the WPT system output voltage. However, the efficiency of this voltage regulation method is a possible concern, which should be further studied and benchmarked in this paper.

2

WPT System design

2.1. WPT Standard for EV

The regulations and standards for wireless power transfer systems facilitate the design compatibility from different manufacturers. The SAE J2954 standard establishes an industry-wide specification that defines acceptable criteria for interoperability, electromagnetic compatibility, EMF, minimum performance, safety, and testing for wireless power transfer of light-duty plug-in electric vehicles. The specification defines various charging levels that are based on the levels defined for SAE J1772 conductive AC charge levels 1, 2, and 3, with some variations. A standard for WPT based on these charging levels enables multiple selections of systems. Different charging systems with different charging rates based on vehicle requirements allow better vehicle packaging and ease of customer use. The specification supports home charging and public wireless charging.

The standards of SAE J2954 cover the reference design up to 11.1 kVA input power. Therein, three power level classes are defined as WPT1 for a 3.7 kVA system, WPT2 for 7.7 kVA, and WPT3 for 11.1 kVA. In this paper, a 3.7 kVA system will be studied. According to the SAE J2954 WPT1 reference design, the system structure is shown as Fig.1.2. There are some assumptions and situations for this structure. The ground clearance and the offset position of the coils will influence the coil coupling coefficients. There are three different vertical distance classes between the ground assembly and the vehicle assembly. In this paper, a vertical distance of 100-150mm is studied. Therein, the value of primary side coil self-inductance L_1 and the value of secondary side coil self-inductance L_2 are 217 uH and 232 uH respectively. The magnetic coupling coefficient k is 0.249 from the standard. Thus the mutual inductance M can be derived as Eq.(2.1).

$$M = k\sqrt{L_1 \times L_2} = 55.87\ \mu\mathrm{H} \tag{2.1}$$

SAE J2954 WPT1 also have a standard range of output voltage between 280 V-420 V and input power between 1 kVA-3.7 kVA. According to the selected standard, V_s is the input voltage after the PFC converter stage, which is assumed to operate with a controlled voltage set to 500 V as the voltage source of the WPT system. The resonant frequency of the system is also defined as f_0 of 85 kHz. The chosen resonant coils for the WPT system have a quality factor of 300 according to the standard, thus the primary coil resistance R_1 and the secondary coil resistance R_2 can be derived as Eq.(2.2) and Eq.(2.3).

$$R_1 = \frac{2\pi f_0 L_1}{Q} = 386\ \mathrm{m\Omega} \tag{2.2}$$

$$R_2 = \frac{2\pi f_0 L_2}{Q} = 413\ \mathrm{m\Omega} \tag{2.3}$$

2.2. Compensation network

In order to design a wireless power transfer system based on a standardized reference structure, a proper compensation network is one of the most important parts. The aim of the compensation network is to minimize the reactive power circulating in the charging system. In this way, it is possible to transfer the required power to charge the battery and achieve high power efficiency. Depending on the type of connection, the most basic compensation network can be either series-series (S-S), series-parallel (S-P), parallel-series (P-S) or parallel-parallel (P-P). Among these combinations, the S-S compensation is the most used one in wireless charging applications because the required values of both capacitors are independent of both coupling and loading conditions and the S-S structure is shown in Fig.2.1.

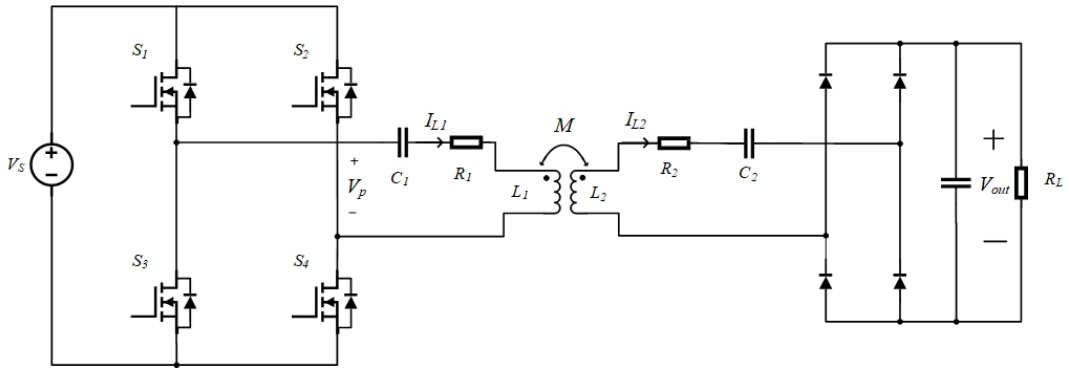

Figure 2.1: WPT circuit with S-S compensation

Based on the magnetic coupling theory Eq.(1.1) and Eq.(1.2), the effect of mutual inductance can be regarded as a controlled voltage source. Based on the fundamental frequency component analysis of the circuit, the voltage equation can be derived as Eq.(2.4), Eq.(2.5) and Eq.(2.6).

$$\overrightarrow{V_p} = \left(R_1 + j\omega_0 L_1 + \frac{1}{j\omega_0 C_1}\right)\overrightarrow{I_{L1}} - j\omega_0 M\overrightarrow{I_{L2}} \tag{2.4}$$

$$0 = \left(R_2 + R_{acL} + j\omega_0 L_2 + \frac{1}{j\omega_0 C_2}\right)\overrightarrow{I_{L2}} - j\omega_0 M\overrightarrow{I_{L1}} \tag{2.5}$$

$$V_s = \frac{\pi}{2\sqrt{2}}V_p \tag{2.6}$$

Where $\overrightarrow{V_p}$ represents the primary inverter output voltage phasor with root-mean-square rms value V_p. $\overrightarrow{I_{L1}}$ is the current phasor flow into the primary inductance L_1 with rms value I_{L1}. $\overrightarrow{I_{L2}}$ is the current phasor flow out of the secondary inductance L_2 with rms value I_{L2}. R_{acL} represents the AC resistance of the load and R_L is the DC load resistance.

In order to minimize the reactive power between the magnetic coupling system, proper capacitance can be designed according to the derived equations. When the reactive powers are fully compensated as Eq.(2.7) and Eq.(2.8), the primary side capacitance C_1 and secondary side capacitance C_2 can be determined as Eq.(2.9) and Eq.(2.10).

$$j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} = 0 \tag{2.7}$$

$$j\omega_0 L_2 + \frac{1}{j\omega_0 C_2} = 0 \tag{2.8}$$

$$C_1 = \frac{1}{\omega_0^2 L_1} = \frac{1}{4\pi^2 f_0^2 L_1} = 16.15\ \text{nF} \tag{2.9}$$

$$C_2 = \frac{1}{\omega_0^2 L_2} = \frac{1}{4\pi^2 f_0^2 L_2} = 15.11\ \text{nF} \tag{2.10}$$

Up to now, all the parameters of the WPT system required by the SAE J2954 have been designed. In order to conduct further research on the efficiency and voltage regulation, more assumptions on the load should be made.

2.3. Equivalent load

Research from Fu, Yin, et al., 2014 suggested that an optimal load could be found for a certain WPT system to acquire maximum efficiency. To calculate the efficiency, the reflected impedance Z_f and the equivalent input impedance Z_{in} should be derived as Eq.(2.11) and Eq.(2.12) and the calculations will be based on Fig. 2.2.

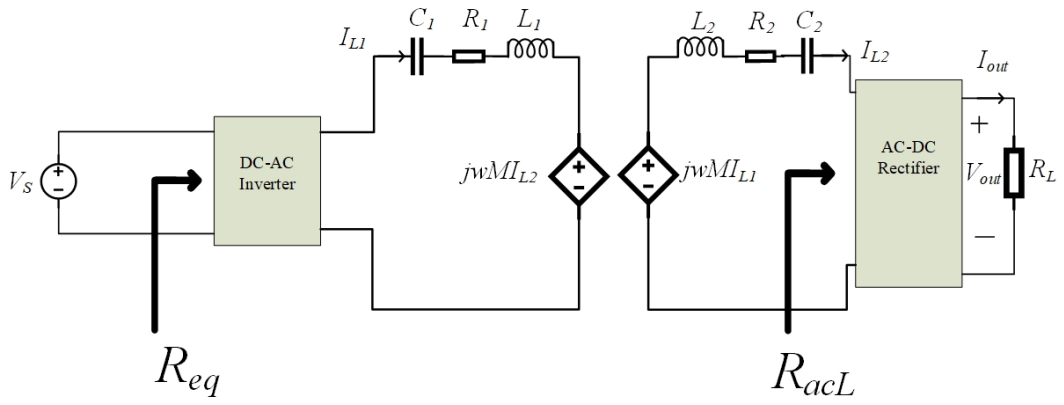

Figure 2.2: WPT circuit with S-S compensation

$$Z_f = \frac{\omega_0^2 M^2}{Z_S} = \frac{\omega_0^2 M^2}{j\omega_0 L_2 + \frac{1}{j\omega_0 C_2} + R_{acL} + R_2} \tag{2.11}$$

$$Z_{in} = j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} + Z_f + R_1 \tag{2.12}$$

Where the Z_S represents the secondary side impedance. When the capacitance is well designed as Eq.(2.9) and Eq.(2.10) calculated, the imaginary part of the impedance could be perfectly eliminated. So the compensated input impedance could be written as Eq.(2.13).

$$Z_{in} = R_1 + \frac{\omega_0^2 M^2}{R_{acL} + R_2} \tag{2.13}$$

Based on the derived input impedance and the fundamental wave voltage, the current of primary side I_{L1} and secondary side current I_{L2} can be derived by circuit analysis as Eq.(2.14) and Eq.(2.15).

$$I_{L1} = \frac{V_p}{Z_{in}} = \frac{V_p}{R_1 + \frac{\omega_0 2M^2}{R_{acL}+R_2}} = \frac{V_p}{R_1 + \frac{\omega_0^2 k^2 L_1 L_2}{R_{acL}+R_2}} \tag{2.14}$$

$$I_{L2} = \frac{V_p - R_1 I_{L1}}{\omega_0 M} = \frac{V_p - R_1 I_{L1}}{\omega_0 k\sqrt{L_1 L_2}} \tag{2.15}$$

To better conclude the calculation of AC and DC power flow, the relation between

$$I_{L2}^2 R_{acL} = {I_{out}}^2 R_L \tag{2.16}$$

$$R_{acL} = \frac{8}{\pi^2} R_L \tag{2.17}$$

where I_{out} is the DC output current. The relation between equivalent AC load resistance and the DC load resistance could be derived by the average output current of the rectifier and the power as

Eq.(2.16) and Eq.(2.17).

Then the efficiency of the system can be derived based on the voltage and current of the circuits as Eq.(2.18). To find the optimal load of the circuit, certain load resistance can be calculated when the circuits have their maximum efficiency. So the derivative of circuit efficiency according to load resistance needs to be derived as Eq.(2.19) and the value that enables the derivation of zero is the optimal load as Eq.(2.20).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{{I_{L2}}^2 R_{acL}}{I_{L1} V_p} = \frac{R_{acL}}{R_{acL} + R_2} - \frac{R_{acL} R_1}{R_{acL} R_1 + R_2 R_1 + \omega_0^2 k^2 L_1 L_2} \tag{2.18}$$

$$\frac{d\eta}{dR_{acL}} = \frac{d\left(\frac{R_{acL}}{R_{acL}+R_2} - \frac{R_{acL}R_1}{R_{acL}R_1+R_2R_1+\omega_0^2k^2L_1L_2}\right)}{dR_{acL}} = 0 \tag{2.19}$$

$$R_{acL} = \sqrt{R_2^2 + \frac{\omega_0^2 k^2 L_1 L_2 R_2}{R_1}} = 31\ \Omega \tag{2.20}$$

Research from Grazian et al., 2020 suggested the influence of coil resistance is negligible when the load resistance is tuned to the optimal value. So in the following research, the influence of the coil resistance R_1 and R_2 are neglected and further calculations will be based on the value of optimal DC load resistance as Eq.(2.21).

$$R_L = \frac{\pi^2}{8} R_{acL} = 38.2\ \Omega \tag{2.21}$$

According to the conservation of input and output power, when the IPT system operates at optimal load conditions, the equivalent optimal load seen from the DC input side is:

$$\frac{V_s^2}{R_{eq\_opt}} = (\frac{2\sqrt{2}V_s}{\pi\omega_0 M})^2 R_{ac\_opt}. \tag{2.22}$$

In (2.22), R_{ac_opt} is the optimal load resistance expressed by (2.20), after simplification, R_{eq_opt} is

$$R_{eq\_opt} = \frac{\pi^2}{8} \frac{\omega_0^2 M^2}{R_{ac\_opt}} \tag{2.23}$$

The voltage across R_{eq_opt} based on power is

$$V_o = \sqrt{P_o R_{eq\_opt}} \tag{2.24}$$

When the input power from the DC side varies between 500 W and 3500 W, the voltage across R_{eq_opt} will be from 133 V to 353 V. They are smaller than the rectified voltage which is set to 500 V. Therefore, a front-end Buck converter is needed. However, in order to analyse the front-end converter more generally, the output voltage of the buck converter can be from 100 V to 400 V. In fact, a back-end dc-dc converter can be used to match the battery charging profile Fu, Ma, et al., 2014, however, this is out of the scope of this thesis study.

In the following research, an additional voltage regulation circuit will be considered. An equivalent load representing the WPT system should be derived to simplify further analysis. When the WPT circuit is well compensated, the equivalent load is a resistance seen from the DC voltage source, representing the power consumed by the whole system without the coil resistance. To find the relation between equivalent load resistance R_{eq} and the real DC load resistance R_L, the rectifier input current I_{L2} and inverter output voltage V_p can be calculated as Eq.(2.25) based on circuit analysis.

$$I_{L2} = \frac{V_p}{\omega_0 M} \tag{2.25}$$

The power consumption at the DC voltage source is equal to the power consumption at the point before the rectifier. Then the power relation can be written as Eq.(2.26). The resistance relation can be derived based on Eq.(2.6) and Eq.(2.26) as Eq.(2.27).

$$I_{L2}{}^2 R_{acL} = \frac{V_s^2}{R_{eq}} \tag{2.26}$$

$$R_{eq} = \frac{\pi^2}{8} \frac{\omega_0^2 M^2}{R_{acL}} \tag{2.27}$$

Then Eq.(2.17) has given the relation between DC load resistance and AC load resistance, the equivalent load resistance can be derived by combining the equations as Eq.(2.28). Up to now, an equivalent DC load resistance seen from the voltage source can be determined once the real DC load resistance is selected for the designed WPT system. For the selected optimal load to get maximum efficiency, the equivalent load will be 35.5 Ω.

$$R_{eq} = \frac{\pi^4}{64} \times \frac{\omega_0^2 M^2}{R_L} = 35.5\ \Omega \tag{2.28}$$

3

Front buck converter design

In this chapter, DC/DC converter will be applied and studied for the voltage regulation of the WPT system. Yu et al., 2021 has studied the application of a back-end boost converter to regulate the output voltage. In this chapter, a front-end buck converter will be designed as Fig.3.1. Normal single-phase buck converters with Continuous Conduction Mode (CCM) have poor performance on efficiency due to large switching losses, especially in high power and high-frequency applications.

The use of Wide Band Gap (WBG) semiconductors, especially Silicon Carbide SiC MOSFETs, allows the operation of power converters at high voltage and high switching frequency with high efficiency according to the research from Millan et al., 2013. SiC MOSFETs working in Zero Voltage Switching (ZVS) can be used to improve the efficiency in a synchronous buck converter by introducing the Triangular Current Mode (TCM). TCM requires a minimum negative inductor current to ensure ZVS operation, which will be studied and designed in detail. Though switching losses can be avoided by TCM, it will cause a high current ripple, increasing conduction losses, especially at full load. Multi-phase typologies have the potential to reduce the large current ripple. To figure out the advantages and disadvantages of the mentioned buck converter solutions, a comparative study will be made in the following subsections.

3.1. Single phase buck converter

In this subsection, a single-phase buck converter will be designed to meet the voltage regulation requirement as Fig.3.2. According to the SAE J2954 standard and the definition of the studied WPT system, the output voltage of the buck converter V_o should cover a range given by Eq.(3.1).

$$100\ \text{V} \leq V_o \leq 400\ \text{V} \tag{3.1}$$

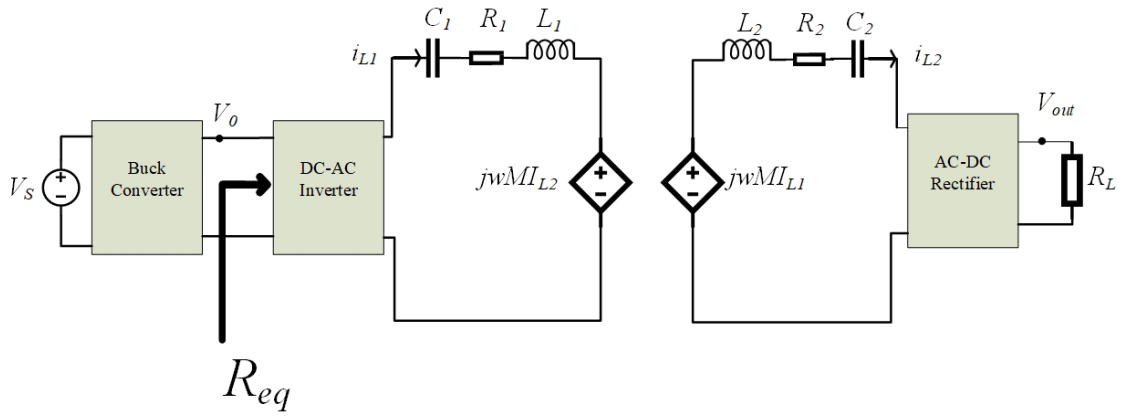

Figure 3.1: Front buck converter WPT structure

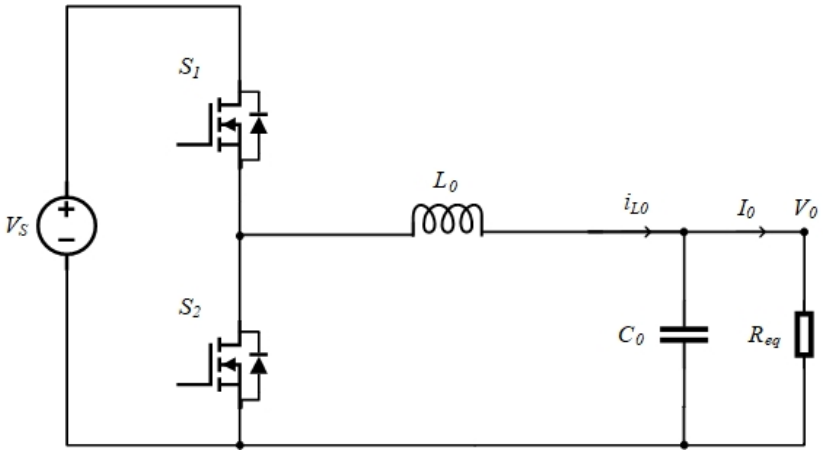

Figure 3.2: Single phase buck converter structure

The Buck converter output voltage can be determined by the duty cycle D and input voltage V_s as Eq.(3.2). Thus the buck converter will be analyzed with the duty cycle from 0.2 to 0.8.

$$V_o = DV_S \tag{3.2}$$

Millan et al., 2013 suggest the advantages of using SiC MOSFETs as switches in high frequency and high power cases. Thus in this thesis, the SiC MOSFET G3R75MT12J is selected due to its low drain to source resistance and high switching speeds. Then the inductor L_0, capacitor C_0 and switching frequency f_s should be designed. The three mentioned parameters will determine the performance of the designed buck converter including power losses, current ripple and output voltage ripple. So the remained parameters should be delicately considered to achieve better performance. The methodologies of deciding the switching frequency and inductor are to find an optimal combination, where the system has minimal power loss and is easy to be built. So in the following design, semiconductor losses will be derived to help decide the system parameters.

3.1.1. CCM Operation mode

The buck converter is designed to work in Continuous Conduction Mode CCM in this part. Its key advantage is the low current ripple, resulting in low conduction losses while high-switching losses are the main drawback. In hard-switched CCM mode, the inductor current is always larger than zero. The inductor current ripple can be written as Eq.(3.3).

$$\Delta I_L = \frac{V_S - V_o}{L_0} DT_s = \frac{D(1-D)}{L_0} T_s V_s \tag{3.3}$$

where the L_0 is the inductance and T_s is the switching period of one duty cycle. Based on the equation of inductor current ripple, the peak inductor current I_P and the valley inductor current I_V can be given as Eq.(3.5) and Eq.(3.6). The average output current I_0 can be given as Eq.(3.4).

$$I_0 = \frac{DV_s}{R_{eq}} \tag{3.4}$$

$$I_P = I_0 + \frac{\Delta I_L}{2} \tag{3.5}$$

$$I_V = I_0 - \frac{\Delta I_L}{2} \tag{3.6}$$

The sources of losses taken into consideration in this paper are the MOSFET channel conduction losses, MOSFET switching losses, body diode conduction losses and body diode reverse recovery losses. Inductor losses are not concluded in this losses calculation due to their much smaller amount compared with the semiconductor losses according to the research of Yu et al., 2021.

- `MOSFET conduction losses`

  MOSFETS conduction losses are shared by the two switches S1 and S2, which can be given by Eq.(3.7)

$$P_{CON} = I_{rms}^2 \times R_{ON} = \left[I_O^2 + \frac{(I_P - I_V)^2}{12} \right] \times R_{ON} \tag{3.7}$$

  where P_{CON} is the MOSFET channel conduction loss, I_{rms} represents the RMS current going through the MOSFETS and R_{ON} represents the MOSFET on-state resistance, which can be found on the datasheet of SiC MOSFET G3R75MT12J.

- `MOSFET switching losses`

  In hard-switched CCM, the MOSFET S1 will generate losses during its turn-ons and turn-offs. MOSFET S2 is able to turn on at ZVS due to the inductor current passing through body diode D2. MOSFET S2 has no turn-off losses as a result of channel current shifting to the body diode. In order to calculate the switching loss, Hayes and Goodarzi, 2018 proposed a reasonable assumption to scale the switching loss below as described by Eq.(3.8).

$$P_{sw} = f_s E_{on+off} \left(\frac{I_{ds}}{I_{ref}} \right)^{K_i} \left(\frac{V_{ds}}{V_{ref}} \right)^{K_v} \tag{3.8}$$

  Where E_{on+off} represents MOSFET one-time turn-on energy and turn-off energy, I_{ref} and V_{ref} are the reference current and voltage, I_{ds} is the drain current and V_{ds} is the drain-source voltage, K_i and K_v are the scaling coefficients. Turn-on and Turn-off energy are not constant value when different drain current flows through the MOSFET at the switching time. The datasheet of SiC MOSFET G3R75MT12J concludes the switching energy curve vs. drain to source current at a certain reference voltage and gate resistance as Fig.3.3. An editable datasheet in MATLAB file format can be plotted as Fig.3.4 by applying the MATLAB grab it toolbox.

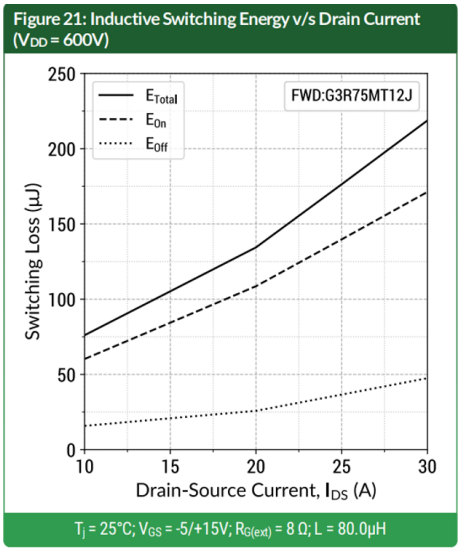

Figure 3.3: Switching loss of SiC MOSFET G3R75MT12J from datasheet

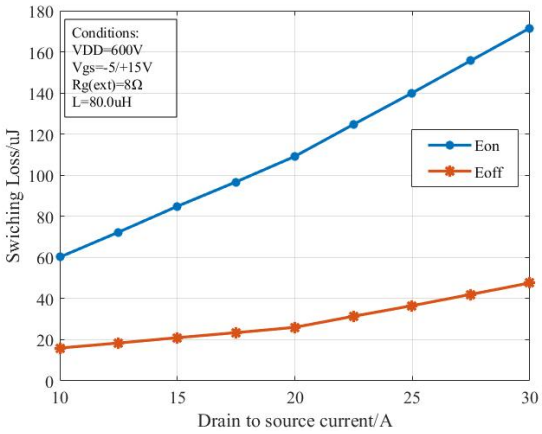

Figure 3.4: Reploted Switching loss datasheet

To figure out the coefficients in Eq.(3.8), a second-order polynomial could be applied to get the expression of switching energy at the different drains to source current using the MATLAB calibration toolbox. The result of calibration is written as Eq.(3.9) and Eq.(3.10).

$$E_{on}\,(I_{ds}) = 0.06542 I_{ds}^2 + 2.984 I_{ds} + 25.36\ \mu\text{J} \tag{3.9}$$

$$E_{off}\,(I_{ds}) = 0.05462 I_{ds}^2 - 0.589 I_{ds} + 17.66\ \mu\text{J} \tag{3.10}$$

Based on the relation between single-time switching energy at the different drains to source currents, the switching loss scaling equation can be reorganized. During the turn-on period, the drain to source current through S1 equals the valley inductor current as Eq.(3.6) and equals the peak inductor current as Eq.(3.5) when S1 is in the turn-off period. Thus the switching losses could be calculated as Eq.(3.11).

$$P_{S_{1\_}sw} = \frac{V_S}{V_{ref}} E_{on}\left(\mathrm{I}_V\right) f_s + \frac{V_S}{V_{ref}} E_{off}\left(I_P\right) f_s \tag{3.11}$$

where $P_{S_{1\_}sw}$ is the overall switching loss of S1.

- `Body diode conduction losses`

  In hard switching CCM, the body diode D2 of the lower MOSFET will conduct during the dead time when both MOSFET are turned off as Fig.3.2. D2 will conduct twice in one duty cycle, first after S1 turn off conducting the peak inductor current and second after S2 turn off conducting the valley inductor current. So the body diode conduction losses can be concluded as Eq.(3.12).

$$P_{D_{2\_}con} = V_F\left(I_P + I_V\right) t_{dead} f_s \tag{3.12}$$

  where $P_{D_{2\_}con}$ is the body diode conduction losses, t_{dead} is the dead time between gate pulses and V_F is the diode forward conduction voltage, which can be found on the datasheet of SiC MOSFET G3R75MT12J.

- `Body diode switching losses`

  In this operation mode, the body diode D2 will have the reverse recovery loss when S2 turn off and S1 turn on. This loss can be calculated as Eq.(3.13).

$$P_{D_{2\_}rr} = Q_{rr} V_S f_s \tag{3.13}$$

  where $P_{D_{2\_}rr}$ is the body diode reverse recovery losses, Q_{rr} is the body diode reverse recovery charge which can be found on the datasheet of SiC MOSFET G3R75MT12J.

To decide the remaining parameters, a trade-off on the converter performance should be considered. A higher switching frequency will lead to a more compact design with smaller passive components while the switching loss will be higher. The optimal combination of inductor and switching frequency can be decided based on the constraint conditions in CCM and reasonable semiconductor losses. As for the converter working in CCM, the peak inductor current should be lower than the SiC MOSFET maximum continuous forward current and the valley inductor current should be higher than zero to keep continuous conduction. These conditions are given as Eq.(3.14) and Eq.(3.15).

$$I_P = I_o + \frac{\Delta I_L}{2} < I_{D\max} \tag{3.14}$$

$$I_V = I_o - \frac{\Delta I_L}{2} > 0A \tag{3.15}$$

According to Eq.(3.3), the largest current ripple will flow through the circuit when the duty cycle is 0.5, where the current ripple sweeping and semiconductor losses sweeping are conducted as Fig.3.5 and Fig.3.6. The sweeping analysis is based on the working condition delivering half power, where the inductor current has its maximum value. The reason why to analyse the parameters at a half-duty cycle is the boundary conduction condition given as Eq.(3.16).

$$I_{LB,\max} = \frac{T_S V_S}{8L} \tag{3.16}$$

where $I_{LB,\max}$ is the maximum inductor current to keep the buck working in BCM, where the duty cycle is 0.5.

Fig.3.5 and Fig.3.6 indicate that a larger inductance results in a smaller current ripple, however, the size of the inductor will also become larger. Taking the constraint condition of the inductor current

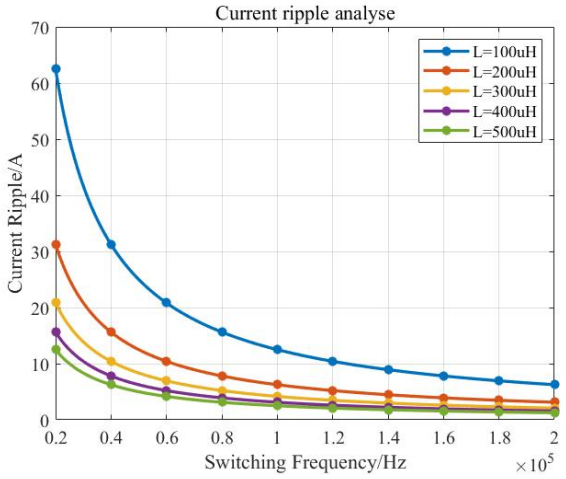

Figure 3.5: Single phase buck CCM inductor current ripple sweeping

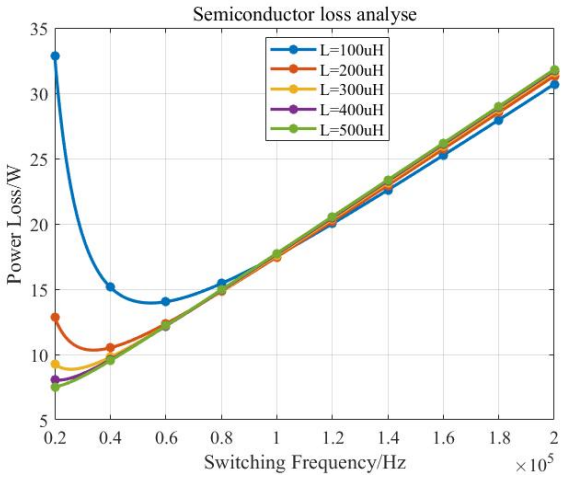

Figure 3.6: Single phase buck CCM semiconductor losses sweeping

ripple Eq.(3.14) and Eq.(3.15) into account, the optimal inductor and frequency value can be decided according to the concluded result. The inductor and switching frequency for single buck CCM should be designed to remain enough margin for keeping in CCM and minimize the semiconductor losses. So the parameters in this scenario are determined according to the analysis. Then the inductance L is 200 uH and the switching frequency is 100 kHz.

Fig.3.7 and Fig.3.8 show the simulation results of the designed buck converter in CCM at the minimum output power with an output voltage of 100 V and maximum output power with an output voltage of 400 V.

3.1.2. TCM Operation mode

In this part, the converter design, especially the inductance value selection will be studied in detail based on the current ripple analysis and loss analysis. Triangular Current Mode (TCM) is proposed to enable the MOSFET S1 turn-on at ZVS by keeping the inductor current negative at the moment of valley inductor current as Fig.3.9 demonstrated.

Rogina et al., 2019 suggested TCM enhances the efficiency of the converter at low power thanks to ZVS soft-switching operation, but it requires variable switching frequency and large current ripple through the inductor. J. Zhang et al., 2007 indicates that fixed valley negative current operation will have smaller current ripple and smaller RMS inductor current compared with fixed frequency operation to keep the circuits working in TCM.

During the dead time t_{dead}, the negative inductor current I_V will flow to S1, discharging the stray capacitance or output capacitance C_{oss} of S1 and charging S2. Only when the capacitance is completely charged will S1 realize ZVS turn on. Thus, the absolute value of I_V should be large enough to ensure ZVS, which can be calculated as Eq.(3.17).

$$|I_V| \geq 2C_{oss}\frac{\Delta V_{IN}}{\Delta t_{dead}} \tag{3.17}$$

C_{oss} can be found from the datasheet of SiC MOSFET G3R75MT12J. t_{dead} is the dead time between two gate pulses, which is set to 100 ns to avoid a short circuit based on the rise and fall time of SiC MOSFET G3R75MT12J. Then the I_V can be set to -2 A with some margin to ensure ZVS.

Based on a constant negative current, the frequency will change with different output voltages. The product of inductance and frequency can be derived from Eq.(3.3) and Eq.(3.4) and concluded as

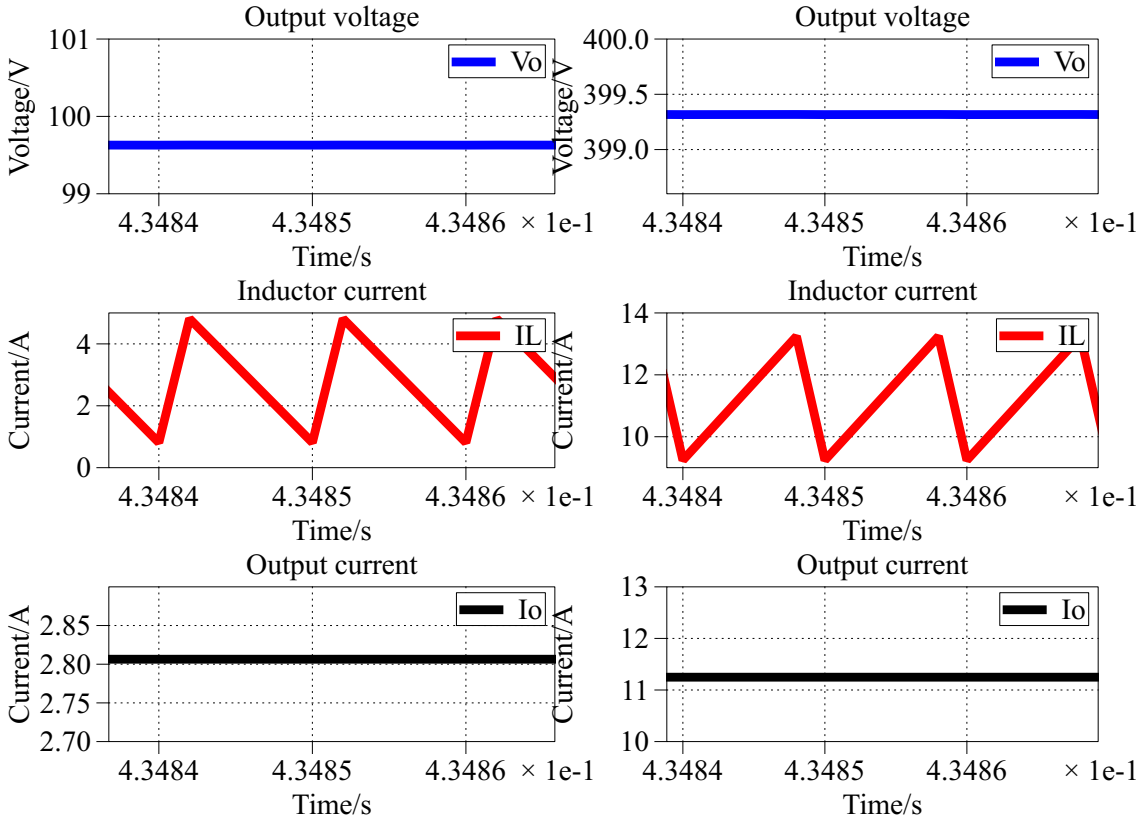

Figure 3.7: Simulation waveforms for designed single phase CCM scenario charging on 100 V, 282 W

Figure 3.8: Simulation waveforms for designed single phase CCM scenario charging on 400 V, 4500 W

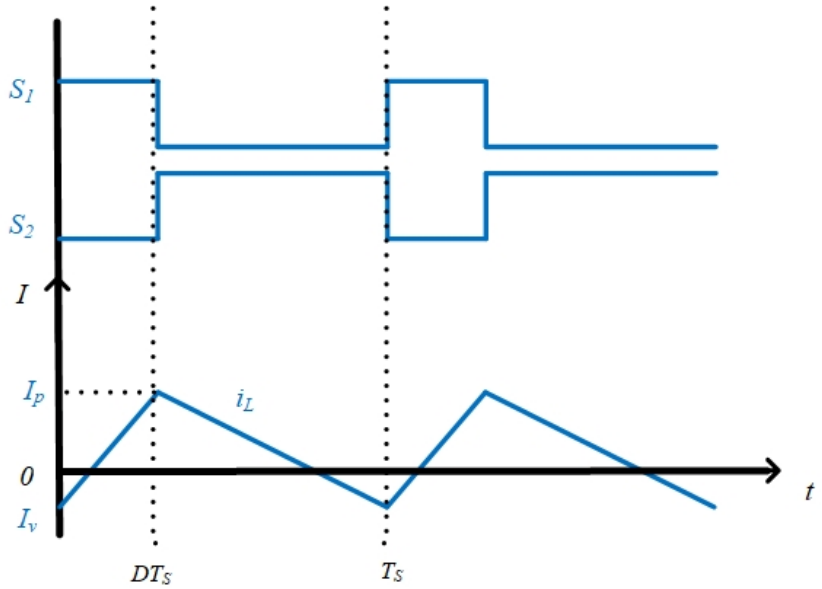

Figure 3.9: Single phase buck inductor current waveform

Eq.(3.18).

$$Lf_{\mathrm{s}} = \frac{R_{eq}V_sD - R_{eq}V_sD^2}{2V_sD - 2R_{eq}I_V} \tag{3.18}$$

The inductance will be determined under the condition of Eq.(3.18). The range of switching frequency should follow the output voltage range and should be not too low or too high. A low switching frequency under 20 kHz will generate noise while a high switching frequency will make the circuit difficult to build. Then a proper inductance should be designed with the consideration of frequency range and power loss.

The power loss of the single-phase buck converter TCM will be analyzed in the following derivation. In the TCM, MOSFET S1 has ZVS turn-on and only the turn-off loss should be calculated. Since the negative current I_V would not flow through the body diode D2 when S2 turns off, so the turn-off losses of S2 should be taken into consideration in this operation mode. There is no body diode D2 reverse recovery loss since no current flow through it during dead time. The channel conduction losses and body diode conduction losses will be similar to Eq.(3.7) and Eq.(3.12).

- `MOSFET channel conduction losses`

  The channel conduction losses are the same as Eq.(3.7).

- `Body diode conduction losses`

  The body diode conduction losses will be calculated similarly to Eq.(3.12).

- `MOSFET switching losses`

  Based on the switching pattern analysis, during the S1 turn-off period, the drain to source current through S1 equals the peak inductor current. During the S2 turn-off period, the drain to source current through S2 equals the absolute value of valley inductor current. According to the single time switching loss Eq.(3.9) and Eq.(3.10), the switching losses could be calculated as Eq.(3.19) and Eq.(3.20).

$$P_{S_{1\_}sw} = \frac{V_s}{V_{ref}} E_{off}\left(I_P\right) f_s \tag{3.19}$$

$$P_{S_{2\_}sw} = \frac{V_s}{V_{\mathrm{ref}}} E_{off}\left(|I_V|\right) f_s \tag{3.20}$$

  where $P_{S_{1\_}sw}$ is the overall switching loss of S1 and $P_{S_{2\_}sw}$ is the overall switching loss of S2.

A proper inductance could be found according to the switching frequency sweeping and semiconductor losses sweeping and they are conducted as Fig.3.10 and Fig.3.11.

Since the frequency should be higher than 20 kHz to avoid noise, the inductance could be decided with the lowest power loss and most reasonable frequency range in the whole voltage regulation range. Then the inductance in this scenario is designed to 140 uH.

Fig.3.12 and Fig.3.13 show the simulation results of the designed buck converter in TCM at the minimum output power with the output voltage of 100 V and maximum output power with the output voltage of 400 V.

3.2. Two-phase interleaved buck converter

The design of a single-phase buck converter has a concise structure and fewer components, while the current stress on both semiconductor switches and passive elements is high according to the former current ripple analysis as Fig.3.5. Additional design margin should be remained for the possible high current through switching devices especially when the load is heavy. In order to relieve the current stress, a two-phase interleaved buck converter is proposed and designed in this subsection. The

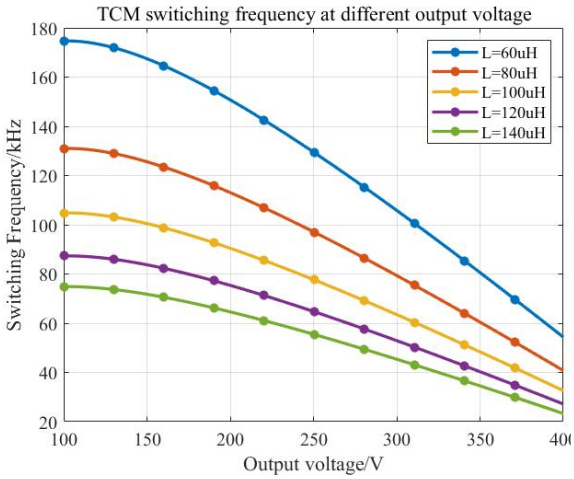

Figure 3.10: Single phase buck TCM switching frequency sweeping

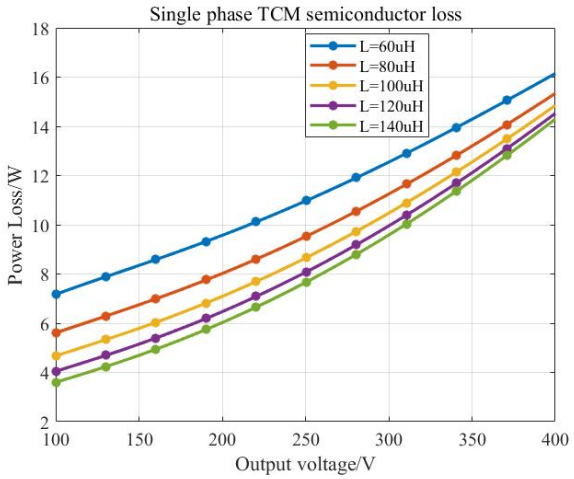

Figure 3.11: Single phase buck TCM semiconductor losses sweeping

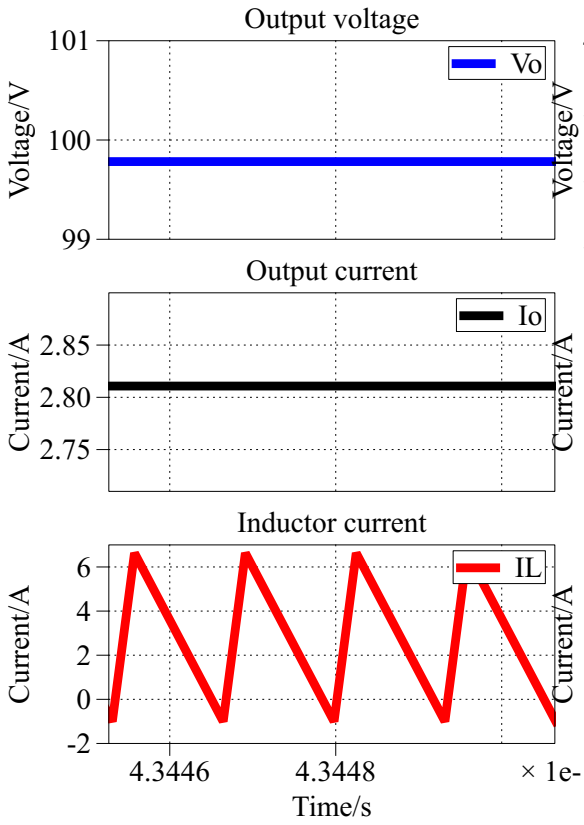

Figure 3.12: Simulation waveforms for designed single phase TCM scenario charging on 100 V, 282 W

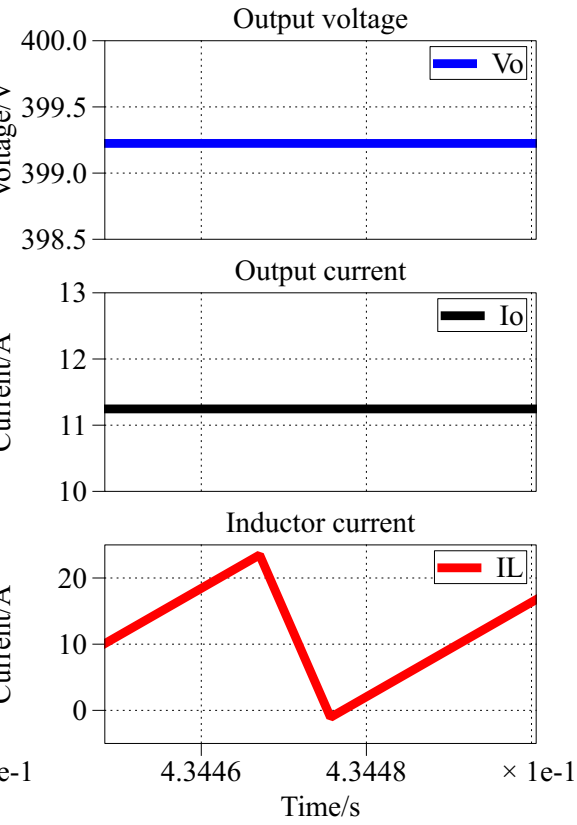

Figure 3.13: Simulation waveforms for designed single phase TCM scenario charging on 400 V, 4500 W

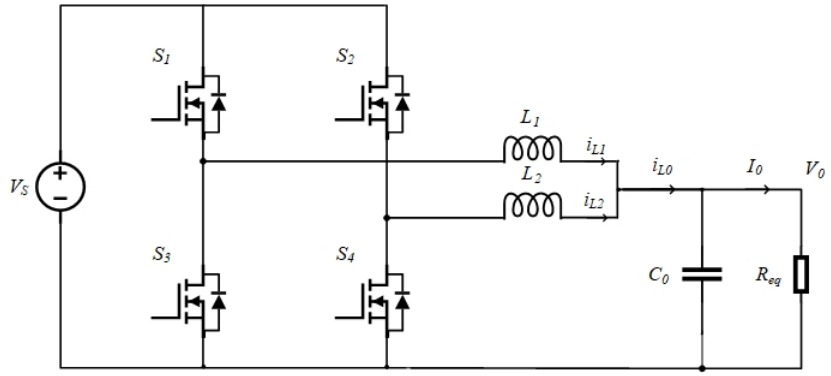

Figure 3.14: Two-phase interleaved buck converter structure

circuits of two-phase interleaved buck are shown in Fig.3.14. Lee et al., 2013 indicated the two-phase interleaved buck converter can also reduce the output current ripple. The following section will study the two-phase interleaved converter in detail.

3.2.1. CCM Operation mode

For a two-phase buck converter, the gate pulses of the two half-bridges will be phase-shifted by 180 degrees. Compared with single-phase CCM operation, the derivation of single-phase inductor current is similar while the output current is different. The relation between phase current and output current should be derived when the buck duty cycle is smaller than 0.5 and larger than 0.5 specifically.

- `Duty cycle D=0.5`

  When the duty cycle is 0.5, the current ripple of the two-phase inductor will eliminate each other. So the overall output current ripple is zero.

- `Duty cycle D<0.5`

  Fig.3.15 demonstrates the gate pulse signal of four switches and L_1 inductor current i_{L_1}, L_2 inductor current i_{L_2} and total inductor current i_{L_0}. Since the two phases are symmetrical, inductor L_1 and L_2 have the same inductance L in the following derivation. The inductor current ripple is given as Eq.(3.3), peak current Eq.(3.5) and valley current Eq.(3.6). Then the upper phase current is given as Eq.(3.21), the lower phase current as Eq.(3.22).

$$\begin{aligned} i_{L_1} &= I_V + \frac{V_o}{L}\left(\frac{1}{D} - 1\right)t \quad 0 \le t \le DT_S \\ i_{L_1} &= I_P - \frac{V_o}{L}(t - DT_S) \quad DT_S \le t \le T_S \end{aligned} \tag{3.21}$$

$$\begin{aligned} i_{L_2} &= I_P - \frac{V_o}{L}(t + 0.5T_S - DT_S) \quad 0 \le t \le 0.5T_S \\ i_{L_2} &= I_V + \frac{V_o}{L}\left(\frac{1}{D} - 1\right)(t - 0.5T_S) \quad 0.5T_S \le t \le (D + 0.5)T_S \\ i_{L_2} &= I_P - \frac{V_o}{L}(t - DT_S - 0.5T_S) \quad (D + 0.5)T_S \le t \le T_S \end{aligned} \tag{3.22}$$

The total inductor current i_{L_0} can be derived by concluding Eq.(3.21) and Eq.(3.23) together. So the total inductor current ripple can be figured out as Eq.(3.25).

$$\begin{aligned} I_V &= \frac{I_0}{2} - \frac{\Delta I_L}{2} \\ I_P &= \frac{I_0}{2} + \frac{\Delta I_L}{2} \end{aligned} \tag{3.23}$$

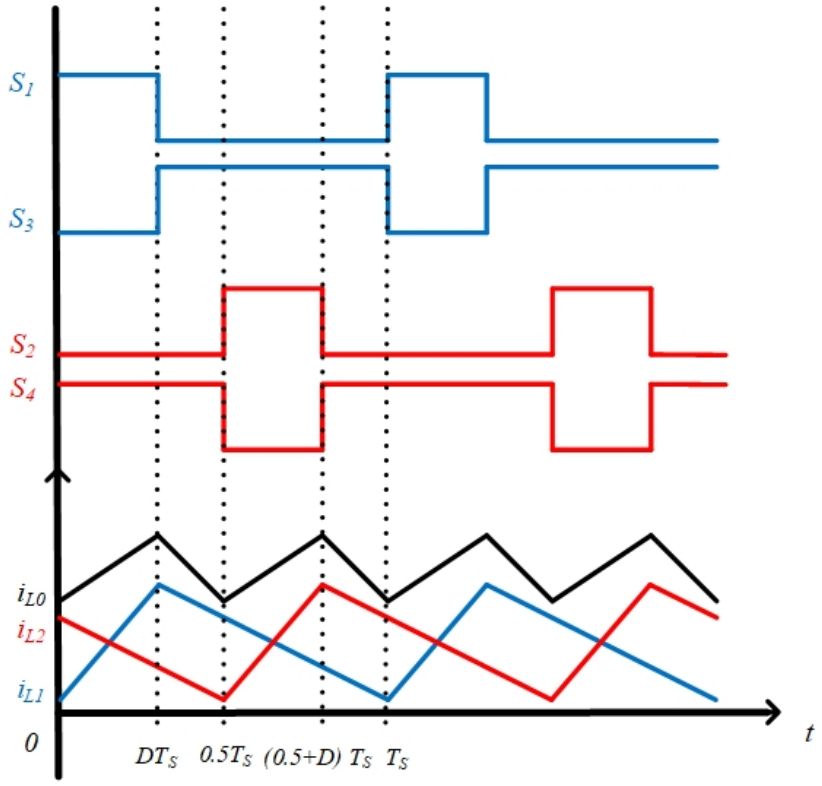

Figure 3.15: Two-phase interleaved buck converter inductor current waveform when D<0.5 in CCM

$$\begin{aligned} i_{L_o} &= I_o + \left(\frac{1}{D} - 2\right)\frac{V_o}{L}t - (0.5 - D)\frac{V_o}{L}T_S \quad 0 \le t \le DT_S \\ i_{L_o} &= I_o - \frac{2V_o}{L}t + (0.5 + D)\frac{V_o}{L}T_S \quad DT_S \le t \le 0.5T_S \end{aligned} \tag{3.24}$$

$$\Delta i_{L_o} = \frac{V_o}{L}(1 - 2D)T_s \tag{3.25}$$

- `Duty cycle D>0.5`

  Fig.3.16 demonstrates the waveform when the duty cycle is larger than 0.5. Total inductor current could be derived similarly as Eq.(3.26), and the total inductor current ripple can be figured out as Eq.(3.27).

$$\begin{aligned} i_{L_o} &= 2I_o + \left(\frac{2}{D} - 2\right)\frac{V_o}{L}t + \left(\frac{1}{2D} - \frac{3}{2} + D\right)\frac{V_o}{L}T_S \quad 0 \le t \le (D - 0.5)T_S \\ i_{L_o} &= I_0 + \left(\frac{1}{D} - 2\right)\frac{V_0}{L}t - \left(\frac{1}{2} - D\right)\frac{V_0}{L}T_S \quad (D - 0.5)T_S \le t \le 0.5T_S \end{aligned} \tag{3.26}$$

$$\Delta i_{L_o} = \frac{V_o}{L}\left(3 - 2D - \frac{1}{D}\right)T_s \tag{3.27}$$

The single phase inductor current ripple Eq.(3.3) is compared with the two-phase total inductor current ripple Eq.(3.25) and Eq.(3.27), the results can be concluded as Eq.(3.28).

$$\begin{aligned} \frac{\Delta i_{L_o,\,\text{two-phase}}}{\Delta i_{L_o,\,\text{single-phase}}} &= \frac{1 - 2D}{1 - D} \quad D < 0.5 \\ \frac{\Delta i_{L_o,\,\text{two-phase}}}{\Delta i_{L_o,\,\text{single-phase}}} &= \frac{2D - 1}{D} \quad D \ge 0.5 \end{aligned} \tag{3.28}$$

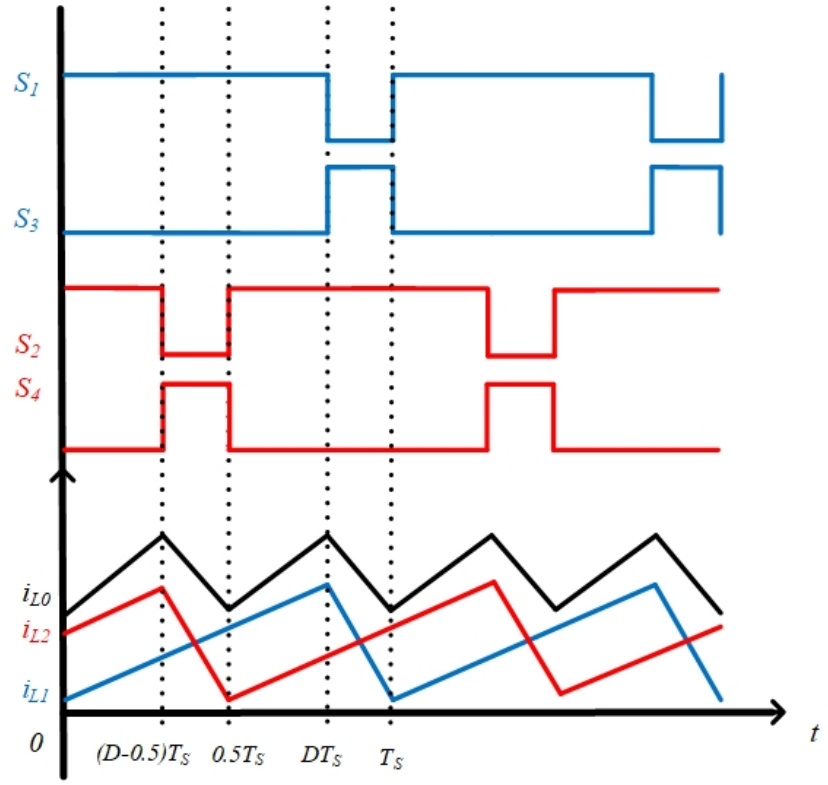

Figure 3.16: Two-phase interleaved buck converter inductor current waveform when D≥0.5 in CCM

Eq.(3.28) shows that a two-phase interleaved structure has a significantly reduced output current ripple compared to that of a single-phase structure shown as Fig.3.17. The stress on single-phase current could also be reduced since only half of the average output current will flow through.

Then the inductance and switching frequency should be designed with the consideration of the conditions of CCM and the requirements of less power loss. The single-phase current ripple should be designed according to Eq.(3.29) and Eq.(3.30).

$$I_{P,\text{ single-phase}} = \frac{I_0}{2} + \frac{\Delta I_{L,\text{ single-phase}}}{2} < I_{D\max} \tag{3.29}$$

$$I_{V,\text{ single-phase}} = \frac{I_0}{2} - \frac{\Delta I_{L,\text{ single-phase}}}{2} > 0A \tag{3.30}$$

The power loss calculation of the two-phase interleaved buck converter is similar to the single-phase buck converter. The semiconductor losses can be calculated as Eq.(3.7), Eq.(3.11), Eq.(3.12), Eq.(3.13) and Eq.(3.11) by replacing the current and voltage value. Then the single-phase current ripple sweeping and semiconductor losses sweeping are given by Fig.3.18 and Fig.3.19.

According to Eq.(3.30) and Eq.(3.16), the single-phase current ripple can not exceed 7A to keep the boundary condition of CCM, which constrains the inductance design and switching frequency selection significantly. In order to remain enough margin for the design safety, the performance on power loss should be satisfied in this case. The optimal parameters are given based on the calculations and trade-offs. According to the analysis above, the phase inductor L should be 300 uH and the switching frequency should be 100 kHz.

Fig.3.20 and Fig.3.21 show the simulation results of the designed buck converter in CCM at the minimum output power with an output voltage of 100 V and maximum output power with an output voltage of 400 V.

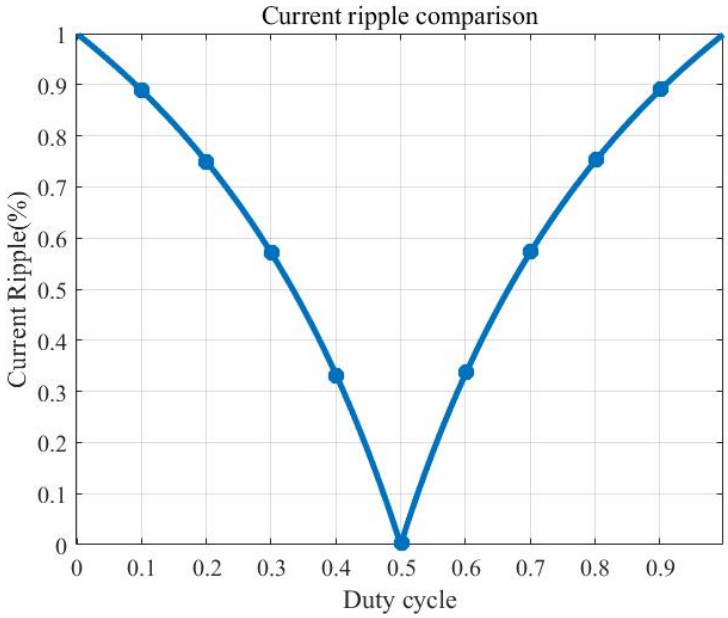

Figure 3.17: The current ripple reduction ratio of the two-phase interleaved output current ripple divided by the single-phase output current ripple

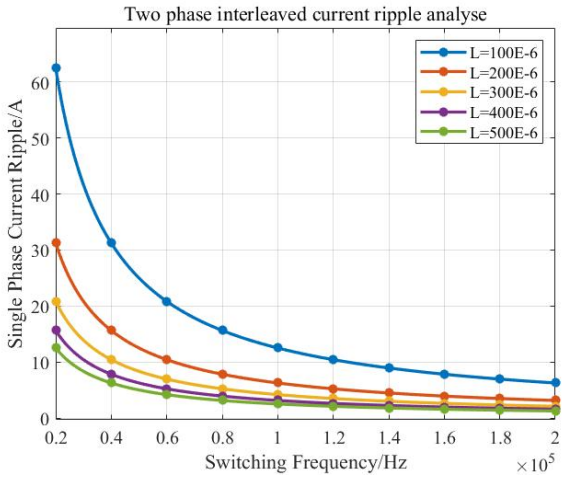

Figure 3.18: Analyses of inductor current ripple with the frequency of a two-phase interleaved buck converter operating at hard-switched CCM.

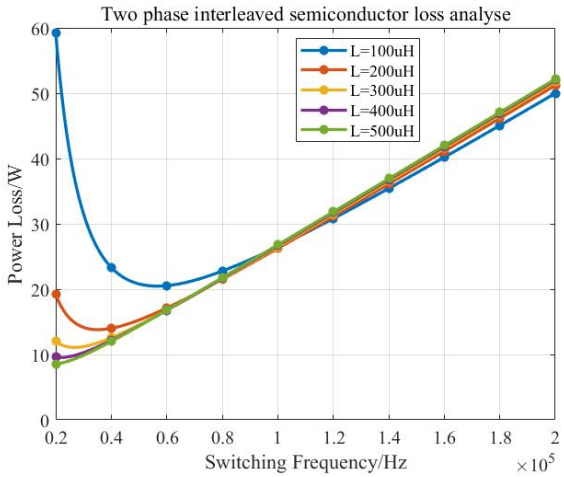

Figure 3.19: Two-phase interleaved CCM semiconductor losses sweeping

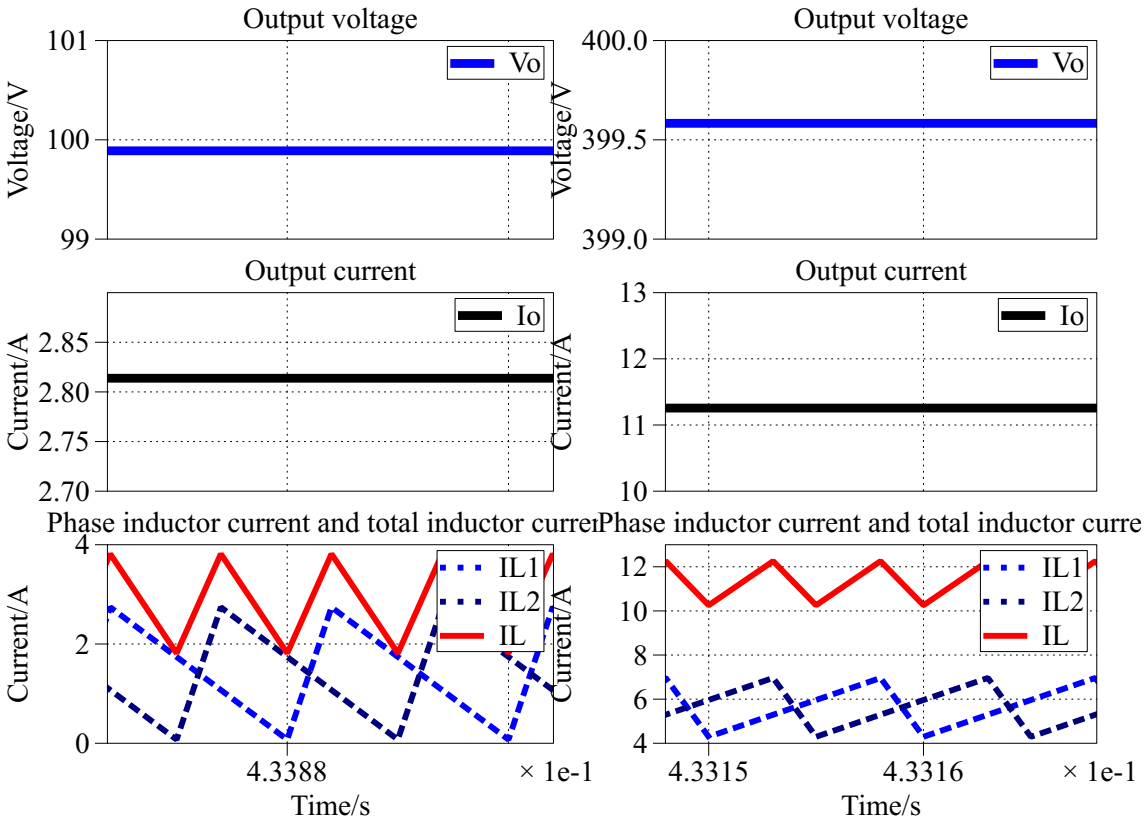

Figure 3.20: Simulation waveforms for designed two-phase interleaved CCM scenario charging on 100 V, 282 W

Figure 3.21: Simulation waveforms for designed two-phase interleaved CCM scenario charging on 400 V, 4500 W

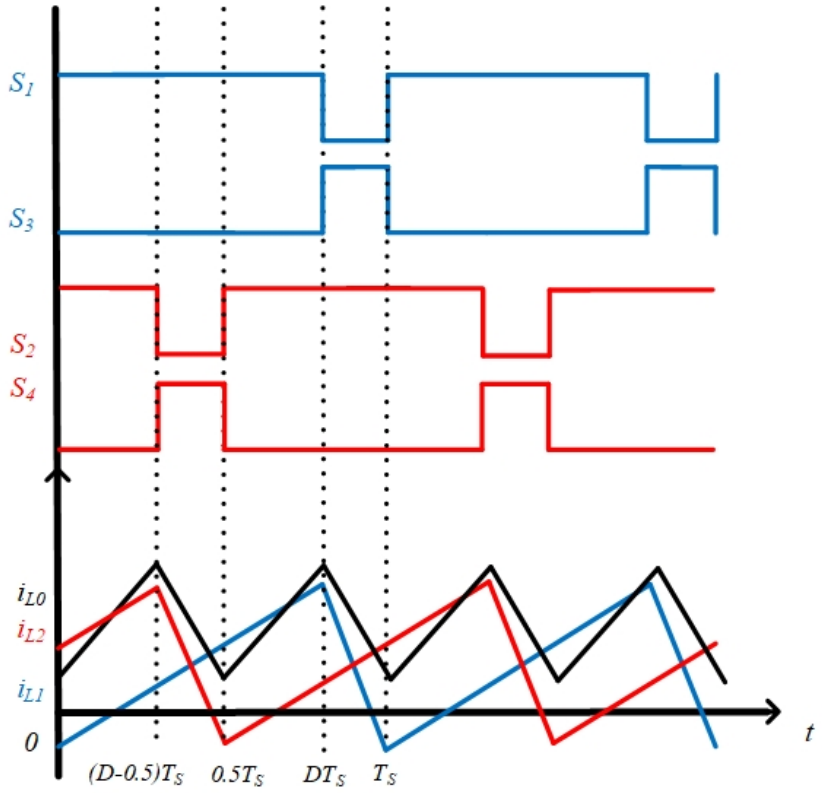

Figure 3.22: Two-phase interleaved buck converter inductor current waveform when D≥0.5 in TCM

3.2.2. TCM Operation mode

The adoption of a two-phase interleaved buck converter reduces the current stress on switching devices and the output current ripple significantly. In the single-phase TCM design, the current ripple is large and the current stress is heavy. Thus the application of a two-phase interleaved structure in TCM will solve this problem and remain enough design margin to maximize efficiency. The waveform of phase inductor current and total inductor current is shown as Fig.3.22 for duty cycle larger than 0.5. The conditions for the converter to work in TCM are derived in a similar way as the methodologies in single-phase cases. The constraint condition is updated as Eq.(3.31).

$$Lf_{\mathrm{s}} = \frac{R_{eq}V_sD - R_{eq}V_sD^2}{V_sD - 2R_{eq}I_{V,\text{ single-phase}}} \tag{3.31}$$

where the phase currents are updated as Eq.(3.29) and Eq.(3.30).

Similarly, the semiconductor losses for two-phase interleaved TCM can be derived according to Eq.(3.7), Eq.(3.12), Eq.(3.19) and Eq.(3.20) with updating single phase current and double the single phase losses. The working frequency sweeping and power loss sweeping are concluded as Fig.3.23 and Fig.3.24.

Fig.3.23 indicates that a higher switching frequency is needed compared with single-phase cases to support the full range voltage regulation. Fig.3.24 shows the power loss is reduced significantly compared with two-phase CCM. Finding optimal inductance enabling a reasonable switching frequency range and the least semiconductor losses will be possible. According to the analysis above, the phase inductance is designed to 210 uH.

Fig.3.25 and Fig.3.26 show the simulation results of the designed buck converter in TCM at the minimum output power with an output voltage of 100 V and maximum output power with an output voltage of 400 V.

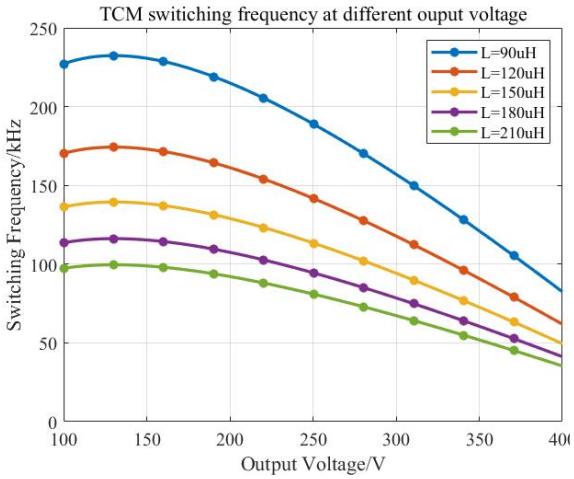

Figure 3.23: Two-phase interleaved buck TCM switching frequency sweeping

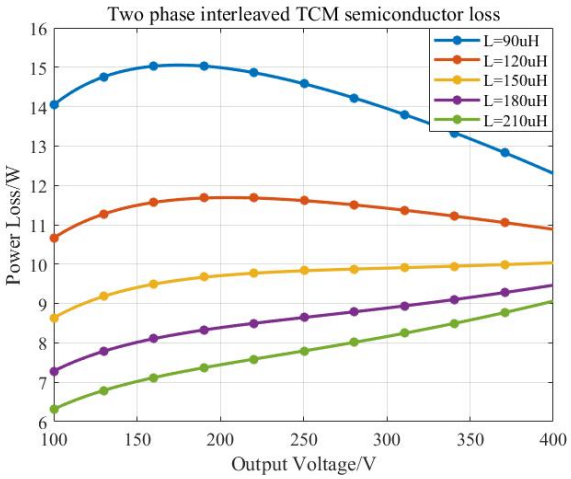

Figure 3.24: Two-phase interleaved buck TCM semiconductor losses sweeping

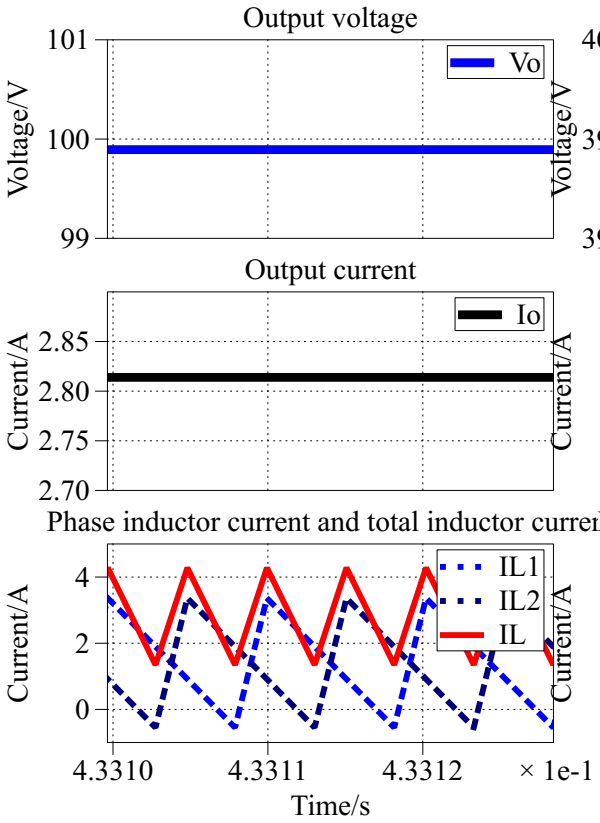

Figure 3.25: Simulation waveforms for designed two-phase interleaved TCM scenario charging on 100 V, 282 W

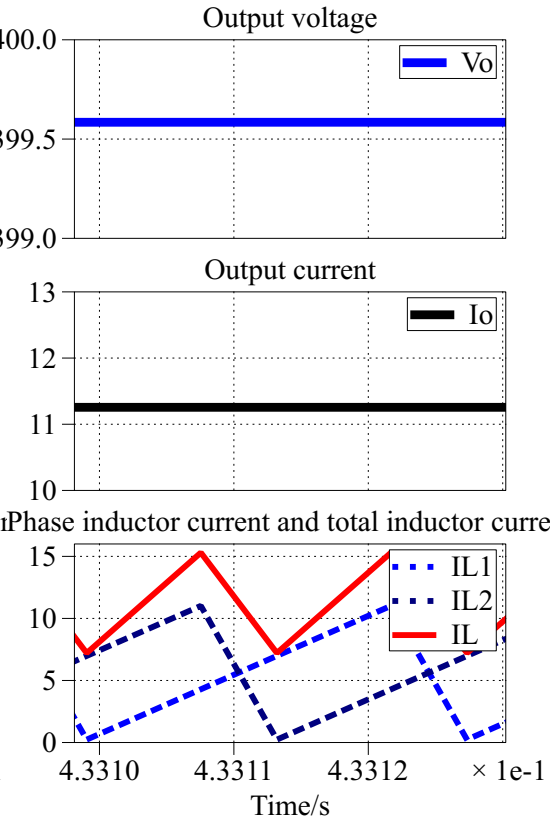

Figure 3.26: Simulation waveforms for designed two-phase interleaved TCM scenario charging on 400 V, 4500 W

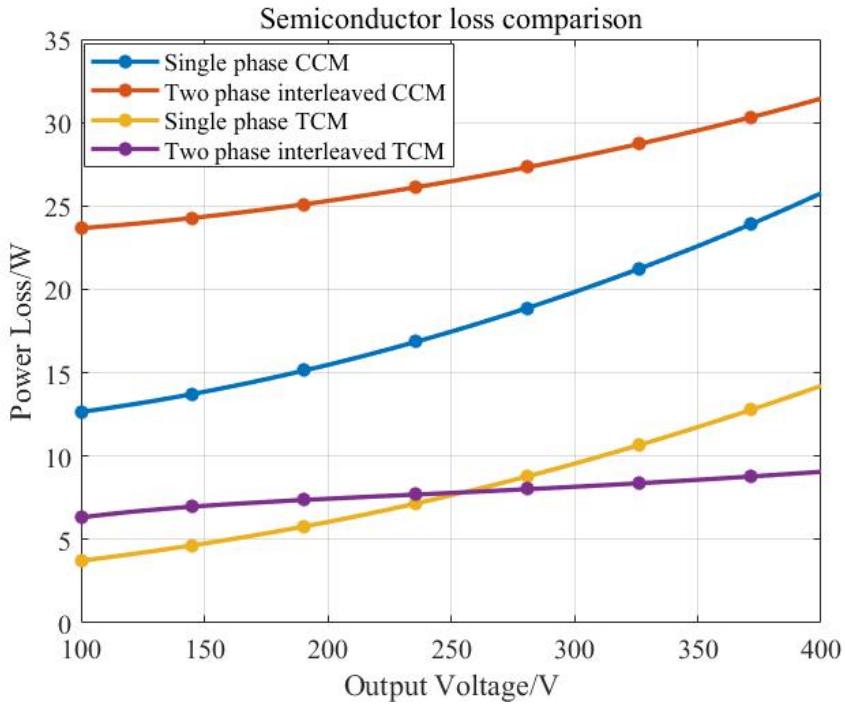

Figure 3.27: Semiconductor losses comparison

3.3. Design evaluation

Four scenarios of WPT buck converters are designed and analyzed in this section.

The semiconductor losses are compared as Fig.3.27. The implementation of TCM reduces semiconductor losses significantly. Both single-phase and two-phase TCM have less than half of the losses as CCM. While the TCM operation has superior performance on power loss, the penalty is its large current ripple.

The output current ripples are compared as Fig.3.28. It is obvious that a single-phase buck converter working in TCM will bring a huge current ripple, which will not only increase the current stress of switching devices significantly but also increase the output current ripple. Large current ripple will bring safety issues and result in choosing larger passive elements, making the circuits not compact. The solution of a two-phase interleaved structure overcomes this problem perfectly, reducing the current ripple over 2 times at least.

In order to further compare the performances of the four scenarios, the overall system efficiency at different power levels should be calculated. The losses of the designed system consist of two parts. One part is the semiconductor losses and the other part is the coil resistance losses. The coil resistance losses are generated by the primary circuit current I_{L1} going through primary coil resistance R_1 and the secondary circuit current I_{L2} going through secondary coil resistance R_2. The derivations of the resistance losses are given by Eq.(2.14), Eq.(2.15), Eq.(3.32) and Eq.(3.33).

$$P_{Rloss1} = {I_{L1}}^2 * R_1 \tag{3.32}$$

$$P_{Rloss2} = {I_{L2}}^2 * R_2 \tag{3.33}$$

where P_{Rloss1} is the primary coil resistance loss and P_{Rloss2} is the secondary coil resistance loss. Then the system efficiency could be calculated as Eq.(3.35).

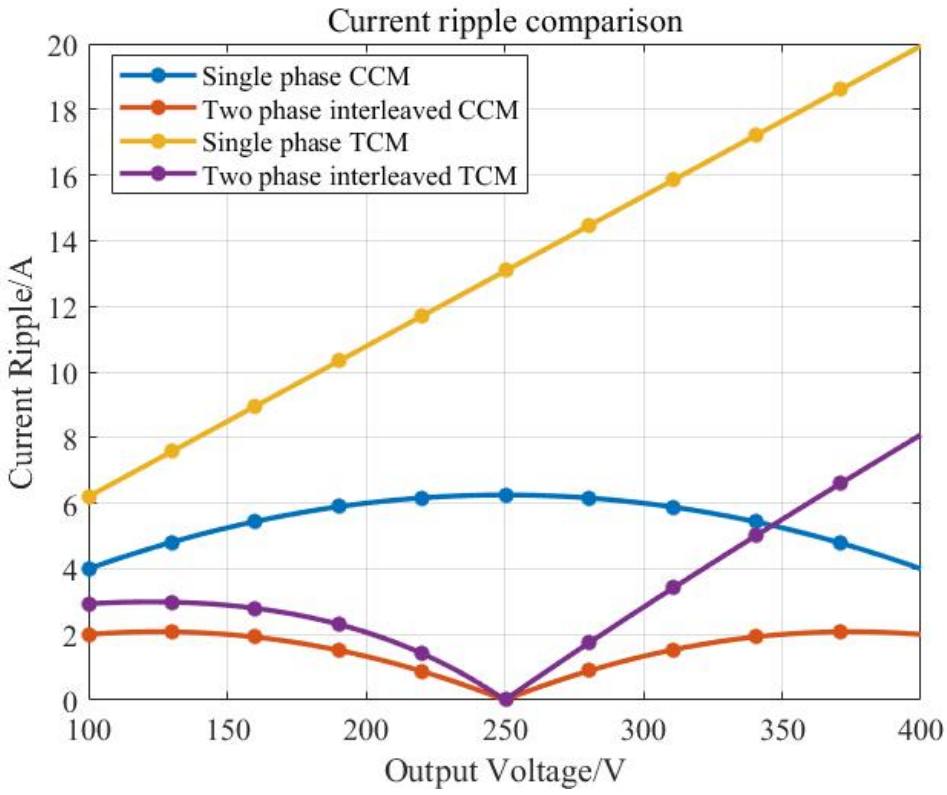

Figure 3.28: Total inductor current ripple comparison

Then the inverter conduction losses are calculated according to the primary coil current and the MOSFET on-state resistance R_{ON}. When the current goes through the inverter, there are always two switches conducting. The inverter conduction losses P_{invcon} are calculated as Eq.(3.34).

$$P_{invcon} = 2{I_{L1}}^2 * R_{ON} \tag{3.34}$$

$$\eta = \frac{P_{in} - P_R - P_{sw} - P_{invcon}}{P_{in}} \tag{3.35}$$

where P_{in} is the input power from the source, P_R is both sides' coil resistance losses, P_{invcon} is the MOSFET conduction loss from the primary side inverter and P_{sw} is the semiconductor losses of the buck converters. The overall efficiencies are calculated based on four designed scenarios and concluded as Fig.3.29.

TCM operation scenarios have higher efficiency during the whole power range and the efficiency is over 97.5 % at light load and over 99 % at most of the power levels. Taking an overall consideration of the performance on efficiency and current stress, the two-phase interleaved buck converter working in TCM has obvious advantages compared to the other scenarios.

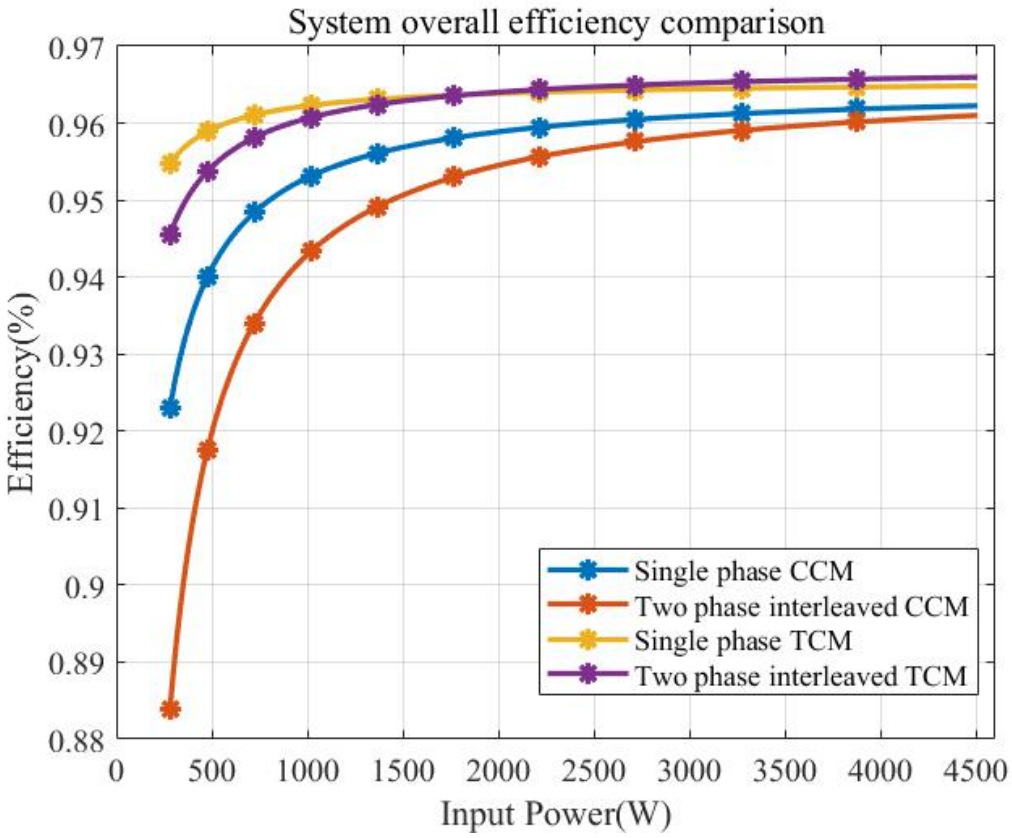

Figure 3.29: System overall efficiency comparison at different power level

4

Phase shift design

Power control strategies are various and important in the resonant wireless power transfer system. Both the output of the system voltage and current could be regulated to meet the requirement of the battery charging profile. In the previous chapters, the power regulation range is determined from 282 W to 4500 W according to Eq.(2.24), which is equal to the input voltage range from 100 V to 400 V. The previous chapters study the adoption of front-end buck converters to regulate input voltage and input power. In this chapter, the phase shift regulation method will be investigated and designed to meet the system requirement.

Colak et al., 2015 developed the charging control strategy for the WPT system using the phase difference between dual-side ac voltages of the converters. Then the output voltages of the converters can be adjusted to regulate the output or conduct bidirectional power flow. The concept of phase shift control for the WPT system is also defined. Phase shift control is implemented by delaying an angle between the two bridge arms. By changing the phase shift angle, the fundamental component of the input voltage of the transmitter can be altered. Consequently, the charging current and the power flow can be regulated.

As there are two H-bridges in the WPT system, there are also multiple implementations of the phase shift regulation method. Aditya and Williamson, 2016 developed the charging control strategy for the WPT system using a receiver side-controlled rectifier. Wang et al., 2019 developed a dual-side phase shift circuit to control both sides ac voltages. However, all the previous regulation strategies require high-frequency sensors to monitor the current zero-crossing point in order to control the rectifier on the receiver side.

In order to avoid the costs of the high-frequency sensors and the complicated additional control circuits, symmetrical phase control implemented in the inverter on the transmitter side was developed. The symmetrical phase shift control only adjusts the phase angle delayed by one phase leg, regulating the inverter output voltage. One of the most disadvantages of this control method implemented on the inverter is that the H-bridges will lose ZVS. In order to improve the system efficiency and realize ZVS of the H-bridges, Berger et al., 2015 introduced a phase delay on H-bridges, enabling the switches to turn on at ZVS. Berger et al., 2015 implemented such methods on the secondary side rectifiers using active switches. Thus this chapter will implement the phase lag method on the primary side inverters. In the following sections, both the symmetrical phase shift method without a phase delay and the proposed method with a phase delay will be investigated and compared in detail.

4.1. Phase shift without phase delay

In this section, the symmetrical phase shift regulation method without phase delay will be investigated and designed. According to the analysis of Eq.(2.24) in chapter 2, regulating the input voltage of the WPT system or the output voltage of the inverters on the primary side will regulate the input power based on the optimal load. The front-end phase shift control structure will be designed based on the

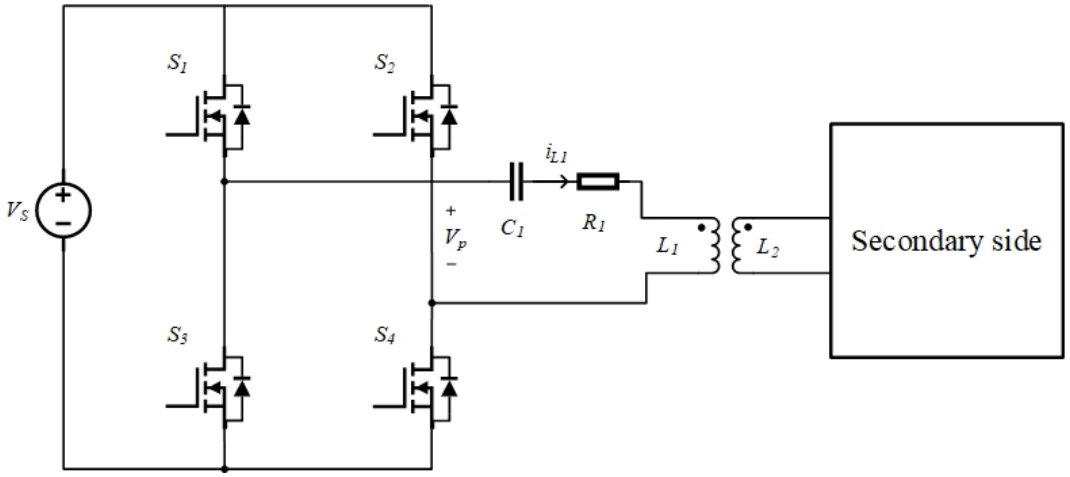

Figure 4.1: Front-end phase shift regulation WPT circuit

primary circuits as Fig.4.1. In order to explain the logic of the designed phase shift regulation method, the H-bridge switching sequences and inverter output voltage and current waveform should be considered. Then the losses and the system efficiency should be calculated and evaluated.

As demonstrated in Fig.4.2, the switching sequences of the H-bridge inverter present the implementation of a phase shift of φ, which is calculated as degrees in the following analysis. The phase shift angle φ represents the phase delay between the two switch legs of the inverter, where the switches S2 and S4 delay φ after the switches S3 and S1 respectively. The first two waveforms of Fig.4.2 give the switching sequences. S1 and S4 are one current path marked as green when a positive primary voltage V_p is delivered as the output voltage of the inverter. On the other hand, S2 and S3 are the other current path marked as yellow when a negative primary voltage V_p is delivered. The switches S2 and S4 on the right phase leg will be turned on after a phase angle φ between the switches S1 and S3 on the left phase leg. Thus the conduction time will be reduced as the phase shift angle φ increases.

The third waveform in Fig.4.2 represents the inverter output voltage and the primary coil current. According to the Fourier series of a quasi-square wave as Eq.(4.25).

$$\begin{aligned} b_n &= \frac{4}{\pi}\int_{\frac{\varphi}{2}}^{\frac{\pi}{2}} v_o \sin(n\omega t)d(\omega t) \\ &= \frac{4}{\pi}\int_{\frac{\varphi}{2}}^{\frac{\pi}{2}} V_S \sin(n\omega t)d(\omega t) \\ &= \frac{4V_S}{n\pi}[-\operatorname{con}(n\omega t)]_{\frac{\varphi}{2}}^{\frac{\pi}{2}} \\ &= \frac{4V_S}{n\pi}\cos\left(n\frac{\varphi}{2}\right) \end{aligned} \tag{4.1}$$

Where φ is the phase shift angle and V_S is the source DC voltage. For a well-compensated S-S compensation network, the high-order harmonics can be neglected. Thus the primary input voltage or the inverter output voltage could be regarded as the fundamental part of the Fourier series of the quasi-square wave shown as Eq.(4.2).

$$V_{\mathrm{p1}} = \frac{2\sqrt{2}}{\pi}V_S\cos\left(\frac{\varphi}{2}\right) \tag{4.2}$$

Based on the requirement of the power regulation range, the phase shift angle regulation range could be derived based on Eq.(2.24) and Eq.(4.2), which could be written as Eq.(4.3). Within this range of angles, the input power flow could be determined and controlled by one certain phase shift angle φ.

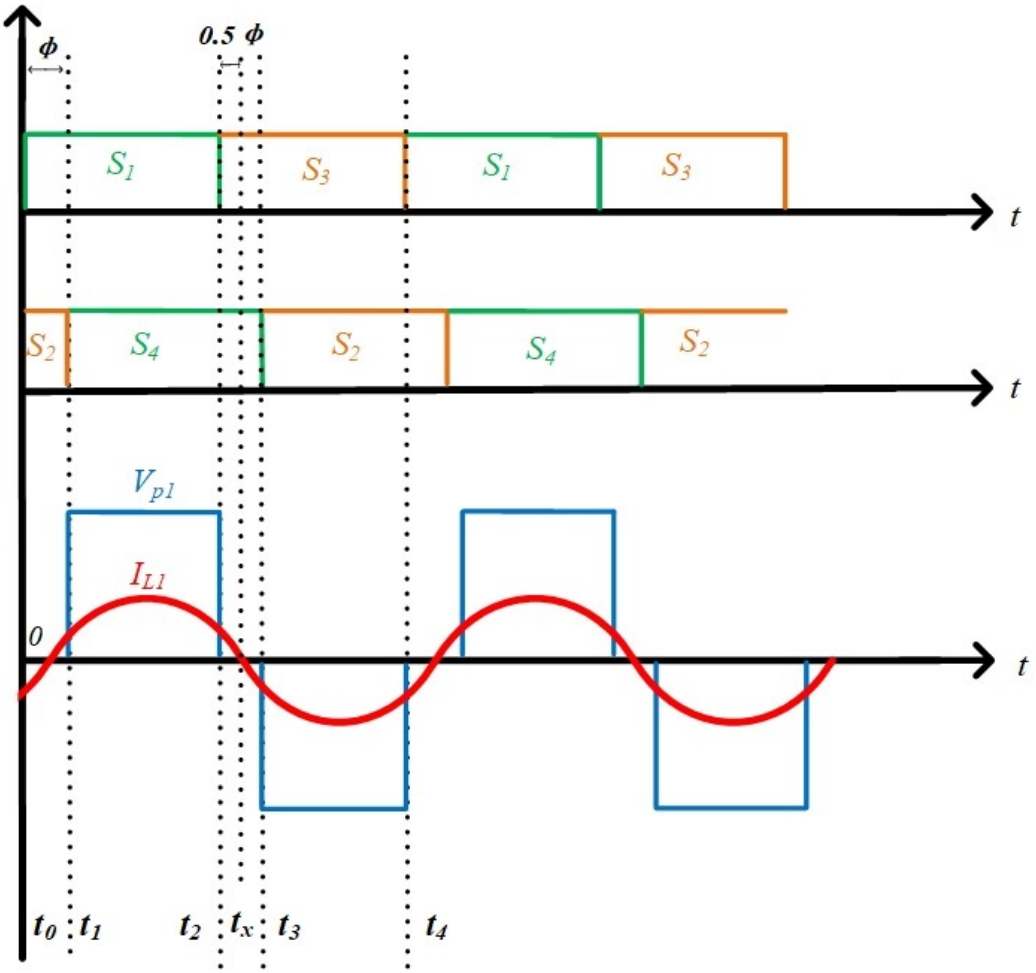

Figure 4.2: Switching sequences and the primary voltage and current waveform of Phase shift control

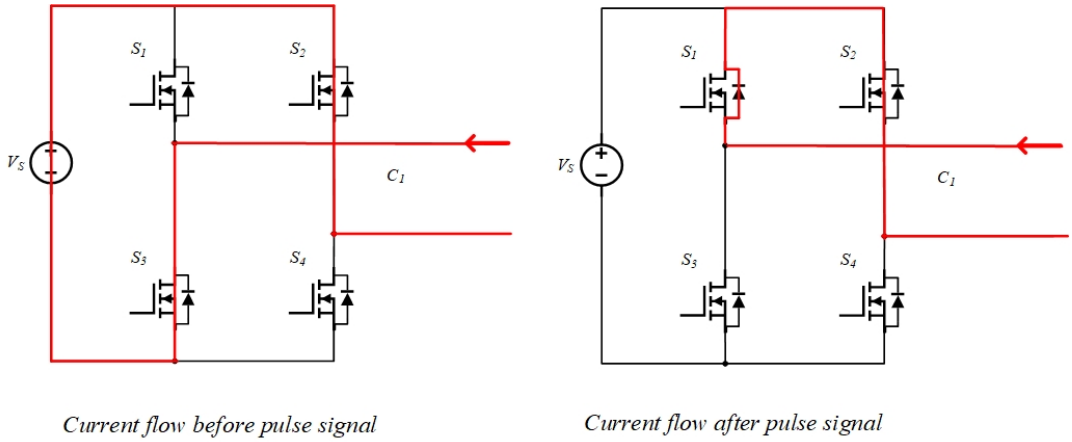

Figure 4.3: Current flow analysis at t_0

$$\begin{aligned} 100\ V \leq\ V_{\mathrm{p1}} \leq 400\ V \\ 73.7° \leq \varphi \leq 156.9° \end{aligned} \tag{4.3}$$

In order to evaluate the efficiency of the phase shift regulation method, the power loss of the system should be calculated. The system power loss contains two parts. One is the coil resistance losses caused by primary coil resistance R_1 and the secondary side resistance R_2. The other part is the semiconductor losses caused by the switches of the inverter H-bridge.

First, the primary coil RMS current I_{L1} and secondary side coil RMS current I_{L2} could be calculated as Eq.(4.4) and Eq.(4.5).

$$I_{L1} = \frac{V_{p1}}{R_1 + \frac{\omega_0^2 M^2}{R_{acL}+R_2}} \tag{4.4}$$

$$I_{L2} = \frac{V_{p1} - R_1 I_{L1}}{\omega_0 M} \tag{4.5}$$

With the coil current and coil resistance, the coil resistance power loss P_R is given by Eq.(4.6).

$$P_R = {I_{L1}}^2 R_1 + {I_{L2}}^2 R_2 \tag{4.6}$$

Then the losses of H-bridge semiconductors will be analyzed and calculated. The switching loss of the inverters should be calculated by figuring out the switching behaviour and the exact current going through the MOSFET channels. Thus, the switching sequences of the H-bridges implemented with the phase shift regulation are investigated.

- `Current flow analysis at t0`

  As demonstrated in Fig.4.2 at t_0, the primary coil current I_{L1} is negative and flows into the H-bridges. Switch S2 and S3 are conducted before t_0, thus the current goes into the MOSFET channel of S3 and then passes through the voltage source and returns to the primary coil through the MOSFET channel of S2. After the turn-off gate pulse at t_0, switch S3 is a hard turn-off at the primary coil current I_{t0}. Then during the dead time between two gate pulses at t_0, the resonant current circulates through the body diode of MOSFET S1 and the MOSFET channel S2. Thus the MOSFET S1 is able to turn on at ZVS because the current has gone through the body diode and discharged the parasitic capacitance of S1. To summarize, there is one hard turn-off of S3 and one ZVS soft turn-on of S1 around t_0 shown as Fig.4.3.

- `Current flow analysis at t1`

  As demonstrated in Fig.4.2 at t_1, the primary coil current I_{L1} is positive and flows out of the H-bridges. Switch S2 and S1 are conducted before t_1, thus the current goes into the MOSFET

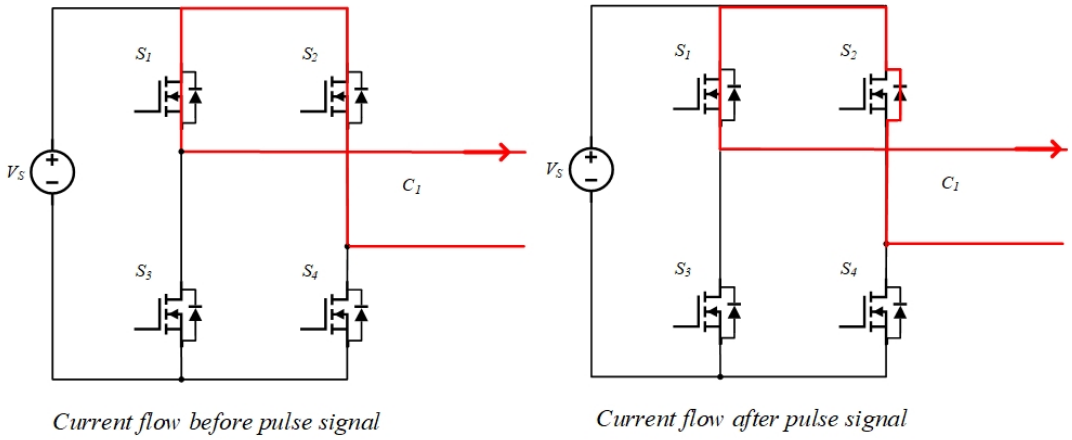

Figure 4.4: Current flow analysis at t_1

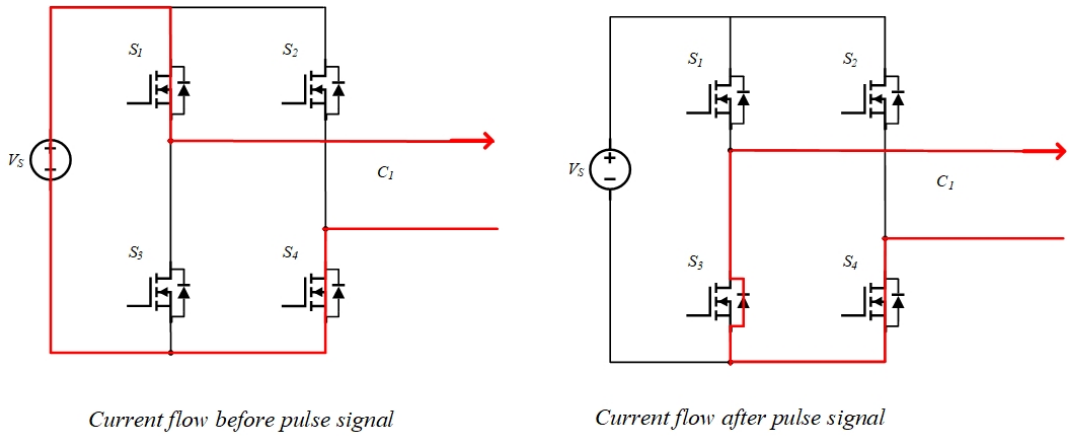

Figure 4.5: Current flow analysis at t_2

channel of S2 and then circulates around the LC resonant circuits through the MOSFET channel of S1. After the turn-off gate pulse at t_1, switch S2 starts to turn off without losses due to the channel current shifting to the body diode of S2. Then during the dead time between two pulses after t_1, the resonant current circulates through the channel of MOSFET S1 and the body diode of S2. At the turn-on gate pulse of S4, the voltage across the S4 equals the source voltage V_S. Thus S4 is a hard turn-on with the primary coil current I_{t1} at the moment of t_1. To summarize, there is one soft turn-off of S2 and one hard turn-on of S4 around t_1 shown as Fig.4.4.

- `Current flow analysis at t2`

  As demonstrated in Fig.4.2 at t_2, the primary coil current I_{L1} is positive and flows out of the H-bridges. Switch S1 and S4 are conducted before t_2, thus the current flows out of the voltage source and passes the MOSFET channel of S1 and then returns through the MOSFET channel of S4. After the turn-off gate pulse at t_2, switch S1 is a hard turn-off at the primary coil current I_{t2}. Then during the dead time between two pulses after t_2, the resonant current circulates through the body diode of S3 and the MOSFET channel of S2. Thus the MOSFET S3 is able to turn on at ZVS because the current has gone through the body diode and discharged the parasitic capacitance of S3. To summarize, there is one hard turn-off of S1 and one soft turn-on of S2 around t_2 shown as Fig.4.5.

- `Current flow analysis at t3`

  As demonstrated in Fig.4.2 at t_3, the primary coil current I_{L1} is negative and flows into the H-bridges. Switch S3 and S4 are conducted before t_3, thus the resonant circulating current goes into the MOSFET channel of S3 and then passes through the MOSFET channel of S4. After the

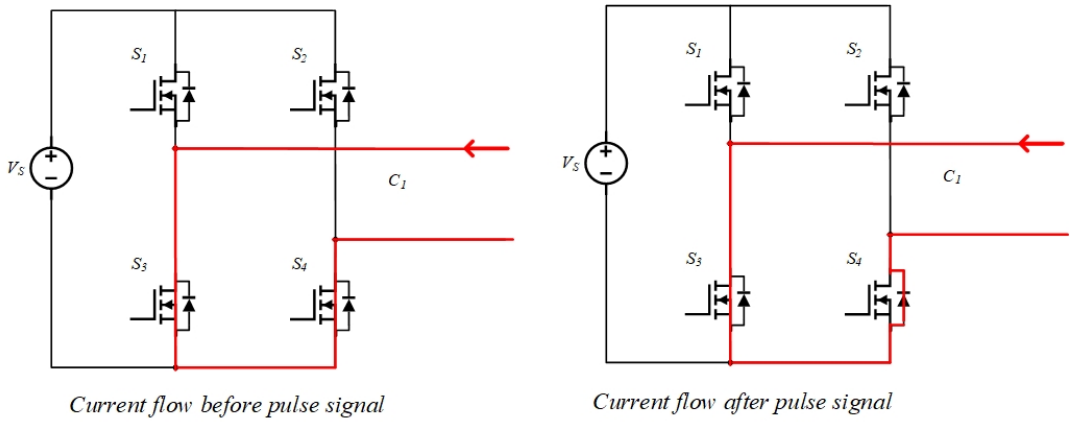

Figure 4.6: Current flow analysis at t_3

turn-off gate pulse at t_3, switch S4 starts to turn off without losses due to the channel current shifting to the body diode of S4. Then during the dead time between two pulses after t_3, the resonant current circulates through the body diode of MOSFET S4 and the MOSFET channel S3. At the turn-on gate pulse of S2, the voltage across the S2 equals the source voltage V_S. Thus S2 is a hard turn-on with the primary coil current I_{t3} at the moment of t_3. To summarize, there is one soft turn-off of S4 and one hard turn-on of S2 around t_3 shown as Fig.4.6.

As a summarization of the switching sequences in a duty cycle, there are two hard turn-ons and two hard turn-offs in total, where S1 S3 turn off with losses and S2 S4 turn on with losses. Thus there are four switching losses in one duty cycle, which will be calculated and analyzed in the following parts.

From the switching sequence analysis above, the switching loss could be figured out theoretically. The four switching current flow analyses at t_0, t_1, t_2 and t_3 conclude the phenomenon that whether the MOSFET is hard switching or soft switching is determined by the primary coil current flow direction at switching moment. Once the positivity or negativity of the primary coil current is known, the numbers of hard switching or soft switching could be estimated. As the switching sequence waveform in Fig.4.2 demonstrated, the positivity or negativity of the primary coil current is fixed and independent of the phase shift angle φ. These analyses give a conclusion that the switching behaviour is fixed on the whole power range.

In order to calculate the switching losses, the primary coil current I_{t0}, I_{t1}, I_{t2} and I_{t3} at the switching moment t_0, t_1, t_2 and t_3 can be calculated respectively as Eq.(4.7).

$$\begin{aligned} I_{t0} &= \sqrt{2} I_{L1} \sin\left(-\frac{\varphi}{2}\right) \\ I_{t1} &= \sqrt{2} I_{L1} \sin\left(\frac{\varphi}{2}\right) \\ I_{t2} &= \sqrt{2} I_{L1} \sin\left(180 - \frac{\varphi}{2}\right) \\ I_{t3} &= \sqrt{2} I_{L1} \sin\left(180 + \frac{\varphi}{2}\right) \end{aligned} \tag{4.7}$$

The switches of the inverter are SiC MOSFET G3R75MT12J. Thus the datasheet of the switching energy is calibrated and concluded as Eq.(3.9) and Eq.(3.10). For a whole duty cycle, the situation in t_4 is the same as t_0. Then the switching losses could be calculated as Eq.(4.8) based on the switching behaviours analysed.

$$P_{sw} = P_{on}(I_{t1}) + P_{on}(I_{t3}) + P_{off}(I_{t0}) + P_{off}(I_{t2}) \tag{4.8}$$

where the $P_{on}(I_{t1})$ and $P_{on}(I_{t3})$ represent the turn-on losses at t_1 and t_3 respectively. $P_{off}(I_{t0})$ and $P_{off}(I_{t2})$ represent the turn-off losses at t_0 and t_2 respectively. The turn-on and turn-off losses are given as Eq.(4.9).

$$\begin{aligned} P_{on}(I_{t1}) &= \frac{V_S}{V_{ref}} E_{on}(I_{t1}) f_0 \\ P_{on}(I_{t3}) &= \frac{V_S}{V_{ref}} E_{on}(I_{t3}) f_0 \\ P_{off}(I_{t0}) &= \frac{V_S}{V_{ref}} E_{off}(I_{t0}) f_0 \\ P_{off}(I_{t2}) &= \frac{V_S}{V_{ref}} E_{off}(I_{t2}) f_0 \end{aligned} \tag{4.9}$$

where the f_0 represents the switching frequency of the H-bridge inverter, which is equal to 85 kHz.

Then the inverter conduction losses are calculated according to the primary coil current and the MOSFET on-state resistance R_{ON}. When the current goes through the inverter, there are always two switches conducting. The inverter conduction losses P_{invcon} are calculated as Eq.(4.10).

$$P_{invcon} = 2{I_{L1}}^2 R_{ON} \tag{4.10}$$

Based on the above analyzes and calculations, the switching loss is determined on the whole range, including two hard turn-ons and two hard turn-offs. The non-ZVS turn-on only happens at the t_1 and t_3 with the positive coil current I_{t1} and negative coil current I_{t3}, respectively. For a high-frequency application in the WPT system, it is essential to assure operation in soft-switching mode. It will improve the system efficiency significantly if the current flow direction could be reversed at t_1 and t_3, enabling the switch S3 and S4 to turn on at ZVS. The details of the method to achieve that reversed current will be investigated in the next section.

4.2. Phase shift with phase delay

For the phase shift control, the output current and the output voltage are controlled by changing the phase shift angle between the switching signals S1 and S4, S2 and S3. The last section analyzed the switching sequences and switching currents during a whole duty cycle and concluded that once the phase shift angle was implemented, the H-bridge inverter was not able to achieve ZVS. In order to change the currents at t_1 and t_3 to achieve ZVS turn-on, the primary coil current should be modified. By implementing a phase delay on the primary side, the waveform and switching sequences are given as Fig.4.7.

In order to ensure ZVS turn-on, the current at t_1 and t_3 should meet the requirement to fully discharge the parasitic capacitors of MOSFET during dead time. The required current could be given as Eq.(4.11).

$$\left|I_{t1,t3}\right| \geq 2C_{oss}\frac{\Delta V_S}{\Delta t_{dead}} \tag{4.11}$$

where C_{oss} can be found from the datasheet of SiC MOSFET G3R75MT12J. t_{dead} is the dead time between two gate pulses, which is set to 100 ns to avoid a short circuit based on the rise and fall time of SiC MOSFET G3R75MT12J. Then the I_{t1} can be set to -1 A to ensure the ZVS turn-on of S4 at t_1. The I_{t3} can be set to 1 A to ensure the ZVS turn-on of S2 at t_3.

In order to ensure the primary coil current meets the requirement of ZVS, the accurate phase delay angle should be found based on the following calculations. The equivalent impedance referred to the primary side is Z_{in}, given as Eq.(4.12). Then the phase delay angle α could be designed by Eq.(4.13) according to the phase angle between primary coil current and inverter output voltage.

$$Z_{in} = j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} + \frac{\omega_0^2 M^2}{j\omega_0 L_2 + \frac{1}{j\omega_0 C_2} + R_{acL} + R_2} + R_1 \tag{4.12}$$

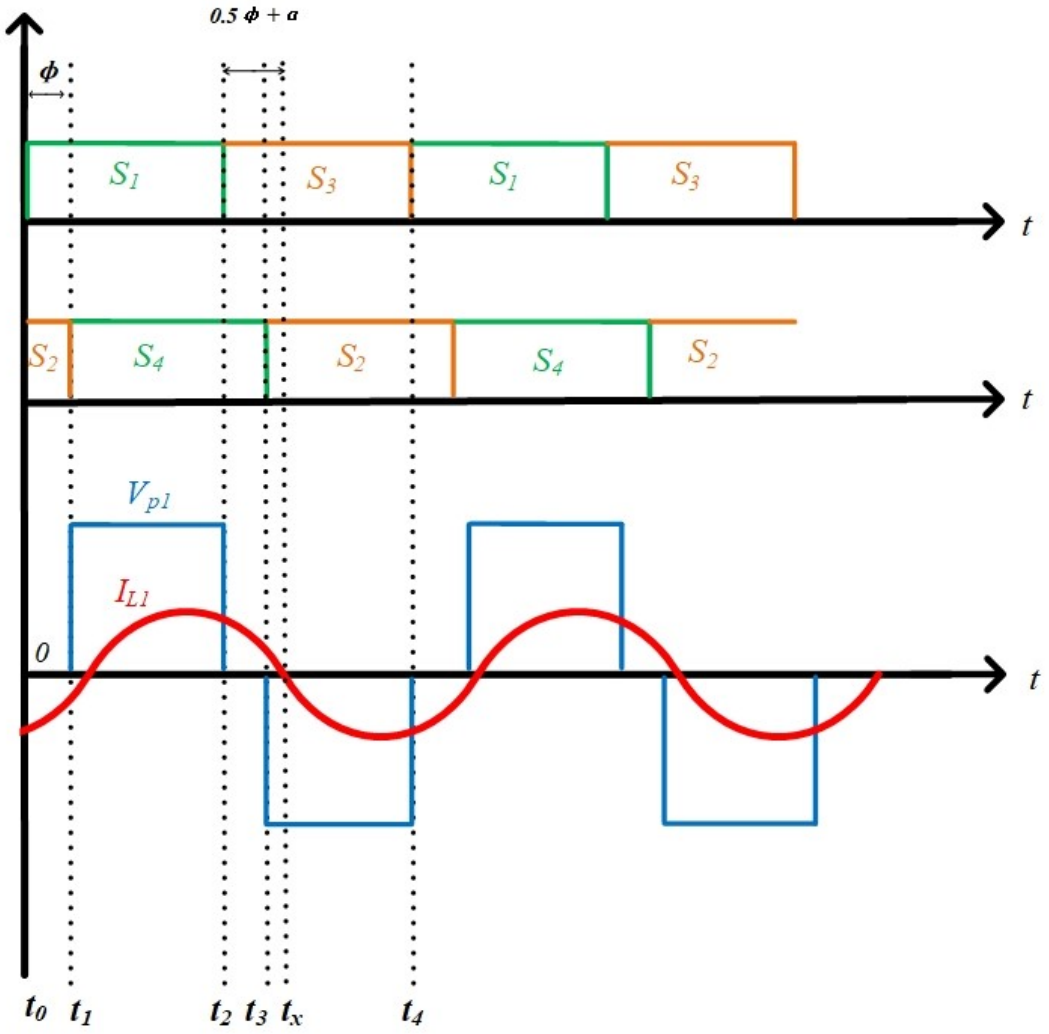

Figure 4.7: Switching sequences and the primary voltage and current waveform of Phase shift control with phase delay

$$\alpha = \tan^{-1}\left(\frac{\omega_0 L_1 - \frac{1}{\omega_0 C_1}}{\frac{\omega_0^2 M^2}{R_{acL}+R_2} + R_1}\right) \tag{4.13}$$

Where the capacitor C_1 should be changed to control the phase delay angle α. The original capacitor C_1 is calculated as Eq.(2.9) to fully compensate the inductor L_1 and to keep the primary side circuit purely resistive. The circuit with a phase lag angle α is no longer pure resistive. Thus the coil currents should be calculated in phasors. First, the primary coil current I_{L1} and secondary side coil current I_{L2} could be calculated as Eq.(4.14) and Eq.(4.15) based on fundamental component analysis.

$$\overrightarrow{I_{L1}} = \frac{\overrightarrow{V_{p1}}}{R_1 + j\omega_0 L_1 + \frac{1}{j\omega_0 C_1} + \frac{\omega_0^2 M^2}{R_{acL}+R_2}} \tag{4.14}$$

$$\overrightarrow{I_{L2}} = \frac{\overrightarrow{V_{p1}} - \left(R_1 + j\omega_0 L_1 + \frac{1}{j\omega_0 C_1}\right) * \overrightarrow{I_{L1}}}{\mathrm{j}\omega_0 M} \tag{4.15}$$

In order to determine the phase delay angle, the primary coil current I_{t0}, I_{t1}, I_{t2} and I_{t3} at the switching moment t_0, t_1, t_2 and t_3 should be calculated respectively as Eq.(4.16).

$$\begin{aligned} I_{t0} &= \sqrt{2}\left|\overrightarrow{I_{L1}}\right| \sin\left(-\frac{\varphi}{2} - \alpha\right) \\ I_{t1} &= \sqrt{2}\left|\overrightarrow{I_{L1}}\right| \sin\left(\frac{\varphi}{2} - \alpha\right) \\ I_{t2} &= \sqrt{2}\left|\overrightarrow{I_{L1}}\right| \sin\left(180 - \frac{\varphi}{2} - \alpha\right) \\ I_{t3} &= \sqrt{2}\left|\overrightarrow{I_{L1}}\right| \sin\left(180 + \frac{\varphi}{2} - \alpha\right) \end{aligned} \tag{4.16}$$

Based on the analysis of Eq.(4.11), the current at t_1 should be lower than -1 A to ensure the ZVS turn-on of S4, and the current at t_3 should be higher than 1 A to ensure the ZVS turn-on of S2. According to the switching sequences as Fig.4.7 demonstrated, the phase delay angle α should be larger than the half of phase shift angle φ to change the direction of current at t_1 and t_3 respectively. So the larger phase shift angle φ, the larger phase delay angle α is needed to keep ZVS. Thus once the phase delay angle α is designed to achieve ZVS at the lowest input power 282 W, the inverter can be operated at ZVS for the whole power range. These requirements can be written as Eq.(4.17), and the equations could be solved to determine the phase delay angle α.

$$\begin{cases} \sqrt{2}\,|I_{L1}| \sin\left(\frac{\varphi}{2} - \alpha\right) \le -1\ A \\ \sqrt{2}\,|I_{L1}| \sin\left(180 + \frac{\varphi}{2} - \alpha\right) \ge 1\ A \\ P_{in} = |V_{P1}| * |I_{L1}| * \cos(\alpha) = 282\ W \end{cases} \tag{4.17}$$

Where phase shift angle φ and the phase delay angle α are the variables to be solved. The solved primary side capacitor is 36.89 nF and the solved phase delay angle is 66.2 degrees. Although the result enables the inverter to be operated at ZVS during the whole power range theoretically, the system can not reach the upper power range. The input power equation in Eq.(4.17) demonstrates that the larger the phase delay angle α, the smaller the real power could be delivered for the system. The maximum input real power, in this case, is 1149 W, which is much lower than the defined maximum power of 4500 W. In order to reach the defined power range, the phase delay angle should be designed smaller to ensure the maximum input power of 4500 W, which means the inverter could only be operated at ZVS in part of the power range.

The modified design strategy is to find a maximum phase delay angle α, which meets the maximum input power requirements and enables the inverter to be operated at ZVS as much as it can in the defined power range. Eq.(4.18) should be solved to stabilise the phase delay angle α for the system.

$$P_{in} = |V_{P1}| * |I_{L1}| * \cos(\alpha) = 4500\ W \tag{4.18}$$

Where the phase delay angle α is the variable to be solved. The parameters in Eq.(4.18) are calculated based on zero phase shift angle φ, representing the maximum input power point. Here the primary side capacitor C_1 is designed to be 19.87 nF and the phase delay angle α is 37 degrees. According to the former analysis, the modified phase delay angle is not capable of guaranteeing ZVS operation for the whole power range. Then it is essential to figure out the input power range, where the inverter can be operated at ZVS. The boundary input power P_{inb} between the power range operated at ZVS and non-ZVS could be found by solving the functions as Eq.(4.19).

$$\begin{cases} \sqrt{2}\,|I_{L1}| \sin\left(\frac{\varphi}{2} - \alpha\right) \le -1\ A \\ \sqrt{2}\,|I_{L1}| \sin\left(180 + \frac{\varphi}{2} - \alpha\right) \ge 1\ A \end{cases} \tag{4.19}$$

Where the boundary phase shift angle φ is the variable to be solved. The parameters in Eq.(4.19) are calculated based on the determined phase delay angle α. The solved boundary phase shift angle is 66.29 degrees and the boundary input power P_{inb} is given by Eq.(4.20).

$$P_{inb} = |V_{P1}| * |I_{L1}| * \cos(\alpha) = 3152\ W \tag{4.20}$$

Up to now, the phase delay parameters are all well designed. By implementing the primary side capacitor C_1 with the value of 19.87 nF, the system can work at ZVS from 3152 W to 4500 W, while the system will work without ZVS from 282 W to 3152 W. To verify the phase delay design, simulations of the primary coil currents and inverter output voltage at t_1 and t_3 are plotted as Fig.4.8 and Fig.4.9 respectively.

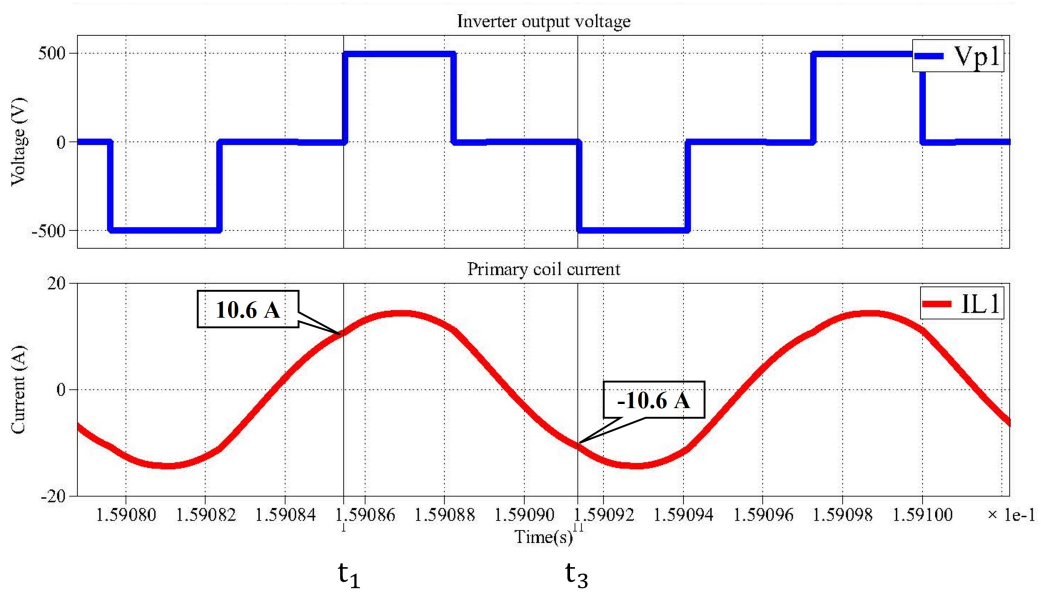

Figure 4.8: Simulation of designed phase shift control at the input power of 3152 W

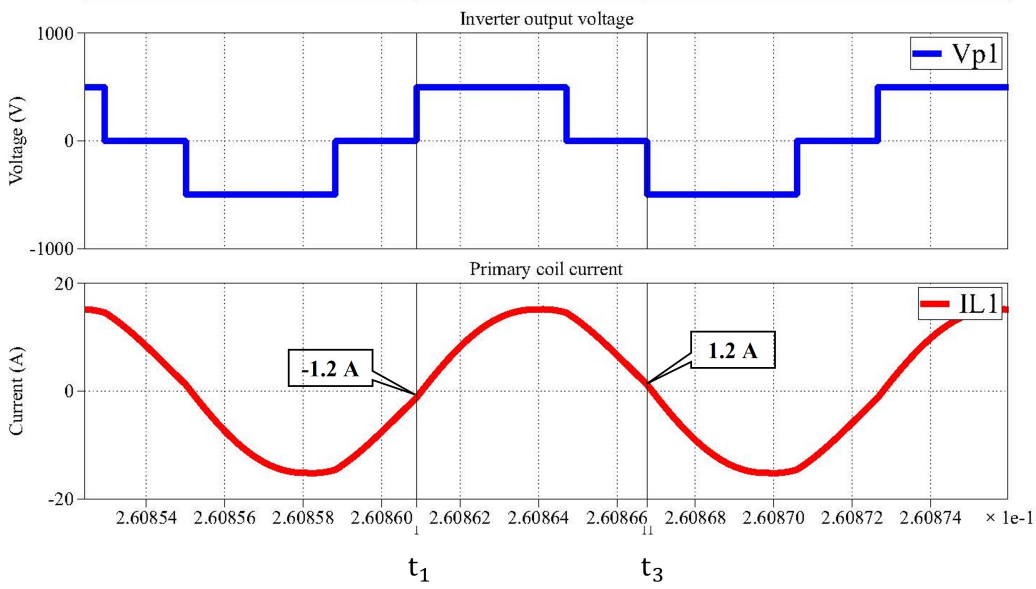

Figure 4.9: Simulation of designed phase shift control without phase delay at the input power of 3152 W

Fig.4.8 and Fig.4.9 demonstrate that the implementation of phase delay successfully changes the primary coil current at t_1 and t_3. Thus the inverter could work at ZVS when the input power is higher than 3152 W. The primary coil currents at t_1 and t_3 will also decrease significantly after the implementation of phase delay, which will help decrease switching losses at non-ZVS operation mode when the input power is lower than 3152 W. In the following analysis, the losses of the system will be specified.

Firstly, the coil resistance losses of the system should be calculated. With the coil current and coil resistance, the coil resistance power loss P_R is given by Eq.(4.21).

$$P_R = \left|\overrightarrow{I_{L1}}\right|^2 R_1 + \left|\overrightarrow{I_{L2}}\right|^2 R_2 \tag{4.21}$$

Then the inverter conduction losses are calculated according to the primary coil current and the MOSFET on-state resistance R_{ON}. When the current goes through the inverter, there are always two switches conducting. The inverter conduction losses P_{invcon} are calculated as Eq.(4.22).

$$P_{invcon} = 2\left|\overrightarrow{I_{L1}}\right|^2 R_{ON} \tag{4.22}$$

Then the MOSFET switching losses are analyzed according to the boundary input power P_{inb}. When the input power is larger than P_{inb}, the inverter is operated at ZVS. When the input power is lower than P_{inb}, the inverter is operated at non-ZVS. Thus the switching losses P_{sw} are given as Eq.(4.23).

$$\begin{cases} P_{sw} = P_{on}(I_{t1}) + P_{on}(I_{t3}) + P_{off}(I_{t0}) + P_{off}(I_{t2}) & \text{when Pin} \le \text{Pinb} \\ P_{sw} = P_{off}(I_{t0}) + P_{off}(I_{t2}) & \text{when Pin} > \text{Pinb} \end{cases} \tag{4.23}$$

where the $P_{on}(I_{t1})$ and $P_{on}(I_{t3})$ represent the turn-on losses at t_1 and t_3 respectively. $P_{off}(I_{t0})$ and $P_{off}(I_{t2})$ represent the turn-off losses at t_0 and t_2 respectively. The turn-on and turn-off losses are given as Eq.(4.24).

$$
\begin{aligned}
P_{on}\left(I_{t1}\right) &= \frac{V_S}{V_{ref}} E_{on}\left(I_{t1}\right) f_0 \\
P_{on}\left(I_{t3}\right) &= \frac{V_S}{V_{ref}} E_{on}\left(I_{t3}\right) f_0 \\
P_{off}\left(I_{t0}\right) &= \frac{V_S}{V_{ref}} E_{off}\left(I_{t0}\right) f_0 \\
P_{off}\left(I_{t2}\right) &= \frac{V_S}{V_{ref}} E_{off}\left(I_{t2}\right) f_0
\end{aligned}
\tag{4.24}
$$

where the f_0 represents the switching frequency of the H-bridge inverter, which is equal to 85 kHz. The primary coil currents are the amplitude of the phasors calculated as Eq.(4.16).

4.3. Phase shift harmonics analysis

For the phase shift control, the output current and the output voltage are controlled by changing the phase shift angle between the switching signals S1 and S4, S2 and S3. It is obvious that as the phase shift angle φ increases, the waveform distortions of the inverter output voltage and primary coil current are more serious. The inverter output voltage is less square and the primary coil current is less sinusoidal when the input power is decreasing.

The designs and calculations of the last two sections are all based on fundamental component approximation. However, the current should be calculated with high accuracy to guarantee ZVS switching. When the waveform distortions are serious at low input power especially, the harmonics will be too large to neglect based on straightforward assumptions. With the mentioned concerns, the harmonic analysis should be conducted to improve the accuracy of the phase shift designs in this section.

Firstly, the phase shift calculations in former sections are mainly based on the rms inverter output voltage, rms primary coil current, the coil current at t_1, t_2, t_3 and t_4. The coil currents at t_3 and t_4 can be referred to the currents at t_1 and t_2 according to Eq.(4.7) and Eq.(4.16), thus the following analysis are only based on the coil current at t_1 and t_2. The calculation results of fundamental component approximation and the simulation results of the designed WPT system are compared. The comparison of the design without phase delay is shown in Fig.4.10. The comparison of the design with phase delay is shown in Fig.4.11.

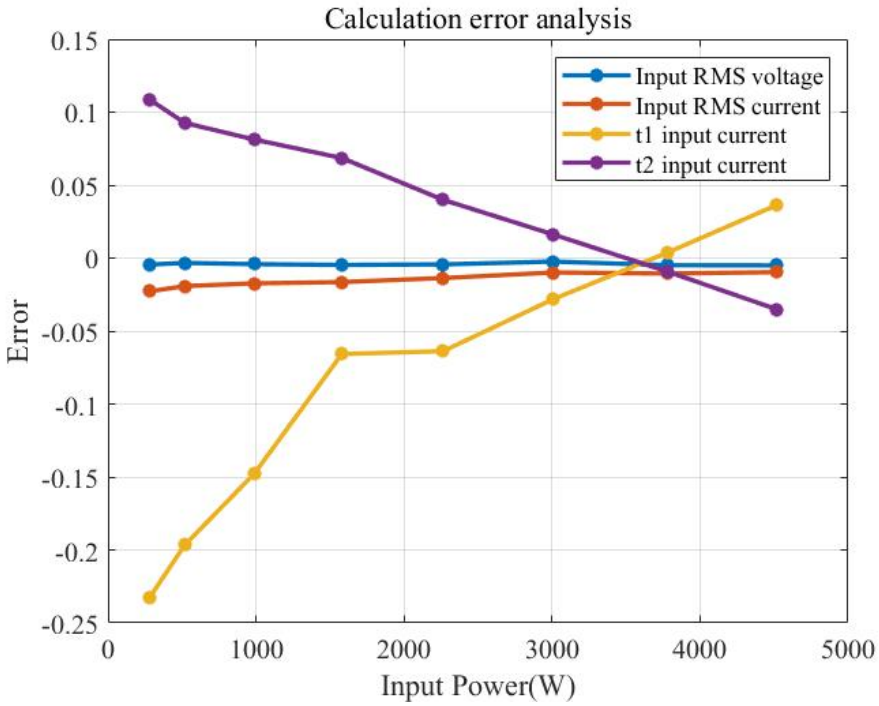

Figure 4.10: Calculation error analysis of phase-shift control without phase delay

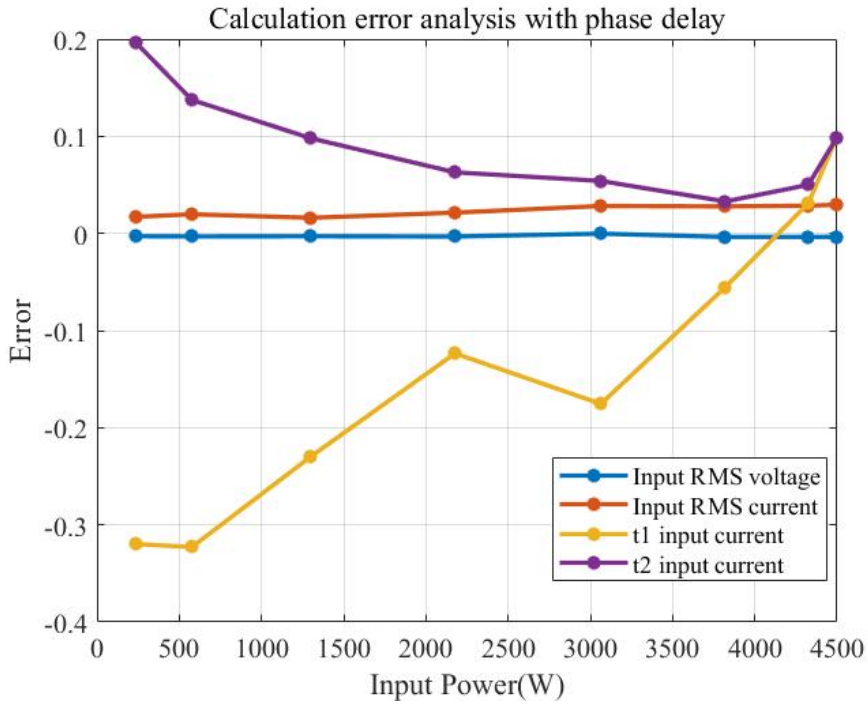

Figure 4.11: Calculation error analysis of phase-shift control with phasedelay

The figures demonstrate that the rms voltages and currents in both scenarios are calculated with very high accuracy, while the instantaneous coil current at t_1 and t_2 have lower accuracy. The figures also support the analysis that the calculation results based on fundamental component approximation have higher errors when the input power is lower, where the current waveforms become less sinusoidal due to the increasing phase shift angle.

In order to numerically analyze the influence of the higher harmonics, the Fourier expression of the inverter output voltage is calculated as Eq.(4.25).

$$\begin{aligned} b_n &= \frac{4}{\pi}\int_{\frac{\varphi}{2}}^{\frac{\pi}{2}} v_o \sin(n\omega t)d(\omega t) \\ &= \frac{4}{\pi}\int_{\frac{\varphi}{2}}^{\frac{\pi}{2}} V_S \sin(n\omega t)d(\omega t) \\ &= \frac{4V_S}{n\pi}[-\operatorname{con}(n\omega t]_{\frac{\varphi}{2}}^{\frac{\pi}{2}} \\ &= \frac{4V_S}{n\pi}\cos\left(n\frac{\varphi}{2}\right) \end{aligned} \tag{4.25}$$

Fig.4.12 gives a visual expression of the harmonics of the inverter output voltage, where the $2K-1$ harmonics are plotted over the defined power range. It is obvious that the higher harmonics have high amplitudes and large variations over the defined power range. Thus the following calculations should consider the 3rd, 5th, 7th and 9th harmonics to increase the accuracy.

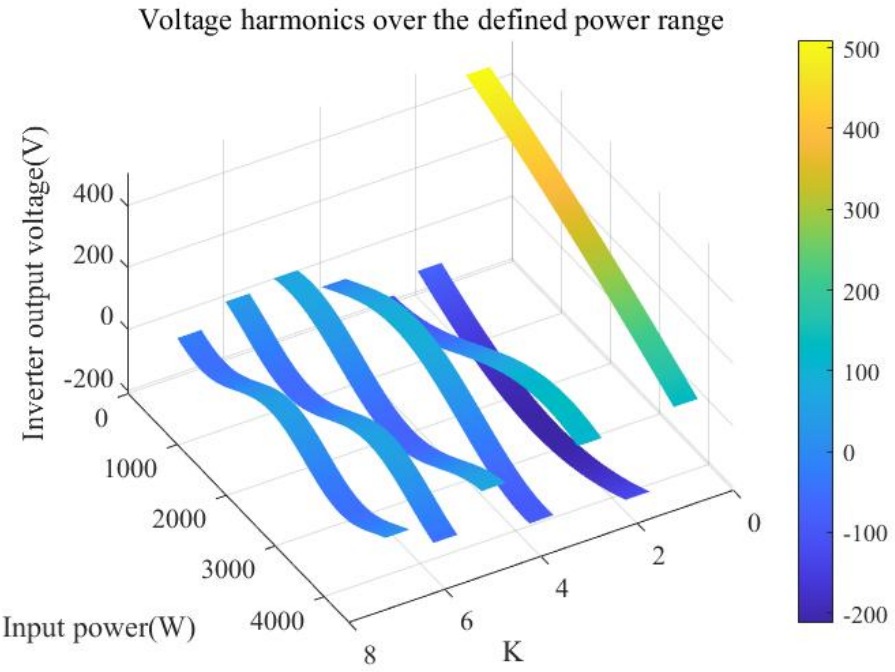

Figure 4.12: Inverter output voltage harmonics analysis

Then the primary coil current harmonics should be derived based on the voltages. As all the harmonics are also sinusoidal waveforms, so the load resistance is R_{ac} according to the calculations based on Eq.(2.20). The equivalent input impedance of the nth harmonics Z_{inn} can be derived as Eq.(4.26).

$$\overrightarrow{Z_{inn}} = R_1 + jnwL_1 + \frac{1}{jnwC_1} + \frac{n^2\omega^2M^2}{R_{acLn} + R_2 + jnwL_2 + \frac{1}{jnwC_2}} \tag{4.26}$$

Where the input impedance is calculated as phasor because it is not pure resistive for 3rd and higher harmonics. Then the phase angle of the equivalent input impedance of the nth harmonics $\theta_{Z_{inn}}$ can be derived as Eq.(4.27).

$$\theta_{Z_{inn}} = \tan^{-1} \frac{\mathrm{Im}\,(Z_{inn})}{\mathrm{Re}\,(Z_{inn})} \tag{4.27}$$

Then the primary coil current harmonics can be derived based on the voltage harmonics and input impedance harmonics. The amplitudes $|I_{L1n}|$ and phase angles $\theta_{I_{L1n}}$ of the primary coil current harmonic are given as Eq.(4.28).

$$\begin{aligned} |I_{L1n}| &= \frac{\left|\overrightarrow{V_{pn}}\right|}{\left|\overrightarrow{Z_{inn}}\right|} \\ \theta_{I_{L1n}} &= \theta_{V_{pn}} - \theta_{Z_{inn}} \end{aligned} \tag{4.28}$$

where the phase angle of inverter output voltage $\theta_{V_{pn}}$ is 0 degrees if the harmonics are positive and $\theta_{V_{pn}}$ is 180 degrees if the harmonics are negative according to Eq.(4.25). Then the amplitudes $|I_{L1n}|$ of the primary coil current harmonics are plotted as Fig.4.13 to give a straightforward comparison. Fig.4.13 demonstrates that both the amplitudes and the variations of the primary coil current harmonics are very small compared to the fundamental component. Although the amplitudes of coil current harmonics $|I_{L1n}|$ are small, the phase angle of higher harmonics $\theta_{I_{L1n}}$ may still influence the calculation accuracy based on fundamental component approximation.

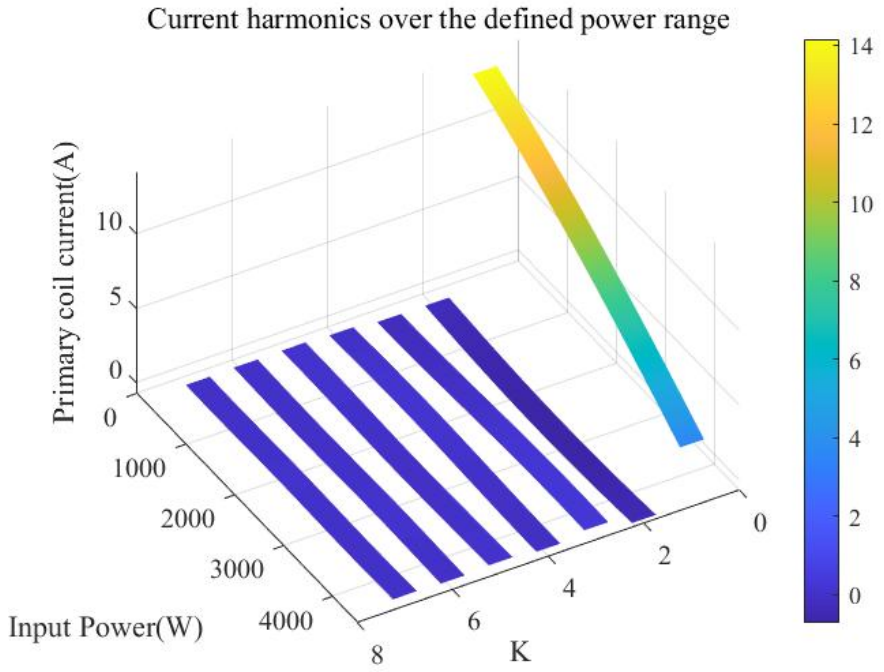

Figure 4.13: Primary coil current harmonics analysis

In order to further evaluate the influences of higher harmonics on the current calculations, the instantaneous primary coil currents at t_1 and t_2 are calculated by including the 3rd, 5th, 7th and 9th harmonics. The nth harmonics of instantaneous primary coil currents I_{t1n} and I_{t2n} at t_1 and t_2 can be derived as Eq.(4.29).

$$\begin{aligned} I_{t1n} &= |I_{L1n}| \sin\left(n\frac{\varphi}{2} + \theta_{I_{L1n}}\right) \\ I_{t2n} &= |I_{L1n}| \sin\left(180n - \frac{\varphi}{2}n + \theta_{I_{L1n}}\right) \end{aligned} \tag{4.29}$$

Where the phase angles $\theta_{I_{L1n}}$ of the primary coil current harmonic are given Eq.(4.28). Then the instantaneous primary coil currents at t_1 and t_2 could be derived by adding up the nth harmonics I_{t1n} and I_{t2n} as Eq.(4.30).

$$I_{t1} = \sum_{n=1,3,5,7,9} I_{t1n}$$
$$I_{t2} = \sum_{n=1,3,5,7,9} I_{t2n} \tag{4.30}$$

To evaluate the calculations of instantaneous primary coil currents at t_1 and t_2, the simulation of the whole designed WPT system is conducted to catch the current. The simulated results are compared with the results based on fundamental component approximation and the calibrated results including higher harmonics. The comparison of the scenario of phase shift without phase delay is shown in Fig.4.14 and Fig.4.15. The comparison of the scenario of phase shift with phase delay is shown in Fig.4.16 and Fig.4.17.

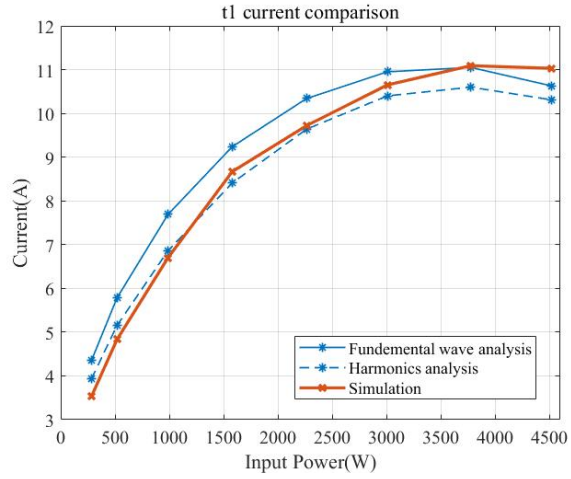

Figure 4.14: Comparison of primary coil current at t_1

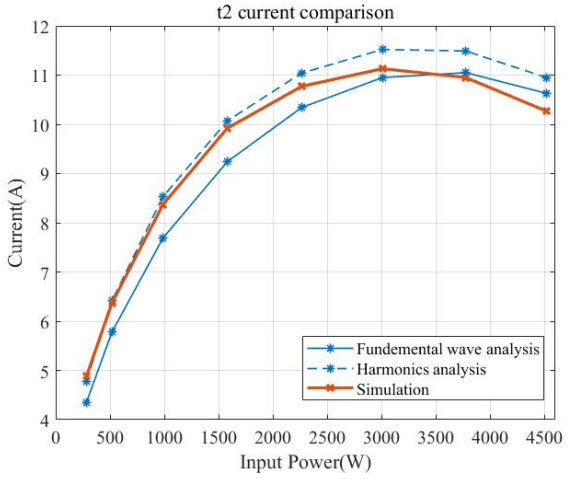

Figure 4.15: Comparison of primary coil current at t_2

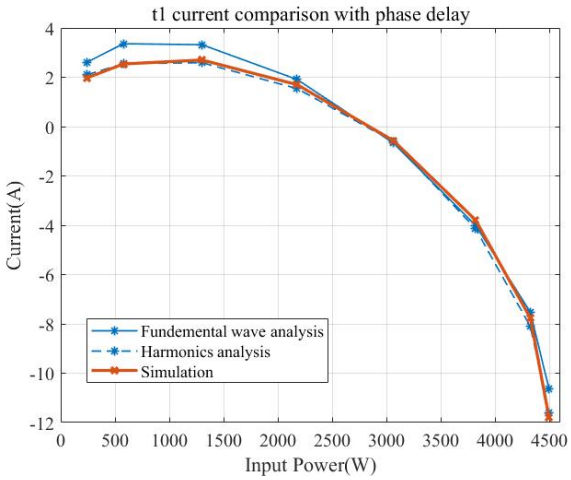

Figure 4.16: Comparison of primary coil current at t_1 with phase delay

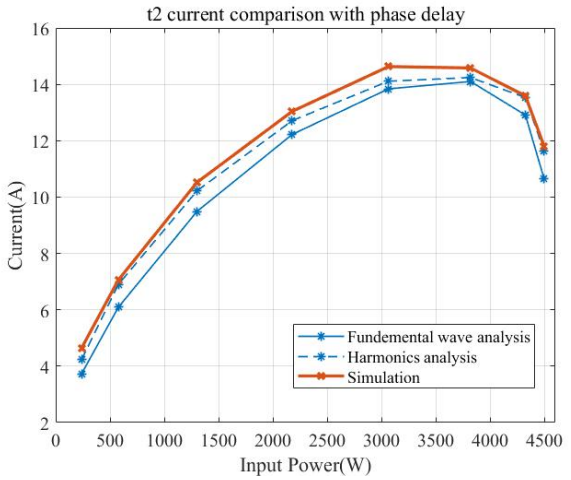

Figure 4.17: Comparison of primary coil current at t_2 with phase delay

Fig.4.14 and Fig.4.15 demonstrate that the calculation results based on fundamental wave analysis are reliable and accurate enough for the designed WPT system. The main reason is that for a

WPT system with S-S compensation, the equivalent input impedance for higher harmonics becomes too large compared to the fundamental component according to Eq.(4.26). Thus the higher harmonics of the coil currents are small enough to be neglected.

Similar conclusions can also be found in the scenario of phase shift with phase delay design according to Fig.4.16 and Fig.4.17. The harmonics analysis increases the current accuracy in the low input power situation while both fundamental wave analysis and harmonics analysis have acceptable accuracy in the high input power situation.

To have an in-depth understanding of the influence of higher harmonics, the dashed lines represent the instantaneous primary coil currents considering the 3rd, 5th, 7th and 9th harmonics. It is obvious that the harmonic analysis successfully improves the accuracy of the current calculations in low input power situations, where the large phase shift angle φ makes the voltage and current waveforms distorted, introducing larger harmonics components. Then the current accuracy is improved by considering higher harmonics and calibrating the calculation.

However, the harmonics analysis is unable to further improve the calculation accuracy in high input power situations. The reason is that the higher harmonics of coil current contribute very little to the real current in high input power situations. While the nonlinear semiconductors contribute to more significantly calculation errors. The on-state resistance of the MOSFET and dead time between switches of the H-bridge inverters makes the derived V_p inaccurate, which can not be neglected if higher accuracy is needed. The diode H-bridge rectifier and the filter capacitor can not be neglected, making the linear equivalent R_{acL} inaccurate.

In conclusion, the fundamental component approximation is reliable and accurate enough for the designed WPT system with an S-S compensation. To further increase the current accuracy in the low input power situation, the harmonics analysis could be applied to calibrate the results based on the fundamental component approximation.

4.4. Phase shift design evaluation

In this chapter, two scenarios of phase shift control methods are designed. In both designs, the output voltage is controlled by changing the phase shift angle between the switching legs of the H-bridge inverter. In this section, the two scenarios will be compared according to the system efficiency.

Firstly, the scenario of phase shift without phase delay will be analyzed. By controlling the phase shift angle φ in the range of 73.7 degrees to 156.9 degrees, the WPT system meets the defined power range of 282 W to 4500 W. The loss in this scenario contains the coil resistance loss P_R given by Eq.(4.6), the inverter MOSFET conduction loss P_{invcon} given by Eq.(4.10) and the inverter MOSFET switching loss P_{sw} given by Eq.(4.8). So the efficiency of the system η_1 can be calculated as Eq.(4.31).

$$\eta_1 = \frac{P_{in} - P_R - P_{sw} - P_{invcon}}{P_{in}} \tag{4.31}$$

where the P_{in} is the system input power, which is given by Eq.(4.32).

$$P_{in} = V_{P1} * I_{L1} \tag{4.32}$$

Secondly, the scenario of phase shift with phase delay will be analyzed. By controlling the phase shift angle φ in the range of 0 degrees to 153.4 degrees, the WPT system meets the defined power range of 282 W to 4500 W. By modifying the primary side capacitor to 19.87 nF, the introduced phase delay angle α enables the coil current lag the inverter output voltage, supporting the inverter works at ZVS. The loss in this scenario contains the coil resistance loss P_R given by Eq.(4.21), the inverter MOSFET conduction loss P_{invcon} given by Eq.(4.22) and the inverter MOSFET switching loss P_{sw} given by Eq.(4.23). So the efficiency of the system η_2 can be calculated as Eq.(4.33).

$$\eta_2 = \frac{P_{in} - P_R - P_{sw} - P_{invcon}}{P_{in}} \tag{4.33}$$

where the P_{in} is the system input power, which is given by Eq.(4.18).

The efficiency comparison between the two phase shift control scenarios is plotted in Fig.4.18. The figure demonstrates that the system efficiency of the scenario with phase delay is higher than the other over the whole defined power range.

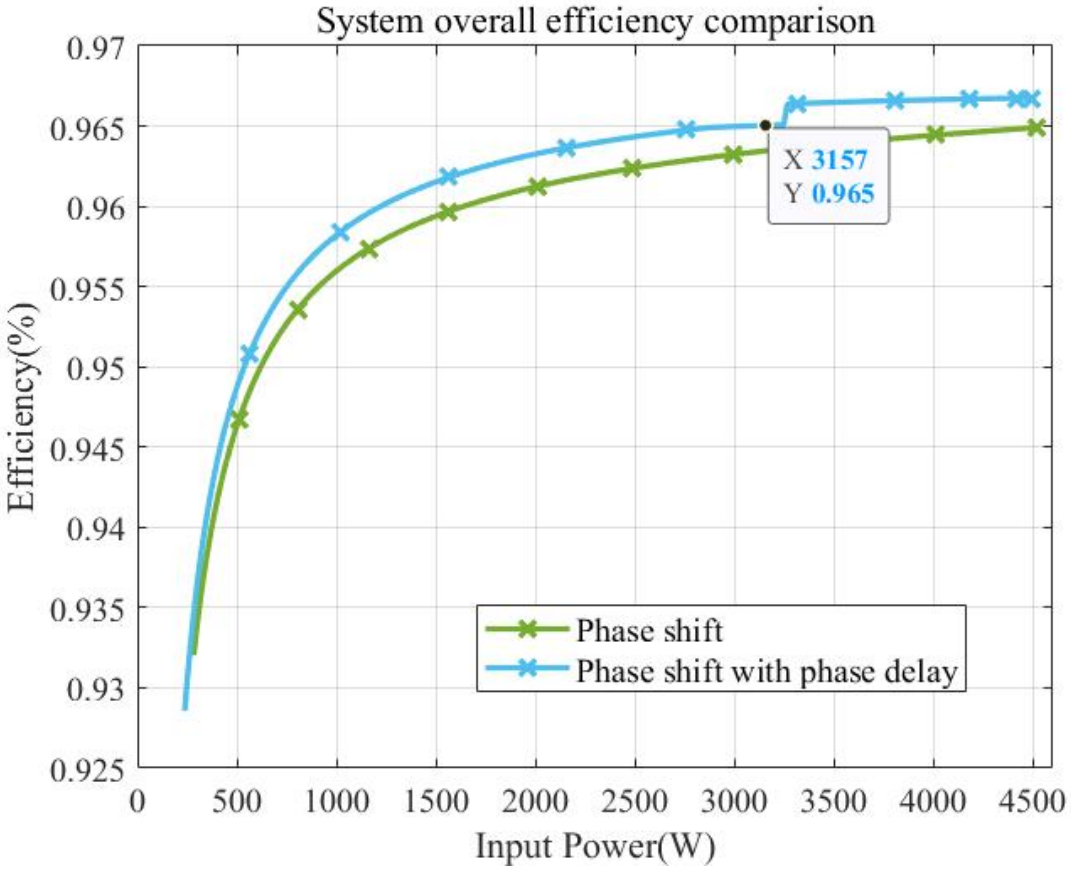

Figure 4.18: Comparison of two scenarios of phase shift methods

At the marked data point in Fig.4.18, the system efficiency increase when the input power is higher than 3157 W. The reason is that when the input power is higher than the designed boundary input power P_{inb}, the inverter could work at ZVS. The figure indicates that the system efficiency could increase significantly when the switches work at ZVS.

It is also obvious that the design with phase delay has higher efficiency than the other design even when the input power is lower than the designed boundary input power P_{inb}. The reason is that the coil current at the switching moment is lower by introducing a phase delay, decreasing the switching losses in non-ZVS operation mode. So for the designed WPT system in the thesis, the phase shift method with phase delay is superior to the phase shift method without phase delay.

4.5. Overall design evaluation

After completing the design of two scenarios of phase shift methods, it is important to evaluate the designed phase shift system by comparing it with the other front-end voltage control methods for this WPT system.

Finally, the four scenarios of front-end buck converters and the two scenarios of inverter-based phase shift methods are compared. The six scenarios meet the same defined power range and the efficiency over the whole power range will be compared. The comparison results are shown in Fig.4.19.

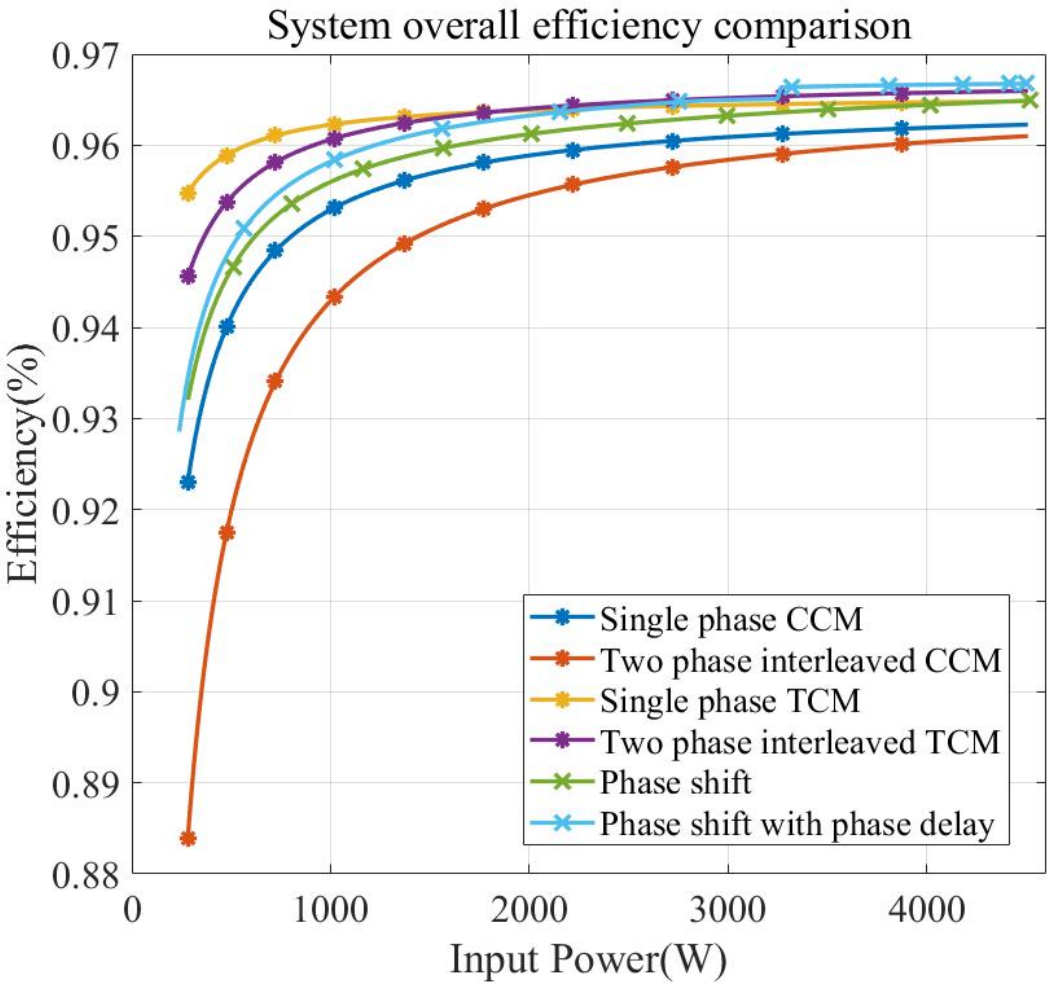

Figure 4.19: System efficiency comparison between all six designed scenarios

From the system efficiency comparison figure, several conclusions could be found.

- (1) The system efficiency is increasing with higher input power. That means the system efficiency at a light load will be relatively lower. The system efficiency in different design scenarios has distinct differences from 88.5% (two-phase interleaved CCM) to 95.5% (single-phase TCM). The major loss at a light load is the semiconductor switching loss. Thus the ZVS should be guaranteed for switches if a high efficiency at a light load is required. A well-designed method should consider the possible solutions to reduce switching losses at a light load such as introducing TCM operation mode or implementing resonant snubber circuits.

- (2) The system efficiency at a heavy load has fewer differences among the six designed scenarios. However, the input power is much higher at a heavy load, which means there is more power

loss with relatively lower efficiency, generating much heat to the system. Thus it is still important to choose the method achieving a higher efficiency at a heavy load. The buck converters worked in TCM have a higher efficiency achieving 96% and the phase shift method with a phase delay has the highest efficiency over 96.5% when the power is high.

- (3) The benchmark should also consider the costs and the complexities of the designed system. The designs of the two phase shift methods have the simplest structure and the least components. While the designs of two-phase interleaved buck converters have the most components. Thus the selection of voltage control methods should consider the trade-offs between different requirements.

5

Conclusion and future work

5.1. Conclusion

In recent years, the Wireless Power Transfer (WPT) system has become more popular due to its prominent advantages for Electrical Vehicle (EV) charging. To charge an EV, the WPT system should be able to follow a certain battery charging profile. Thus, an additional voltage control circuit should be designed to help the WPT system meet the EV battery charging requirement. With the growing popularity of the WPT system used for EV charging, more and more voltage control methods with distinctive characteristics are proposed and studied. The goal of this thesis report is to conduct a comprehensive benchmark of the front-end voltage control solutions.

This thesis report focuses on the front-end voltage control solutions including the front-end buck converter and the phase shift control based on the primary inverter. Six different front-end voltage control scenarios are designed and compared. There are four scenarios of the front-end buck converters including the single-phase buck converter working in Continuous Conduction Mode (CCM), the single-phase buck converter working in Triangular Current Mode (TCM), the two-phase interleaved buck converter working in CCM and the two-phase interleaved buck converter working in TCM. There are two scenarios of primary inverter-based phase shift controls including phase shift with and without phase delay. Different from previous research on phase shift control, this thesis report conducts an in-depth harmonic analysis and compares the accuracy of harmonics analysis with the accuracy of fundamental wave analysis.

In the first step, the WPT circuits are analyzed and designed according to the SAE J2954 standard in chapter 2. The circuit parameters are designed based on a Series to Series (S-S) compensation network. The equivalent AC load resistance and the equivalent DC load resistance are derived, which will significantly simplify the design of the phase shift methods and the front-end buck converters respectively. The optimal load resistance is also derived to achieve the highest system efficiency based on the coil quality factors.

Then the four scenarios of front-end buck converters are designed and analyzed according to the defined WPT system in chapter 3. The semiconductor losses are calculated dedicatedly for all the buck converters including the MOSFET channel conduction loss, the MOSFET switching loss, the body diode conduction loss and the body diode reverse recovery loss. In order to reduce switching losses, the TCM operation mode is designed to guarantee ZVS. The two-phase interleaved structure is analyzed and designed to reduce the output current ripple and reduce the current stress on the switches. The two-phase interleaved buck converter working in TCM has the best performance with high system efficiency and a low current ripple.

Last but not least, two inverter-based phase shift control methods are analyzed and designed for the defined WPT system in chapter 4. The switching sequences are analyzed including the gate pulses, inverter output voltage and primary coil current waveforms. The instantaneous current amplitudes and

directions are figured out at each gate pulse timings in a duty cycle, which helps to conclude the switching behaviour of the inverter. In order to reduce switching losses, the phase delay angle is introduced by changing the primary compensation capacitor. The phase delay angle is precisely designed with the consideration of trade-offs between power range and efficiency. The scenario of phase shift with phase delay achieves a much higher efficiency compared to the scenario without phase delay.

For the phase shift method implemented in the WPT system, most research uses fundamental component approximation without considering the possible calculation errors caused by the higher harmonics. This thesis report conducts an in-depth harmonic analysis, which not only proves that the fundamental wave analysis is reliable and accurate enough to calculate the phase shift parameters for the S-S compensation but also improves the calculation accuracy at a light load by harmonics calibration.

Finally, the four scenarios of front-end buck converters and the two scenarios of inverter-based phase shift methods are compared. The single-phase buck converter working in TCM has the highest efficiency of 95.5% in light load situations. The major loss at a light load is the semiconductor switching loss so the designed scenarios working in ZVS have better performance. The scenario of phase shift with phase delay has the highest efficiency over 96.5% in heavy load situations.

5.2. Future work

The studies and contributions in this thesis report are limited. There are a lot of meaningful topics that remain to be further studied based on the conclusions from this thesis report.

- (1) The loss calculation of the front-end buck converter in this thesis excludes the magnetic losses of the inductor. The core losses and winding losses of the inductor are relatively small compared to the semiconductor losses in the designed buck converter. However, a more dedicated magnetic design will reduce the magnetic losses, especially for the two-phase interleaved buck converters.

- (2) The phase shift method with phase delay in this thesis is implemented with a fixed primary compensation capacitor. If this capacitor is too large, the system could not deliver enough real power. If this capacitor is too small, only when the load is heavy can the system work at ZVS. Thus the fixed capacitor will limit the upper power range if the system should be designed to work at ZVS over the whole power range. Thus a controllable capacitor could be introduced to improve this.

Bibliography

Aditya, K., & Williamson, S. S. (2016). Simplified mathematical modelling of phase-shift controlled series-series compensated inductive power transfer system. *2016 IEEE 25th International Symposium on Industrial Electronics (ISIE)*, 842–848.

Berger, A., Agostinelli, M., Vesti, S., Oliver, J. A., Cobos, J. A., & Huemer, M. (2015). A wireless charging system applying phase-shift and amplitude control to maximize efficiency and extractable power. *IEEE Transactions on Power Electronics*, *30*(11), 6338–6348.

Colak, K., Asa, E., Bojarski, M., Czarkowski, D., & Onar, O. C. (2015). A novel phase-shift control of semibridgeless active rectifier for wireless power transfer. *IEEE Transactions on Power Electronics*, *30*(11), 6288–6297.

Covic, G. A., & Boys, J. T. (2013). Modern trends in inductive power transfer for transportation applications. *IEEE Journal of Emerging and Selected topics in power electronics*, *1*(1), 28–41.

Fu, M., Ma, C., & Zhu, X. (2014). A cascaded boost–buck converter for high-efficiency wireless power transfer systems. *IEEE Transactions on Industrial Informatics*, *10*(3), 1972–1980. https://doi.org/10.1109/TII.2013.2291682

Fu, M., Yin, H., Zhu, X., & Ma, C. (2014). Analysis and tracking of optimal load in wireless power transfer systems. *IEEE Transactions on Power Electronics*, *30*(7), 3952–3963.

Garnica, J., Chinga, R. A., & Lin, J. (2013). Wireless power transmission: From far field to near field. *Proceedings of the IEEE*, *101*(6), 1321–1331.

Gautam, D. S., Musavi, F., Edington, M., Eberle, W., & Dunford, W. G. (2012). An automotive onboard 3.3-kw battery charger for phev application. *IEEE Transactions on Vehicular Technology*, *61*(8), 3466–3474.

Grazian, F., Shi, W., Soeiro, T. B., Dong, J., van Duijsen, P., & Bauer, P. (2020). Compensation network for a 7.7 kw wireless charging system that uses standardized coils. *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 1–5.

Hayes, J. G., & Goodarzi, G. A. (2018). Electric powertrain: Energy systems, power electronics and drives for hybrid, electric and fuel cell vehicles.

Lee, J.-P., Cha, H., Shin, D., Lee, K.-J., Yoo, D.-W., & Yoo, J.-Y. (2013). Analysis and design of coupled inductors for two-phase interleaved dc-dc converters. *Journal of power electronics*, *13*(3), 339–348.

Lu, F., Zhang, H., & Mi, C. (2017). A review on the recent development of capacitive wireless power transfer technology. *Energies*, *10*(11), 1752.

Millan, J., Godignon, P., Perpiñà, X., Pérez-Tomás, A., & Rebollo, J. (2013). A survey of wide bandgap power semiconductor devices. *IEEE transactions on Power Electronics*, *29*(5), 2155–2163.

Mizuno, T., Yachi, S., Kamiya, A., & Yamamoto, D. (2011). Improvement in efficiency of wireless power transfer of magnetic resonant coupling using magnetoplated wire. *IEEE Transactions on Magnetics*, *47*(10), 4445–4448.

Rogina, M. R., Rodriguez, A., Vazquez, A., & Lamar, D. G. (2019). Improving the efficiency of sic-based synchronous boost converter under variable switching frequency tcm and different input/output voltage ratios. *IEEE Transactions on Industry Applications*, *55*(6), 7757–7764.

Vinod, M., Kishan, D., Harishchandrappa, N., & Reddy, B. D. (2021). Comparative analysis of symmetrical and asymmetrical phase shift control strategy for resonant wireless inductive charging system. *2021 IEEE International Power and Renewable Energy Conference (IPRECON)*, 1–6.

Wang, C., Chen, M., Cui, H., Liu, X., Zhong, W., & Shi, F. (2019). A novel soft-switching dual-side phase shift circuit for wireless power transfer. *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 5344–5351.

Yu, G., Soeiro, T. B., Dong, J., & Bauer, P. (2021). Study of back-end dc/dc converter for 3.7 kw wireless charging system according to sae j2954. *2021 IEEE 15th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 1–8.

Zhang, J., Lai, J.-S., Kim, R.-Y., & Yu, W. (2007). High-power density design of a soft-switching high-power bidirectional dc–dc converter. *IEEE Transactions on power electronics*, *22*(4), 1145–1153.

Zhang, Z., Pang, H., Georgiadis, A., & Cecati, C. (2018). Wireless power transfer—an overview. *IEEE Transactions on Industrial Electronics*, *66*(2), 1044–1058.