Ultra-Low Idle Power Class-D Amplifier

Miao Zhang

Master of Science Thesis

https://www.porsche.com/netherlands/nl/models/panamera/panamera-turbo-models/panamera-turbo/comfort-audio/burmester-3d-high-end-surround-sound-system/

TU Delft Delft University of Technology

NXP

Challenge the future

Ultra-Low Idle Power Class-D Amplifier

by

Miao Zhang

In partial fulfillment of the requirements for the degree of
Master of Science in Electrical Engineering
At Department of Microelectronics, Faculty of EEMCS, Delft University of Technology
To be defended on Monday October 7, 2019 at 9:30 AM.

Student number:	4737156	
Project duration:	June 1, 2018 – October 7, 2019	
Thesis committee:	Prof.dr. Kofi Makinwa,	TU Delft, chair
	Dr. Qinwen Fan,	TU Delft, supervisor
	Dr. Fabio Sebastiano,	TU Delft
	Dr. Marco Berkhout,	NXP Semiconductors

This thesis is confidential and cannot be made public.

This thesis project was supported by NXP Semiconductors.

TU Delft NXP

Abstract

Class-D amplifiers are widely used in automotive audio systems because of their high efficiency. In modern car sound systems, multiple amplifiers are used to provide good audio effect. However, typical class-D amplifiers have a high idle-power, which can drain the battery quickly. To solve this problem, an ultra-low idle power class-D amplifier is proposed in this thesis. The simulation results show that this amplifier can achieve very low idle power while maintaining competitive linearity and efficiency.

Contents

Chapter 1 Introduction

1.1 Background

1.1.1 Class-D Amplifier Principles

Class-D amplifier is widely used in audio systems due to its high efficiency [1-9]. It is a kind of switching amplifier, which modulates low frequency input signal into high frequency pulses and outputs the amplified pulses from rail to rail. Then the useful output signal can be restored by low pass filtering output pulses.

Figure 1.1 shows the operation principles of a class-D amplifier with bridge-tied-load (BTL) configuration [10]. Compared with linear amplifiers, class-D amplifiers can achieve a much higher power efficiency. This is because their output transistors operate as switches, and there is no other path for current to flow apart from the load.

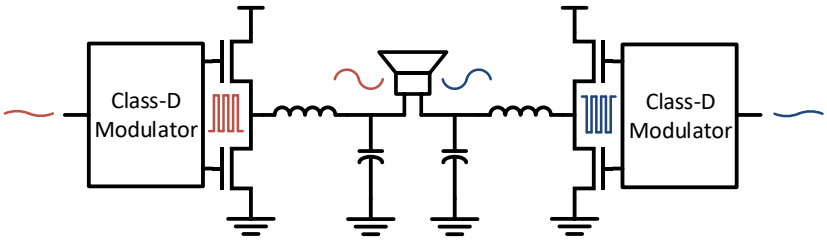

Figure 1.1 Simplified class-D amplifier.

The most widely used modulation scheme is pulse width modulation (PWM) [11], which is implemented by comparing the low frequency input signal with high frequency triangle waves. With the BTL configuration, there are two traditional modulation schemes [12]: AD-PWM modulator generates complementary pulses by comparing the triangle wave with a single-ended input signal, as shown in Figure 1.2; while the BD-PWM modulator generates non-complementary pulses by comparing the triangle wave with differential input signals respectively, as shown in Figure 1.3.

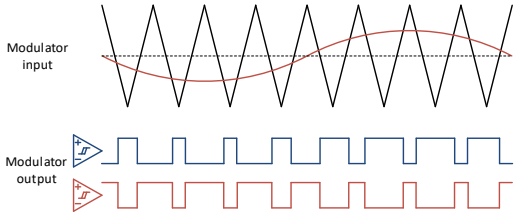

Figure 1.2 AD-PWM.

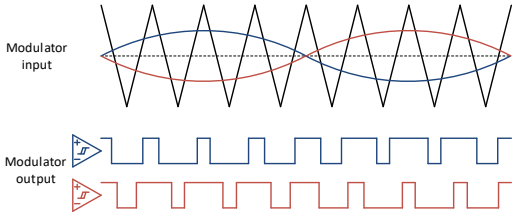

Figure 1.3 BD-PWM.

Power loss of class-D amplifiers can be divided into switching loss and conduction loss [13]: the former is the power used for charging parasitic capacitors (Cgs, Cgd,

Cdb, etc.); the latter is the ohmic loss while conducting current. During the idle state, when there is no differential input signal, both AD and BD modulated class-D amplifiers keep switching at PWM frequencies; thus the gate charging (switching) loss of output power transistors dominates the total power loss.

1.1.2 Problems

1.1.2.1 Standby Battery Draining

Modern automotive audio systems employ high power speakers in multiple channels to provide good sound effects, for example, the Audi Q7 WFS has 62 individually driven speakers [14]. Due to the limited space in vehicles, high-efficiency audio amplifiers should be used to reduce the size of heat sinks, which makes class-D amplifiers preferable.

However, automotive audio amplifiers should be turned on all the time regardless of the on/off status of the engines, because the clicks and pops occur during the power on/off transition moments can be very annoying [15]. Therefore, when the engines are turned off, traditional multi-channel class-D amplifiers drain the batteries quickly via constant idle switching.

1.1.2.2 Electromagnetic Compatibility and System Cost

As vehicles continue to integrate an increasing number of electronic devices (wireless transceivers, radars, motor controllers, etc.), automotive audio systems have to meet stringent electromagnetic compatibility (EMC) requirements to ensure that the unwanted electromagnetic interference (EMI) is within specified limits, so that they do not disturb other systems within the vehicle.

For a pulse width modulated class-D amplifier, an output LC low pass filter is employed to suppress EMI emissions at the switching frequency and its harmonics [16], the suppression depends on the ratio of the switching frequency (f_{PWM}) to the low pass cut-off frequency (f_{LC}). Increasing the switching frequency causes more switching loss in the idle state; while decreasing the cut-off frequency leads to the use of large capacitors and inductors, which are bulky and expensive.

As a part of the audio signal chain, LC components should exhibit good linearity to ensure sound quality, which also increases the cost significantly.

1.2 Objectives

This class-D amplifier is designed for automotive audio systems supplied by 14.4V batteries. In this application, idle power, system cost, and audio quality are main requirements.

The major objective is to reduce idle power consumption. Among commercial class-D amplifiers, the idle power can be as low as 122mW per channel [17]. In academia, the best reported idle current is 2.95mA per channel [18], which can be translated to 42.48mW with a 14.4V supply. In this thesis, the idle power target is less than 40mW per channel.

This cost-sensitive application prefers small value LC components. To balance cost and performance, the minimum LC components used in industry are 3.3uH and 1uF (cut-off at 88kHz) [19]. By using a high switching frequency, this thesis work targets at 3.3uH and 0.68uF (cut-off at 106kHz) LC components.

As an automotive audio amplifier, signal quality and efficiency are also important. With ultra-low idle power and low-cost LC components, this thesis work also aims for competitive SNR, THD, and efficiency.

Based on the discussion above, the target specifications are summarized in Table 1.1.

Table 1.1 Target specifications.

Specification	Target
Idle power	<40mW
LC cut-off frequency	106kHz
THD (1kHz, 1W)	<-90dB
SNR (A-weighted)	>106dB
Maximum efficiency	>90%

1.3 Innovations and Highlights

1.3.1 Idle Power Reduction

In idle state, the dominant power loss is switching loss; therefore, the key idea of idle power reduction is to reduce switching frequency in idle state.

This thesis proposed a novel modulation scheme called push-pull modulation, which means the two half-bridge output pulses in a push-pull manner. Figure 1.4 shows the push-pull PWM principle: the class-D amplifier modulates positive/negative input signal into positive/negative PWM pulses, and zero signal into no pulse; hence, the idle power should be zero under ideal conditions. Besides, power efficiency can also benefit from push-pull modulation: while outputting positive/negative pulses, the negative/positive half-bridge does not switch. Thus, the switching loss is halved.

However, in reality, when a small signal (noise, offset, etc.) is present, the push-pull PWM modulator has to output narrow pulses at a fixed PWM frequency, which fails the effort of idle power reduction. To solve this high switching frequency problem, pulse-skipping modulation (PSM) [20, 21] is used to deal with the small input signal. Unlike PWM that modulates the small signal into narrow pulses every cycle, PSM skips some of the cycles while maintaining the same averaged output as PWM (Figure 1.5).

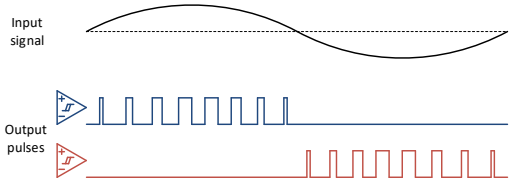

Figure 1.4 Push-pull PWM.

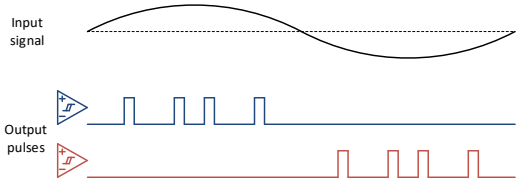

Figure 1.5 Push-pull PSM.

1.3.2 Linearity Improvement

The major disadvantage of push-pull modulations is the dead band distortion due to the minimum output pulse width, which is limited by rising and falling transition time of the output stage. This issue can be settled by reducing the output stage supply voltage. As shown in Figure 1.6, after low-pass filtering, high voltage narrow pulses are equivalent to low voltage wide pulses. Hence, a low voltage output stage can produce much smaller signals, reduce the dead band, and improve linearity.

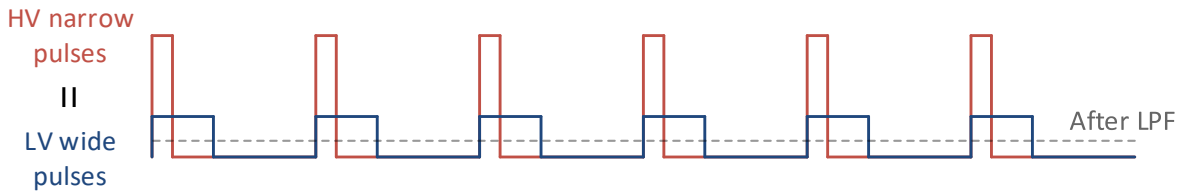

Figure 1.6 High voltage and low voltage pulses transformation.

A traditional BTL configured class-D amplifier employs a single-level output stage, as shown in Figure 1.7. To cooperate high voltage and low voltage output stages, this thesis employs a multi-level output stage [22], as shown in Figure 1.8. When the output

stage works in the high voltage mode, isolation switches are turned off to protect low voltage transistors; in the low voltage mode, isolation switches are turned on, the low voltage output stage shares the same low side transistors with the high voltage output stage.

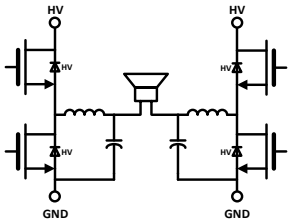

Figure 1.7 Single level output stage.

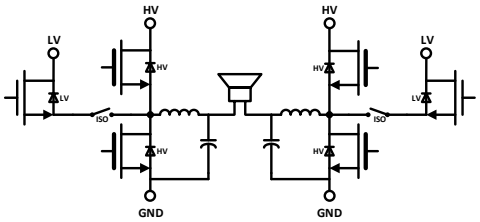

Figure 1.8 Multi-level output stage.

1.3.3 LC Components Cost Reduction

As for the LC components cost problem, the solution in this thesis is to reduce the rating and capacitance/inductance of the components.

Low-rated LC components are cheap, but they suffer from current/voltage dependencies. One solution is closing the feedback loop after the LC filter [23], and suppressing LC non-linearity by a high loop gain, as illustrated in Figure 1.9.

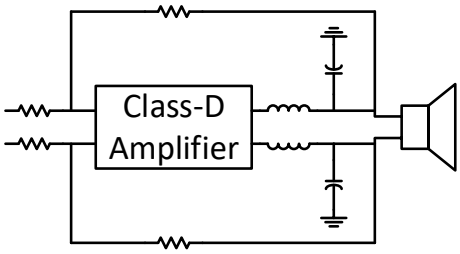

Figure 1.9 Simplified closed-loop class-D amplifier with feedback after LC.

High switching frequency allows the use of small value LC components, but the selection of switching frequency should meet EMC requirements. The CISPR 25 standard [24] EMI mask is shown in Figure 1.10. A proper switching frequency should be located in the relaxed EMI mask area. In this thesis, the selected switching frequency is 4MHz, whose second order harmonic (8MHz) is also in the relaxed EMI mask area.

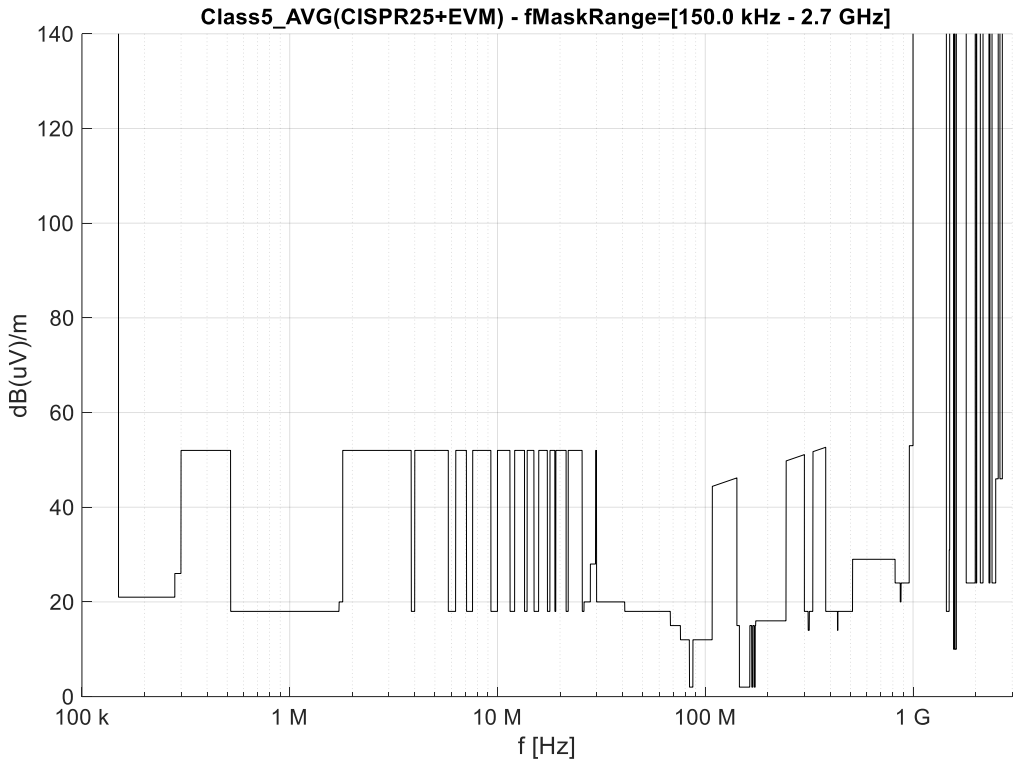

Figure 1.10 The CISPR 25 EMI mask.

1.4 Thesis Organization

The rest of this thesis is organized as follows.

The complete class-D amplifier can mainly be divided into loop filter, modulator, common-mode regulator, and output stage. And they are discussed in chapters 2 to 5 respectively, including architecture, circuit, and simulations. In chapter 6, system level schematic simulations are presented, showing the achieved specifications. Thesis conclusions and possible future work are shown in chapter 7.

Chapter 2 Loop Compensation

For any closed-loop amplifiers, stability is always an essential topic. This chapter begins with feedback compensation objectives; it then describes compensation techniques and implementation; it concludes by presenting simulation results.

2.1 Compensation objectives

2.1.1 Loop Gain

In a closed-loop class-D amplifier, as shown in Figure 2.1, a major distortion contributor is the output stage, while the primary gain producing element is the loop filter (integrator). The idea behind feedback is to suppress output stage non-linearity by high-gain loop filters.

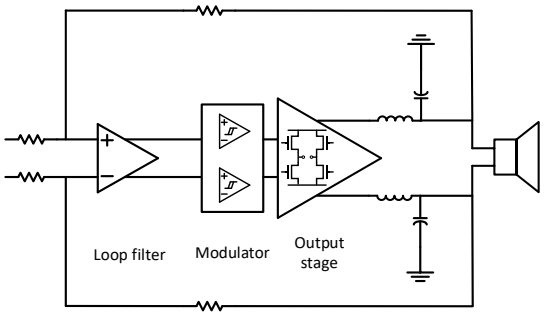

Figure 2.1 Simplified closed-loop class-D amplifier.

Figure 2.2 shows the open-loop class-D output stage output spectrum with 1W output power. To achieve the targeted THD (-90dB) with a 10dB margin, the feedback loop should provide at least 50dB loop gain at 20kHz to suppress the high order harmonics.

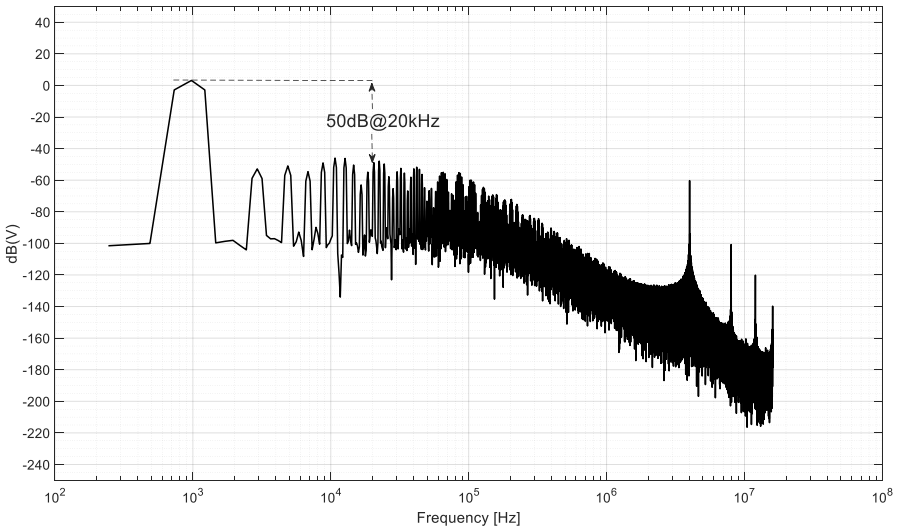

Figure 2.2 Output stage spectrum with 1W output power.

2.1.2 Loop Bandwidth

A fundamental limitation of a closed-loop class-D amplifier is that loop unity-gain bandwidth (f_{BW}) should be less than f_{PWM}/π [1]; besides, a lower f_{BW} is favorable for noise considerations. Due to the feedback after LC, the filter introduces high-Q complex conjugate poles in the feedback loop, which causes a peaking at f_{LC}. For feedback stability, f_{BW} should be higher than f_{LC}. The loop bandwidth restrictions are summarized in (2.1).

$$f_{LC} < f_{BW} < f_{PWM} / \pi \tag{2.1}$$

2.1.3 Phase Compensation

As discussed above, the feedback loop should have high loop gain in the audio band, but with relatively low bandwidth, which leads to a second order loop filter design.

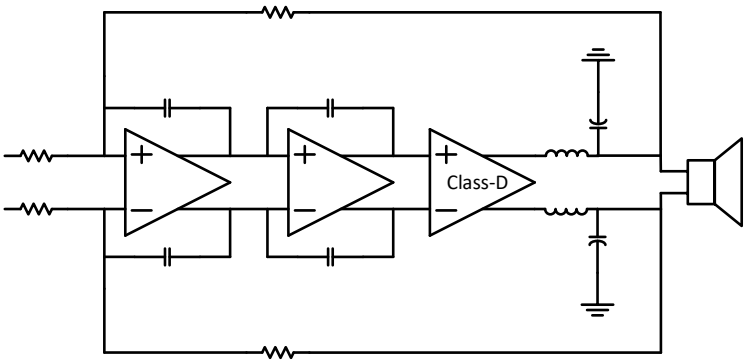

Figure 2.3 Simplified closed-loop class-D amplifier with 2nd order loop filter.

Figure 2.3 shows the closed-loop setup, the second order loop filter lags the loop by 180°, and the LC filter also introduces a 180° phase lag. To achieve a 60° phase margin, the loop should provide a +240° phase lead, which requires 3 compensation zeros.

2.1.4 LC Spread Tolerance

Because the off-chip LC filter is part of the feedback loop, their value spread impacts the loop stability. For normal automotive grade components, capacitors and inductors exhibit ±10% and ±20% spreads, respectively. To leave some margin, in this thesis project, the target spread tolerance is ±20% for both inductors and capacitors.

2.2 Compensation Methodology

In this section, the non-linear class-D output stage is modeled by a fixed-gain linear amplifier, whose gain equals to the ratio of class-D amplifier output swing to loop filter

output swing. Based on the relative position of compensation zeros and LC poles, there are four possible compensation schemes; Figure 2.4 shows the feedback loop gain after compensation. To reduce f_{BW}, the compensation zeros should be at higher frequencies; therefore, loop (d) is preferred, whose three compensation zeros are all higher than f_{LC}.

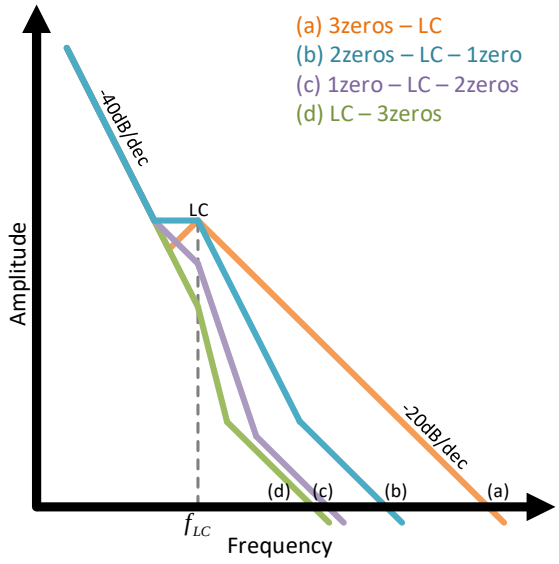

Figure 2.4 Loop gain with four compensation schemes.

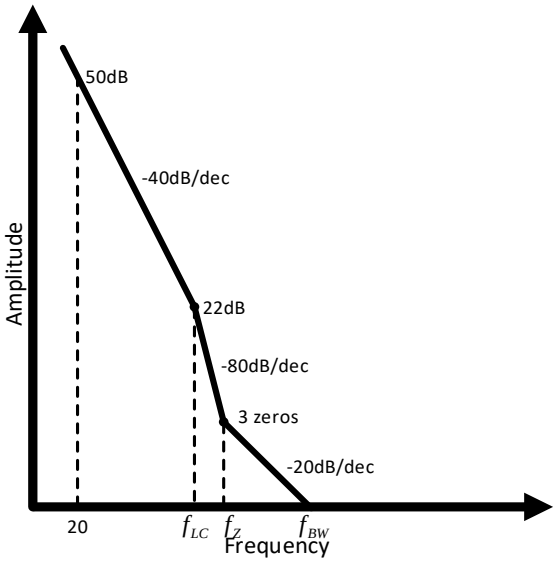

Figure 2.5 Loop gain after compensation scheme (d).

2.2.1 Compensation for Stability

Compensation zeros are used to provide phase lead in the feedback loop; for more phase margin, the zeros should be placed farther from f_{BW}. Assuming that those three compensation zeros are at the same frequency, with second order loop filter and in-loop LC, the phase margin is

$$3\times\arctan(\frac{f_{BW}}{f_Z})-180° \tag{2.2}$$

Where f_{BW} is the unity-gain bandwidth of the feedback loop, f_Z is the frequency of compensation zeros. With all the feedback loop information (loop gain, loop order, poles and zeros) above, Figure 2.5 shows a draft Bode plot of the compensated loop gain, where only f_{BW} and f_Z are unknown; thus, the constrain between f_{BW} and f_Z is

$$50dB-40\log(\frac{f_{LC}}{20kHz})-80\log(\frac{f_Z}{f_{LC}})-20\log(\frac{f_{BW}}{f_Z})=0 \tag{2.3}$$

$$f_Z^3 f_{BW} = 12.59 f_{LC}^4 \quad (2.4)$$

For at least 60° phase margin, by combining (2.2) and (2.4), the lower bound of f_{BW} is 734kHz.

2.2.2 Compensation for LC Tolerance

As shown on the left side of Figure 2.6, feedback loop gain varies with LC components value; consequently, f_{BW} changes with f_{LC}. With smaller/larger LC value, f_{BW} is higher/lower.

The quantitative relationship between LC resonance frequency spread ($\Delta f_{LC}, in\ dec$) and unity-gain bandwidth variation ($\Delta f_{BW}, in\ dec$) is shown on the right side of Figure 2.6. In this loop gain bode plot, the slope difference before and after LC is 40dB/dec; thus, the amplitude difference between small and big LC is $\Delta f_{LC} \times 40dB/dec$. Because the loop gain is ended with -20dB/dec slope, Δf_{BW} is two times of Δf_{LC} in decade; hence, bandwidth variation is the square of LC resonance frequency spread. Moreover, this relationship is independent from the exact position of zeros and poles, as long as the zero-crossing slope of loop gain is -20dB/dec.

With the relationship above, for ±20% inductance and ±20% capacitance spread, f_{BW} varies from 69% nominal to 156% nominal; and the maximum allowable f_{BW} is f_{PWM}/π; therefore, the upper bound of nominal f_{BW} is 816kHz.

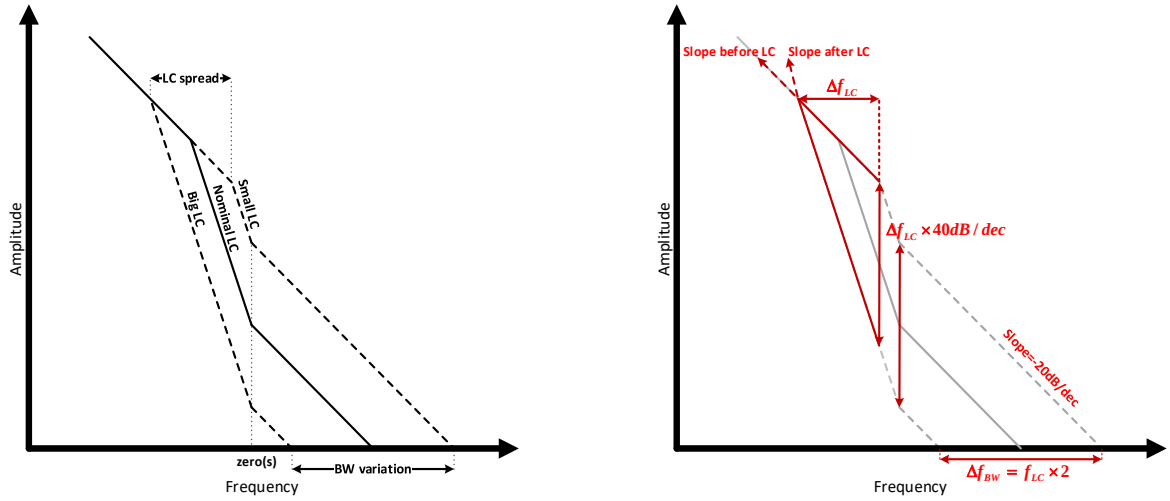

Figure 2.6 LC spread and bandwidth variation relationship.

2.2.3 Compensation Scheme

From 2.2.1 and 2.2.2, the available unity-gain bandwidth range is from 734kHz to 816kHz. In this thesis, f_{BW} is designed as 800kHz; f_Z is 130kHz to achieve 62° phase margin.

2.3 Loop Filters Implementation

Loop filters are used to implement the compensation scheme above, and the breakdown of total loop gain in the Bode plot is shown in Figure 2.7. The first loop filter is an integrator with one compensation zero at f_Z, and the second loop filter is an integrator with two compensation zeros at f_Z and one band-limiting pole at f_P. The gain of the output stage and feedback network are fixed.

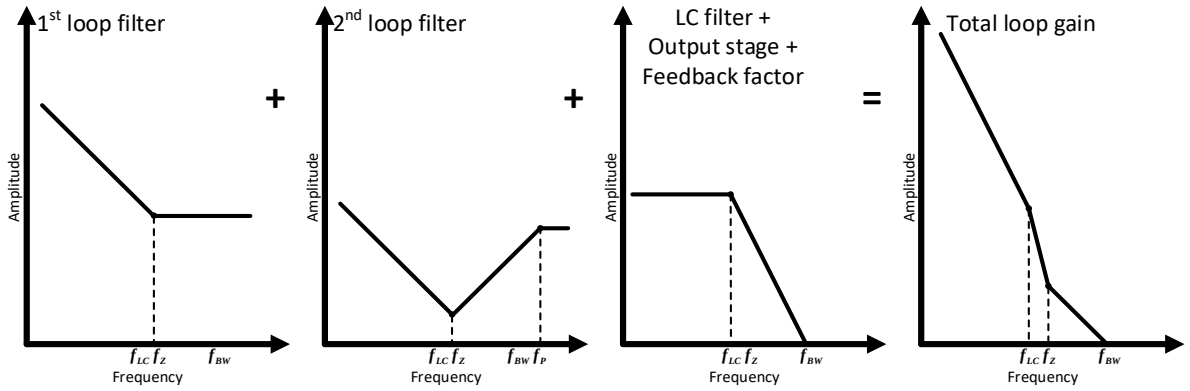

Figure 2.7 Loop gain breakdown.

2.3.1 RC feedback network design

The transfer function of loop filters depends on the RC network, Figure 2.8 illustrates the system block diagram with detailed loop filters.

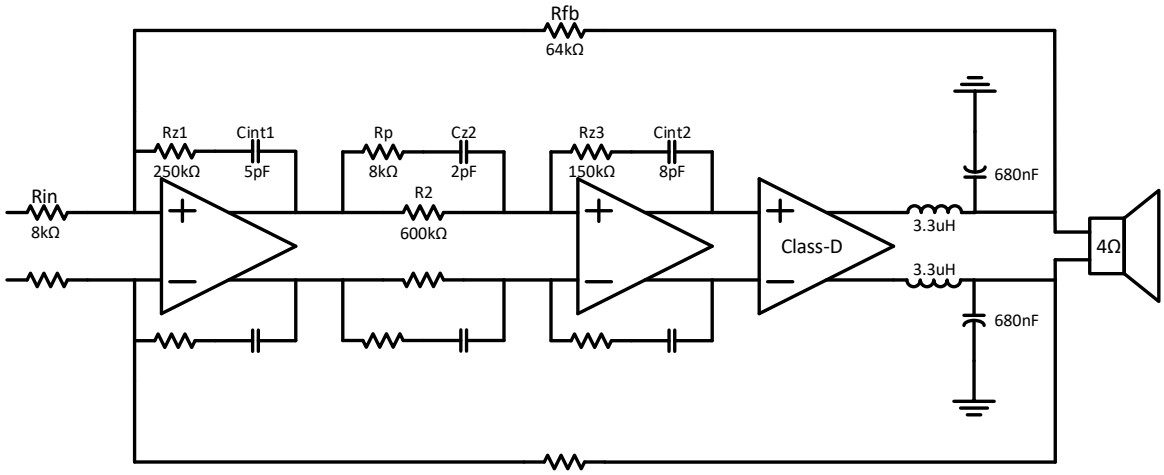

Figure 2.8 Closed-loop class-D amplifier with detailed loop filter.

The transfer function of the first loop filter is

$$\frac{R_{Z1}}{R_{in}} \times \frac{s + \frac{1}{R_{Z1}C_{\text{int1}}}}{s} \tag{2.5}$$

The transfer function of the second loop filter is

$$\frac{R_{Z3}}{R_P} \times \frac{(s + \frac{1}{R_{Z3}C_{\text{int2}}})(s + \frac{1}{R_2 C_{Z2}})}{s(s + \frac{1}{R_P C_{Z2}})} \tag{2.6}$$

At low frequency (below f_Z), both of the loop filters are integrators, $R_{in}C_{int1}$ and R_2C_{int2} defines the loop gain. At middle frequency (f_Z to f_P), the first loop filter is a proportional amplifier with a gain of R_{Z1}/R_{in}; while the second loop filter is a differentiator, whose gain is set by C_{Z2} and R_{Z3}. At high frequency (above f_P), the first loop filter is still a proportional amplifier as it is in middle frequency; and the second loop filter is also a proportional amplifier with a gain of R_{Z3}/R_P. The design considerations and trade-offs are as follows:

- Input resistance R_{in} is a trade-off between noise and drivability: smaller R_{in} is favorable to reduce noise; while larger R_{in} is easier to be driven by the proceeding stage.
- The band-limiting pole f_P ($R_P C_{Z2}$) is designed for system and local stabilities. For system stability, to avoid lagging the phase, f_P should be significantly higher than f_{BW}; but for the local stability of the second loop filter, f_P should be lower than the second pole (f_{P2}) of the opamp, as shown on the right side of Figure 2.9.
- Since f_P is at high frequency, C_{Z2} is the major capacitive load of the first opamp; R_2 and C_{Z2} form a compensation zero at f_Z. To reduce C_{Z2}, R_2 should be large. But large resistors introduce more parasitic capacitance, which lags the phase, destabilizes the feedback loop.
- Due to the band-limiting pole f_P and differentiating feature, the second loop filter exhibits more bandwidth than the first one, as shown in Figure 2.9; to relax the second opamp design, the second loop filter high frequency gain (R_{Z3}/R_P) should be lower than the first one (R_{Z1}/R_{in}).

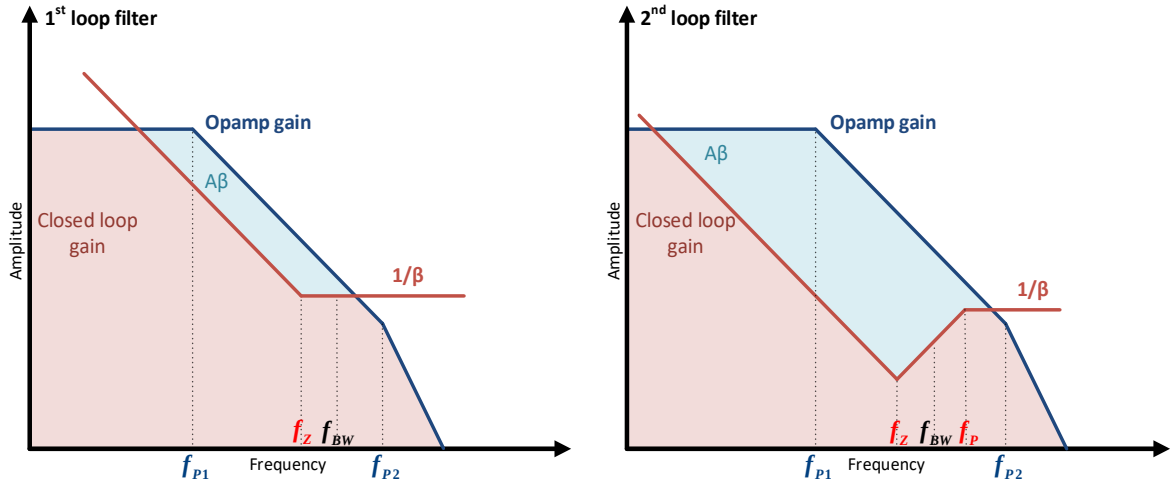

Figure 2.9 Loop filters local feedback analysis.

2.3.2 Opamp Design

In the loop filters, opamps are used to produce sufficient and stable gain for implementing transfer functions (2.5) and (2.6); the required frequency responses of opamps are shown in Figure 2.9. For the first opamp, $f_{P2} > f_Z$ is the guarantee of stability, and the phase lead of the first loop filter depends on the ratio of f_{BW} to f_Z. For the second opamp, $f_{P2} > f_P$ ensures the stability, and the phase lead of the second loop filter depends on the ratios of f_{BW} to f_Z and f_P to f_{BW}.

Both of the opamps are general-purpose with the same input/output common mode (CM) voltage; hence, they can share the same topology, as shown in Figure 2.10.

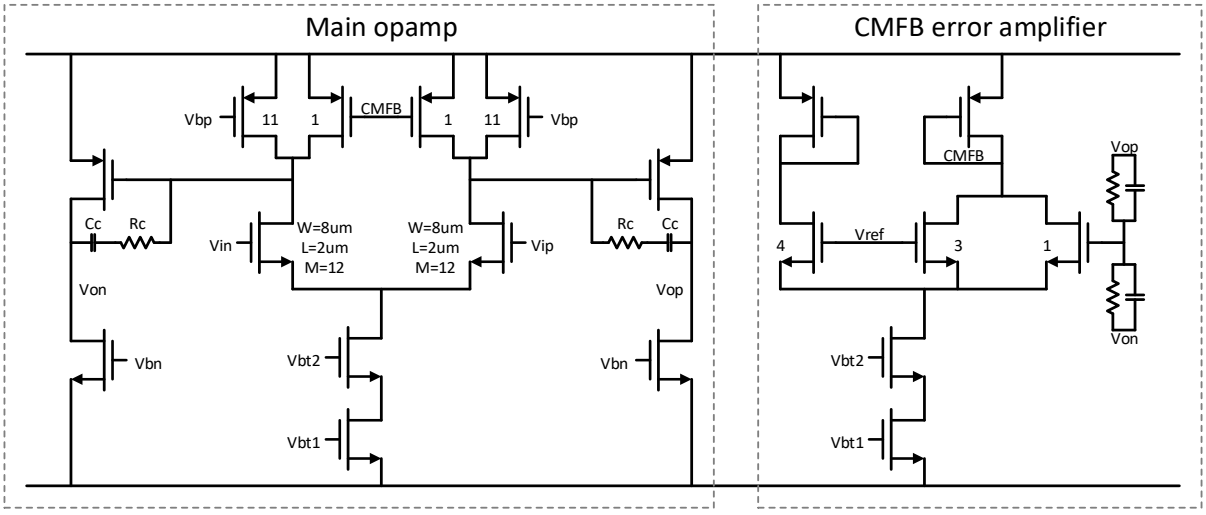

Figure 2.10 Opamp schematic.

For common mode feedback (CMFB) stability, the first stage tail current source is cascoded to increase output impedance, which degenerates CM gain; also, both the

first stage PMOS current source and the CMFB error amplifier input pair are split to further reduce the CMFB loop gain.

Because of the lack of chopping, flicker noise of the first opamp is a significant contributor to audio in-band noise. To achieve the target SNR, the input pair of the first opamp should be made large. However, large input capacitance forms a low-frequency parasitic pole with input resistance, which impairs system stability. Its sizing (W=8um*12, L=2um) is chosen as a trade-off between the two requirements.

2.4 Simulations and conclusions

With linearized class-D amplifier model, the feedback loop gain can be simulated by AC stability analysis. Loop gain Bode plots over LC spread are shown in Figure 2.11.

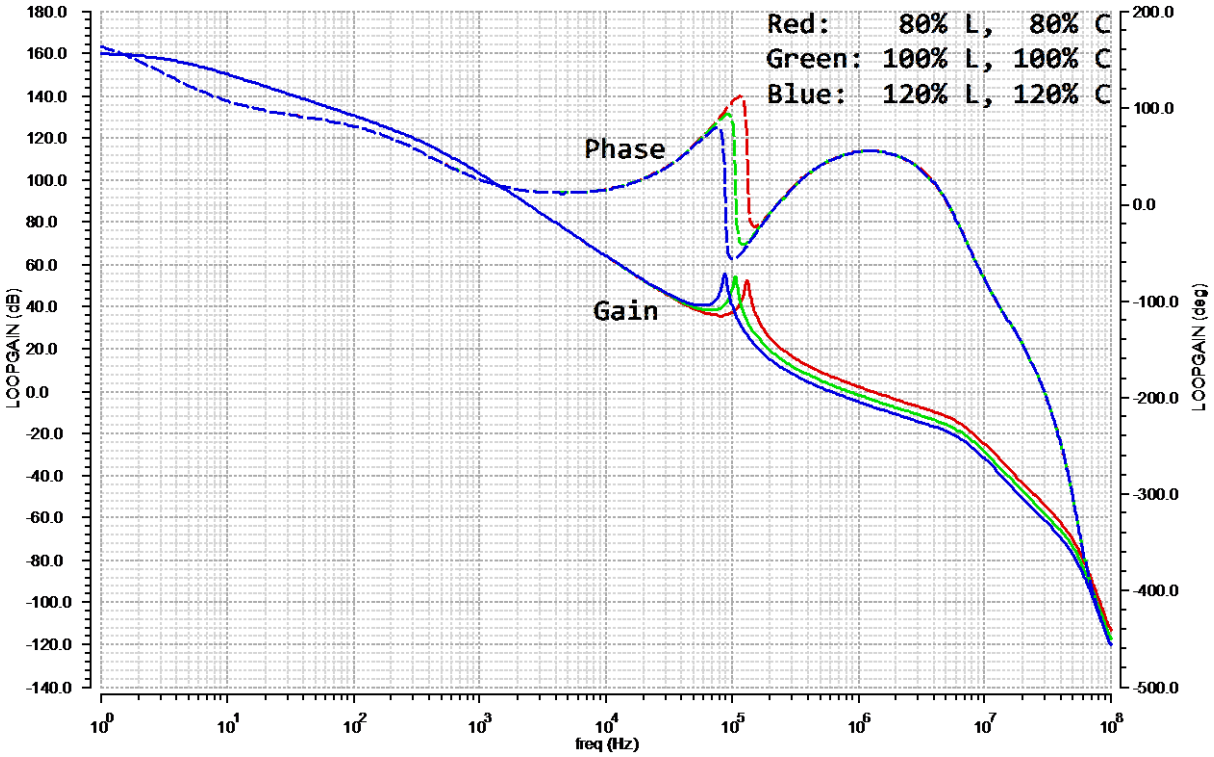

Figure 2.11 Loop gain over LC spread.

Bandwidth and phase margin over LC spread are summarized in Table 2.1. Over ±20% inductance and ±20% capacitance spread, the feedback loop is stable; Δf_{LC} is 0.17dec and Δf_{BW} is 0.33dec, which agrees with the conclusion in 2.2.2 that $\Delta f_{BW} = 2 \times \Delta f_{LC}$.

Table 2.1 Bandwidth and phase margin over LC spread.

Inductance	Capacitance	f_{LC}	f_{BW}	Phase margin
80% nominal	80% nominal	133kHz	1.27MHz	54.93°
100% nominal	100% nominal	106kHz	830kHz	51.94°
120% nominal	120% nominal	89kHz	598kHz	45.03°

Figure 2.12 shows loop gain Bode plots over corners, it is obvious that the loop gain exhibits more variation over corners than the variation over ±20% LC spread.

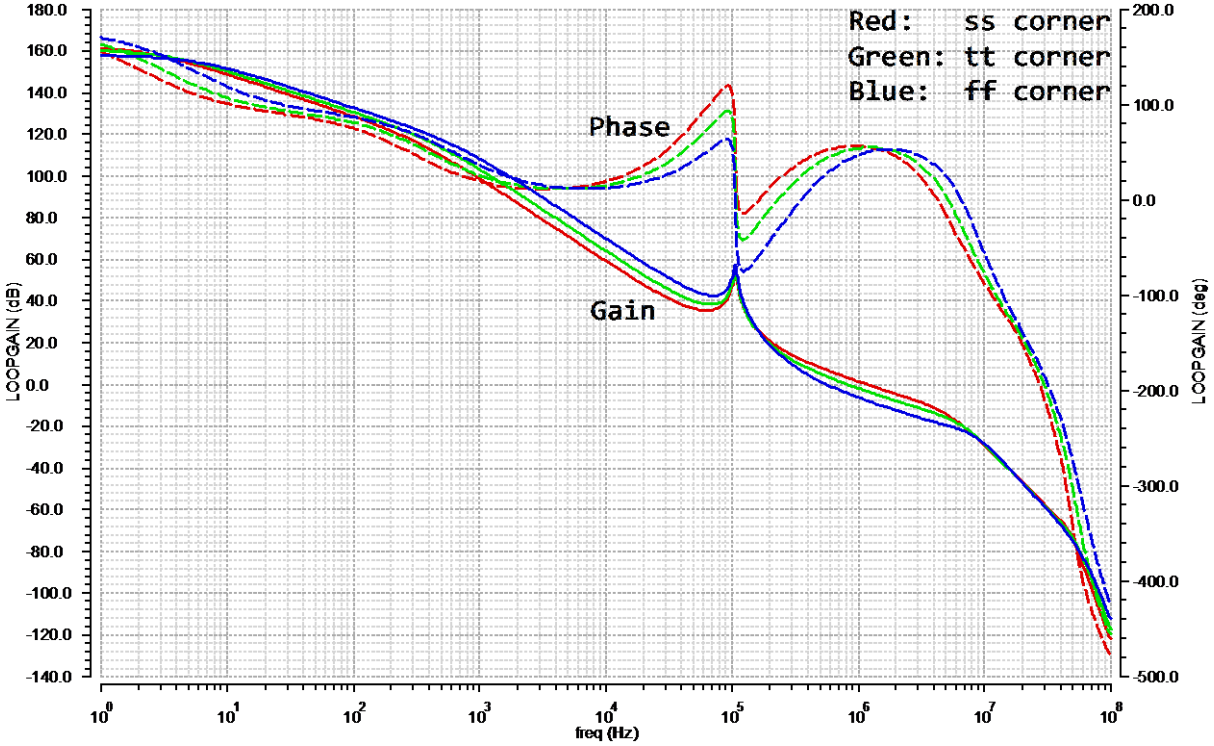

Figure 2.12 Loop gain over corners.

Bandwidth and phase margin over corners are summarized in Table 2.2. In the ff corner, phase margin is low, therefore, trimming is necessary to ensure stability.

Table 2.2 Bandwidth and phase margin over corners.

Corner	f_{BW}	Phase margin
ss	1.19MHz	55.30°
tt	830kHz	51.94°
ff	566kHz	27.11°

In Figure 2.12, loop gain variance over corners is only ±5dB; thus, one-bit trimming is sufficient, which modifies one of the compensation zeros by changing the resistor Rz3. The trimming scheme is illustrated in Figure 2.13.

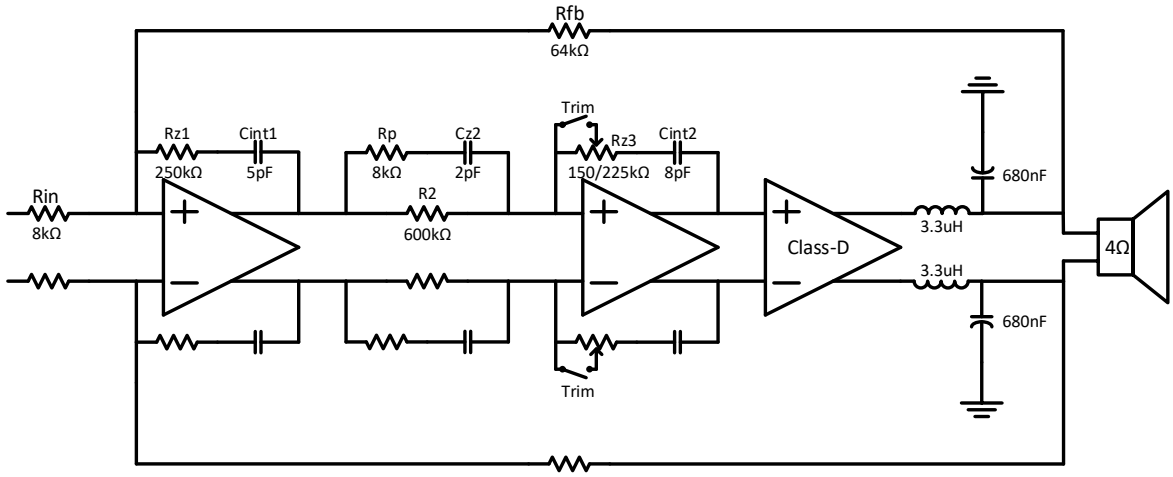

Figure 2.13 One-bit trimming scheme.

In the ff corner, Bode plots before and after trimming are shown in Figure 2.14, where f_{BW} is 761kHz, phase margin is 44.16°.

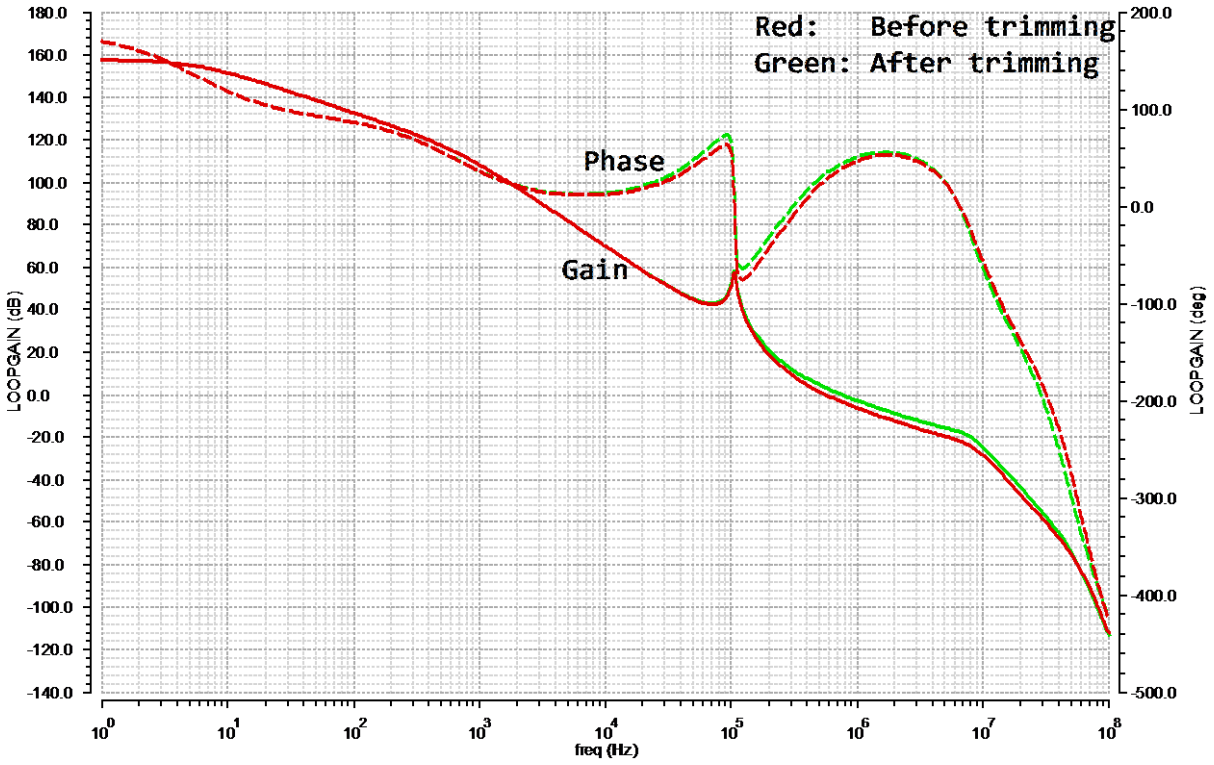

Figure 2.14 Loop gain before/after trimming in the ff corner.

Compared to the calculated compensation scheme in 2.2.3, the phase margin is 10° smaller. The band-limiting pole f_P (10MHz), which is essential for the second loop filter local stability, lags the phase by 4.6° at f_{BW}; besides, the input resistance (8kΩ) and

the first opamp input capacitance (1pF) forms a pole at 20MHz, which lags the phase by 2.3° at f_{BW}; the rest 3° phase is lagged by other parasite capacitance and resistance in the RC network.

Chapter 3 Modulation Scheme

Modulation scheme is the key factor to realize the essence of this thesis — low idle power consumption. After introducing modulation modes, this chapter elaborates on push-pull modulation and pulse-skipping modulation. This is followed by the design of comparator, which is the core part of the modulator. The chapter ends with simulation results and conclusions.

3.1 Modulation Modes Introduction

Modulation methods for class-D amplifiers can be classified into two types: time-domain modulations (PWM, PSM, PDM, etc.), and common-mode modulations (AD, BD, push-pull, etc.). In this thesis, the proposed class-D amplifier employs PWM and PSM for time-domain modulations, push-pull for common-mode modulation. With the multi-level output stage, this class-D amplifier has three operation modes:

- Low voltage PSM (LV PSM): The low voltage output stage generates fixed-width pulses whose density is proportional to the input signal level.
- Low voltage PWM (LV PWM): The low voltage output stage generates pulse width modulated signal at a fixed frequency (f_{PWM}).
- High voltage PWM (HV PWM): The high voltage output stage generates pulse width modulated signal at a fixed frequency (f_{PWM}).

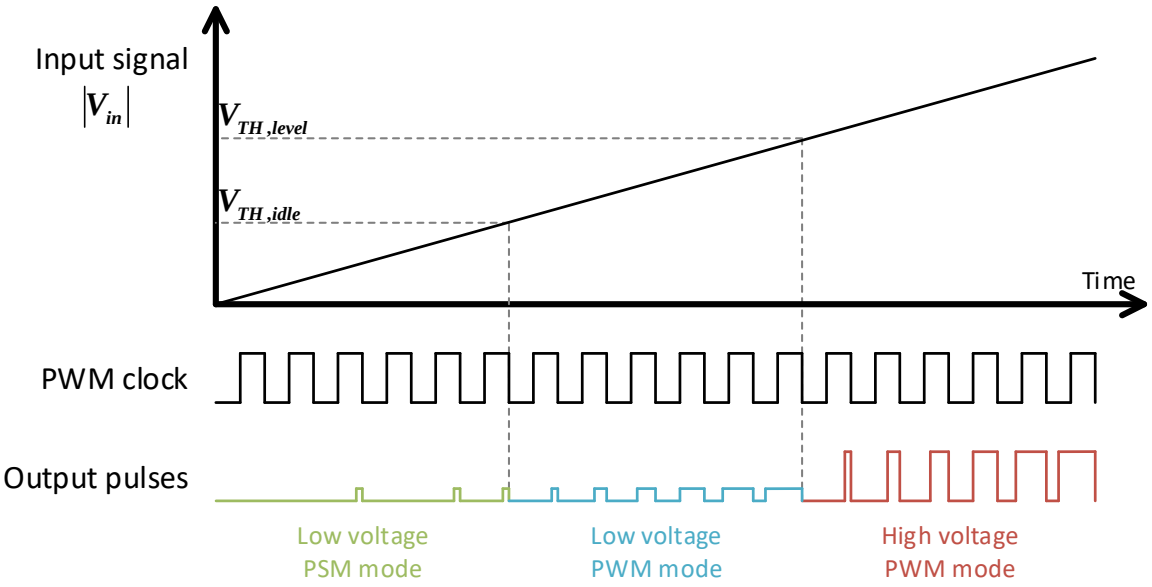

Figure 3.1 Three modulation modes division.

Figure 3.1 shows the three modulation modes. The absolute value of the input signal ($|V_{in}|$) is compared with $V_{TH,level}$ and $V_{TH,idle}$ ($V_{TH,level} > V_{TH,idle}$). When the input signal is smaller than $V_{TH,idle}$, the class-D amplifier works in the low voltage PSM mode to save idle power; when the input signal is intermediate between $V_{TH,idle}$ and $V_{TH,level}$, the class-D amplifier works in the low voltage PWM mode to improve linearity; when the input signal is larger than $V_{TH,level}$, the class-D amplifier works in the high voltage PWM mode to achieve high efficiency.

3.2 Push-Pull Modulation

3.2.1 Introduction

A push-pull modulator generates two trains of pulses in a push-pull manner. The key idea is that only half of the output stage is switching at any time.

Figure 3.2 shows the modulation mechanism of an inverting push-pull modulator, unlike that in AD or BD modulation, the triangle wave for push-pull modulation swings from loop filter minimum output level to CM output level. The differential outputs of the loop filter are compared against the triangle wave by two comparators. Therefore, after the LC filter, output terminals produce rectified waves alternatively, from which the audio signal can be obtained by taking the output voltage differentially.

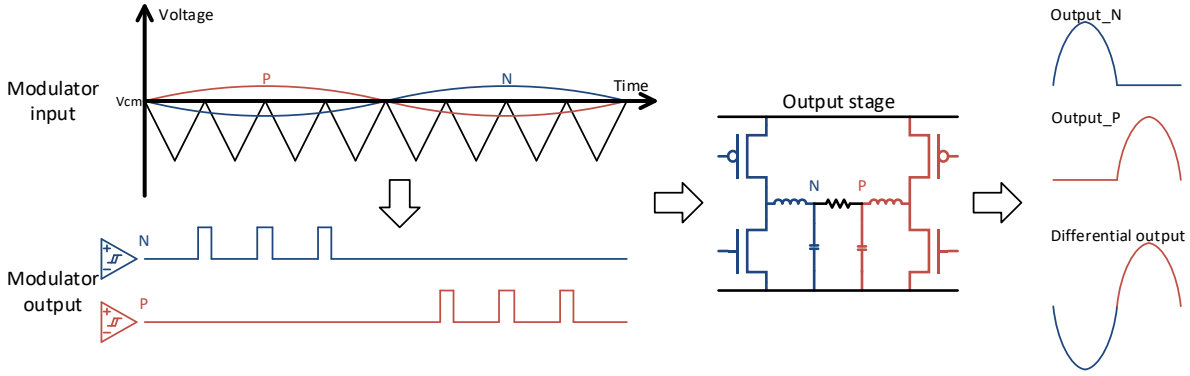

Figure 3.2 Push-pull modulation mechanism.

3.2.2 Dead Band in Push-pull Modulation

When the top of the triangle wave is misaligned with the loop filter CM output, a dead band problem occurs as shown in Figure 3.3, where the misalignment depends on the loop filter output CM and comparator offset.

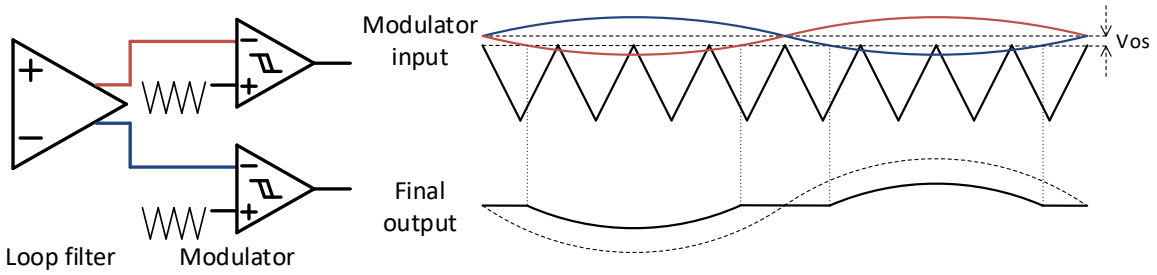

Figure 3.3 Push-pull modulation misalignment.

Figure 3.4 shows the spectra of dead band distortion in an ideal, open-loop class-D amplifier. Because the loop filter is second order, the roll-off of odd-order harmonics is 20dB/dec slower than the roll-off of loop gain, which indicates that the dominant tone in the audio band is at the maximum frequency (20kHz).

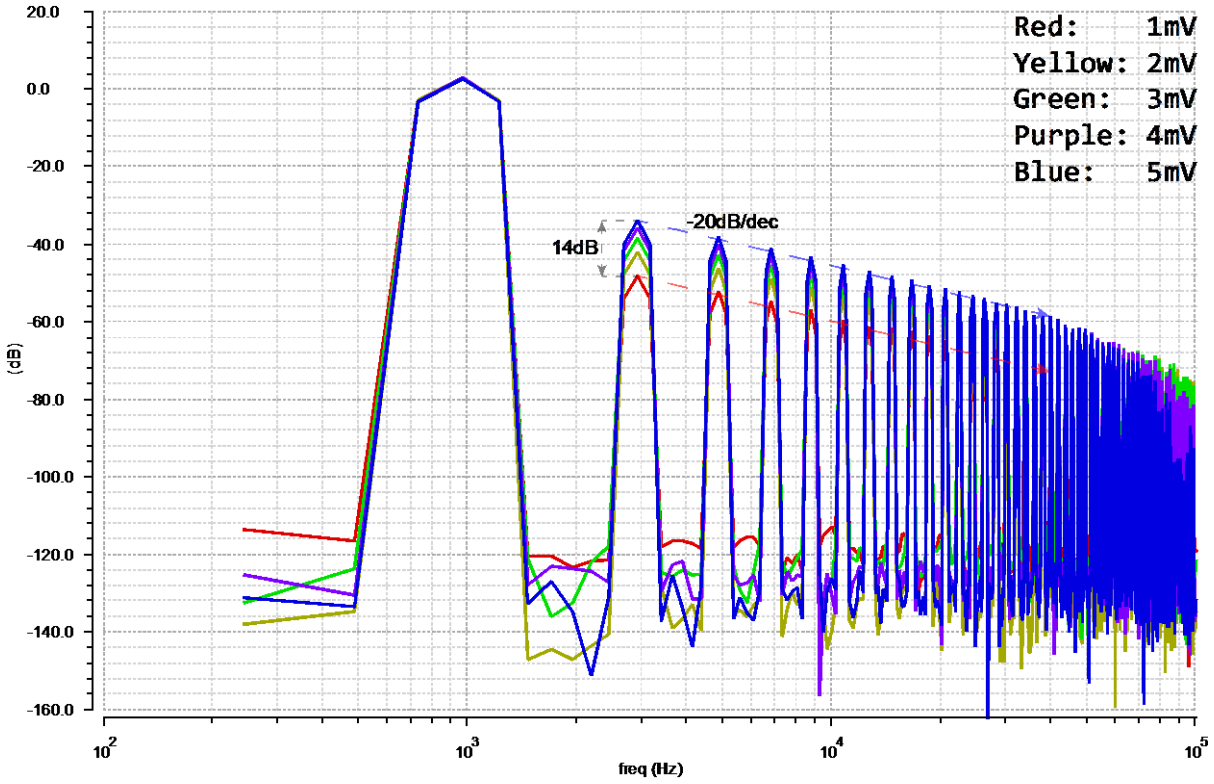

Figure 3.4 Spectra of dead band distortion over modulation misalignment.

Figure 3.5 plots harmonic distortion at 20kHz (HD20) over modulation misalignment in an ideal, open-loop class-D amplifier. With increased misalignment, HD20 is saturated to -50dB, which equals to the HD20 of the output stage (Figure 2.2). Therefore, modulation misalignment will not pose a serious distortion problem. Besides, in this thesis project, the triangle wave is generated externally, modulation misalignment can be eliminated by adjusting the DC offset of the triangle wave.

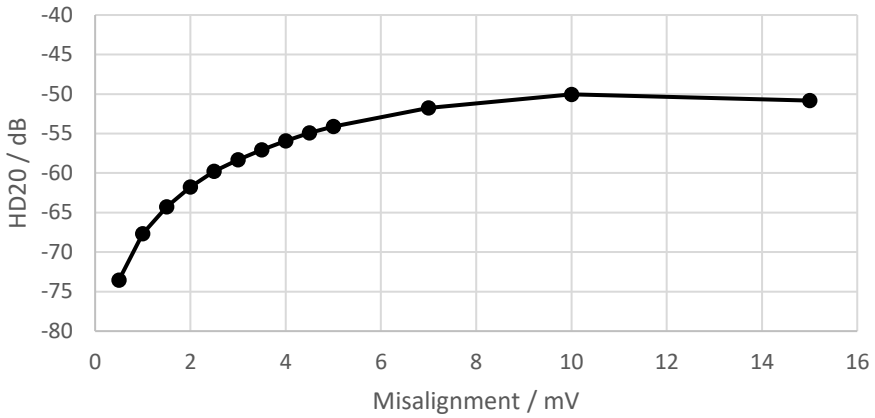

Figure 3.5 Harmonic distortion at 20kHz over modulation misalignment in an ideal amplifier.

3.3 Pulse-Skipping modulation

3.3.1 Introduction

In a PWM based class-D amplifier, small input signals, such as noise and offset, will be modulated into narrow pulses every cycle. To reduce switching loss in idle and near-idle states, the modulator should skip some narrow pulses, and output wider pulses only occasionally instead. Thus, pulse skipping modulation is introduced.

For simplicity, Figure 3.6 demonstrates a single-ended PSM modulator and its related waveforms. In contrast to PWM that compares the loop filter output signal with a triangle wave, PSM compares the loop filter output signal with a DC threshold (Vcm-Vth). With a small input signal, the load slowly discharges integration capacitors of the loop filter; when the loop filter output drops below the threshold, the modulator produces a short pulse, which charges the integration capacitors at a much higher rate. Hence, the switching frequency is proportional to the input signal level, idle power is reduced significantly.

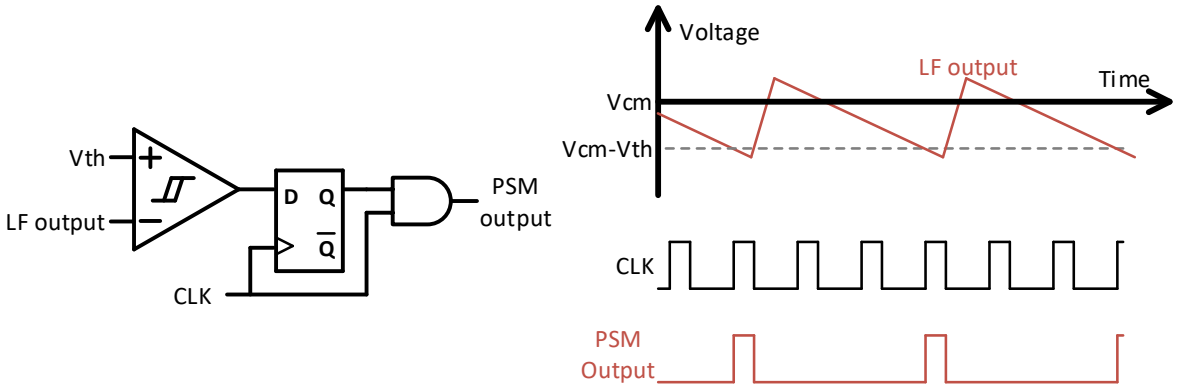

Figure 3.6 Single-ended pulse skipping modulation.

However, in the idle state, the loop filter output can exceed Vth due to noise, which increases switching loss. To address this problem, the PSM modulator employs a D flip-flop to synchronize comparator output pulses with a clock signal. This synchronization functions as a sample-and-hold, which offers low-pass filtering for noise.

In the actual circuit, both the loop filter and the PSM modulator are fully differential; thus, fully differential loop filter output signals always fluctuate in between Vcm±Vth. According to control theory, PSM is a typical kind of hysteretic control (bang-bang control), which is non-linear but inherently stable [25]. In this class-D amplifier design, PSM is only used to produce small signals near zero-crossings, which has a negligible impact on large-signal linearity performance.

3.3.2 Small Signal Linearity and Idle Power

In a class-D amplifier, total harmonic distortion plus noise (THD+N) in the audio band is expected to be dominated by noise under small input conditions. But the PSM modulator exhibits more distortion with higher Vth because the fluctuation amplitude of the loop filter output is higher [26].

Wide-band thermal noise from the loop filter is a stochastic signal centered at Vcm, whose amplitude follows Gaussian distribution. Increasing Vth helps to reduce idle power, because noise is less likely to generate PSM pulses.

Therefore, Vth is a trade-off between idle power and small-signal linearity. Figure 3.7 illustrates idle power and THD over PSM Vth, where the signal is small (0.8mW output power) and fully pulse skipping modulated. A Vth of 10mV balances THD and audio band noise, but idle power is highly sensitive to Vth at this point: a small variation of Vth can lead to a significant change in idle power. To guarantee low idle power consumption, which is the primary objective of this thesis project, Vth is designed as 15mV; in this case, distortion is 3dB higher than audio in-band noise, which is acceptable.

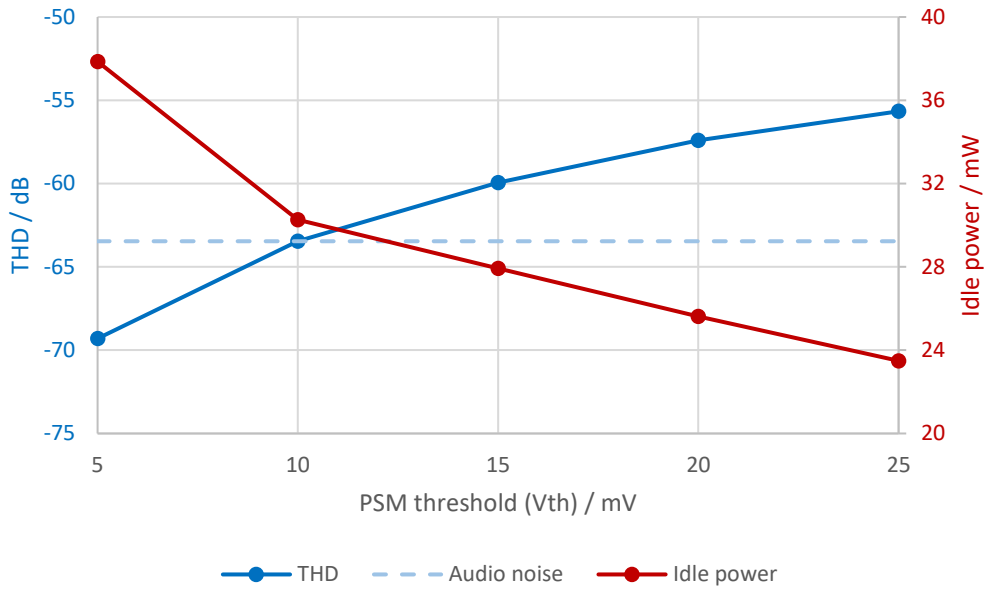

Figure 3.7 Idle power and small signal THD over PSM threshold.

3.4 Comparator Design

3.4.1 Introduction

Comparators are the core parts of the modulator, which generate pulses and determine the modulation modes. The requirements are as follows.

- The comparators should be able to handle a common-mode input range of 900mV to 150mV, which is the range of Vcm to Vmin in Figure 3.8.
- For pulse generation, the comparators are required to produce pulses shorter than 16ns, which is the minimum pulse width of the output stage.
- As described in 3.1, the comparators determine modulation modes by comparing system input signal with two DC thresholds; the offset voltage of comparators is supposed to be less than $0.5V_{TH,idle}$ (2.5mV).

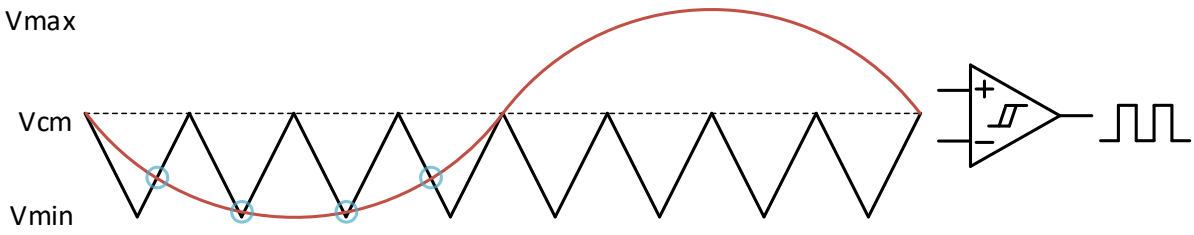

Figure 3.8 Input signals of a push-pull modulator.

3.4.2 Circuit Implementation

The proposed comparator employs a three-stage structure. The first stage accepts a wide input CM range and has a fixed output CM. The second stage offers high gain and large output swing. The third stage is an inverter-based driver.

The first stage design is illustrated in Figure 3.9, where a folded cascode structure is employed to support the required input CM range. To fix the common-mode output level, the first stage should be designed for high common-mode rejection. Hence, the load employs a cross-coupled pair and diodes in parallel [27].

For the differential signal, the diodes act as positive resistors, while the cross-coupled transistors act as negative resistors. The negative resistance cancels the positive, thus presenting a high differential output impedance. For the common-mode signal, the cross-coupled transistors also act as diodes, which results in a low common-mode output impedance. The common-mode output voltage is stabilized at one Vgs below the positive power supply.

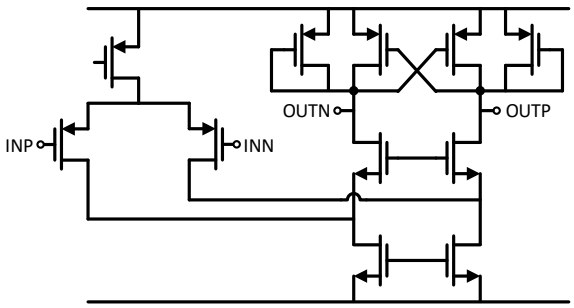

Figure 3.9 The first stage of the proposed comparator.

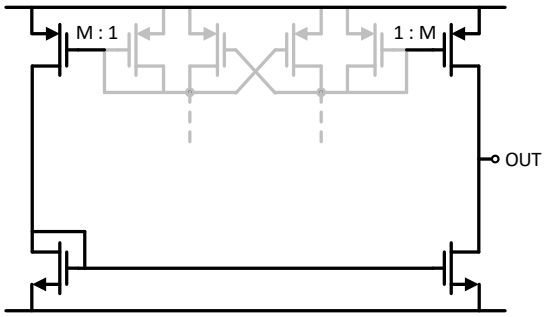

Figure 3.10 The second stage of the proposed comparator.

The second stage design is shown in Figure 3.10, which employs three current mirrors. The PMOS current mirrors have a ratio of 1:M, hence increasing the transconductance and slew rate by a factor of M. This stage also offers a rail-to-rail output swing.

3.5 Simulations and Conclusions

3.5.1 Distortion due to Push-pull misalignment

Figure 3.11 plots THD of the closed-loop class-D amplifier over modulation misalignment, where millivolt-level misalignment only degrades the linearity by a few dB. This result confirms the inference in 3.2.2 that the modulation misalignment is not the dominant distortion source, given that the misalignment introduced by device mismatch is on the order of millivolts.

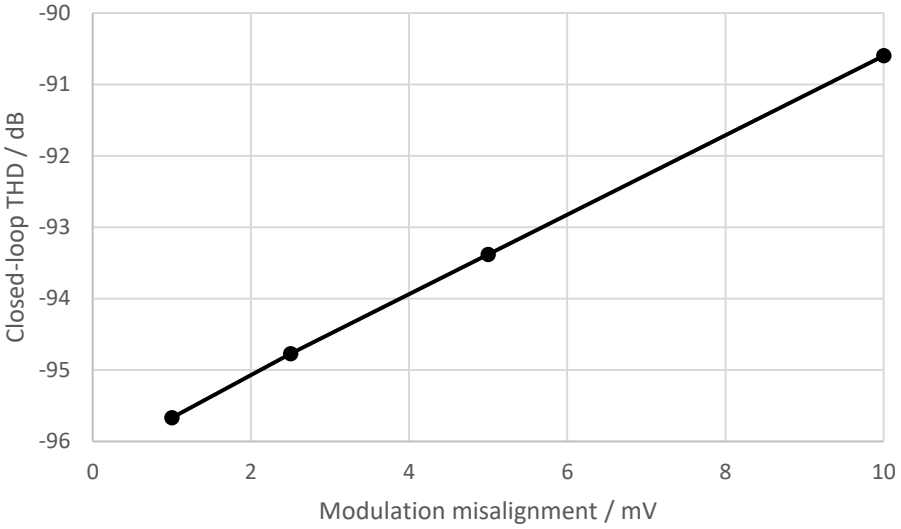

Figure 3.11 Closed-loop THD over modulation misalignment.

3.5.2 Distortion due to Modes Shifting

The full-scale input range is divided into three operation modes by two threshold voltages. To investigate the impact of shifting between modes, Figure 3.12 plots THD over input amplitude.

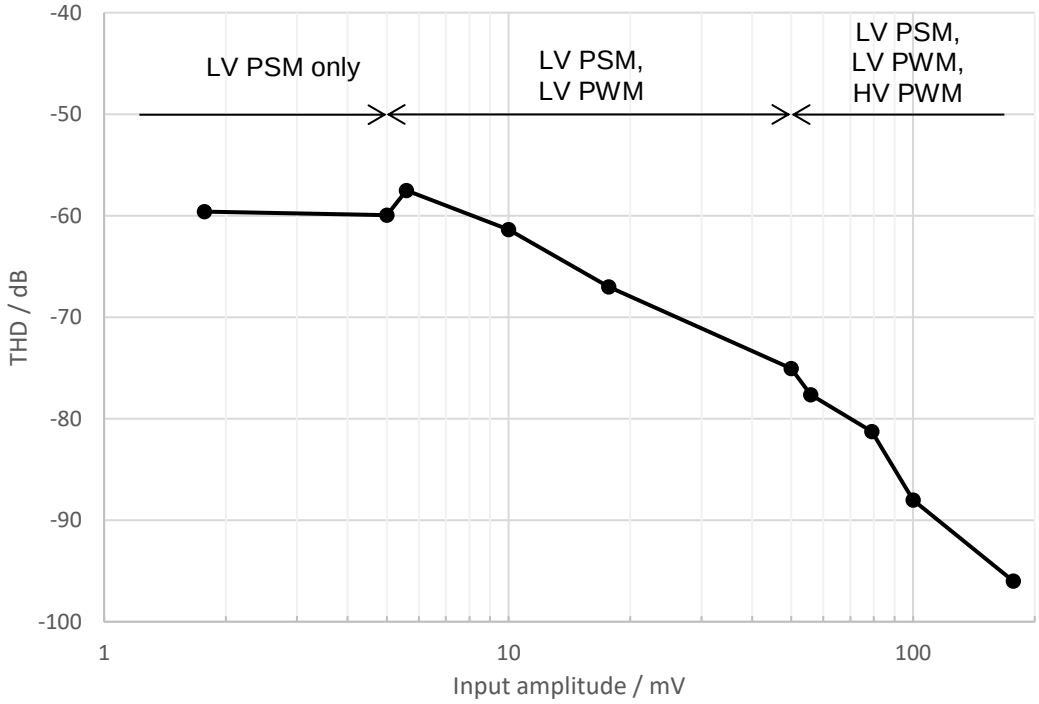

Figure 3.12 THD over input amplitude.

When input amplitude is lower than 5mV, the class-D amplifier operates in LV PSM mode only, THD is independent of input amplitude, but it is related to the PSM threshold (Vth) as discussed in 3.3.2.

When input amplitude is higher than 5mV but lower than 50mV, the class-D amplifier switches between LV PSM and LV PWM modes every input cycle. Hence, the class-D amplifier exhibits more distortion than the PSM-only mode, which is indicated by the THD peaking in Figure 3.12 (input amplitude = 5mV). Besides, the slope of the THD plot is -20dB/dec; this slope demonstrates that the distortion is from the transition itself, which is signal-independent.

When input amplitude is higher than 50mV, the class-D amplifier works in all three modes, two transitions happen during every input cycle. However, the THD plot around the transition point (50mV) is smooth. This is because the modulation method is the same before and after transition, only supply voltage is changed.

3.5.3 Impact of PSM on Large-signal Linearity

For an automotive audio amplifier powered by 14.4V battery, linearity of large signals is more important than that of small signals within the operation range of PSM.

Figure 3.13 plots the spectra of output signals (1kHz with 1W output power) with and without PSM mode. Closed-loop THD (20Hz-20kHz) is -96.41dB with PSM mode, and -98.44dB without PSM mode. PSM introduces more harmonics in the band of 30kHz to 100kHz, but the difference is small in the audio band.

This simulation result agrees with the conclusion in 3.3.1 that PSM does not impair large-signal linearity, given that the class-D amplifier only employs PSM to produce small signals.

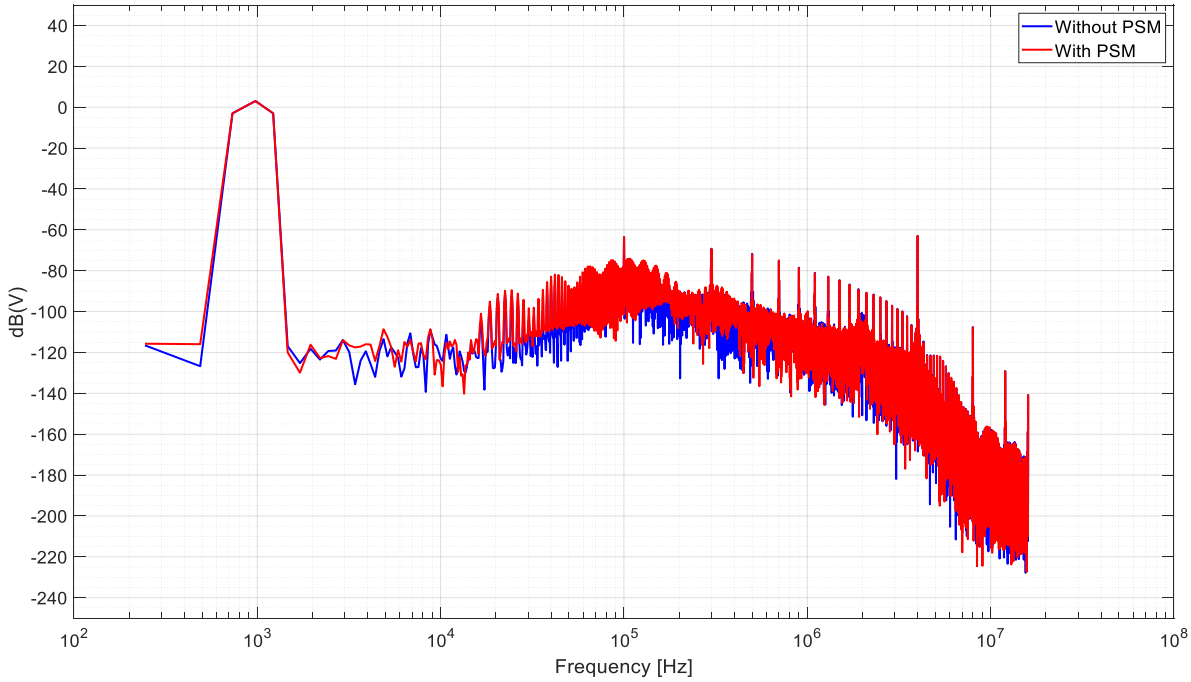

Figure 3.13 Large signal spectra with/without PSM.

Chapter 4 Common-Mode Regulation

In a push-pull class-D amplifier, a common-mode regulator is required to fix the potential at the input of the first opamp, so that the low-voltage loop filter can operate normally. This chapter starts with the motivation and objective of the proposed common-mode regulator. Then, it presents the dynamic element matching technique to solve the mismatch problem of the common-mode regulator. In the end, it shows simulation results and conclusions.

4.1 Introduction

4.1.1 Common-Mode Behavior in a Push-pull Amplifier

In a push-pull class-D amplifier, positive and negative output branches take turns producing output signals, which leads to a rectified output waveform in common-mode. Figure 4.1 illustrates the signal flow in a push-pull class-D amplifier, where the changing common-mode output is fed back to the virtual ground by a factor of 1/9.

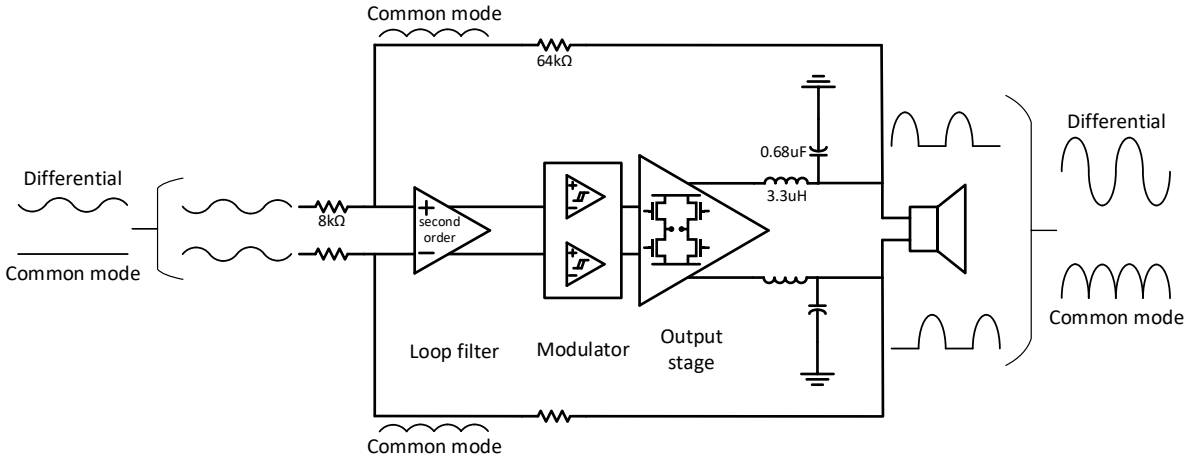

Figure 4.1 Signal flow in a push-pull class-D amplifier.

Because the output stage is powered by 14.4V, the common-mode output swings from 0 to 7.2V, which drives the virtual ground from 0.8V to 1.6V, given that the common-mode input is 0.9V DC. This signal-dependent common-mode voltage at virtual ground requires a more complicated opamp capable of dealing with large common-mode input range. High common-mode rejection is also required to ensure linearity.

4.1.2 Common-Mode Ringing Problem

In a class-D amplifier, the output LC low-pass filter is also a resonator, whose quality factor (Q) is given by (4.1), where R_L is the load resistance.

$$Q = R_L\sqrt{\frac{C}{L}} \tag{4.1}$$

From a common-mode perspective, the only load of the LC filter is the feedback resistor, thus resulting in a high Q factor. With pulses at the input, the LC filter exhibits high-Q ringing at the output, which also appears at the virtual ground through the feedback network. Due to the high quality factor, virtual ground ringing can easily exceed 2V, damaging the 1.8V devices in the loop filter.

4.1.3 Common-Mode Regulator Principles

To solve the aforementioned problems, Figure 4.2 illustrates the operation principle of the proposed common-mode regulator, which stabilizes the common-mode voltage at the virtual ground by removing common-mode current from these nodes. The common-mode regulator consists of a resistive common-mode sensor, an error amplifier, and two identical output stages that can both sink and source current.

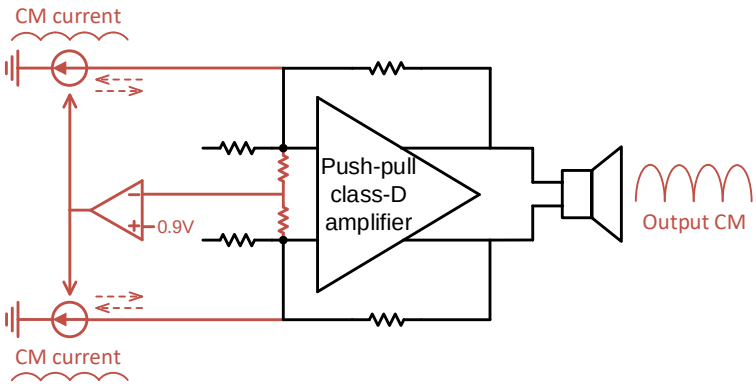

Figure 4.2 Common-mode regulator in a push-pull class-D amplifier.

Essentially, the common-mode regulator is a closed-loop common-mode voltage buffer. The reference voltage (0.9V) is fed into the non-inverting input, and the output is fed back to the inverting input. Therefore, the common-mode voltage at the virtual ground is stabilized by negative feedback.

4.2 Common-Mode Regulator with Mismatch

4.2.1 Distortion due to Mismatch

The common-mode regulator is supposed to operate in the common-mode domain only, which requires both of its output stages to sink or source the same amount of

current. However, with device mismatch in the output stages, signal-dependent differential current can be injected into the virtual ground, which results in distortion.

Figure 4.3 illustrates the impact of output stage mismatch in the common-mode regulator, where one output stage is stronger than the other. This asymmetric structure causes even-order harmonic distortion in the differential output signal, as shown in Figure 4.4.

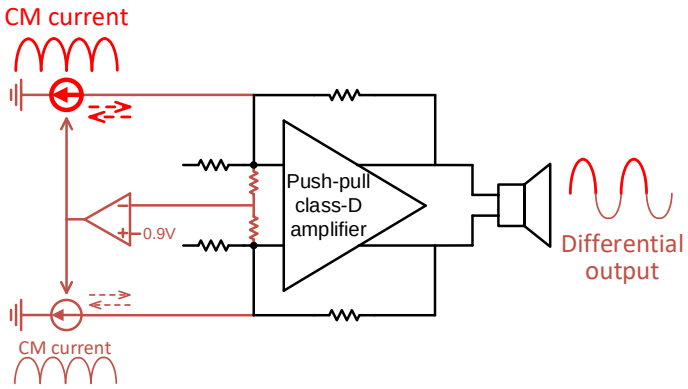

Figure 4.3 Common-mode regulator with mismatch.

In Figure 4.4, although the output stage of the common-mode regulator is large in size (PMOS, W=18um*4, L=18um; NMOS, W=12um*4, L=18um), THD of the differential output signal is -85.96dB (1kHz, 1W output power), which does not meet the targeted specification.

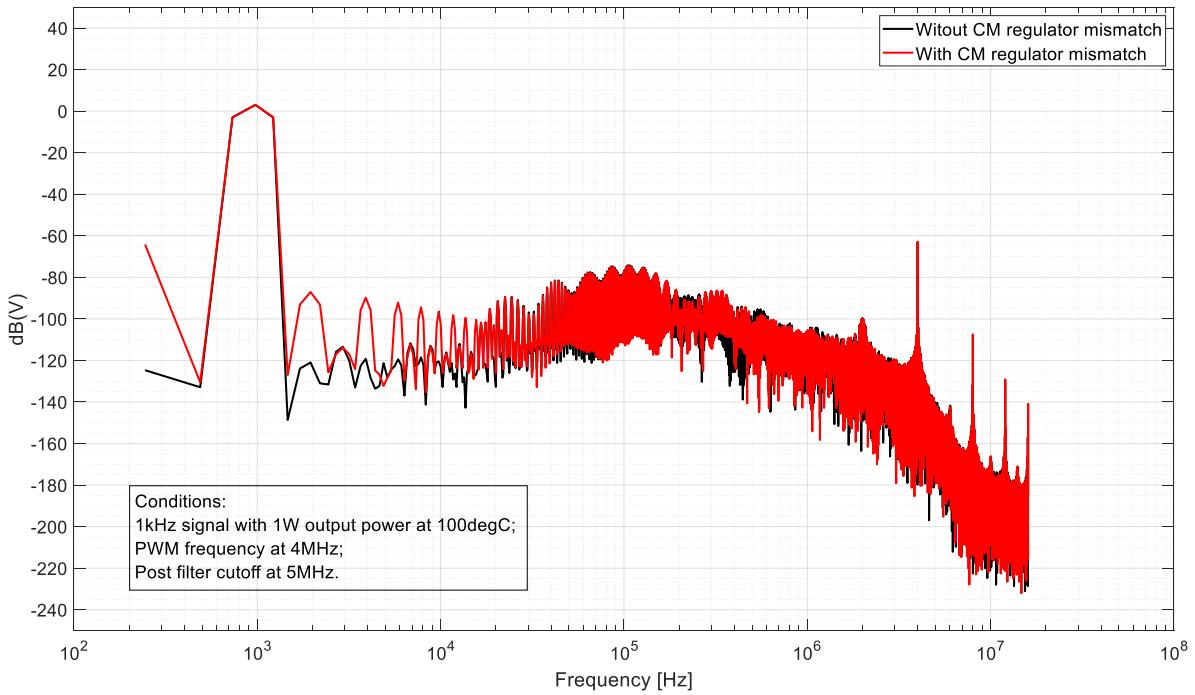

Figure 4.4 Output spectrum with CM regulator mismatch.

4.2.2 Dynamic Element Matching

To reduce distortion due to device mismatch, Figure 4.5 illustrates the dynamic element matching (DEM) technique applied to the output stages of the common-mode regulator. The two output stages are chopped, and the mismatch is averaged over time. In the frequency domain, DC mismatch is modulated to the clock frequency, which also results in a flicker noise reduction.

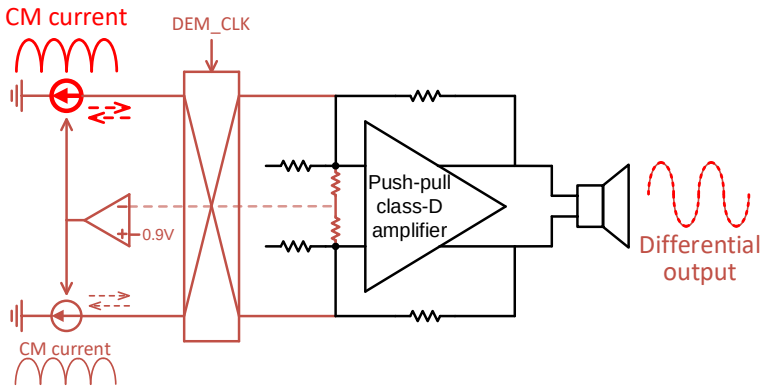

Figure 4.5 Common-mode regulator with DEM.

However, DEM technique injects differential ripple current into the virtual ground, which is proportional to the offset. Amplified by the loop filter, this ripple can disrupt the modulation and deteriorate system linearity. Thus, DEM should operate at a frequency where the loop filter has minimum gain. Figure 4.6 plots the frequency response of the loop filter. The DEM frequency is chosen to be 100kHz.

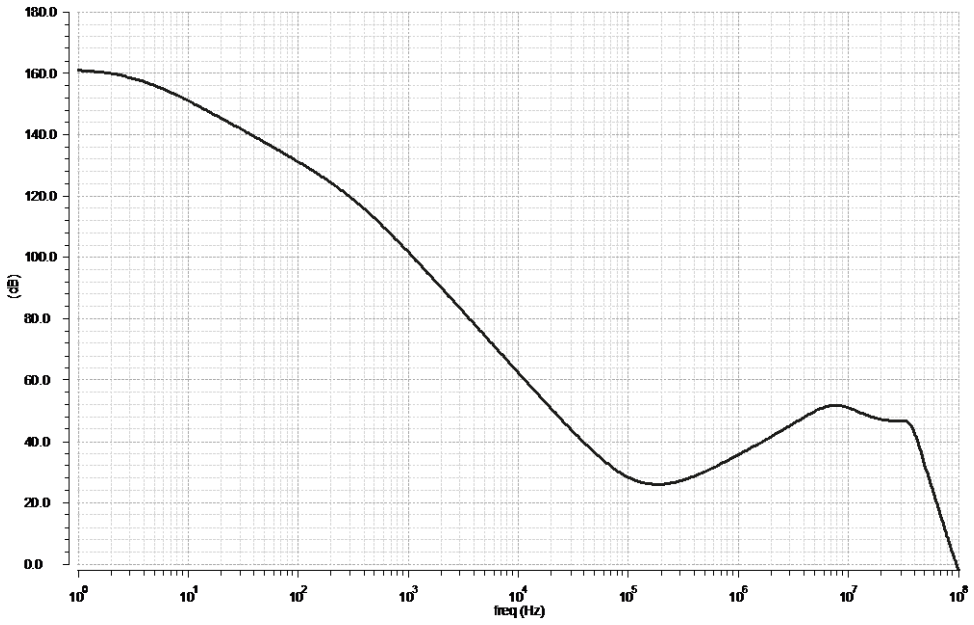

Figure 4.6 Frequency response of the loop filter.

4.3 Circuit Implementation

The schematic of the proposed common-mode regulator is illustrated in Figure 4.7, which includes a common-mode sensor, an error amplifier, and two identical class-AB output stages.

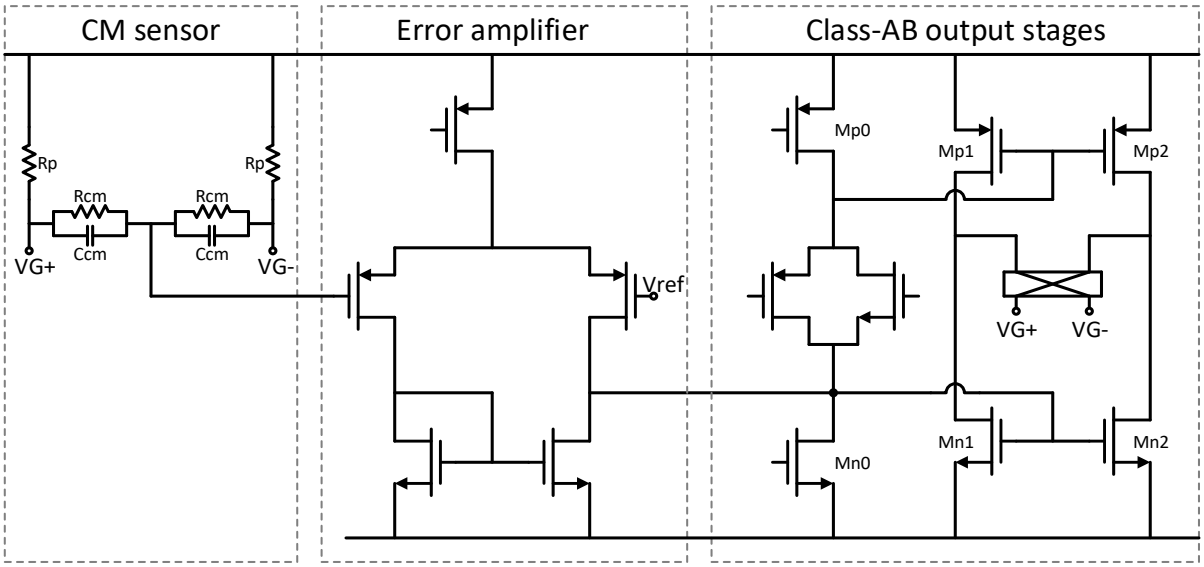

Figure 4.7 Common-mode regulator schematic.

The common-mode sensor extracts the common-mode voltage from virtual ground nodes by R_{cm} and C_{cm}, where R_{cm} offers low-frequency averaging, and C_{cm} offers high-frequency averaging. The error amplifier is a differential pair with an active load that provides high gain to the feedback loop. For sinking and sourcing current, Monticelli class-AB amplifiers [28] are employed as the output stages.

4.3.1 Output Stage Design

The output stage is the most critical part of the common-mode regulator, whose area is inverse proportional to the mismatch [29] and thus the distortion. Table 4.1 summarizes this relationship, where Vos is the 3-σ input-referred DC offset voltage, and THD is simulated with the corresponding mismatch in the output stage.

In the schematic level simulation, an area of 270um^2 can achieve the target THD specification (<-90dB). But a margin of 5dB should be left to ensure the THD after layout still meets the requirement. Therefore, the area of the output stage is designed to be 4320 um^2, leading to a THD that is close to the ideal case (without mismatch in the common-mode regulator).

Table 4.1 THD and mismatch over output stage area

Area / um^2	Vos / uV	THD / dB
270	842	-91.65
1080	423	-93.85
4320	220	-96.41
Without mismatch		-96.80

Because the common-mode regulator is connected to the virtual ground, low noise is a key requirement. Especially in the idle state, noise triggers the modulator, causing switching loss. Therefore, the class-AB output stages should exhibit low gm in the idle state, which requires low quiescent biasing current and small aspect ratio.

But sufficient gm of the output stage is required to keep the current sources (Mp0 and Mn0) in saturation under the worst conditions (sink 200uA, source 110uA). As a trade-off, gm of the PMOS and NMOS are designed as 30uS and 50uS respectively, quiescent biasing current (4uA) and aspect ratios (1/1 for PMOS, 2/3 for NMOS) are chosen accordingly.

In the idle state, the common-mode voltage of the system output is 0V. Two pull-up resistors (Rp) are employed to maintain 0.9V common-mode voltage at the virtual ground. The advantage is that passive pull-ups introduce less noise than the active circuit.

4.4 Simulations and Conclusions

Figure 4.8 plots the spectra of output signals under the following three conditions:

- Black curve is the spectrum without mismatch in the common-mode regulator;
- Red curve is the spectrum with 3-σ mismatch in the common-mode regulator;
- Blue curve is the spectrum with 3-σ mismatch and DEM.

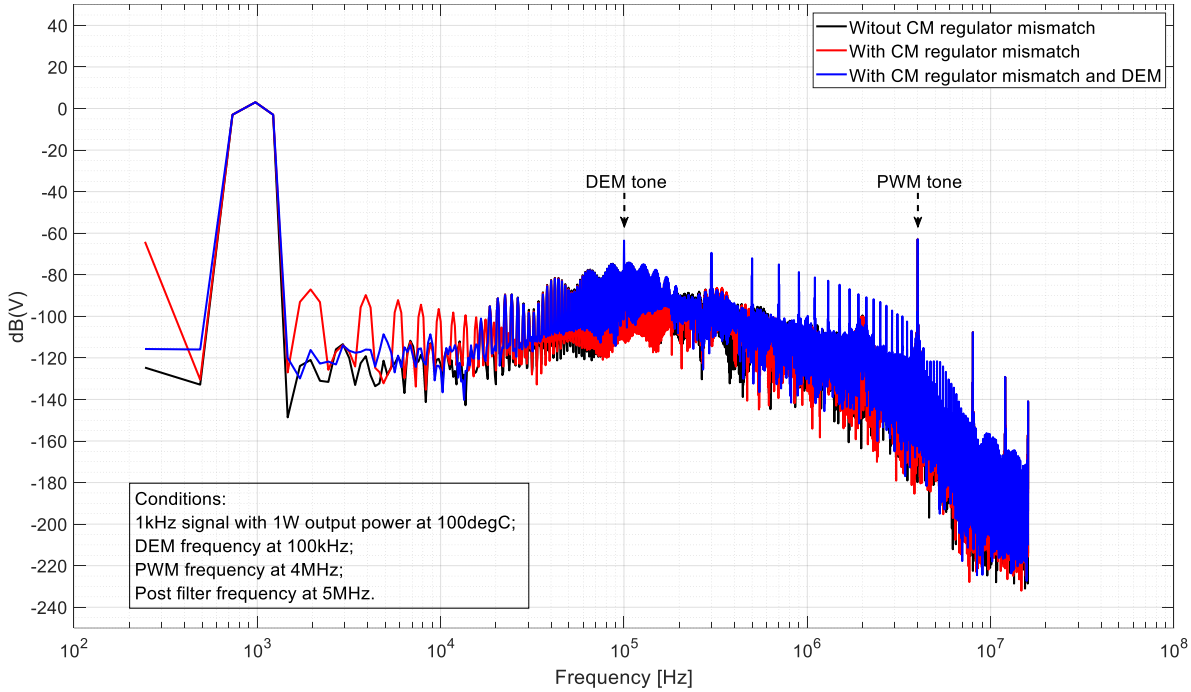

Figure 4.8 System output spectra under three conditions.

THD results under those three conditions are summarized in Table 4.2, which shows that the DEM technique can effectively reduce distortion due to mismatch in the common-mode regulator.

Table 4.2 THD under three conditions.

Conditions	Without mismatch (black)	With 3-σ mismatch (red)	With 3-σ mismatch and DEM (blue)
Audio band THD	-96.80dB	-85.96dB	-96.41dB

Because output stages of the common-mode regulator are class-AB amplifiers, the worst case scenario for stability happens when the current output is minimal. Figure 4.9 shows the worst case AC loop gain, where the phase margin is 65.92°. Hence, the common-mode regulator is stable.

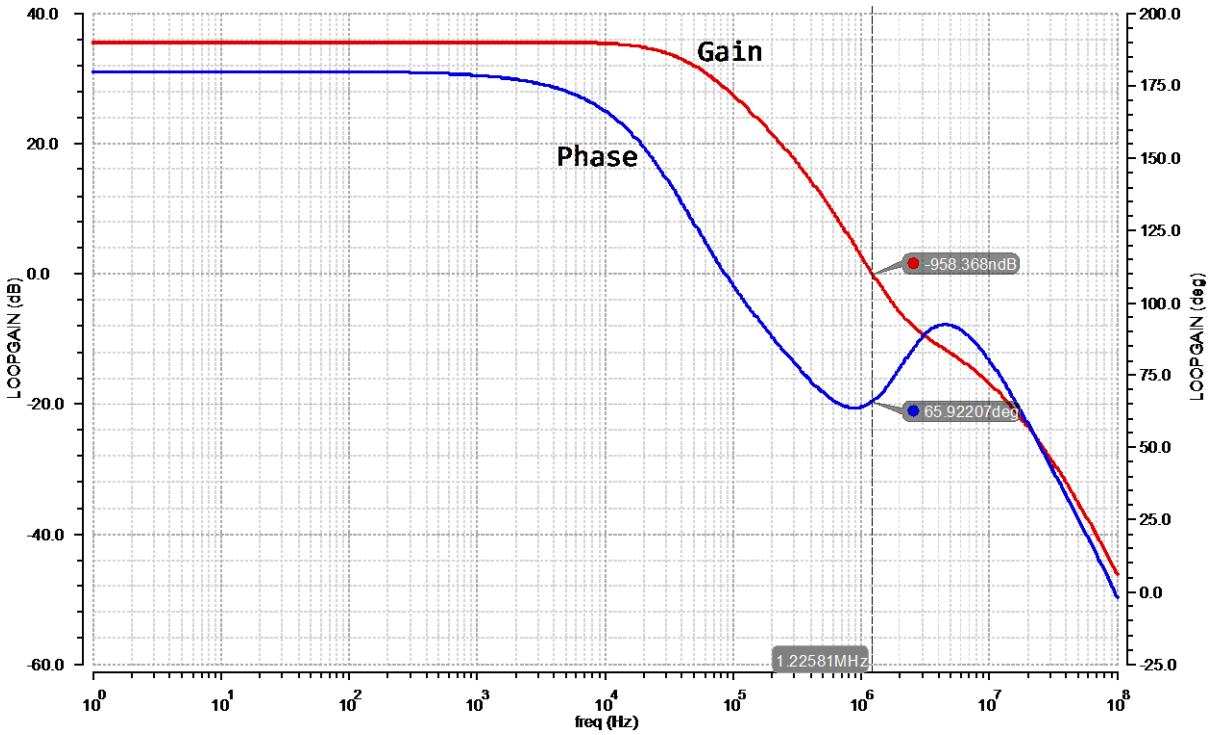

Figure 4.9 The worst case AC loop gain of the common-mode regulator.

Chapter 5 Output Stage

In this class-D amplifier design, a multi-level output stage is employed to generate both high voltage and low voltage pulses. This chapter describes the high voltage and low voltage operations in the following two sections.

5.1 High Voltage Operation

Figure 5.1 illustrates the high voltage part of the multi-level output stage, which consists of four N-channel power transistors and their respective gate drivers, level shifters and voltage regulators.

Low voltage logic signals generated by the modulator are sent to the level shifters, which transmit the control signals from the low-voltage digital domain (DVDD = 1.8V) to the HV domains; these signals are used to turn on or off the power transistors with the gate drivers. As the VGS of the HV transistors (M_{HV1-4}) is limited to 5V, on-chip regulators are used to power their respective level shifters and gate drivers.

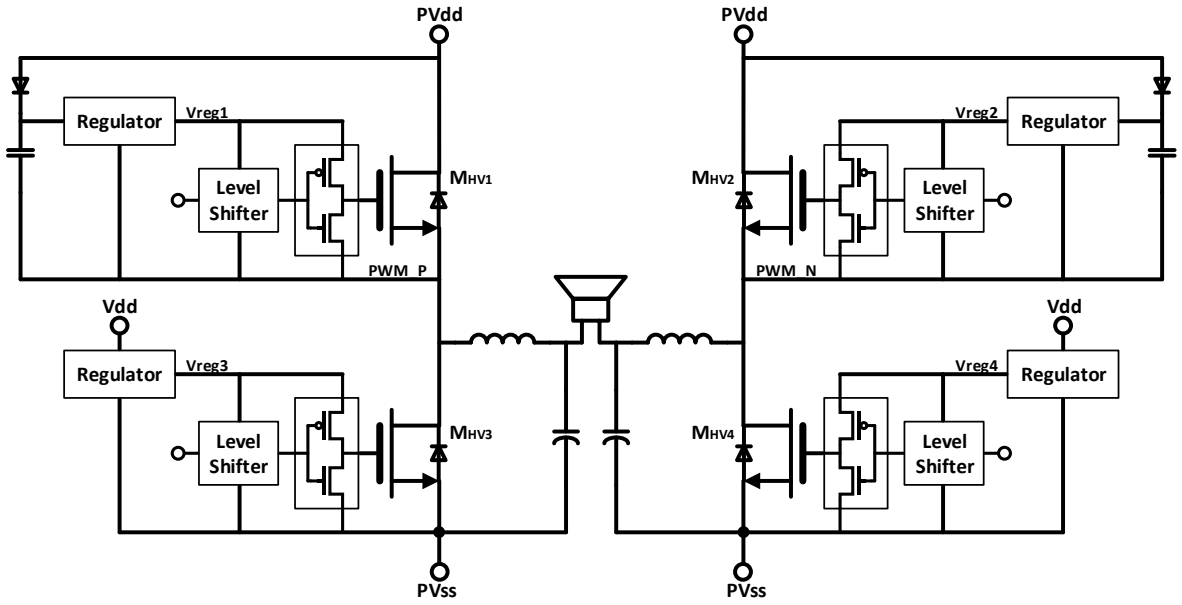

Figure 5.1 The high voltage part of the multi-level output stage.

5.1.1 Power transistor

A major design consideration for the output power transistors is the on-resistance, which is critical for power efficiency.

Given that the load resistance is 4Ω, the total resistance of bonding wires is 100mΩ. To achieve the targeted peak efficiency of 90%, on-resistance of each power transistor should be less than 172mΩ. To leave some margin for switching loss, the on-

resistance is chosen as 100mΩ, thus leading to an area of 9122um^2 for each transistor.

5.1.2 Gate Driver

Gate drivers are required to provide fast transitions and prevent cross-conduction of the power transistors. The schematic of the proposed gate driver is illustrated in Figure 5.2.

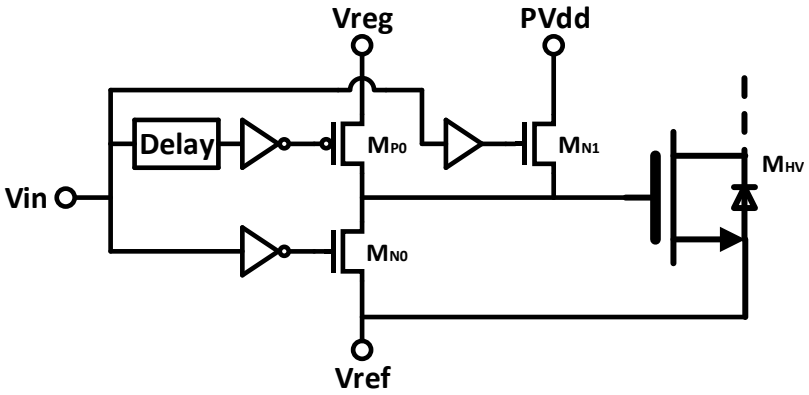

Figure 5.2 Gate driver design.

To avoid loading the regulator excessively, an additional NMOS (M_{N1}) is employed to pull up the power transistor (M_{HV}) during the beginning of turning on moments [30]. This transistor charges the gate of M_{HV} to Vreg-Vth, where Vreg is the output voltage of the regulator and Vth is the threshold voltage of the NMOS. The PMOS (M_{P0}) then turns on, providing the remaining gate-charge required to pull up the gate of M_{HV} completely to Vreg. The delay line before M_{P0} ensures that M_{N1} is turned off when M_{P0} starts conducting current.

To avoid cross-conduction [2], the ratio between the on-resistances R_P and R_N of M_{P0} and M_{N0} has to obey:

$$R_N / (R_P + R_N) < V_{th} / V_{reg} \tag{5.1}$$

Thus, the size of M_{N0} should be much larger than the size of M_{P0}. In this design, the area ratio is 10:1.

5.1.3 Level Shifter

Level shifters are required to transfer signals in a fast, reliable, and power-efficient way between low-voltage and high-voltage domains. This output stage employs dynamic two-step level shifters [30], as shown in Figure 5.3. The first step is to shift

the signal reference from DVss to Vdd_x, which is the high voltage supply or the boosted supply; the second step is to shift the signal reference from Vdd_x to Vss_x, which is the power ground or the output nodes (PWM_P, PWM_N).

The load of the first stage is a cross-coupled pair in parallel with diodes. As demonstrated in 3.4.2, this structure offers high output impedance in differential-mode but low output impedance in common-mode, thus leading to a good rejection of common-mode disturbance [30].

A one-shot signal generator produces the enable signal (EN), which detects transitions in the low voltage input and produces short pulses during transition, ensuring that the level shifter draws current only during transitions, making it very power efficient.

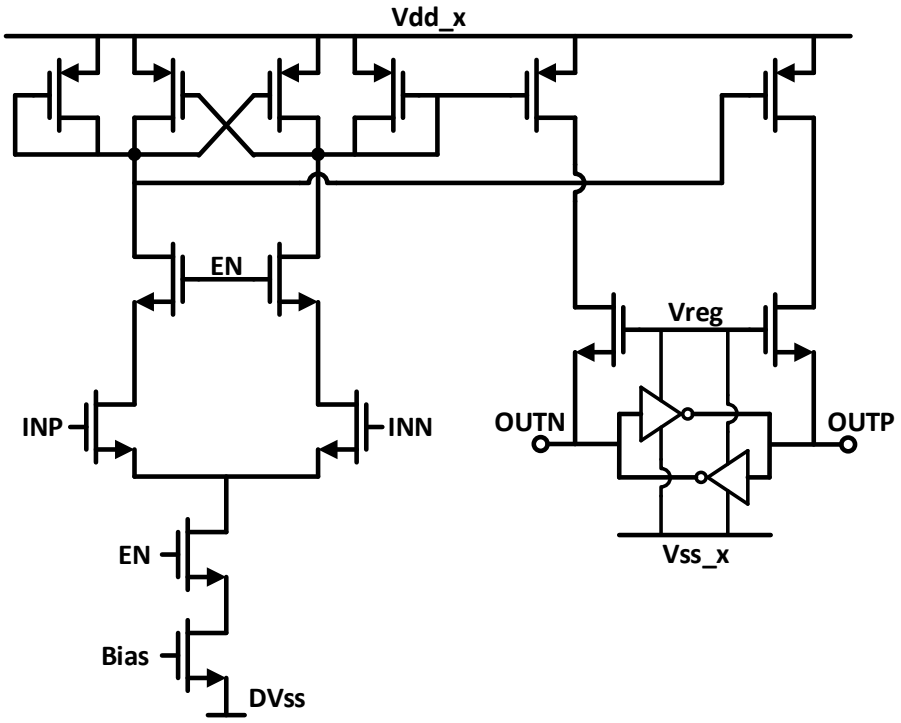

Figure 5.3 Level shifter design.

The challenge for the dynamic level shifter is the ringing that arises on account of the parasitic inductances due to bond wires [1, 6, 30]. The large ringing during high dv/dt transitions, result in supply bounce, as shown in Figure 5.4. When the supply voltage drops below the nominal output voltage of the regulator (5V), the latched result of the level shifter can erroneously flip and cause a faulty turn-on transistor, resulting in shoot-through problems and possible damage to the power transistors.

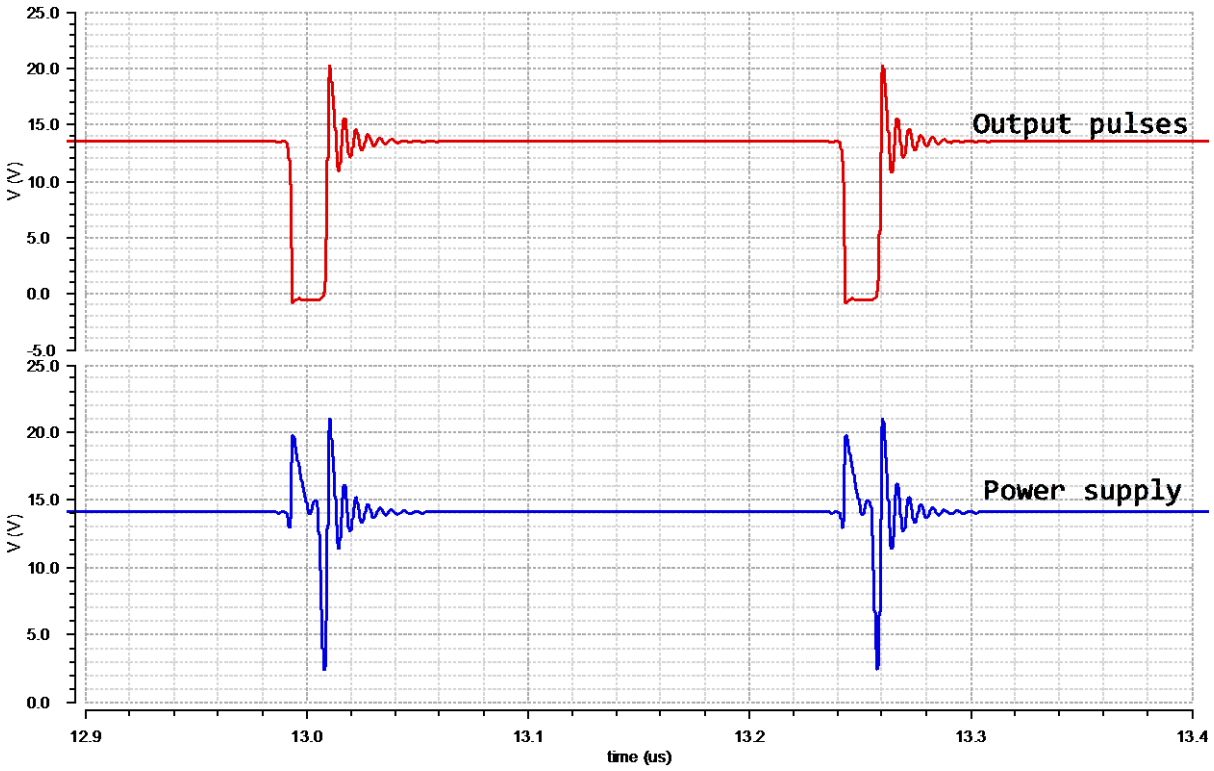

Figure 5.4 Supply bounce during high dv/dt transition.

Therefore, the enable signal should be constant high during the high voltage mode, which refreshes the level shifter in real-time. But during the low voltage mode (low-dv/dt transitions in the output stage), the duty cycle of the enable signal should be low to save power.

5.1.4 Regulator

The regulators have to power the fast-switching gate drivers and level shifters, and as such, the primary requirement for them is a fast transient response, which makes an open-loop structure favorable.

The high side regulator acts as a current source to charge the gate of the power transistor when the output transit from low to high, but it acts as a current sink when the output transit from high to low because it has to discharge the N-well that contains the floating gate driver and level shifter. Therefore, the regulator employs a push-pull output stage.

The schematic of the proposed regulator is shown in Figure 5.5, where the 5.5V reference from a Zener diode is buffered by a class-AB amplifier to the output.

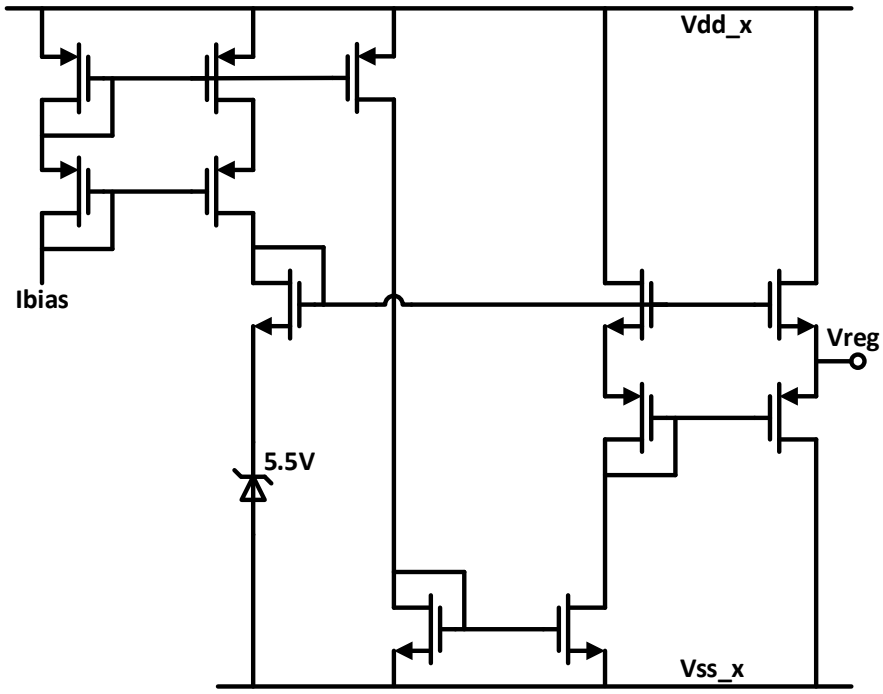

Figure 5.5 Regulator design.

5.2 Low Voltage Operation

Figure 5.6 illustrates the multi-level output stage in the low voltage mode, where gate drivers and level shifters are not shown for simplicity.

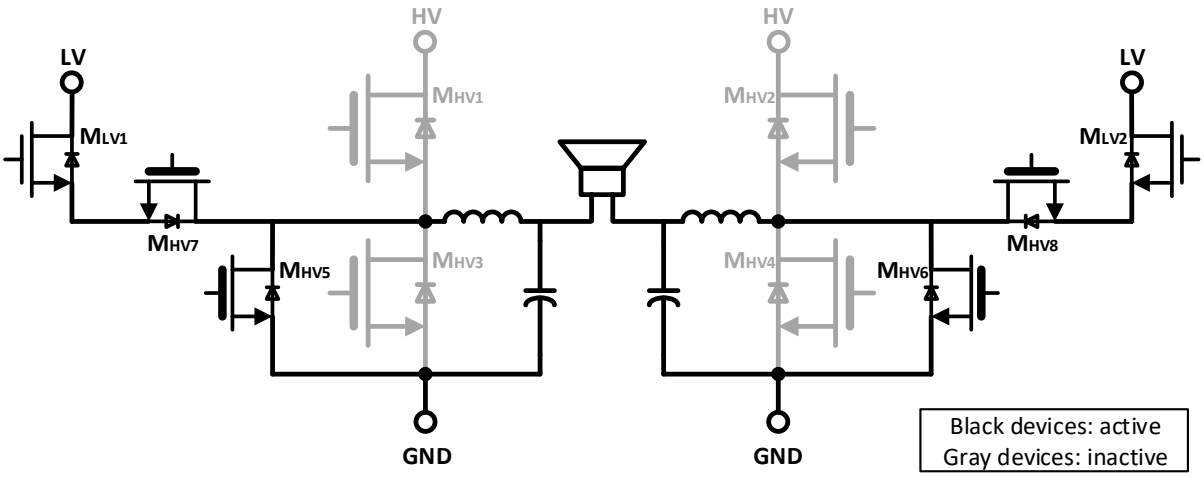

Figure 5.6 Simplified multi-level output stage in low voltage mode.

M_{LV1} and M_{LV2} are low voltage transistors while the rest are high voltage transistors. Isolation switches (M_{HV7} and M_{HV8}) are turned off to protect M_{LV1} and M_{LV2} during high voltage operation and turned on to conduct current during low voltage operation.

Low side transistors in the high voltage stage are reused for the low voltage stage, but they are split to reduce the power loss due to gate charging [31]. Specifically,

M_{HV5}+M_{HV3} and M_{HV6}+M_{HV4} form the low side of the high voltage stage, but only M_{HV5} and M_{HV6} are active during low voltage operation.

For the low voltage output stage, the specification of interest is area, which is related to the system cost, and this area is mainly occupied by the isolation transistors (M_{HV7} and M_{HV8}). In this design, the isolation transistor size is scaled to 18% of the power transistor size, keeping the area of the low voltage stage (includes MOSFETs, level shifters and gate drivers) less than the area of one HV power transistor.

Chapter 6 System Level Simulation Results

Unless otherwise noted, all data in this chapter was simulated under the following conditions:

- Load resistance is 4Ω, power supply is 14.4V;
- In the LC filter, inductance is 3.3uH, capacitance is 680nH;
- Ambient temperature is 100°C.

6.1 Idle Power

With the worst-case offset in opamps, comparators, and common-mode regulators, the idle power is 27.93mW, 60% of which is due to quiescent loss, and the rest 40% is due to switching loss.

The switching loss in the idle state is mainly caused by wide-band thermal noise, which turns on the modulator, triggers the power stage, as shown in Figure 6.1. Integrated noise before the modulator is 33mVrms (1Hz-1GHz), in which input resistors contributes 38%, the first opamp contributes 25%, and the common-mode regulator contributes 22%.

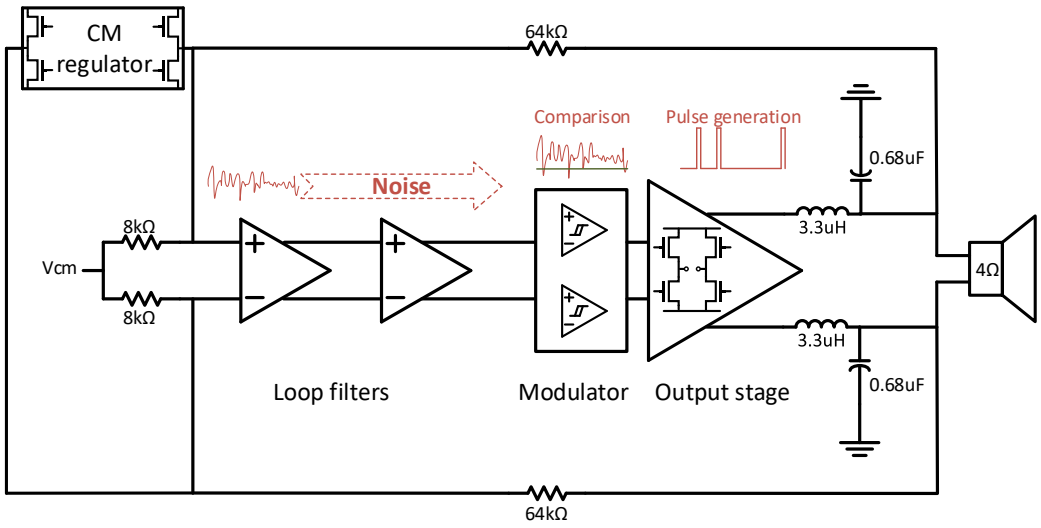

Figure 6.1 Switching due to noise the idle state.

In the idle state, the modulator operates in the LV PSM mode, meaning that it compares loop filter outputs with a DC threshold voltage, synchronizes its output pulses to a clock signal. Figure 6.2 plots the related signals in this modulation process, the reason for low idle power consumption is that the output pulse density is significantly lower than the clock frequency.

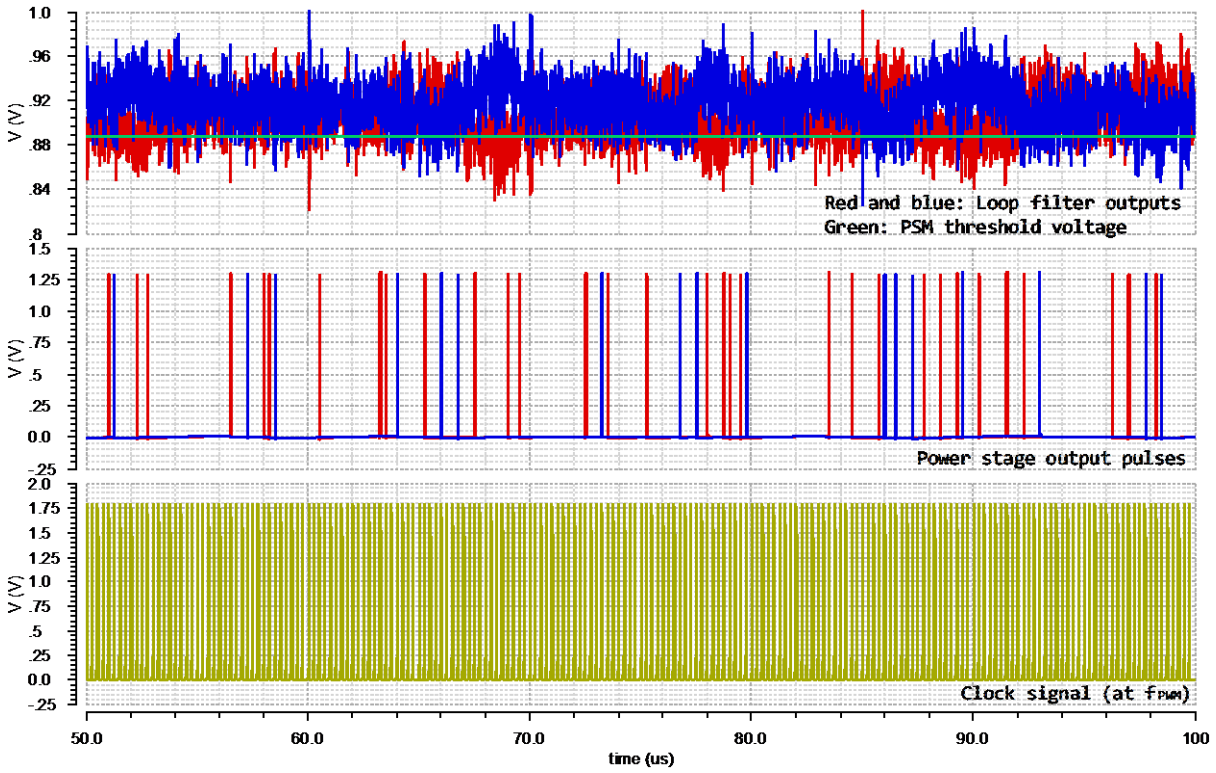

Figure 6.2 Modulation and pulses in the idle state.

6.2 Linearity

Figure 6.3 plots the spectrum of the output signal (1kHz, 1W output power), THD is -96.41dB in the audio band, where high order harmonics due to dead band distortion dominates.

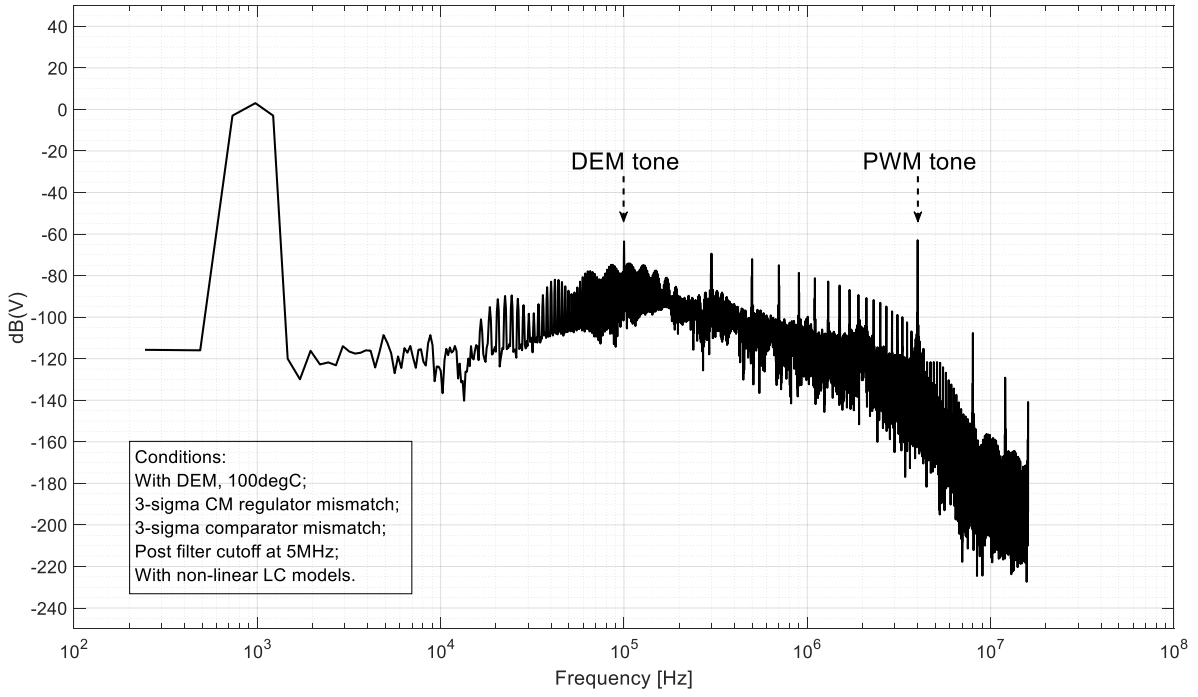

Figure 6.3 Output spectrum.

THD over output power is shown in Figure 6.4. For small signals (output power below 10mW), the major distortion source is the transition between PSM and PWM, as demonstrated in 3.5.2. For large signals, the class-D amplifier exhibits the peak THD of -105.64dB when the output power is 10W.

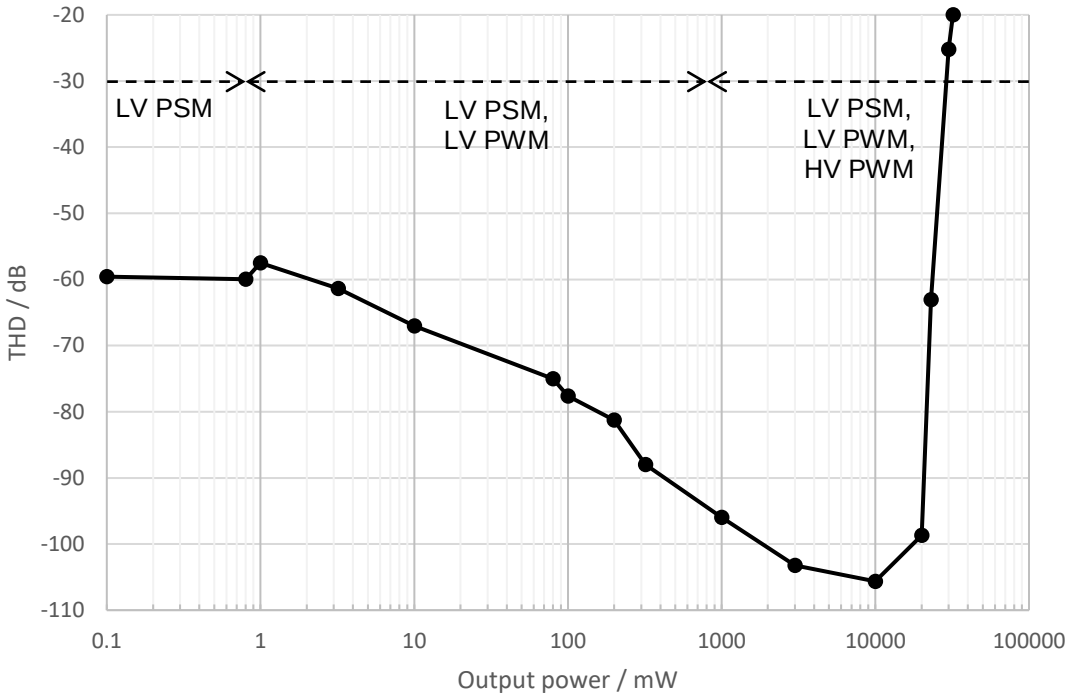

Figure 6.4 THD over output power.

6.3 Noise in the Audio Band

With zero and full-scale input signals, integrated noise (A-weighted) in the audio band is summarized in Table 6.1.

Table 6.1 Noise simulation results.

Input amplitude / Specifications		Zero	Full-scale
Integrated output noise voltage (uV)		37.93	40.01
SNR (dB)		N.A.	-107.96
Contributors	Flick noise of the first opamp	57.00%	51.70%
	Thermal noise of input resistors	21.92%	18.96%
	Thermal noise of the CM regulator	7.82%	15.90%

The difference between these two noise simulations is mainly caused by class-AB output stages of the common-mode regulator. Because the common-mode current is proportional to signal amplitude, the higher output current leads to a higher gm and thus generating more noise.

6.4 Efficiency

Efficiency over output power is plotted in Figure 6.5. The peak efficiency is 90.4% which is achieved above 25W.

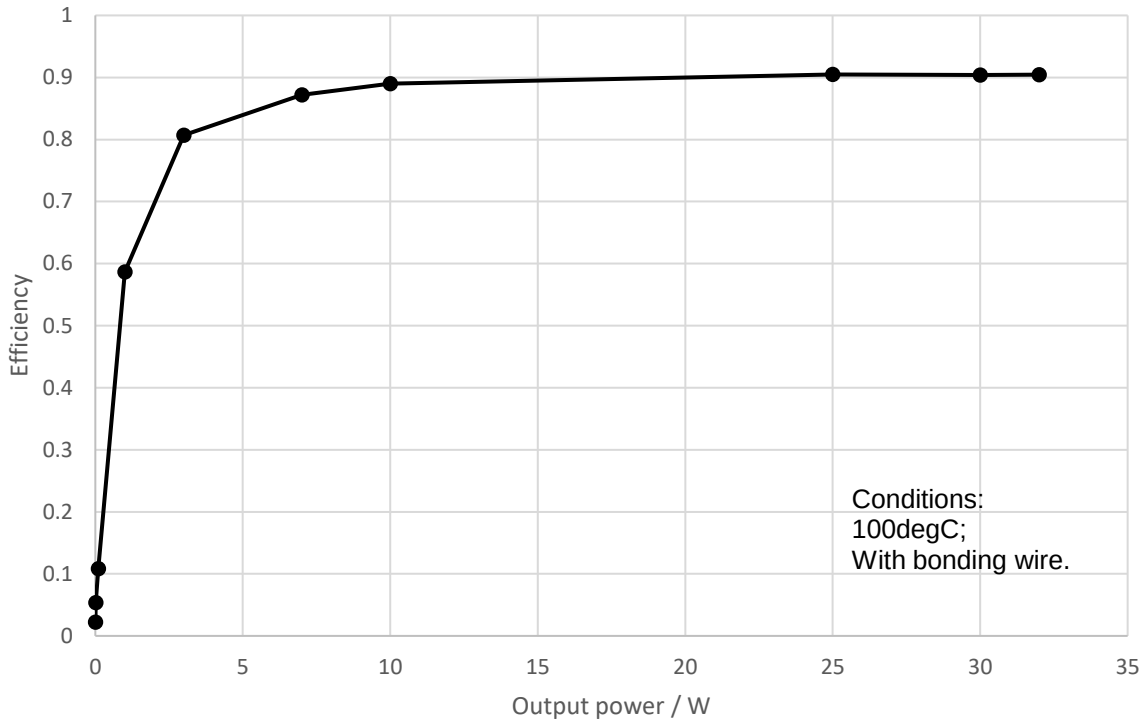

Figure 6.5 Efficiency over output power.

The maximum output power at 10% THD is 32W, and its efficiency is 90.47%. Switching loss contributes 5.6% to the total power loss, while conduction loss contributes the rest 94.4%.

6.5 Step Response

Step response characterizes stability in the time domain. Figure 6.6 shows step responses of the class-D amplifier over LC mismatch and corners. The input step signal is 20% of the full-scale, as shown in Figure 6.6(a), which ensures that all three operation modes are involved.

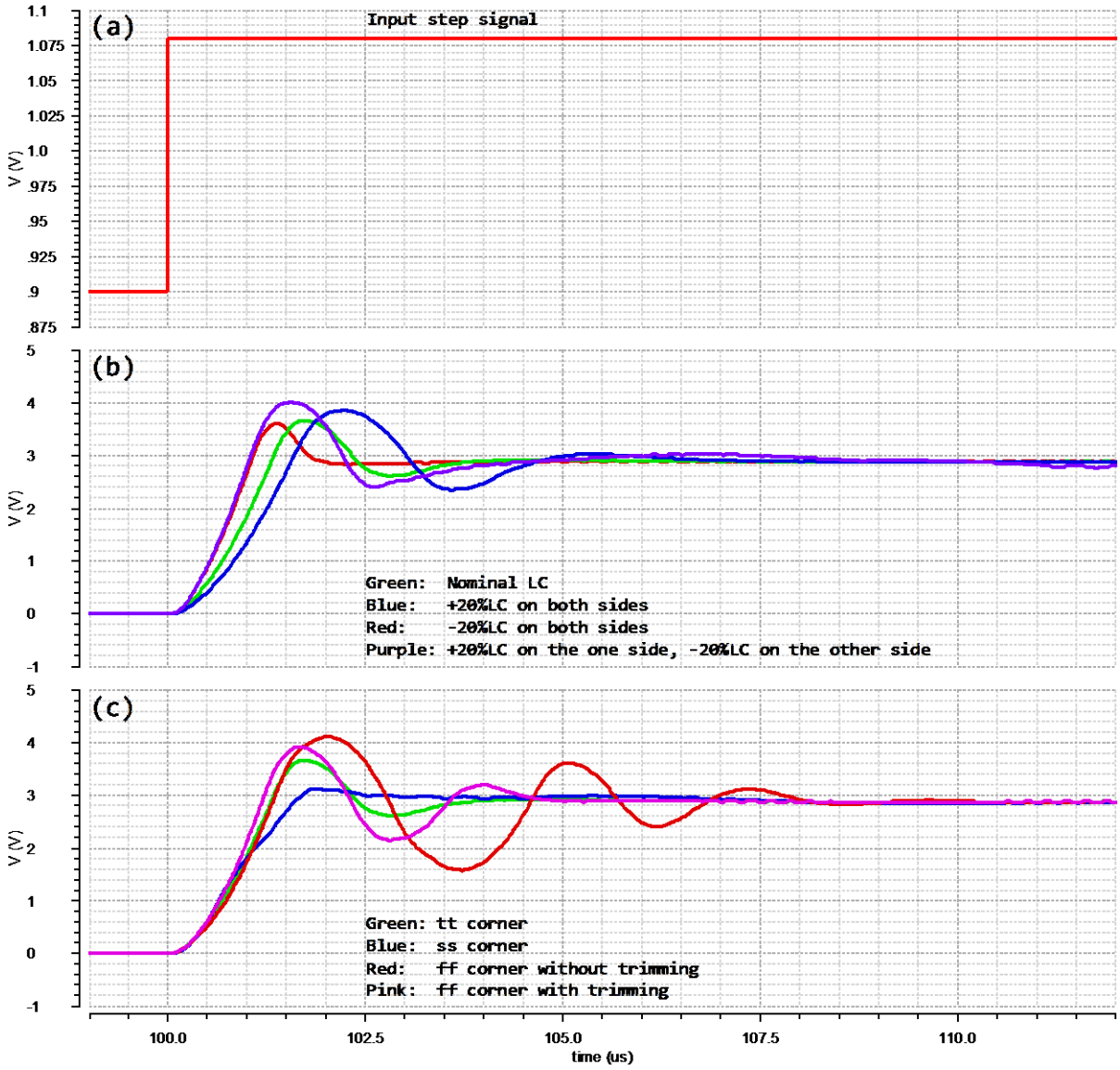

Figure 6.6 Step response.

Because this class-D amplifier is configured in BTL, two LC filters are employed. To verify this design with ±20% inductance spread and ±20% capacitance spread, three extreme conditions are simulated in Figure 6.6(b). This class-D amplifier is stable over ±20% LC spread.

Figure 6.6(c) plots step responses over corners, where the untrimmed ff corner exhibits the largest ringing while the ss corner exhibits the smallest ringing, this result agrees with the AC stability simulation in 0 that phase margins in ss, tt, trimmed ff, and untrimmed ff corners are 55.30°, 51.94°, 44.16°, and 27.11°, respectively.

Chapter 7 Conclusions and Future Work

7.1 Conclusions

An ultra-low idle power class-D amplifier has been designed for automotive audio applications. Using push-pull and pulse skipping modulations, this class-D amplifier reduces the effective switching frequency in the idle state, thus resulting in an idle power of 28mW, which is the lowest among all automotive grade class-D amplifiers.

To mitigate the inherent dead-band distortion of push-pull modulation, a multi-level output stage is employed, which includes a high voltage stage to generate large signals and a low voltage stage for small signals. Besides, the feedback loop is closed after the LC filter to suppress the non-linearity of the off-chip LC components. With the help of these techniques, this class-D amplifier achieved a competitive THD of -96dB (1kHz, 1W output power).

The full performance of this class-D amplifier is compared with that of other automotive grade class-D amplifiers in Table 7.1.

Table 7.1 Comparison table.

Specifications	This work	[19]	[32]	[33]
Supply	14.4V	14.4V	25V	12V
Load	4Ω	4Ω	4Ω	6Ω
Idle power per channel	28mW	606mW	>400mW	194mW
THD+N (1W)	-92.14dB	-81.93dB	-87.95dB	-90dB
Output noise	40.01uV (A weighted)	42uV	19uV (A weighted)	50uV (A weighted)
Pout, max (10% THD)	32W	27W	80W	10W
Efficiency	90.47% (@ Pout, max)	86% (@ Pout, max)	>90% (@ Pout, max)	88% (@5W)
Switching frequency	4MHz	2.1MHz	400kHz	<700kHz (Avg.)
LC cutoff frequency	106kHz	88kHz	≈40kHz	41kHz

7.2 Future work

- In this class-D amplifier, the first opamp employs a large input pair to reduce flicker noise, which introduces a low-frequency pole in the feedback loop, impairing stability. Chopping technique can be implemented to remove flicker noise, thus allowing the use of a small input pair.
- Due to the feedback-after-LC structure, loop stability relies on the accuracy of off-chip LC components. To further reduce the cost of LC components and maintain good stability, it is necessary to diagnose the LC values and then adjust loop parameters accordingly.

Acknowledgements

I would like to dedicate my sincere gratitude to all of those who helped and supported me during my master thesis.

My foremost thanks go to my supervisor, Dr. Qinwen Fan, for introducing me to this challenging but rewarding project. She not only enlightened me with insightful ideas but also shaped my methodology of analog circuit design. Besides, I learned how to behave in a team from her, which is beneficial for my future career.

I would like to thank Prof. Kofi Makinwa, who leads this world-class research group. I very much appreciated his broad knowledge and critical thinking. In particular, I highly value the presentation skills from him during the group meetings.

This thesis would not have been possible without the help and support from NXP semiconductors. I would like to thank Dr. Marco Berkhout and Prof. Lucien Breems, who act more like my teachers. I deeply appreciate all the delight and fruitful meetings we have had.

I would like to thank Sining for answering my questions and encouraging me to go through tough challenges. Although he is not my daily supervisor, he offered a tremendous amount of help and advice to me. I would also like to thank Shoubhik and Huajun, who passed their designs to me and reviewed my thesis.

Furthermore, I would like to thank people in the EI lab. I would like to thank Zu-yao and Joyce for their support; Çağrı and Jan for suggestions during group meetings and design reviews; Mengying for passing me her designs. Thanks to all my friends and colleagues: Angqi, Arvind, Daguang, Efraïm, Matheus, Matthew, Mengxin, Nuriel, Qiyou, Rishabh, Shardul, Shrinidhi, Shubham, Thomas, Wencong, and Xianglong.

Bibliography

[1] M. Berkhout, “An integrated 200-W class-D audio amplifier,” *IEEE Journal of Solid-State Circuits,* vol. 38, no. 7, pp. 1198-1206, 2003.

[2] M. Berkhout, “A class D output stage with zero dead time,” in 2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC., 2003, pp. 134-135 vol.1.

[3] M. Berkhout, “A 460W class-D output stage with adaptive gate drive,” in 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, 2009, pp. 452-453,453a.

[4] M. Berkhout, L. Breems, and E. v. Tuijl, “Audio at low and high power,” in ESSCIRC 2008 - 34th European Solid-State Circuits Conference, 2008, pp. 40-49.

[5] B. Krabbenborg, and M. Berkhout, “Closed-Loop Class-D Amplifier With Nonlinear Loop Integrators,” *IEEE Journal of Solid-State Circuits,* vol. 45, no. 7, pp. 1389-1398, 2010.

[6] J. Liu, S. Chien, and T. Kuo, “A 100W 5.1-channel digital class-D audio amplifier with single-chip design,” *IEEE Journal of Solid-State Circuits,* vol. 47, no. 6, pp. 1344-1354, 2012.

[7] P. Morrow, E. Gaalaas, and O. McCarthy, “A 20-W stereo class-D audio output power stage in 0.6-/spl mu/m BCDMOS technology,” *IEEE Journal of Solid-State Circuits,* vol. 39, no. 11, pp. 1948-1958, 2004.

[8] F. Nyboe *et al.*, “A 240W monolithic class-D audio amplifier output stage,” in 2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers, 2006, pp. 1346-1355.

[9] P. P. Siniscalchi, and R. K. Hester, “A 20 W/Channel Class-D Amplifier With Near-Zero Common-Mode Radiated Emissions,” *IEEE Journal of Solid-State Circuits,* vol. 44, no. 12, pp. 3264-3271, 2009.

[10] *“LC filter design,”* Texas Instruments [Online]. Available: http://www.ti.com/lit/an/slaa701a/slaa701a.pdf.

[11] K. Nielsen, “A review and comparison of pulse-width modulation (PWM) methods for analog and digital input switching power amplifiers,” in Audio Engineering Society Convention 102nd, Munich, Germany, 1997.

[12] J. D. Martin, “Theoretical efficiencies of class-D power amplifiers,” *Proceedings of the Institution of Electrical Engineers,* vol. 117, no. 6, pp. 1089-1090, 1970.

[13] H. Ma, R. v. d. Zee, and B. Nauta, “A high-voltage class-D power amplifier with switching frequency regulation for improved high-efficiency output power range,” *IEEE Journal of Solid-State Circuits,* vol. 50, no. 6, pp. 1451-1462, 2015.

[14] *“Audi sound concept in the Audi Q7,”* Audi [Online]. Available: https://www.audi-technology-portal.de/en/electrics-electronics/multimedia_en/sound-systems.

[15] E. Gaalaas. *“Class D audio amplifiers: what, why, and how,”* Analog Devices [Online]. Available: https://www.analog.com/en/analog-dialogue/articles/class-d-audio-amplifiers.html.

[16] X. Jiang *et al.*, “Integrated class-D audio amplifier with 95% efficiency and 105 dB SNR,” *IEEE Journal of Solid-State Circuits,* vol. 49, no. 11, pp. 2387-2396, 2014.

[17] *“TPA3129D2 Data Sheet,”* Texas Instruments [Online]. Available: http://www.ti.com/lit/ds/symlink/tpa3129d2.pdf.

[18] M. Høyerby *et al.*, “A 2X70W monolithic five-level class-D audio power amplifier in 180 nm BCD,” *IEEE Journal of Solid-State Circuits,* vol. 51, no. 12, pp. 2819-2829, 2016.

[19] *“TAS6424-Q1 Data Sheet,”* Texas Instruments [Online]. Available: http://www.ti.com/lit/ds/symlink/tas6424-q1.pdf.

[20] H. Huang, K. Chen, and S. Kuo, “Dithering skip modulation, width and dead time controllers in highly efficient DC-DC converters for system-on-chip applications,” *IEEE Journal of Solid-State Circuits,* vol. 42, no. 11, pp. 2451-2465, 2007.

[21] H. Lee, and P. Chen, “A single-inductor dual-input dual-output (SIDIDO) power management with sequential pulse-skip modulation for battery/PV hybrid systems,” in 2016 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2016, pp. 293-296.

[22] J. Doutreloigne, J. Buyle, and V. D. Gezelle, “A multi-level switching amplifier with improved power efficiency for analog signals with high crest factor,” in WSEAS International Conference. Proceedings. Mathematics and Computers in Science and Engineering, 2009.

[23] N. Anderskouv, K. Nielsen, and M. A. E. Andersen, “High-fidelity pulse-width modulation amplifiers based on novel double-loop feedback techniques,” in Audio Engineering Society Convention 100th, 1996.

[24] IEC, "Vehicles, boats and internal combustion engines - Radio disturbance characteristics - Limits and methods of measurement for the protection of on-board receivers," 2016.

[25] S. Dietrich, R. Wunderlich, and S. Heinen, “Stability considerations of hysteretic controlled DC-DC converters,” in PRIME 2012; 8th Conference on Ph.D. Research in Microelectronics & Electronics, 2012, pp. 1-4.

[26] M. C. W. HØyerby, and M. A. E. Andersen, “Carrier Distortion in Hysteretic Self-Oscillating Class-D Audio Power Amplifiers: Analysis and Optimization,” *IEEE Transactions on Power Electronics,* vol. 24, no. 3, pp. 714-729, 2009.

[27] K. Bult, and A. Buchwald, “An embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm2,” *IEEE Journal of Solid-State Circuits,* vol. 32, no. 12, pp. 1887-1895, 1997.

[28] D. M. Monticelli, “A quad CMOS single-supply op amp with rail-to-rail output swing,” *IEEE Journal of Solid-State Circuits,* vol. 21, no. 6, pp. 1026-1034, 1986.

[29] M. Pelgrom, *Analog-to-digital conversion*, 3rd ed., Springer, 2017.

[30] H. Ma, R. v. d. Zee, and B. Nauta, “Design and analysis of a high-efficiency high-voltage class-D power output stage,” *IEEE Journal of Solid-State Circuits,* vol. 49, no. 7, pp. 1514-1524, 2014.

[31] L. Dooper, and M. Berkhout, “A 3.4 W Digital-In Class-D Audio Amplifier in 0.14um CMOS,” *IEEE Journal of Solid-State Circuits,* vol. 47, no. 7, pp. 1524-1534, 2012.

[32] D. Schinkel *et al.*, “A multiphase class-D automotive audio amplifier with integrated low-latency ADCs for digitized feedback after the output filter,” *IEEE Journal of Solid-State Circuits,* vol. 52, no. 12, pp. 3181-3193, 2017.

[33] E. Gaalaas *et al.*, “Integrated stereo delta-sigma class D amplifier,” *IEEE Journal of Solid-State Circuits,* vol. 40, no. 12, pp. 2388-2397, 2005.