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Solution-Based Fabrication of Polycrystalline Si Thin-Film Transistors from Recycled Polysilanes

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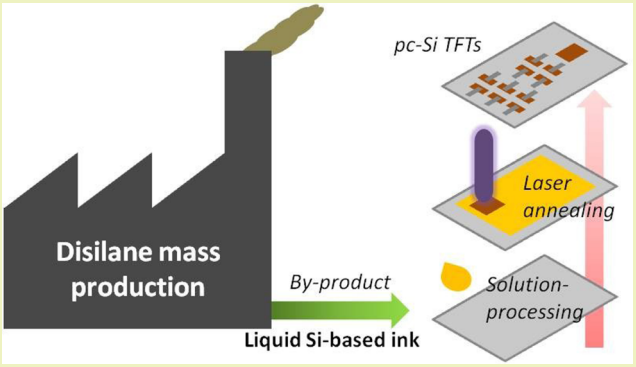
Supporting Information

ABSTRACT: Currently, research has been focusing on printing and laser crystallization of cyclosilanes, bringing to life polycrystalline silicon (poly-Si) thin-film transistors (TFTs) with outstanding properties. However, the synthesis of these Si-based inks is generally complex and expensive. Here, we prove that a polysilane ink, obtained as a byproduct of silicon gases and derivatives, can be used successfully for the synthesis of poly-Si by laser annealing, at room temperature, and for n- and p-channel TFTs. The devices, fabricated according to CMOS compatible processes at 350 °C, showed field effect mobilities up to 8 and 2 $cm^2/(V\ s)$ for n- and p-type TFTs, respectively. The presented method combines a low-cost coating technique with the usage of recycled material, opening a route to a convenient and sustainable production of large-area, flexible, and even disposable/single-use electronics.



KEYWORDS: *Disilane byproduct, Byproduct recycle, Polysilane, Low-temperature fabrication, Thin-film transistor, Polycrystalline silicon, Solution processing*

INTRODUCTION

The proved capacity to fabricate polycrystalline silicon (poly-Si) thin-film transistors (TFTs) employing liquid-phase silicon precursors opened a flourishing route toward large-area and flexible electronics with high performance.[1−3] The first advantage of using solution-processed silicon instead of the commonly used organic (O) or metal-oxide (MO) semiconductors comes from its intrinsic higher electrical mobility (low-T printed fine-grained poly-Si TFTs can reach tens of $cm^2/(V\ s)$, while low-T printed O and MO TFTs reach mobilities, respectively, lower than 1 and 4 $cm^2/(V\ s)$).[4−6] Moreover, contrary to O and MO materials, which yet allow too low mobilities for, respectively, n- and p-type TFTs,[7,8] solution-processed poly-Si permits integrating in a chip low power consumption CMOS circuitry since both p- and n-channel TFTs show high performance.[2,3]

The liquid silicon (L-Si) precursors of poly-Si studied so far are cyclosilanes, such as cyclopentasilane (Si_5H_{10}) and cyclohexasilane (Si_6H_{12}), which need, in general, dedicated expensive and complex manufacturing.[1,9] However, some L-Si inks, as polysilanes molecules (Si_nH_{2n+2}), can be obtained as the byproduct of disilane (Si_2H_6) synthesis and purification, which is widely used by the semiconductor and photovoltaic industries.[10] The fruitful usage of this polysilane ink for the solution-based fabrication of poly-Si devices would bring down significantly the production costs, not only because of the economic advantages brought by the materials solution processing (roll-to-roll coating, additive microstructures patterning, no high vacuum processes) but also due to the efficient recycling of a byproduct. Regarding the environmental sustainability, the perspective to fabricate microelectronics devices employing a byproduct material would, moreover, shade a positive light on the future wide diffusion of disposable, single-use devices and sensors. In this work, we demonstrate, for the first time, that n- and p-channel poly-Si TFTs, with field effect mobilities (μ_{FE}) from 2 to 8 $cm^2/(V\ s)$, can be fabricated at temperatures lower than 360 °C (Kapton foil compatible) coating a mixture of liquid polysilanes (PS), provided by REC Silicon, Inc., which is the byproduct of silicon gases and derivatives. The poly-Si thin film has been prepared at room temperature (RT) by excimer laser annealing of the PS layer; thus, it is possible to fabricate TFTs on lower thermal budget substrates, e.g., paper, when combined with a low-temperature device fabrication process.[3]

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EXPERIMENTAL SECTION

The transistors in this work have been fabricated (see fabrication schematic in Figure S1) on top of a crystalline Si wafer, capped with 600 nm of Si_3N_4, deposited by plasma-enhanced chemical vapor deposition (PE-CVD). The nitride layer has been chosen because PS can be more uniformly spread on slightly hydrophobic surfaces owing to increased film wettability. The used PS liquid consists of a mixture of Si_nH_{2n+2} molecules. PS has been coated in an oxygen-free environment (nitrogen-filled glovebox) by a soft palette to form a continuous film of around 200 nm. During coating, the film has been shortly illuminated by UV light (λ = 365 nm, photon energy = 3.4 eV, power = 300 mW/cm^2) to prevent partial film dewetting. Indeed, UV curing causes Si−Si cross-linking between the polysilane molecules by breaking the Si−H bonds (bond energy = 3.3 eV).[1] PS does not need UV curing, like CPS,[1,3] to be stabilized, and this is one of its greatest advantages compared to CPS. Directly after the polysilane formed a solid layer, it was converted at RT into poly-Si by KrF excimer laser (λ = 248 nm, pulse length = 20 ns) multiple irradiations at 75 mJ/cm^2. Successively, the poly-Si film has been dry etched to create the TFTs islands, with channel length (L) and width (W) ranging between 1 and 16 μm. For the gate dielectric, 60 nm of PE-CVD SiO_2 has been deposited from tetraethyl orthosilicate (TEOS) at 350 °C. The relatively high deposition temperature has been chosen here to grow a high quality oxide and thus was able to highlight the semiconductor properties influencing the TFTs performance. The gate electrode has been formed sputtering at 50 °C 900 nm of Al/Si (99/1%) and patterning it by dry etching. Source and drain regions in the island have been created by implanting through the oxide boron (energy = 20 keV, dose = 2 × 10^{15} atoms/cm^2) and phosphorus (energy = 50 keV, dose = 2 × 10^{15} atoms/cm^2) for, respectively, p- and n-channel devices. The energy values of B and P ions have been chosen, according to SRIM-2008 calculations (Figures S2 and S3) to obtain ions concentration profiles that peaked within the first 10−30 nm of poly-Si source and drain regions. These shallow profiles facilitate the electrical activation by laser since the laser radiation is mainly absorbed by the superficial poly-Si layers. During ions implantation, the thick Al gate electrode protects the channel region; moreover, diffusion from the gate electrode surface to the gate oxide is hindered by the thick Al film and by the extremely short laser annealing during dopants activation. Dopants electrical activation has been conducted at RT by KrF laser annealing (10 pulses at 60 mJ/cm^2). Later, the whole structure was passivated by 800 nm of PE-CVD (TEOS) SiO_2 at 350 °C. After contacts opening in the oxide, 1475 nm of Al/Si (99/1%) were sputtered at 50 °C and patterned to form the source, drain, and gate contact pads.

RESULTS AND DISCUSSION

The laser crystallization has been investigated by Raman spectroscopy (laser probe λ = 514 nm) and scanning electron microscopy (SEM). The TFTs have been characterized by an HP 4156 parameter analyzer. The Raman spectrum and fitted curves of the films irradiated with multiple pulses at 75 mJ/cm^2 are shown in Figure 1. The predominant peak around 520 cm^{-1} reveals that the lasered PS film has been successfully converted into poly-Si. Compared to the standard c-Si peak (520−521 cm^{-1}) here, the poly-Si peak is shifted toward lower energies and has a wider fwhm mainly due to the small size of crystalline grains and spatial confinement of phonons.[11] The fitted peak below the shoulder at 510 cm^{-1} is related to the presence of lattice defects, such as grain boundaries (GBs).[9] The broad curve, centered at 480 cm^{-1}, shows that there is a residual 30% fraction of amorphous silicon (a-Si) below the poly-Si layer.

The SEM planar view image in Figure 2 shows that the surfaces of the irradiated films are rough (we estimated a root-mean-square of >60 nm), with hillocks. This kind of morphology is a direct consequence of hydrogen degassing during laser crystallization.

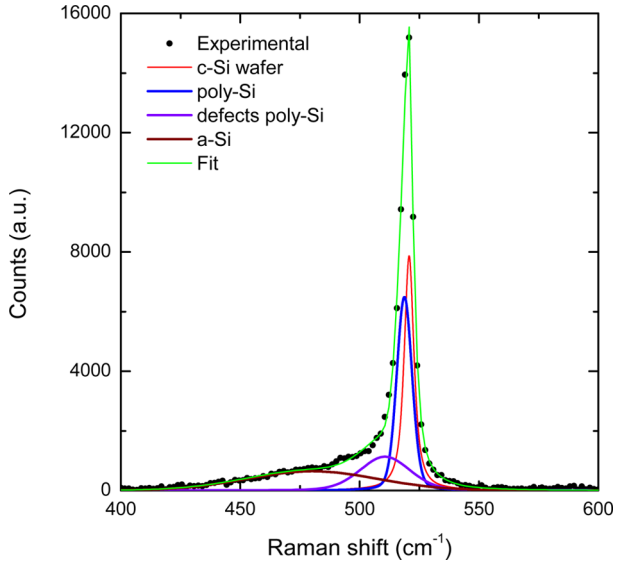

Figure 1. Raman spectrum, fit curves, and convolution fit curve of the PS film irradiated 100 times at 75 mJ/cm^2.

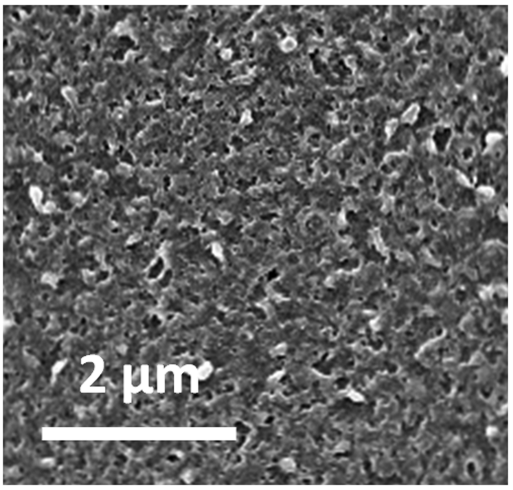

Figure 2. SEM image of the surface of the sample irradiated 100 times at 75 mJ/cm^2.

The transfer and output characteristics of some of the n-channel TFTs are reported in Figures 3 and 4, respectively. From the small drain voltage transfer characteristics, we calculated μ_{FE} ranging from 3 to 8 cm^2/(V s) and a subthreshold swing (SS) of 0.5 V/dec The average threshold voltage (V_T) is 5 V, while the typical I_{on}/I_{off} is 10^6. Plotting the transconductance (T) vs gate voltage (V_g) (Figure S4), we observed, for high gate voltages, a steep degradation of the transconductance due to SiO_2/poly-Si interface roughness scattering of free charge carriers in the TFT channel.[12] Indeed, at higher transverse electric fields, free charge carriers are forced to flow along a narrower path (effective channel thickness) below the SiO_2/channel interface. From the curve T(V_g), the parameter ΔV has also been calculated, which is defined as the maximum T divided by the differential of T at V_T. Here, V_T and ΔV are related to the density of channel defect states and their position into the band gap.[13] From our calculations (SI), it has been found also that in the channel there is a defect states density of at least 2 × 10^{12} cm^{-2} with energy levels closer to the conduction band edge. These band-tail states are originated by

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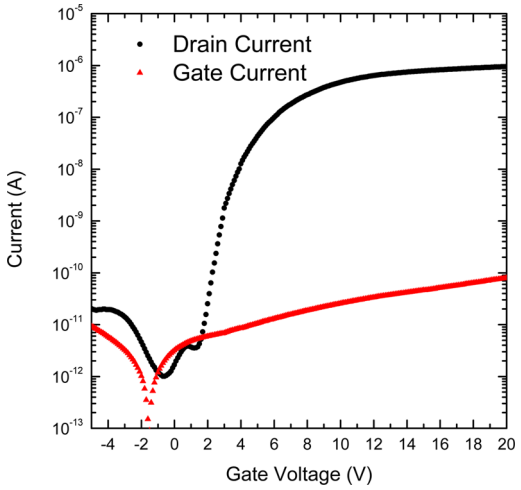

Figure 3. Transconductance characteristics of an n-channel TFT with W/L = 2, acquired at a drain voltage of 500 mV. The curves show the drain current and the gate leakage current.

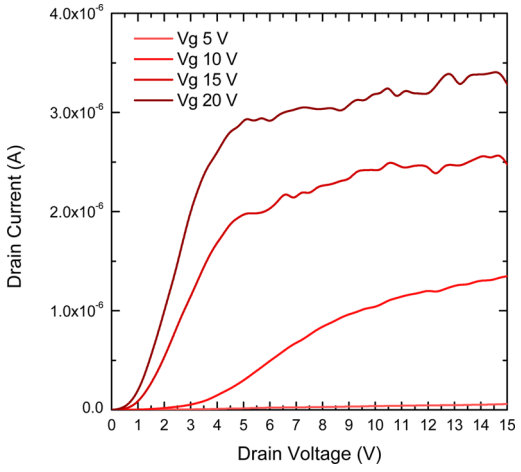

Figure 4. Output characteristics of an n-channel TFT with W/L = 2. The gate voltage V_g is swept from 5 to 20 V.

GBs[14] and contribute to lower the μ_{FE}. Furthermore, the triode region in the output curves is not perfectly linear because of not ideal contact resistance at source and drain contacts. This fact again is a consequence of the poly-Si roughness at source and drain areas and of not fully optimized implantation-induced defects recovery by laser annealing.[15] On the other hand, the saturation region curve is not flat as expected. This nonideal trend is caused by two effects. The first one consists in the shrinkage of the channel length as the pinch-off point moves toward the source. This effect, which for a-Si and poly-Si TFTs is already visible for L = 10 μm, contributes with making the channel length shrink proportional to the drain voltage and drain current sloped in the saturation regime.[16,17] The second mechanism, which is more severe in other not shown n-channel devices, is the nonlinear multiplication of I_d with V_d due to the creation of electron−hole couples by impact ionizations close to the drain edge.[18] In particular, for poly-Si, the presence of GBs and defects favor the impact ionization.[19]

The transfer and output characteristics of some of the p-channel TFTs are reported in Figures 5 and 6, respectively. For these devices, we calculated, on average, a μ_{FE} of 2 $cm^2/(V\ s)$, a SS of 0.7 V/dec, a V_T of −12 V, and an I_{on}/I_{off} of 10^4. These

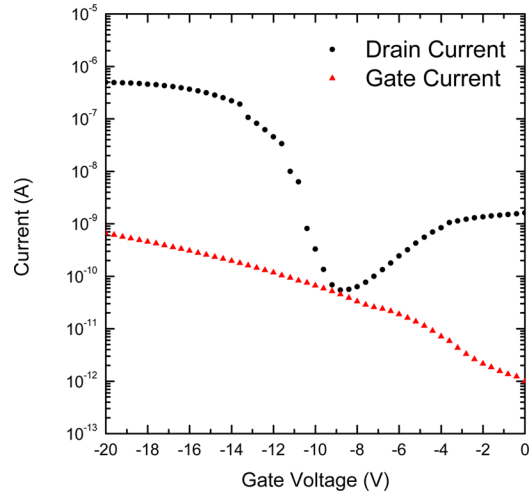

Figure 5. Transconductance characteristics of a p-channel TFT with W/L = 2, acquired at a drain voltage of 500 mV. The curves show the drain current and the gate leakage current.

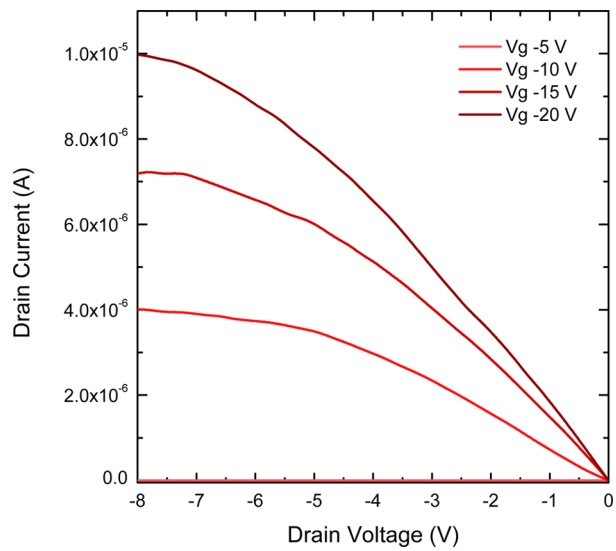

Figure 6. Output characteristics of a p-channel TFT with W/L = 2. The gate voltage V_g is swept from −5 to −20 V.

data, combined with the analysis of the transconductance versus gate voltage curve, reveal that in the channel the defect states density is slightly higher than the n-type devices. Regarding the output characteristics, the same conclusion for n-channel TFTs apply.

CONCLUSIONS

These characteristics for n- and p-channel devices surpass the performance achieved by commercial a-Si ($\mu_{FE} \leq 1$ $cm^2/(V\ s)$) and by the state of the art low-temperature solution-processed O and MO TFTs.[6,20,21] The good mobilities obtained for both n- and p-type devices allows also the implementation of C-MOS circuitry. The μ_{FE}, SS, V_T, and I_{on}/I_{off} values can be even further improved optimizing the laser crystallization in terms of a smother gate oxide/channel interface and larger poly-Si grains. The V_T mismatch between the n- and p-channel TFTs can be overcome by lightly doping with boron the channel of the p-type devices. Higher TFT on-state current can then be obtained by improvements in source and drain doping. Finally,

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optimization of the PS coating process and substrate surface pretreatment would also contribute to higher device performance. In conclusion, we proved for the first time that an industrial byproduct material, the Si_nH_{2n+2} molecules mixture, can be fruitfully employed to fabricate solution-based poly-Si n- and p-channel TFTs with properties far exceeding commercial a-Si devices and solution-based O TFTs. The fabrication performed in this work used an extremely simple printing method, similar to roll-to-roll coating, and employed an RT crystallization process, which is compatible with future low thermal-budgeted substrates usage. Therefore, this work demonstrates that the combination of low-cost coating methods and recycled Si-based precursors can definitely trace an industrial roadmap toward inexpensive and sustainable large-area and flexible electronics.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acssuschemeng.7b00626.

Details about TFTs fabrication steps, calculated phosphorus and boron implantation profiles, and analysis of n-channel TFTs transconductance. (PDF)

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Author Contributions

All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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