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Battery Storage System as Power Unbalance Redistributor in Distribution Grids Based on Three Legs Four Wire Voltage Source Converter

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***Abstract*— This article discusses the application of battery energy storage systems (BESSs) as power redistributors in three-phase distribution grids as an add-on functionality to typical BESS applications, such as congestion management and energy arbitrage. Combining those ancillary services into a single power unit is not yet performed in practice but may constitute an emerging business opportunity to increase the BESS revenues. The unbalanced operation of the BESS voltage source converter (VSC) leads to the circulation of low-frequency current harmonics in the dc-link through the capacitors and the battery cells. Therefore, it is particularly interesting whether relatively large 50- and 100-Hz currents can safely circulate within these components. Analytical modeling and design guidelines for the dc-link of a three-leg four-wire two-level VSC operating under unbalanced loads are detailed. Furthermore, a low-power VSC prototype is used to demonstrate the working principle of the BESS, providing power unbalance redistribution and symmetric power exchange. Additionally, the ICR18650-26F Lithium-ion cells are cycled to reach end-of-life with different current profiles and C-ratings. The analysis shows that charging with a 100 Hz ripple superimposed to the dc current leads to a 10% increment in degradation.**

***Index Terms*— Battery energy storage system (BESS), distribution grid, power redistributor, unbalanced load, voltage source converters (VSCs).**

I. Introduction

LOW-VOLTAGE (LV) distribution grids are characterized by the connection of single-phase loads, which can lead to unbalanced power consumption between the three phases during the real-time operation [1], [2]. This issue is amplified with the proliferation of high-power single-phase elements, e.g., electric vehicle (EV) chargers, electric heaters, and residential photovoltaic (PV) generation systems, which have higher peak power and less predictable time of use. The phenomenon of phase-unbalance can negatively affects the distribution grid. Transformers become underutilized since their capacity is limited by the highest loaded line [3], induction motors can experience additional losses and heating in the windings [4], and the neutral current deriving from unbalanced phase currents may unnecessarily trip the protective device [1]. A power redistributor can be used to balance the phase powers and ensure an efficient and reliable grid operation [5]. Possible technical solutions to mitigate this problem are the implementation of shunt active power filters and STATCOM, which typically employ a grid-connected voltage source converter (VSC) that can reroute the unbalanced active power from one phase to another [6], [7]. The dc-link of VSC deployed as power redistributors require particular design attention [5], since the unbalanced three-phase power operation of the VSC leads to low-frequency current harmonics in the dc-link, namely the 50- and 100-Hz components, for a grid with a frequency of 50 Hz, which do not appear under balanced conditions.

Grid-connected VSCs of similar topologies to active filters and STATCOMs are also present in high power, e.g., >100 kW, grid-connected battery energy storage systems (BESSs) [8], [9]. BESSs are flexible assets that can be deployed in the electrical grid for both supporting the local grid by relieving it from congestion and controlling the grid voltage, and for profiting from the oscillating spot energy prices [10]. These ancillary services typically require the exchange of symmetric three-phase active or reactive power, which aims at maintaining a specific voltage and frequency level, in the range mandated by the electrical system operators [11], [12]. However, they do not influence the power quality. The power redistributor functionality, instead, targets the voltage and current waveforms symmetry between the three phases, by providing asymmetric power exchange. Such service cannot be achieved by the typical BESS circuitry which was optimized for the exchange of symmetric power, but it requires some adjustments.

The power redistribution service, which does not strictly require large energy storage capabilities to function [5], and the various ancillary services which BESS can provide, are typically performed separately by different power units. However, the integration and provision of additional ancillary services by a single BESS may constitute a reasonable

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business opportunity if the technical requirements for all committed services are met. This is particularly true for ancillary services requiring BESSs that function with contracted energy, e.g., frequency regulation, where it has been shown that the power utilization is typically low [13], [14]. Therefore, enabling the incorporation of adds-on ancillary services can maximize the utilization of the power unit. In such an interesting application, particular attention may need to be paid to the effects of the add-on functionality on the power unit's components. The latter is of particular interest in this work.

To achieve the power redistributor functionality, the BESSs' VSC needs to be connected to the neutral conductor of the distribution grid [5]. BESSs' VSCs are typically implemented through the two-level topology, which is composed of three half-bridge legs, one per phase [15]. Therefore, the connection to the grid neutral can be achieved with minimum hardware expansion by interconnecting the available grid neutral to the VSC's dc-link capacitors midpoint. In this context, such functionality can be an additional or optional service, even to already deployed BESS. Alternatively, a fourth half-bridge leg can be connected in the dc-link to provide the connection to the grid neutral [6]; however, this solution makes the retrofit of already deployed BESS significantly more complex. In the light of including the power redistribution functionality as an add-on service also to already deployed BESS, the grid neutral connection to the dc-link midpoint is considered in this article.

The dc-link capacitors and the battery cells are the BESS components that are more critically relevant to the additional stress and design requirements for enabling the functionality of three-phase power redistribution. In a three-phase leg, four wires (3L-4W) VSC, the unbalanced currents will circulate through the neutral of the three-phase system, and thus through the BESS's widely employed dc-link split electrolytic capacitors. Therefore, the dc-link capacitors must be sized to withstand the extra 50-Hz current component. On the other hand, the 100-Hz current component will mostly flow through the battery cells, e.g., flowing from the dc-link positive to the negative rail. This occurs because the battery offers a lower impedance path for the low-frequency current than the electrolytic capacitors. The analytical modeling of the dc-link currents flowing in a two-level VSC operating under an unbalanced three-phase load has been presented in [16]. However, Pei *et al.* [16] considered a three-wire system without a neutral connection. Therefore, the effects of the zero-sequence component in the dc-link current, which is highly relevant to the power redistributor application, is not evaluated in [16], and so it is presented in this article.

Furthermore, this article investigates whether low-frequency current ripple is detrimental to the battery lifetime, which is a critical parameter for the deployment of grid-connected BESS [13]. In fact, previous research mainly focused on whether it is possible to boost the charging performance by superimposing the dc current with an ac ripple at an optimal frequency, which typically corresponds to the frequency of the battery minimum impedance to reduce losses in the cells, which is generally found around 200 Hz–1 kHz [17], [18], [19]. The results of such studies are mixed [20], [21]. However, in the BESS power redistributor application, the dominant ac ripple is fixed at twice the grid frequency, e.g., 2×50 Hz $= 100$ Hz, and not necessarily optimized for the battery minimum impedance since it is a direct consequence of the 50-Hz three-phase current unbalance operation of the VSC.

This article thoroughly investigates the design and application of a BESSs' 3L-4W VSC for power unbalance redistribution in distribution grids. The power redistribution functionality is considered an add-on service to grid-connected BESS deployed for other typical applications requiring the exchange of symmetric power with the grid, e.g., congestion management, energy arbitrage, primary frequency regulation, etc. The mathematical modeling of the dc-link current and voltage ripples are presented, providing a design guideline for the dc-link capacitors. The ICR18650-26F Lithium-ion cells from Samsung SDI are cycled with different C-ratings until end-of-life (EoL) by superimposing a 100-Hz current ripple over the typical dc current component typically found in conventional BESS grid service provision. This is done to evaluate whether such ac current ripple harms the battery lifetime. Furthermore, a low-power 2-kW VSC prototype is used to demonstrate the functionality of power redistribution in a laboratory setup. The main contributions of this article are as follows:

1) the design methodology for a 3L-4W two-level VSC for BESSs providing power redistribution functionality superimposed to the conventional symmetric power injection/absorption grid ancillary service provision;
2) the mathematical modeling of the dc-link currents of the 3L-4W VSC under different phase unbalance conditions; and
3) the 100-Hz ac current ripple analysis on the degradation of a commercial Lithium-ion battery cell.

The remainder of this article is organized as follows. Section II describes the application of a BESS as grid power redistributor and its control strategy. Section III derives the mathematical models for the dc-link current and voltage under different unbalance conditions, furthermore, it provides an example of how to design the dc-link for a 100-kW BESS providing power redistribution. Section IV investigates the 100-Hz ac ripple impacts on the degradation of Lithium-Ion battery cells. Section V provides the experimental results validating the dc-link mathematical models and showing the working principle of the unbalance compensation. Finally, Section VI concludes the work.

II. Battery Storage System as Grid Power Balancer

Power unbalance operation occurs when the phase currents of a three-phase ac network differ in terms of amplitude or they are not in a perfect 120° phase shift between them. To better analyze the current unbalanced behavior of three-phase systems, the phase quantities can be transformed into their symmetrical components utilizing the Fortescue transformation [22]. In this way, a given three-phase network, whose phase's currents are expressed as I_a, I_b, and I_c, can be transformed into symmetrical components, I_+, I_- and I_0,

being, respectively, the positive, negative, and zero-sequence components, as [23]

$$\begin{bmatrix} I_0 \\ I_+ \\ I_- \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{1}$$

where $a = e^{j(2\pi/3)}$.

These symmetrical components are three sets of balanced phasors: the positive, negative, and zero-sequence systems. The positive sequence has its phasors with the same amplitude and shifted by 120° rotating at the same frequency as the original system and in the same direction; the negative sequence phasors also have the same amplitude and are shifted by 120° rotating at the same frequency of the original system, but in the opposite direction. Finally, the zero-sequence system is composed of three phasors of the same amplitude and the same phase rotating at the same frequency as the original system and in the same direction. More details regarding the symmetrical components analysis of polyphase power systems can be found in [23]. The positive-sequence current represents the power flow from the source to the load, responsible for the active and reactive power transfer. The negative-sequence current is caused by the ripple power, which oscillates at double the grid frequency. The zero-sequence current is the summation of the individual line currents. Thus the unbalance factor of a three-phase network, as specified by the IEC [24], can be defined as the ratio between the negative and zero-sequence currents and positive sequence currents

$$\mathrm{Un}_- = \frac{I_-}{I_+} \cdot 100[\%] \tag{2}$$

$$\mathrm{Un}_0 = \frac{I_0}{I_+} \cdot 100[\%]. \tag{3}$$

Following (1)–(3), the unbalance factors are found to reach considerably high values, up to 90%, when the phase currents strongly differ between them in terms of amplitude or power factors.

In this context, a BESS can act as a power redistributor by helping to balance the three-phase currents seen by the upstream grid or local distribution transformer. A typical layout of a distribution grid is shown in Fig. 1, where it can be seen that in the LV feeders, household loads are connected between a single-phase terminal and the neutral. Additionally, one has seen the proliferation of residential and industrial PV generation and EV chargers in recent years. Furthermore, a BESS can be connected at the MV/LV substation to utilize the locally produced renewable energy better, boosting its self-consumption and deferring network investments. A BESS connected as shown in Fig. 1 can also be used as a power redistributor. In fact, in this arrangement, the BESS can monitor the currents through the transformer, and if an unbalance is detected, the BESS could compensate it through its intrinsic three-phase VSC.

A. Three-Phase VSC for BESS-Based Power Redistributor

As previously mentioned, the BESS uses a VSC to interface the battery with the ac grid, and this allows, among other

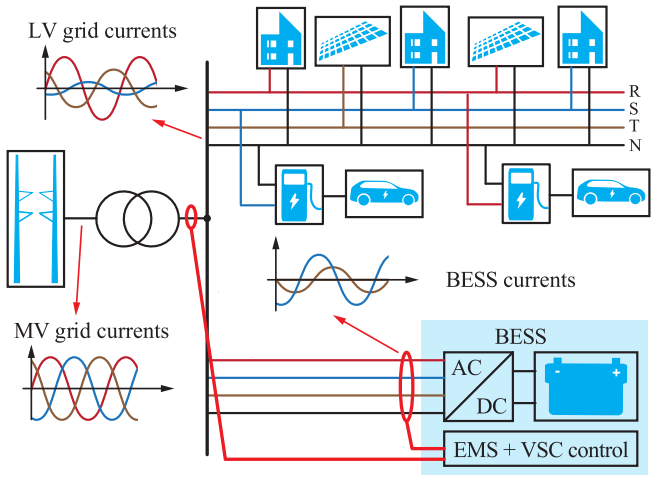


Fig. 1. Example of an LV distribution grid where unbalanced loads are connected in the LV side and a BESS acts as power redistributor balancing the MV currents.

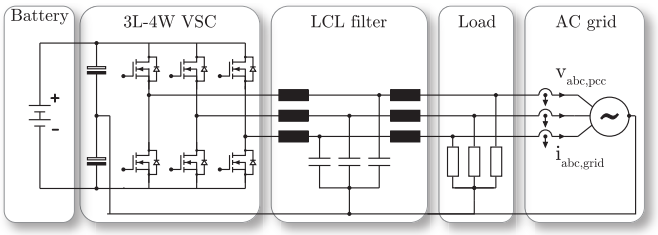


Fig. 2. Circuit schematic of a BESS based on a 3L-4W VSC while supplying three-phase loads and interfacing with the distribution ac grid and.

functionalities, the possibility for the BESS to act as a power redistributor. The VSC can be realized using various topologies, each with advantages and limitations. Typical high power BESSs rely on three-phase two- or three-level VSC topologies. A three-phase two-level converter is assembled with three half-bridge legs, i.e., one per ac phase. Instead, three-level topologies use more complex bridge leg configurations, such as the neutral-point-clamped and T-type converters [9]. This article focuses on the two-level topology due to its robustness and widespread usage in commercial high-power BESS.

Unbalance grid currents lead to negative and zero-sequence currents. Negative sequence currents flow uniquely in between the three-phase terminals, as the positive sequence does; however, zero-sequence currents have a return path through the neutral conductor. Therefore, the application of BESS as power redistribution requires a VSC topology that can control zero-sequence currents. So the VSC must have access to the neutral conductor of the distribution grid. The three half-bridge legs of the VSC are connected one per phase; therefore, the neutral conductor can be connected to the midpoint of the dc-link capacitors, as shown in Fig. 2. The capacitor midpoint voltage indirectly controls the neutral current in the system since the zero-sequence current flows through the two split capacitors. The circuit schematic of this three-phase legs four-wires (3L-4W) VSC is depicted in Fig. 2.

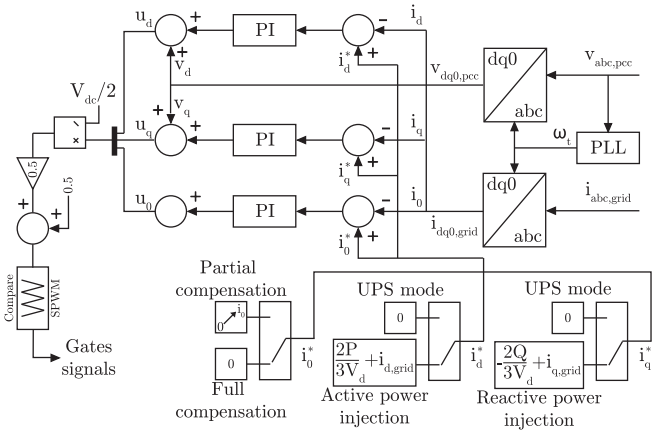


Fig. 3. Current control and grid synchronization loop of a BESS's VSC operating as power redistributor.

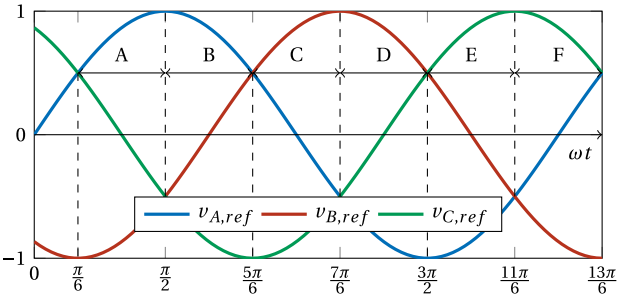


Fig. 4. Modulation waveforms, $\upsilon_{A,\mathrm{ref}}$, $\upsilon_{B,\mathrm{ref}}$, and $\upsilon_{C,\mathrm{ref}}$, of a three-phase VSC with the highlighted sector division, A–F according to the relative position of the modulation waveforms.

B. BESS 3L-4W VSC Control for Power Redistributor

To achieve the power redistribution functionality, the VSC needs to control independently the active, reactive, and zero-sequence power. The control scheme of a BESS's VSC operating as a power redistributor is conceptually similar to standard grid-connected VSC control, and it is shown in Fig. 3. A phase-locked-loop circuit is used to synchronize the VSC with the grid, then the converter is controlled in the $dq0$ frame, allowing the independent control of active, reactive, and zero-sequence power. In fact, the current references, i_d^*, i_q^*, and i_0^*, can be set to match the unbalance calculated from the measured grid currents, following (1). Additionally, the current references i_d^* and i_q^* can be increased or decreased to inject or absorb active and reactive power from the grid. In this way, the converter currents can be efficiently controlled to supply unbalanced loads and therefore balance the grid currents.

III. DC-Link Design for Power Unbalance Compensation

The dc-link is the critical VSC part for enabling the power redistribution capability in a BESS. In this context, it is fundamental to analyze how the provision of this functionality impacts its design.

A. DC-Link Capacitance Sizing

The PWM operation of the VSC generates harmonic currents in the dc-link, which in turn cause dc voltage ripple. To limit such voltage ripple and high-frequency currents through the battery, capacitors are placed in the dc-link. Additionally, the dc-link capacitors function as an energy buffer. In fact, a fast transient load step causes a dc voltage variation so that safe VSC operation is guaranteed. In this case, in the first few modulation periods, around hundredths of μs, the dc-link has to supply a certain amount of energy to limit the voltage drop, until the control system reacts and limits the power output. Therefore, for such short time constants, the battery pack will not be able to provide the required energy, since its equivalent series resistance is significantly larger than the one of the dc-link electrolytic capacitors. Therefore, it is necessary to size the capacitors assuming that they fully provide the load step energy, according to [25]

$$C_{\mathrm{dc}} \geq \frac{T_r \cdot \Delta P}{(2 \cdot V_{\mathrm{dc}} \cdot \Delta V_{\mathrm{dc}})} \tag{4}$$

where the load step is indicated with ΔP, T_r is the period during which the capacitors have to provide the load step power, which depends on the VSC control delay and it is usually selected as 5–10 modulation periods, and ΔV_{dc} is the allowed voltage deviation. This design consideration is important for the BESSs' VSC since grid-connected BESS are required to provide fast load steps, but also because of the grid connection standards which require fault tolerance and LV ride through [26], [27].

This equation estimates the energy that needs to be supplied from the dc-link in case of an unexpected load step. In this case, the dc-link has to supply a certain amount of energy to limit the voltage drop until the control system can react and limit the power output. Therefore, the load step time, T_r, is very small, in the order of a few modulation periods and so around hundredths of μs. For such short time constants, the battery pack will not be able to provide the required energy, since its equivalent series resistance is significantly larger than the one of the dc-link electrolytic capacitors. Therefore, it is necessary to size the capacitors assuming that they fully provide the load step energy.

To ensure a safe and efficient dc–ac power conversion, without overmodulating the PWM controlled VSC, it is required that the absolute partial dc-link voltage (the voltage across the upper and bottom capacitors) is higher than the maximum absolute ac phase-to-neutral voltage $\hat{V}_{\mathrm{ac,max}}$ [9]

$$\frac{V_{\mathrm{dc,min}}}{2} - \frac{\Delta V_{\mathrm{dc},r}}{2} \geq \hat{V}_{\mathrm{ac,max}} \tag{5}$$

where $V_{\mathrm{dc,min}}$ is the minimum battery dc voltage and $\Delta V_{\mathrm{dc},r}$ is the dc voltage ripple. Hence, the battery's open-circuit voltage variations due to the SoC, and the international grid codes, that require the normal operation for $\pm 10\%$ ac grid voltage deviation from the nominal value play a crucial role.

$V_{\mathrm{dc,min}}$ and $\hat{V}_{\mathrm{ac,max}}$ are dependent on the battery and grid conditions and cannot be controlled by the VSC. On the other hand, $\Delta V_{\mathrm{dc},r}$ depends on the loading conditions and the dc-link capacitance, and therefore it must be addressed in the VSC design stage.

As discussed in [16], the dc-link voltage ripple $\Delta V_{\mathrm{dc},r}$, for sinusoidal PWM (SPWM) modulation strategy, symmetrical grid, and balanced load, is composed of only the high-frequency components, and it can be expressed as

$$\Delta V_{\mathrm{dc},r} = \frac{3m\hat{I}_+ \cos\varphi}{8 f_{\mathrm{sw}} C_{\mathrm{dc}}}(1+m) \tag{6}$$

where m is the modulation index, $\hat{I}_+$ is the peak value of the positive sequence current, $\cos\varphi$ is the power factor, and f_{sw} is the converter switching frequency. However, in the case of unbalanced fundamental frequency loading, a second harmonic component in the dc voltage ripple arises [16]. In this case, the low-frequency component dominates the high-frequency one, and so the dc ripple takes the following expression [16]:

$$\Delta V_{\mathrm{dc},r} = \frac{3m\hat{I}_-}{8\pi f_g C_{\mathrm{dc}}} \tag{7}$$

where $\hat{I}_-$ is the peak value of the negative sequence current and ω_g is the grid nominal frequency of 50 Hz.

Instead, the neutral current, I_n, does not create a voltage ripple in the full dc-link, but it causes the split capacitor midpoint to oscillate. I_n is three times the zero-sequence current since each phase zero-sequence current gets summed in the neutral conductor. Therefore, given the neutral current flowing through the capacitors, the midpoint voltage ripple, $\Delta V_{\mathrm{dc},0}$ can be calculated by solving the capacitor differential equation and expressed as

$$\Delta V_{\mathrm{dc},0} = \frac{3I_0}{4\pi f_g C_{\mathrm{dc}}}. \tag{8}$$

The oscillation of the midpoint has to be limited to ensure that the capacitors do not see negative voltage, otherwise, they get reversely polarized which causes the failure of electrolytic capacitors.

All in all, the dc-link capacitors have to be sized to fulfill several requirements, namely, the energy buffer, (4), limiting the dc-link voltage ripple to ensure a safe dc–ac energy conversion, (5)–(7), and limiting the midpoint oscillation to avoid the reverse polarization of the capacitors, (8). Each of these equations defines a minimum capacitance that satisfies the requirement, and therefore, the dc-link capacitance must be chosen as the largest between them, so that all the conditions expressed by (4)–(8) are met.

B. DC-Link Current Calculation

The dc-link current of a VSC is inevitably related to the nature of its ac currents. If the VSC processes balanced ac power, the dc-link current would be only a positive sequence current. However, considering unbalanced phase currents, additional components, the negative and zero-sequence components, arise in the dc-link current. Pei *et al.* [16] presented the derivation of the dc-link current under unbalanced load, however, considering only negative sequence, since a three-wire system has been analyzed. Therefore, the approach used in [16] can be extended to consider also the zero sequence. The three-phase currents can be decomposed into their respective symmetrical components and expressed as

$$\begin{cases} i_a(t) = \hat{I}_+ \sin(\omega t - \phi_+) \\ \qquad +\hat{I}_- \sin(\omega_- t - \phi_-) + \hat{I}_0 \sin(\omega_0 t - \phi_0) \\ i_b(t) = \hat{I}_+ \sin\left(\omega t - \phi_+ - \frac{2\pi}{3}\right) \\ \qquad +\hat{I}_- \sin\left(\omega_- t - \phi_- + \frac{2\pi}{3}\right) + \hat{I}_0 \sin(\omega_0 t - \phi_0) \\ i_c(t) = \hat{I}_+ \sin\left(\omega t - \phi_+ + \frac{2\pi}{3}\right) \\ \qquad +\hat{I}_- \sin\left(\omega_- t - \phi_- - \frac{2\pi}{3}\right) + \hat{I}_0 \sin(\omega_0 t - \phi_0) \end{cases} \tag{9}$$

where $\hat{I}_+$, $\hat{I}_-$, $\hat{I}_0$ are the positive, negative and zero-sequence currents peak values, ω, ω_-, and, ω_0 the angular frequencies, and ϕ_+, ϕ_-, ϕ_0 are the phase-angle differences of the positive, negative and zero-sequence currents with their respective voltage reference vector. In the following derivation, $\hat{I}$ denotes the peak current value and I the rms value. The phase output currents are assumed to be perfect sinusoidal currents, neglecting the high-frequency ripple. The converter side ac current ripple can be limited with an LCL filter designed to have a large converter side inductance [28]. Furthermore, the dc-link current derivation is based on the fact that the switching frequency, f_{sw} is much larger than the grid frequency, f_g, so that in a switching period the quantities at grid frequency can be approximated as a constant.

In this context, one grid frequency period can be divided into six sub-periods, depending on the relative position between the three-phase reference voltages, and therefore on the switching sequence of the upper switches during a switching period, T_{sw}, as shown in Fig. 4. In one interval, the dc-link current in the positive rail can be derived according to the switching sequence of the upper switches, which is given by the position between the voltage reference signals and the carrier waveform. Fig. 5 shows the dc-link current profile during a switching period in the interval A. When the modulating waveform, $v_{\mathrm{A,ref}}$, $v_{\mathrm{B,ref}}$, or $v_{\mathrm{C,ref}}$, is above than the carrier signal, v_{car}, the upper switch of that half-bridge leg will turn on and therefore the current of that phase will flow through the positive rail of the dc-link. When all the three upper switches are turned on, the three ac phase currents are summed in the positive rail of the dc-link, and the resulting current will be equal to three times the zero-sequence current $i_n = 3 \cdot i_0$.

Then, starting from the interval T_0, one can see that the carrier waveform v_{car} is above all the modulation waveforms, therefore the upper switches of the three half-bridge legs are turned off. Consequently $i_{\mathrm{dc}} = 0$. During T_1 only $v_{A,\mathrm{ref}}$ is above v_{car} and so $i_{\mathrm{dc}} = i_a$, during T_2 instead $v_{A,\mathrm{ref}}$ and $v_{C,\mathrm{ref}}$ are above v_{car} and so $i_{\mathrm{dc}} = i_a + i_c$. In T_3 sees all modulation waveforms above the carrier and so $i_{\mathrm{dc}} = i_n$ in all intervals. Following this method, it is possible to derive the waveform of i_{dc} during interval A. Accordingly, the mean square value of i_{dc} during interval A can be found as

$$\begin{aligned} I^2_{\mathrm{dc},A} &= \frac{1}{T_{\mathrm{sw}}}\int_{t_0}^{t_8} i^2_{\mathrm{dc}} dt \\ &= \frac{2T_1}{T_s} i_a^2 + \frac{2T_2}{T_s}(i_a + i_c)^2 + \frac{2T_3}{T_{\mathrm{sw}}} i_n^2. \end{aligned} \tag{10}$$

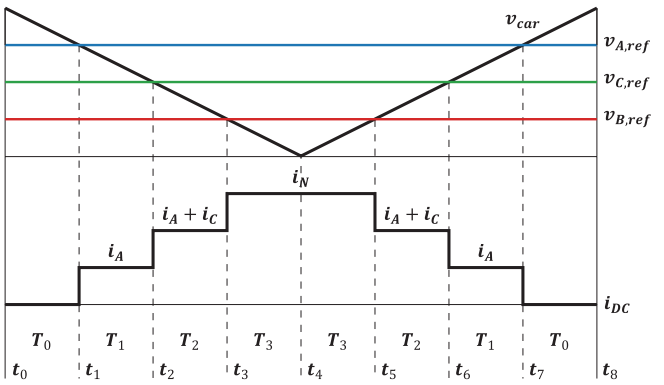


Fig. 5. Modulation, $v_{A,\mathrm{ref}}$, $v_{B,\mathrm{ref}}$, and $v_{C,\mathrm{ref}}$, and carrier,v_{car}, waveforms over one carrier period for interval A of Fig. 4 and current profile in the positive rail of the dc-link.

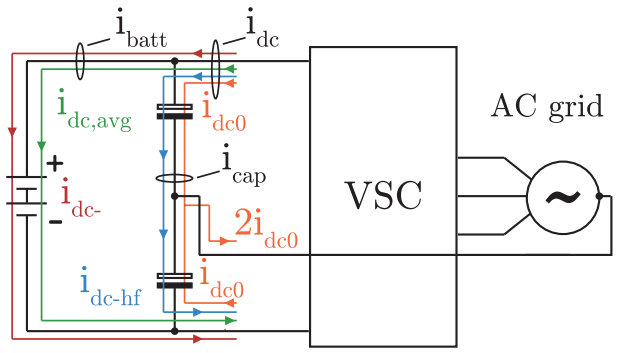


Fig. 6. Current paths of the various dc-link current harmonic components in a BESSs' VSC operating as power redistributor.

The same approach can be extended to the interval B-F. These intervals only differ from each other by the relative position of the modulation waveforms, therefore, the methodology applied in one interval can be directly applied in the other ones, with the only difference in the i_{dc} values in T_1 and T_2 of Fig. 5.

Finally, the total dc-link rms current can be found summing the mean square components of each interval, and substituting the expression of (9) to i_a, i_b, and i_c, resulting in

$$I_{\mathrm{dc}}^2 = \frac{\sqrt{3}}{4\pi} \cdot [(1 + 4\cos^2\phi_1)\hat{I}_+^2 m + 3m\hat{I}_-^2 + (\sqrt{3}\pi - 2m)3\hat{I}_0^2 - 2m\hat{I}_-\hat{I}_0\cos(\phi_- + \phi_0)] \quad (11)$$

where m stands for the modulation index, which is function of the peak single-phase ac voltage, $\hat{V}_{\mathrm{ac}}$, and the total dc-link voltage, V_{dc}, and it is defined as $m = (2 \cdot \hat{V}_{\mathrm{ac}}/V_{\mathrm{dc}})$.

Equation (11) predicts the full dc-link rms current, considering all its harmonic components: the high-frequency, the dc, the 50 Hz, and the 100-Hz sequence components. This equation is therefore the starting point for the estimation of the current flowing through the capacitors and the battery. Fig. 6 shows the current paths of the various dc-link current harmonic components in a BESSs' VSC operating as a power redistributor. As possible to see, the dc and the 100-Hz component flow through the battery cells, while the zero sequence and the 50-Hz component through the capacitors. also, it is important to note that the zero-sequence component, I_{dc0}, flows in equal value from the positive and the negative dc-link rail, and then goes back to the grid neutral conductor through the capacitors' midpoint.

TABLE I

PARAMETERS IMPLEMENTED IN THE CIRCUIT SIMULATOR SOFTWARE PLECS USED FOR THE VERIFICATION OF THE DERIVED ANALYTICAL EQUATIONS (11) (20)

Parameter		Value
V_{dc}	[V]	400
$V_{\mathrm{ac,ph}}$	[V]	110
f_{sw}	[kHz]	36
L_{f}	[mH]	1.45
C_{dc}	[μF]	492

The average value of the dc-link current defines the active power flowing through the converter. It can flow only from and to the battery since the other elements cannot deliver continuous active power. Therefore, the average dc-link current for one fundamental period of the converter is given by only the positive sequence component, and it can be derived equalling the converter active dc and ac powers

$$I_{\mathrm{dc,avg}} \cdot V_{\mathrm{dc}} = 3V_{\mathrm{ac}}I_+\cos\phi_+. \quad (12)$$

$$I_{\mathrm{dc,avg}} = \frac{3m\hat{I}_+}{4}\cos\phi_+. \quad (13)$$

The low-frequency components of the dc currents also impact the dc-link design. The 100-Hz component, in a 3L-4W VSC, is shared between the dc-link capacitors and the battery cells. However, in contrast with the battery cells, the capacitor bank has a much higher impedance at low frequency. Therefore, it can be assumed that the low-frequency components flow entirely through the battery cells and not through the capacitors unless a bulky dc LC filter filters these out. Due to the necessary low cut-off frequency, it would require very large component values and, therefore, impractical. As presented in [16], the rms value of the negative sequence current in the dc-link can be determined

$$I_{\mathrm{dc-}} = \frac{3m}{4\sqrt{2}}\hat{I}_-. \quad (14)$$

The zero-sequence currents of the three ac phases are summed up in the dc-link. In the symmetric and conventional SPWM, this flows evenly in the positive and negative rail of the dc-link; therefore, the rms value of the zero-sequence component in the positive rail of the dc-link is half the three times the phase zero-sequence current, since it is equally split between the positive and negative dc-link rails, and can be expressed as

$$I_{\mathrm{dc0}} = \frac{3I_0}{2} = \frac{3\hat{I}_0}{2\sqrt{2}}. \quad (15)$$

Having quantified the various components of the dc-link rms current, it is possible to evaluate the current flowing through the capacitors, I_{cap}, which is composed of the 50 Hz and the high-frequency component. I_{cap} can be derived

subtracting (13) and (14) from (11)

$$I_{\text{cap}} = \sqrt{I_{\text{dc}}^2 - I_{\text{dc,avg}}^2 - I_{\text{dc}-}^2} \tag{16}$$

$$I_{\text{cap}} = \sqrt{\frac{\sqrt{3}}{4\pi} \cdot \left[\left(1 + \left(4 - \frac{9\pi}{4\sqrt{3}}m\right)\cos^2\phi_1\right)\hat{I}_+^2 m + 3m\hat{I}_-^2\left(1 - \frac{\sqrt{3}\pi m}{8}\right) + \left(\sqrt{3}\pi - 2m\right)3\hat{I}_0^2 - 2m\hat{I}_-\hat{I}_0\cos(\phi_- + \phi_0)\right]}. \tag{17}$$

The 50-Hz component flows through the capacitors because their midpoint provides the connection to the neutral conductor. The high-frequency component, instead, flows through them because the electrolytic capacitors offer a lower impedance path for the high-frequency currents than the battery. From (17), the rms value of high-frequency dc-link current can be calculated by nullifying the negative and zero-sequence component as

$$I_{\text{cap,hf}} = \sqrt{\frac{\sqrt{3}}{4\pi} \cdot \left[\left(1 + \left(4 - \frac{9\pi}{4\sqrt{3}}m\right)\cos^2\phi_1\right)\hat{I}_+^2 m\right]}. \tag{18}$$

The dc and 100-Hz components flow through the battery cells, therefore the rms current flowing through the battery, I_{batt}, can be calculated as

$$I_{\text{batt}} = \sqrt{I_{\text{dc,avg}}^2 + I_{\text{dc}-}^2} \tag{19}$$

$$I_{\text{batt}} = \frac{3m}{2\sqrt{2}}\sqrt{\hat{I}_+^2 \cdot \cos^2\phi_+ + \frac{\hat{I}_-^2}{4}}. \tag{20}$$

To verify the accuracy of the derived equations, the circuit simulation software PLECS is used. A simulation model of a 3L-4W VSC has been built so to calculate the rms current flowing through the dc-link and its components. The parameters implemented in the circuit simulation software PLECS are listed in Table I. The simulations are run with a variable step solver, DOPRI (non-stiff), with maximum step size and relative tolerance of 1 μs. Several values of unbalance are analyzed. In fact, the loading of one phase is varied from 0% to 100% of the loading of the other two phases, which are kept constant at rated power. Fig. 7 displays the total rms current in the dc-link and its various components, following the conditions of Table I. Fig. 8, instead, plots the rms currents flowing through the dc-link split capacitors and the battery cells. In the two figures, both the analytically calculated values through (17) and (20) and the ones derived from the circuit simulator PLECS are reported. The analytical equations slightly underestimate the current values, and this is because the ac current is not perfectly sinusoidal, as assumed in the derivation of the equations. In fact, in PLECS, the high-frequency ripple has a peak value of 20% of the low-frequency 50-Hz component. This ripple level of 20% is compatible with the typical design criteria of L and LCL filter for the grid connection of VSC [28], [29]. All in all, it can be noted that the analytical expressions provide excellent accuracy to the circuit simulator; hence such equations can be used to design the dc-link components of a 3L-4W VSC.

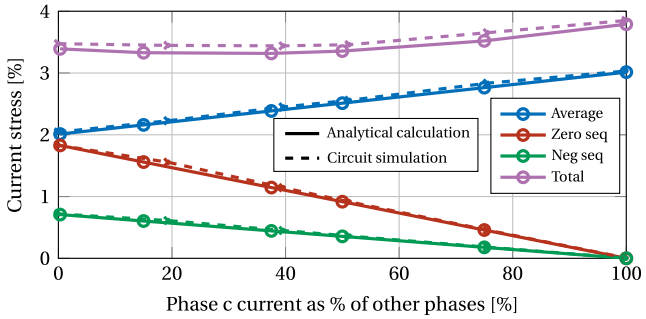


Fig. 7. Total rms current in the dc-link and its various components, when I_a and I_b are equal to 3.7 A and I_c is varied from 0 to 3.7 A. Both the analytically calculated values through (11)–(15), and the ones derived from the circuit simulator PLECS are reported.

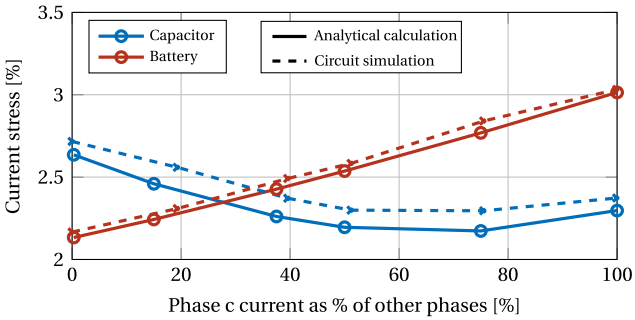


Fig. 8. RMS currents flowing through the dc-link split capacitors and the battery cells, when I_a and I_b are equal to 3.7 A and I_c is varied from 0 to 3.7 A. Both the analytically calculated values through (17) and (20), and the ones derived from the circuit simulator PLECS are reported.

TABLE II

DC-LINK CAPACITORS CURRENTS AND CAPACITANCE REQUIREMENTS FOR A 100-kW VSC, UNDER BALANCED AND UNBALANCED CONDITIONS, DERIVED THROUGH THE METHOD DESCRIBED IN SECTION IV, WHERE I_a IS FIXED TO THE NOMINAL VALUE AND I_b AND I_c VARIED

Parameter and relevant equation		Operating condition				
		Case A I_b=I_a I_c=I_a	Case B I_b=I_a/2 I_c=I_a/2	Case C I_b=0 I_c=0	Case D I_b=I_a I_c=0	Case E I_b=I_a I_c=I_a/2
I_+ [A]	(1)	144.34	96.23	48.11	120.28	96.23
I_{cap} [A]	(17)	83.70	68.93	85.62	80.64	98.31
I_{dc0} [A]	(15)	0	36.08	72.17	36.08	72.17
$I_{\text{cap,hf}}$ [A]	(18)	83.70	58.73	46.06	72.12	66.76
$C_{\text{dc,e}}$ [mF]	(4)	0.794	0.794	0.794	0.794	0.794
C_{dchf} [mF]	(6)	0.306	0.204	0.102	0.255	0.204
$C_{\text{dc}-}$ [mF]	(7)	0	2.063	4.125	2.063	4.125
C_{dc0} [mF]	(8)	0	1.911	3.822	1.911	3.882

C. Example Design of an 100-kW 3L-4W VSC

The conventional approach for achieving the power redistribution functionality consists of using a separate compensator for processing the unbalanced power. This solution requires an additional converter which is inevitably more expensive than the integrated solution proposed in this article. Fig. 9 shows that integrating the power redistributor functionality in a single BESS unit is advantageous in terms of dc-link overall ratings, such as current stress and capacitance requirement

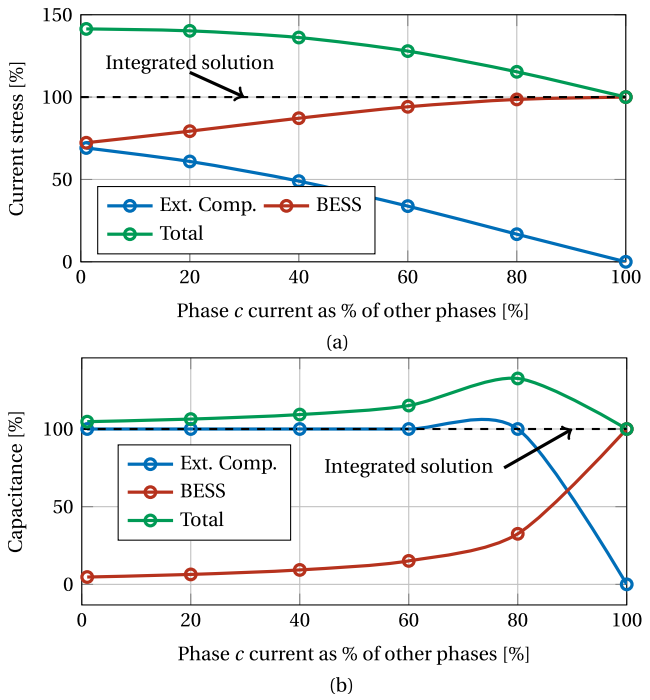


Fig. 9. (a) DC-link current stress and (b) required capacitance on the external compensators and on the BESS providing symmetric power as percentage of the values of the integrated solution while varying the unbalance processed by the system. The BESS values are calculated for the active power processed by an integrated solution at that unbalance point.

when compared to two separate devices, a BESS operating symmetric active power and an external compensator to manage the unbalance. Fig. 9 plots the dc-link current stress and required capacitance on the external compensators and on the BESS providing symmetric power as a percentage of the values of the integrated solution. In terms of current stress, it is seen in Fig. 9(a) that splitting the unbalance management and symmetric power exchange between two units leads to lower current stress in the individual units, but when aggregated it is always higher than the integrated solution. Additionally, Fig. 9(b) shows that an external compensator would require the same capacitance of the integrated solution nullifying the advantage of splitting the functionalities between two units. Moreover, an external compensator would require additional, power semiconductor half-bridge modules, LCL filters for the interconnection to the grid, control systems, measurements sensors, protection systems, and finally the mechanical switches and structure. However, in an integrated solution such as the one proposed here, all these components are already present since they are necessary for interfacing the battery storage system to the ac grid. Therefore these can be leveraged as power redistributor, resulting in a much lower overall component count and costs.

The design process of a two-level 3L-4W VSC consists of several steps. At first, the power and voltage levels of the converter have to be set. A LV dc-link is taken into account, $V_{\rm dc} = 750$–950 V, coherently with the specifications of commercial battery racks [30], [31]. The ac voltage is set to 400-V line-to-line, a standard rating found in European's LV distribution grids. Given these specifications, it is possible to select the semiconductors and design the output LCL filter properly [9], [28], [29]. Therefore, the design of the dc-link capacitor bank is of particular interest to this article. The dc-link capacitor bank is also the main component whose size is affected by the unbalance redistribution. Therefore, the system size increment is related to the increase of the required capacitance. The other components, e.g., the semiconductor modules, the cooling systems, and the LCL output filters, do not see a size increase when enabling the power redistributor functionality in a 3L-4W VSC.

As already mentioned in this section, the capacitors have to be rated for a certain capacitance and current to respect the component's thermal limits. Such design requirements are listed in Table II, for certain operating conditions. Table II, reports the dc-link currents and capacitance values required in a 100-kW VSC, operating under balanced power conditions, Case A, and for different power unbalanced conditions, Cases B to E. In these case studies, I_a is fixed to the nominal value and I_b and I_c are intentionally varied. Cases B and C see phase b and c operating at equal value at 50% I_n and 0% I_n respectively. Case D and E consider two phases at nominal current and one phase at 50%I_n and 0% I_n respectively. The highest capacitance requirement is found in Case C and E, together with the highest 50 Hz current harmonics in the capacitor. In comparison, the highest total rms current in the capacitors is found in Case E, which is, therefore, the most demanding case for the design of the dc-link capacitors.

For this study, the commercially available capacitors of the 500 $V_{\rm dc}$ class from Cornell Dubilier [32] have been considered. Given the maximum value of $I_{\rm cap}$ and the current capability of the single capacitors, the number of parallel capacitor strings, which consists of two series capacitors, are found. In this way, several dc-link designs are derived according to the components' characteristics. The solutions that do not satisfy the minimum capacitance constraints given in (4)–(8) or that show a maximum hot-spot temperature, $T_{\rm hs}$, higher than 95 °C, the limit set in the data-sheet, $T_{\rm max}$, are discarded. Following this procedure, in Fig. 10, the cost of several dc-link capacitors designs that meet the requirements for a 100-kW VSC operating under balanced load is plotted versus their expected lifetime. The commercial cost figures are derived from a component distributor [33], while the capacitor lifetime is derived according to the methodology suggested by the manufacturer [34]. The capacitors' operating voltage and the hot-spot temperature are the main degradation drivers. [35], [36]. The manufacturer of the considered capacitors gives the capacitor lifetime model as [34]

$$L_c = L_b \cdot \left(4.3 - 3.3\frac{V_{\rm dc}}{V_r}\right) \cdot 2^{\frac{T_m - T_c}{10}} \tag{21}$$

where L_b is the rated lifetime, V_r is rated voltage, T_m is the maximum rated core temperature, and T_c the operating core temperature [34]. T_m and L_b are related to the capacitor packaging and manufacturing, as specified by the manufacturer [34]. The operating hot-spot temperature, T_c, is estimated based on the capacitor equivalent series resistance, ESR, the thermal resistance $Z_{\rm th}$, both from data-sheet, and on the current

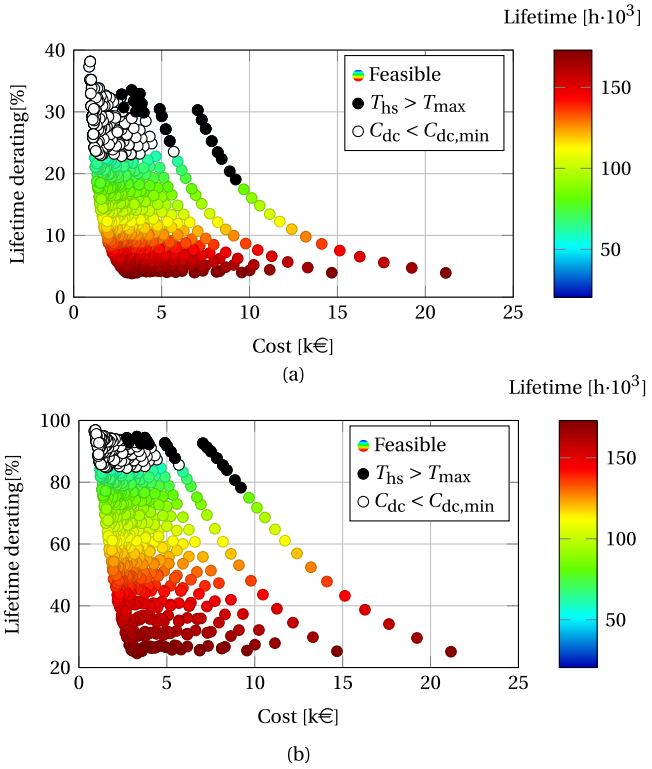


Fig. 10. Costs and expected operating hours of the dc-link capacitors designs for a 100-kW VSC operating under balanced conditions. The y-axis shows the lifetime derating of such designs when operating in unbalanced condition: (a) Case C and (b) Case E of Table II.

flowing through the capacitor [34]

$$T_c = T_a + 1.5 \cdot Z_{\text{th}} \cdot \left(I_{\text{cap}}^2 \cdot \text{ESR} + I_{\text{leak}}(V_{\text{op}}) \cdot V_{\text{op}} \right) \quad (22)$$

where I_{leak} is the capacitor leakage current as function of V_{dc}, given by the datasheet and V_{dc} the operating voltage [32]. The manufacturer recommends the addition of the coefficient 1.5, so that the heat rise due to current ripple weights more than the ambient temperature T_a effect [34].

Furthermore, in Fig. 10(a) and (b), the y-axis shows the lifetime derating of such designs when operating in two unbalanced conditions, which are Case C and E of Table II, respectively. The lifetime derating indicates the capacitor lifetime if operating in unbalanced conditions, $L_{c,\text{ub}}$, as a percentage of their lifetime if operating under balanced conditions, $L_{c,b}$, and it is calculated as

$$\text{Derating} = \frac{L_{c,\text{ub}}}{L_{c,b}} \cdot 100[\%]. \quad (23)$$

The designs in black and white are the ones that are feasible for the operation under balanced load, but not for unbalanced loads, due to a too low capacitance value or a thermal reason, respectively. Nonetheless, the designs in the top left of the figures are the ones that typically offer low safety margins, especially in terms of thermal performance. Therefore, for a marginal cost increase, the designs at the bottom left of the graphs significantly improve operating hours during both balanced and unbalanced operations. Hence these designs

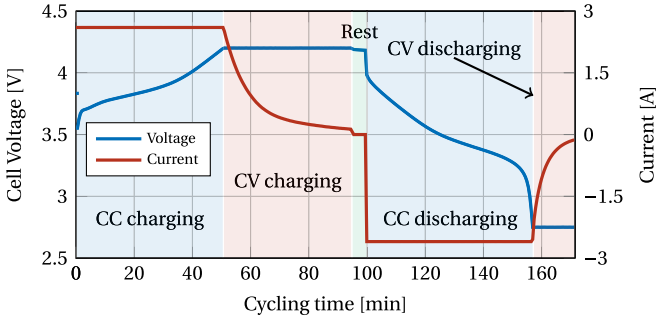


Fig. 11. Measured cycling parameters of the ICR18650-26F battery cell when cycled with the CC-CV method at 1-C. The cell is cycled with the Arbin Laboratory Battery Testing LBT22043 of Fig. 12 and the cell voltage and current are measured with a 30-s sampling time.

should be prioritized for the dc-link of the grid-connected VSC.

IV. 100-Hz Ripple Battery Testing

As discussed in Section IV, due to the high impedance, the dc-link capacitors cannot filter the 100-Hz component of the dc-link current, which then flows through the battery. In this regard, it is important to investigate whether the 100-Hz component impacts the battery degradation. Researches available in the literature [17], [18], [19], [20], [21], [37] have investigated the electrochemical phenomena that drive the cells' impedance variation with frequency, and the effect of ac current ripple on Lithium-ion batteries charging. However, the focus on these studies is typically found on ac frequencies at which the battery shows the minimum impedance to optimize the charging time and power efficiency. Several waveform shapes have been investigated, such as sinusoidal, triangular, and square, and some of the reviewed literature claim positive results when superimposing an ac ripple at the minimum impedance frequency [21]. However, other studies challenge these results, showing contrasting facts [20].

In this context, the effect of the ac current ripple in Lithium-ion cells is investigated. The tested cells are the ICR18650-26F from Samsung SDI, based on the NMC cathode technology, which is well suitable for stationary application [10]. Their nominal voltage is 3.7 V, and they have a rated capacity of 2600 mAh. These low-voltage cells are the building blocks for high-capacity battery packs. Several lithium-ion cells of this kind can be stacked up together in series and parallel strings to assemble battery packs with higher voltage and capacity ratings.

Various ICR18650-26F cells have been cycled to evaluate the impact of the 100 Hz ripple. The manufacturer recommended method for charging and discharging such cells consists of the constant current and constant voltage (CC-CV) method [38]. The CC-CV method is the industry standard for the charging of electrochemical batteries [39], [40]. This method consists in two parts. The first part, constant current, foresees the charging of the battery with constant current, I_{cc} until the cell voltage reaches a threshold, which is the maximum allowed cell voltage, V_{max}. Once this voltage is

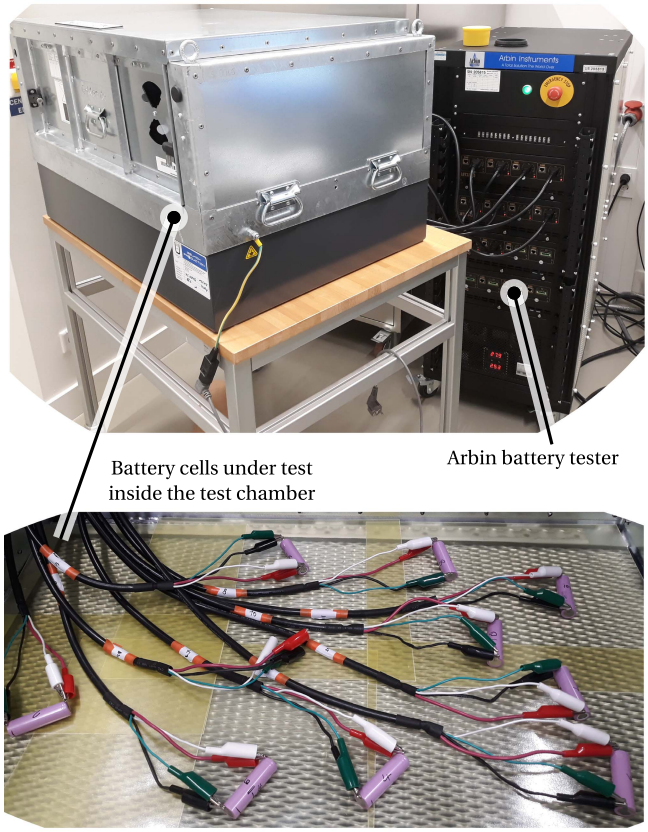


Fig. 12. Battery cells test set up consisting of test chamber and the Arbin Laboratory Battery Testing LBT22043 used to perform the power cycling tests.

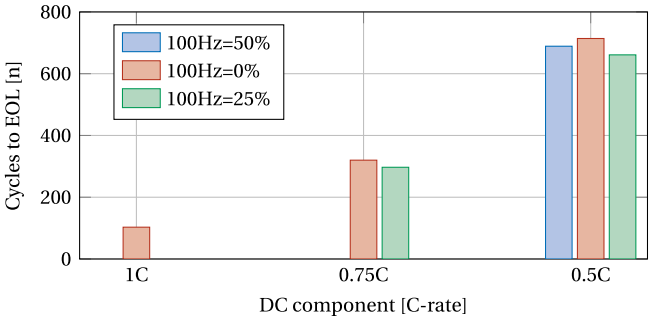


Fig. 13. Charge-discharge cycles performed by the ICR18650-26F Lithium-ion cell to reach EoL under different charging and discharging conditions. Note that for all cases the superimposed instant peak current, i.e., dc + ac components, circulating through the battery cells is limited to 1 C-rating.

reached, the current is gradually reduced until it reaches a cut-off threshold. The measured current and voltage waveform of the CC-CV method of a charge and discharge cycle at 1-C of a ICR18650-26F cell is shown in Fig. 11. The cell is cycled with the Arbin Laboratory Battery Testing LBT22043 of Fig. 12 and the cell voltage and current are measured with a 30-s sampling time. Note that the plotted CC-CV profile of Fig. 11 is obtained from a new cell which has not been cycled before. As possible to see in Fig. 11, the manufacturer recommends a cell charging voltage of 4.2 V and a discharge cut-off voltage of 2.75 V; the maximum charging current allowed (1-C) is

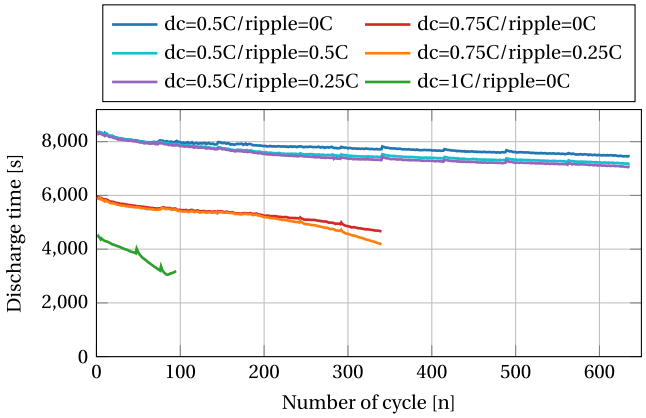


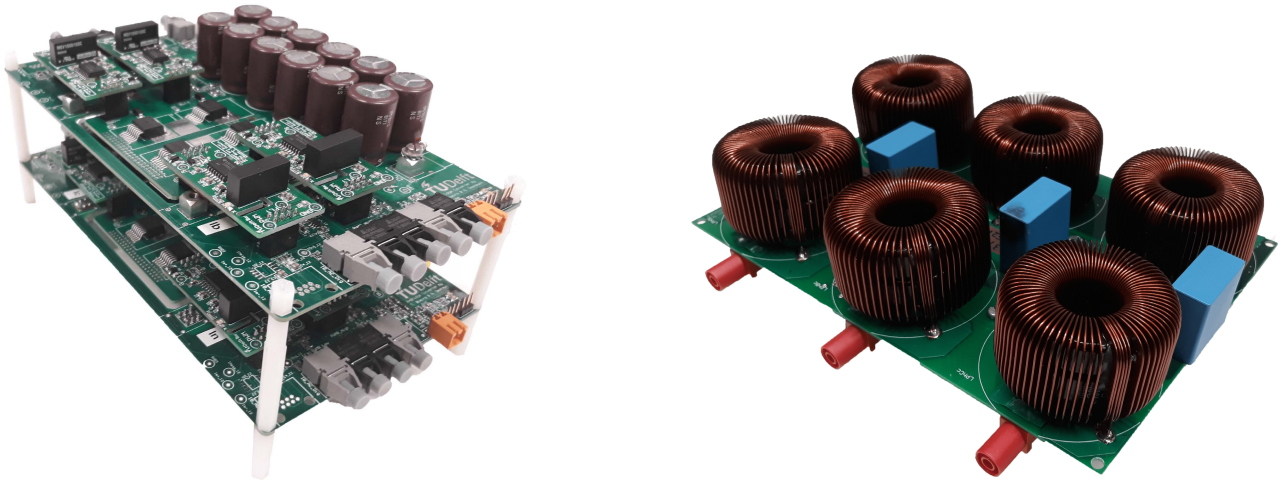
Fig. 14. Discharge time during the cycling life of the ICR18650-26F battery cell when cycled in different conditions. It can be seen that higher dc C-rate leads to faster discharging time, as well as the superimposition of the 100-Hz ac ripple.

2.6 A [38]. The cells under test are cycled with 100% depth of discharge (DoD), following the manufacturer's recommended maximum and cut-off voltages to reach 20% capacity fading, the threshold for the battery EoL.

Three battery cells are cycled with CC-CV method, with different C-rates of 0.5, 0.75, and 1. The cycling method of the other cells, instead, differs during the CC region. Two cells, in fact, are charged and discharged with a dc C-rate of 0.5 with a superimposed ac sinusoidal current ripple of 100 Hz with a peak amplitude of 25% and 50% the rated charging current. Lastly, one battery cell is cycled with a dc C-rate of 0.75 with a superimposed 100-Hz ripple with a peak amplitude of 25% the rated charging current of 1C. The combination between dc current and ac ripple is set not to exceed the maximum allowed charging and discharging current, which is 1C. Note that during the tests of the cells which are cycled with superimposed ac ripple, when the cell reaches the maximum voltage allowed by the manufacturer during charging, the current is gradually reduced so to keep the cell voltage constant at the maximum value, as shown in Fig. 11. For the discharging of the cell, when the cut-off voltage is reached, the discharging current is reduced so to keep the cell voltage from not dropping below the minimum allowed value.

The batteries are tested with the Arbin Laboratory Battery Testing LBT22043 [41] which allows precision measurements for simultaneous testing and characterization of up to 16 battery cells. The battery tester can be seen in Fig. 12. The cells are kept at a temperature of 20 °C, which is compatible with the operating temperature of large scale BESS, where the cells are stored in containers equipped with air conditioning which keep the cells at a constant temperature in the range of 20 °C–25 °C [42].

The number of cycles performed to reach EoL of the ICR18650-26F Lithium-ion cell under different charging conditions is shown in Fig. 13. The lifetime of the ICR18650-26F cells cycled with the CC-CV method is used as a benchmark versus the charging with the superimposed ripple. It can be noted that there is a strong correlation between the cell's



(a) (b)

Fig. 15. (a) Three phase legs two-level VSC prototype used for the experimental verification of the BESS functionality as power redistributor and (b) LCL filter used to interface the VSC to the ac grid.

degradation and the dc C-rate; with a high C-rate the cells degrade more and reach EoL sooner, which is compatible with previous literature finds [21]. Furthermore, regarding the influence of the 100-Hz ripple, Fig. 13 shows that the cells which have been cycled with the superimposed ripple shows higher degradation than the ones cycled with pure dc current, with approximately 10% fewer cycles to reach EoL. This phenomenon can be traced back to the additional losses due to the ripple component. The 100-Hz ripple, in fact, does not match the minimum impedance frequency of the battery, which is generally found at higher frequencies than 100 Hz, $\geq$400 Hz [21], and therefore leads to additional losses. Additionally, in Fig. 14 the discharge time of the ICR18650-26F battery cells when cycled in different conditions are shown. These are displayed under the different cycling conditions previously mentioned, where the dc C-rate and the amplitude of the superimposed 100-Hz ac ripple are varied. It can be seen that higher dc C-rate leads to faster discharging time, as well as the superimposition of the 100-Hz ac ripple. The discharge times of Fig. 14 are in agreement with the number of cycle displayed in Fig. 13, where the cycling pattern that leads to faster degradation also leads to faster discharge time.

The application of BESS as power redistributors, when interfaced to the grid with a 3L-4W VSC, has the drawback of the higher cells degradation during unbalance compensation when a negative sequence arises. To contrast this, an additional half-bridge leg can be added to prevent the 100-Hz ripple from flowing to the battery. All in all, from the cycling tests performed, it is clear that keeping the other cycling parameters fixed, the dc C-rate is the dominant factor for cells degradation, and that superimposing the 100-Hz ripple leads to additional cell degradation.

V. Experimental Verification of the Power Redistributor Functionality

This section shows experimentally the working principle of a BESS acting as a power redistributor. The setup consists of

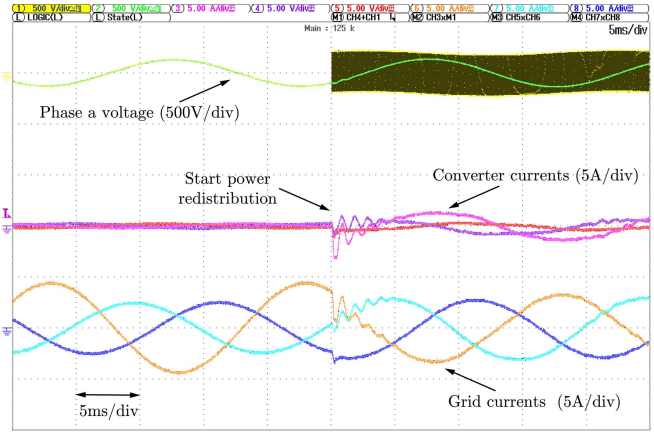


Fig. 16. Grid and VSC currents when supplying an unbalanced load; when it is turned on, the VSC redistributes the power among the phases, compensating the unbalance in the grid currents. The yellow and green waveforms represent the phase *a* voltage before and after the LCL filter. The other channels represent the grid and converter phase currents, as indicated in this figure.

a 2-kW 3L-4W VSC, shown in Fig. 15(a), which interfaces a SM500-CP-90 dc voltage source from Delta Elektronika, representing a battery storage, with the GE15 ac source from Cinergia, which emulates the ac distribution grid. A LCL filter, shown in Fig. 15(b), between the VSC and the ac grid is used to attenuate the current harmonics according to the IEEE-519/2014 [43]. The VSC is digitally controlled, with Sinusoidal PWM, through an OP5700 real-time simulator from OPAL-RT Technologies. The experimental testing fixed the dc-link voltage to 400 V and the ac phase rms voltage to 110 V. Furthermore, unbalanced loads, consisting of two resistors of 60 Ω and one resistor of 30 Ω and whose unbalance the BESS is tasked to compensate, are connected in parallel with the ac source. The experimental setup, based on the 3L-4W VSC of Fig. 15 is used to demonstrate the capability of such VSC to operate as power redistributor, uninterruptible power supply (UPS), and exchanging power with the grid.

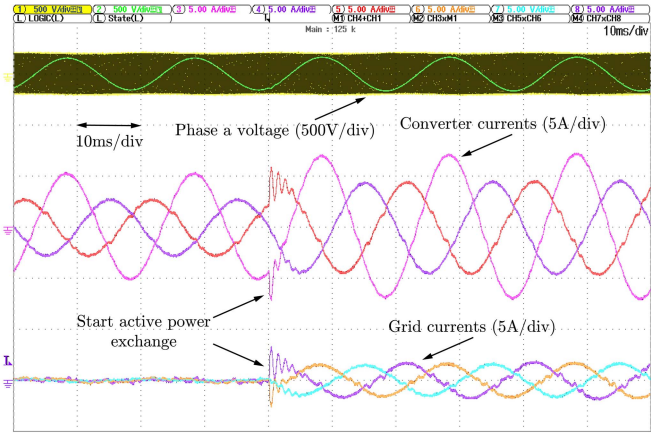


Fig. 17. VSC supplying an unbalanced loads and injecting active power to the ac source. The yellow and green waveforms represent the phase *a* voltage before and after the LCL filter. The other channels represent the grid and converter phase currents, as indicated in the figure.

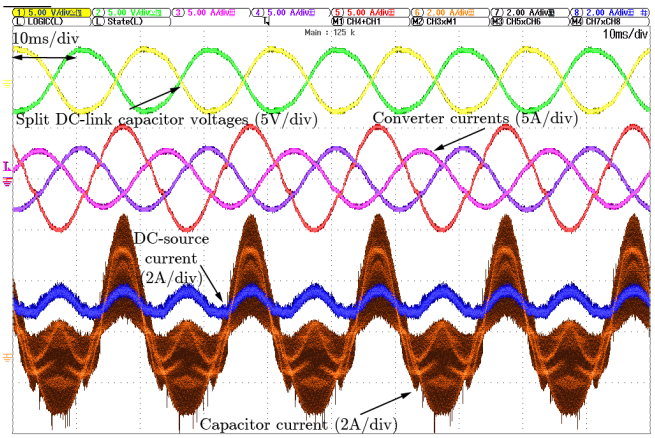


Fig. 19. AC currents, dc-link split capacitor voltages, and current flowing through the capacitor and the dc-source of a 3L-4W VSC when supplying an unbalanced load.

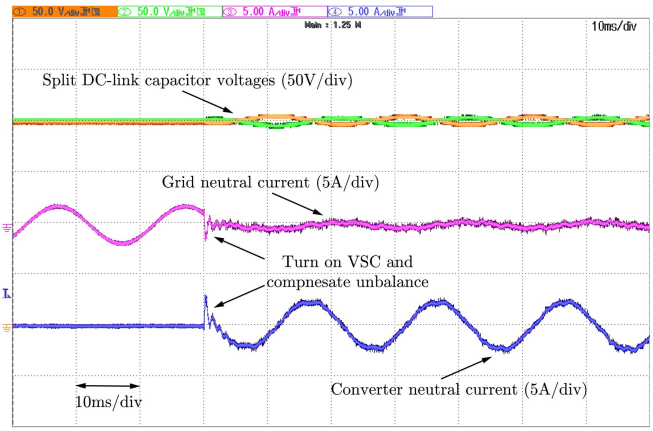


Fig. 18. VSC and grid neutral current when supplying power unbalanced loads. The green and orange waveforms shows the voltage across the two split dc-link capacitors.

Fig. 16 shows the BESS working as a power redistributor, therefore supplying only the unbalance power. When the converter turns on, the grid currents get balanced by the converter operation. The VSC provides the negative and zero-sequence powers, leaving the ac grid balanced and supplying only the load active power. On top of the power redistribution functionality, the 3L-4W BESS can also operate as a UPS and exchange active and reactive power with the grid. These functionalities are demonstrated in Fig. 17. In the left part, the BESS is acting as UPS, fully supplying the load, while in the right side of the figure, together with the UPS operation, the BESS can superimpose the exchange of active power to the ac grid. Hence, it is shown that the technical compatibility of the power redistribution functionality with the core grid-connected BESS applications, which require symmetric active and reactive power exchange with the grid.

Fig. 18 displays the neutral currents of the ac grid and of the VSC, together with the voltages across the two split dc-link capacitors, the green, and orange waveforms. When the VSC starts compensating the power unbalance, it provides the neutral current to the load or the whole zero-sequence current component; therefore, the current in the neutral conductor of the ac grid will be considerably reduced. It can be seen that the split dc-link capacitors are subject to a 50-Hz ripple, deriving by the flow of the neutral current. This fact can be seen better in Fig. 19, where the dc-link split capacitors voltages are displayed with the oscilloscope in ac coupling in so to better show the 50-Hz ac ripple. Furthermore, Fig. 19 shows the current flowing through the dc-link capacitors, in orange, and the dc-source, in blue, which represents the electrochemical battery storage. Note that, since the 3L-4W VSC of Fig. 15(a) is assembled with two parallel boards, the current flowing through the dc-link capacitors shown in Fig. 19 is measured in only one of the two boards capacitors. Therefore, the dc-link capacitors current shown in Fig. 19 represents half of the total dc-link capacitors current. The experimental verification confirms the theoretical analysis of Section III-B, which predicted that the dc source would absorb the 100-Hz current ripple, while the dc-link capacitor takes the high-frequency ripple and the 50-Hz current which then flows to the neutral conductor.

VI. Conclusion

This article investigated the application of BESSs as power redistributors in unbalanced distribution grids. The modeling and design guidelines for the dc-link of a two-level 3L-4W VSC operating under unbalanced loads have been detailed. Closed-form expression for the rms currents in the dc-link capacitors and the voltage ripple across them, which can be used for their design, have been derived. The analysis shows that the dc-link capacitors can satisfy the thermal and capacitance requirements under unbalanced power loads if designed adequately for the balanced power operation. Furthermore, a down-scaled VSC prototype is used to demonstrate the working principle of the BESS providing unbalance redistribution. The VSC was able to verify the study demonstrating that the power redistributor functionality can be added as an optional grid ancillary service to the classic BESS applications. Additionally, several ICR18650-26F Lithium-ion cells have

been cycled with an Arbin LBT22043 to reach EoL. A 100-Hz ac current sinusoidal ripple has been superimposed, and its effect on the cells' lifetime has been compared to the standard CC-CV charging method. The cycling tests show that the ac ripple's superimposition leads to an increase in degradation of 10% with respect to the standard CC-CV method; nonetheless, the main driving for degradation remains the charging and discharging C-rate.

All in all, in this article, it was shown that the power redistribution functionality could be successfully implemented in commercially available BESSs as an add-on functionality without significant hardware upgrades and performance deterioration.

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