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Ji, Xinrui ; van Zeijl, Henk; Romijn, Joost; van Ginkel, H.J.; Liu, Xu; Zhang, Guoqi

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Xinrui Ji
Electronic Components, Technology and Materials
Delft University of Technology
Delft, The Netherland
X.Ji@tudelft.nl

Henk van Zeijl
Electronic Components, Technology and Materials
Delft University of Technology
Delft, The Netherland
H.W.vanZeijl@tudelft.nl

Joost Romijn
Electronic Components, Technology and Materials
Delft University of Technology
Delft, The Netherland
J.Romijn@tudelft.nl

Hendrik Joost van Ginkel
Electronic Components, Technology and Materials
Delft University of Technology
Delft, The Netherland
H.J.vanGinkel@tudelft.nl

Xu Liu
Electronic Components, Technology and Materials
Delft University of Technology
Delft, The Netherland
X.Liu-12@tudelft.nl

Guoqi Zhang
Electronic Components, Technology and Materials
Delft University of Technology
Delft, The Netherland
G.Q.Zhang@tudelft.nl

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***Abstract*—The continuous trend to integrate more multi-functions in a package often involves, Heterogeneous Integration of multi-functional blocks in some kind of 3D stacking. The conventional flip chip for die-on-substrate technology applies solder for integration. However, solder joint integration has the disadvantages of restricting height, reflow issues and re-melting at high operating temperatures. Nanometallic particle sintering offers a potential solution for these solder related issues. Nanometallic particle sintering occurs at low temperature and does not reflow and melt at higher temperatures. Hence, it can be applied for quite precise alignment and integration technologies, such as photonic components on silicon for harsh environment applications. In order to test this concept, we use sapphire and Si wafers with different mechanical properties, which can lead to the coefficient of thermal expansion mismatch. The sapphire chip can operate at a higher temperature applied for ultraviolet photonics application. This report describes a novel approach using copper nanoparticles paste patterned through photolithographic stencil printing. The photoresist acts as the stencil mask, and a photoresist lift-off process is applied to strip the photoresist stencil. This process has the advantages of lithographic form factor and precision and provides a chip to chip interconnect with a standard height of 20 µm.**

Keywords—flip chip, heterogeneous integration, copper nanoparticle, nano Cu bump, low temperature sintering

I. INTRODUCTION

The trend to integrate more microelectronic functions per unit area is not solely supported by Moore's law anymore [1]. Heterogeneous and 3D integration are now the key enablers to drive further integration, which will put chip assembly technologies more in the center of system creations. Moreover, not only the system in packages (SiPs) but also the heterogeneous integration (HI) can broaden the spectrum of applications beyond the conventional microelectronic application. Hence, novel packaging solutions are required. With the high demand for more multi-functionalization and "more-than-Moore" application, the 3D stack integration can be the approach at chip- and wafer-level such as chip to wafer (C2W) and chip to chip (C2C) [2]. Flip chip technology plays an important role in 3D integration and is recognized as an essential building block that can support more complex C2W and C2C assemblies [3].

Currently, flip chip technologies rely on lead-free solder joints on copper micro bumps. The lead-free solder has a reflow temperature of 220-280 °C, which is challenging applications in a harsh environment, such as power electronics and aerospace applications. In addition, the solder joints are restricted by dimensions and height. To investigate the 3D heterogeneous integration for the state of art devices, such as silicon carbide and sapphire-based devices, the conventional solder joints may not be suitable. Nanometallic particle (NMP) materials have low sintering temperature [7]. The higher melting point of NMP material than that of solder, and it has the potential to become a novel packaging material to replace solder [4][7].

Copper nanoparticles (nano-Cu) joint bonding technology is investigated due to its good thermal dissipation ability, mechanical property and electrical conductivity. In this study, we used nano-Cu paste as the bonding materials. The lithographically patterned photoresist was defined as a stencil mask, combined with stencil printing, to obtain nano-Cu paste joints after the lift-off process. Sapphire chips were applied as the top chip, which had the advantages of higher temperature operation and UV light photonics applications, to be used in harsh environments [8]. The sintering process of Nano-Cu was applied at 280 ℃ at low pressure of 9 MPa and was performed to obtain the interconnect between the top chip and bottom substrate.

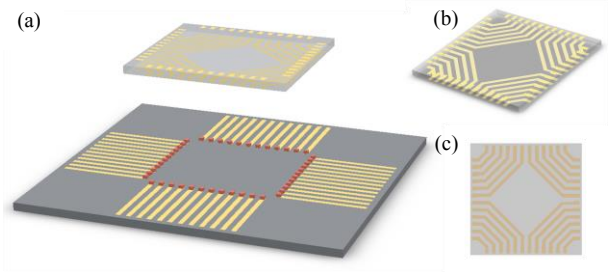

Fig. 1. Schematic illustration of (a) 3D stacked structure of sapphire chip to Si substrate nano-Cu joints filp chip, (b) filpped sapphire chip with Au deposition patterns and (c) the front side of sapphire chip with the Au interconnect lines.

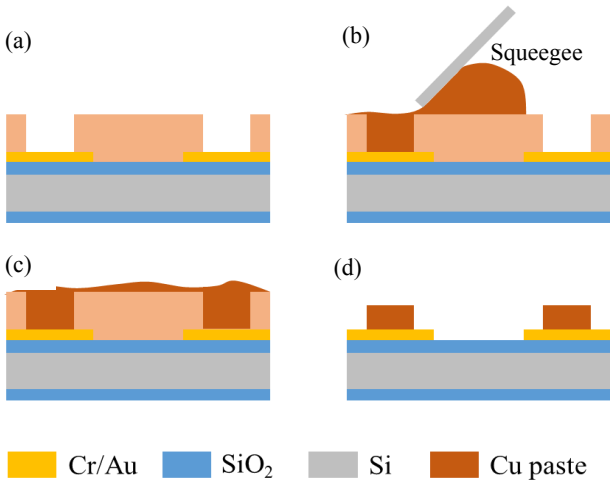

Fig. 2. An overview of the patterns transferring process using photolithography stencil printing on photoresist mask and sequential lift-off process.

II. Methods and Materials

A. Test Interconnecting Specimens Design and Fabrication

To implement the interconnects, two types of the wafers are prepared. One was a single side polished 525 µm silicon substrate and the other was a 650 µm sapphire wafer. The Si wafer was first insulated with 300 nm thermal oxide on both sides, and then both the Si wafer as well as the sapphire wafer were patterned with 10/100 nm Cr/Au by photolithography and lift-off. To fabricate the stacked integration sample, the Si substrate and sapphire chip were designed as 20x20 mm^2 dies and 10x10 mm^2 dies with measurement pads and interconnect patterns, respectively. As shown in Fig. 1a, the bottom Si substrate has fan-out interconnects measurement pads consisting of four blocks of 12 parallel Cr/Au (10/100 nm) lines with a length of 5.6 mm, and a width of 300 µm. For interconnecting, four interconnecting corners of 12 Cr/Au lines with a width of 300 µm were patterned on the topside of a sapphire chip (Fig. 1c) to connect the Si substrate through nano-Cu. Finally, alignment pads are deposited on the backside of the sapphire chip (Fig. 1b) [9].

B. Photographic Pattering and Wafer Bonding Process

To transfer the nano-Cu paste, the patterned photoresist and stencil printing was applied [4][5]. Fig. 2 depicts the process flow of nano-Cu paste photolithography stencil printing in this study. A 10 µm positive photoresist layer was first spin-coated on the Si wafer, then was exposed and developed with a contact opening, as demonstrated in Fig. 2a. Nano-Cu paste was manually spread by a silicon squeegee on the patterned Si wafer substrate, as shown in Fig. 2b. Then, test wafers were dried in an oven at 110 ℃ for 15 minutes (Fig. 2c). Sequently, the lift-off process was applied in a bath at 70 ℃ by N-methyl-2-pyrrolidone to strip the photoresist. The nano-Cu paste patterns were then completed, as shown in Fig. 2d.

For the flip chip bonding process, the test Si wafer was cut into four quarters and the sapphire wafer was diced into 10x10 mm^2 dies. Fig. 1a illustrates the structure schematic of the resulting stacked flip chip. The top sapphire die was flipped and aligned under optical microscopy to stack onto the patterned Si substrate. The nano-Cu were applied as squares

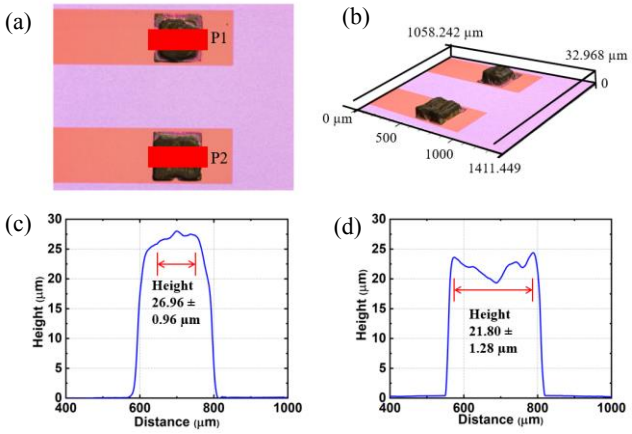

Fig. 3. (a) Top view of microscopy image for the specimen after lift-off process, (b) 3D image of nano-Cu bumps after lift-off, (c) the profile of the nano-Cu bump indicated at P1 in (a) and (d) the profile of the nano-Cu bump indicated at P2 in (a).

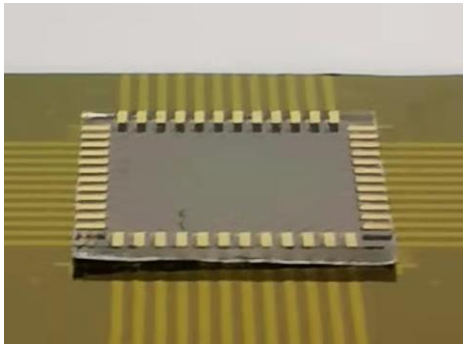

Fig. 4. Resulting specimens after bonding, image at tilted.

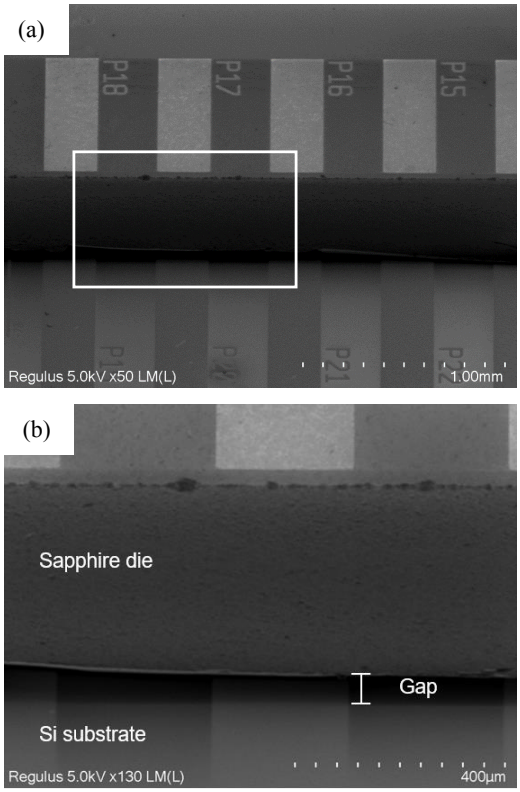

Fig. 5. (a) SEM image of the bonding edge at a 45° tilt angle. (b) Close-up view of the side-edge, indicated by the white box in (a), showing the alignment result and the gap due to Cu bumps..

of 260x260 µm^2 on the overlapping area between the upper and lower interconnect lines using the previously mentioned patterning method. After alignment, the sapphire to Si flip chip was transferred to a AML waferbonder for nano-Cu sintering. That bonding tool provided a high vacuum environment (~1x10^{-3} mbar) to prevent Cu nanoparticles from oxidation. The specimen was bonded with a pressure of 9 MPa at 280 °C for 60 min.

C. Experiment Setup

The samples were inspected using a Hitachi Regulus 8230 scanning electron microscope (SEM) after flip chip bonding. A Keyence 3D profilometer was applied to image the nano-Cu bumps before sintering and estimate the height of sintered Cu bump after bonding. The IV characteristics were measured by a Cascade Microtech probestation.

III. Results and Discussion

A. Specimen Inspection

To inspect the nano-Cu bump after photolithography stencil printing, two nano-Cu patterns were characterized by optical profiling and microscopy (Keyence VK-X250). Fig. 3a and 3b show 2D and 3D optical images of the nano-Cu bumps after lift-off. In the 2D image. Due to the weak adhesion during the lift-off process, the sides of the nano-Cu bump was partially lost, but the edge of the nano-Cu pattern on the substrate was clear, corresponding to the open area of the photoresist mask. The surface topography of the nano-Cu bump was observed in the 3D image, showing slight unevenness due to manual stencil printing, which could be improved by using dedicated stencil printing equipment. To estimate the average height of the nano-Cu bumps, 50 profile lines at intervals of 1.5 µm on P1 and P2 were characterized and averaged, represented by the red box in Fig. 3a. The average surface topographic profiles of P1 and P2 are shown in Fig. 3(c) and 3(d), respectively. The border of the side-well and the top surface is selected as the boundary for calculating the average height of the nano-Cu bumps. The average heights of P1 and P2 are estimated to be 26.96 ± 0.96 µm and 21.80 ± 1.28 µm, respectively. It can be observed on these shape profiles that the tops of the nano-Cu bumps are slightly smaller than the bottoms due to the shrinkage of nano-Cu paste during drying (Fig. 2c).

The final sapphire to Si flip chip is shown in Fig. 4. The SEM images in Fig. 5 illustrate the bonding edge between the sapphire die and Si substrate at a 45° tilt angle. The gap between the top die and substrate was attributed to the nano-Cu bumps. The alignment inspection of the sapphire chip and Si surface is indicated in Fig. 5b, showing bare overlaying on the flip chip.

To estimate the height of the copper bumps after the bonding process, the stacked die profile was measured at various locations on the edge of the sapphire die using Keyence. It is known that the sapphire wafer is 650 µm, hence, the nano-Cu bumps can be derived from the difference between the thickness of the sapphire wafer and the measured data using Keyence. Fig.6 demonstrates the distribution of nano-Cu bump height after measurement and calculation. The mean height and standard deviation were 21.17 µm and 2.36 µm, respectively. Compared with the height information of the Cu bump before bonding (26.96 µm and 21.80 µm), the height of the Cu bump lowered to the shrinkage of the nano-

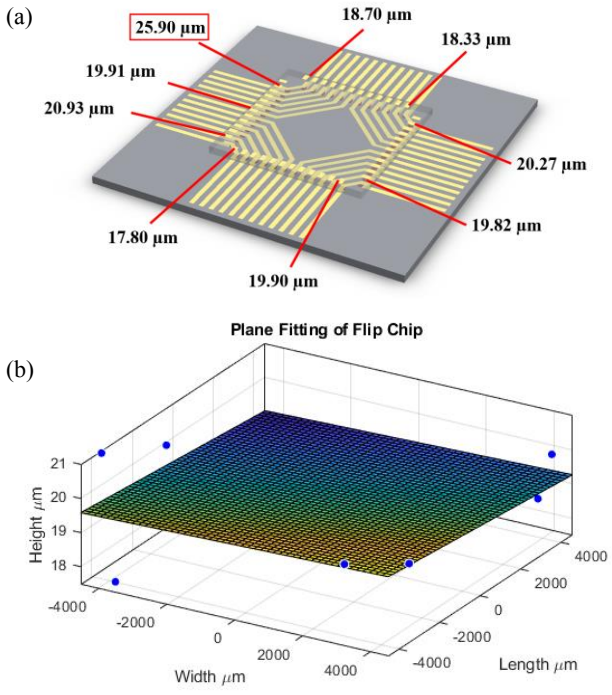

Fig. 6. (a) Schematic of Cu bumps height distribution and the red box representing an outlier and (b) Fit plane of flip chip according the height distribution.

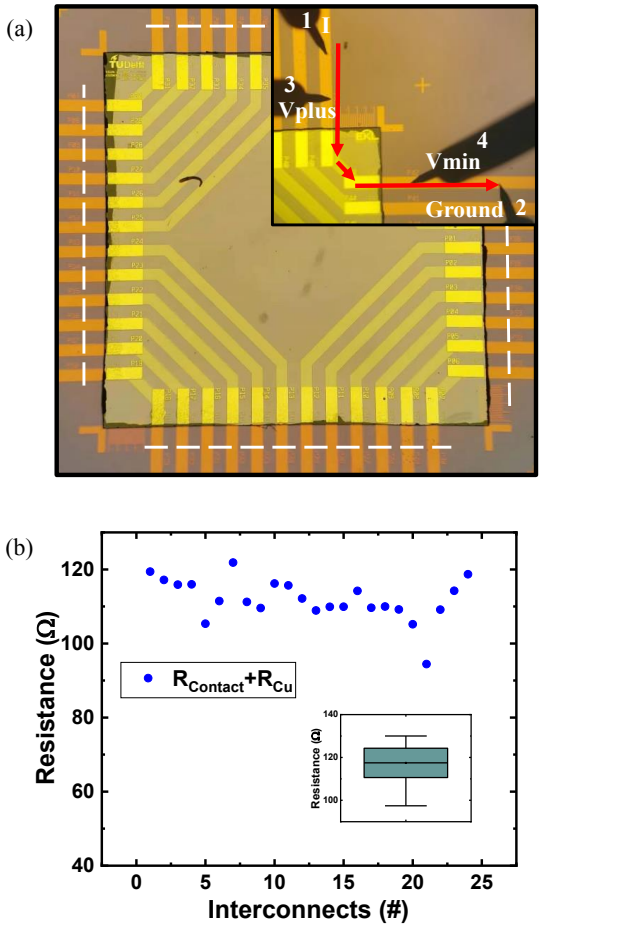

Fig. 7. (a) Sketch of a simplified four terminal configuration for electrical measurement in probestation. (b) Total resistance of 24 interconnects on the specimen obtained by (1). The mean value and standard deviation can be observed in the box chart in the inset.

Cu paste during sintering and the compression during bonding under pressure. After stencil printing and the sintering process, the height of the nano-Cu bumps was higher than that of the spin-coated photoresist (10 µm) in the first step. It was assumed that the spread amount of the nano-Cu paste was larger than the required amount, and there was excess coverage on the photoresist mask. Therefore, the actual thickness of nano-Cu bumps was not the estimated 10 µm after lift-off.

In addition, the uniformity of the bonded flip chip can also be detected according to the schematic of nano-Cu bumps height distribution, as shown in Fig. 6a. It can be observed that there is only one outlier of 25.90 µm in the upper left corner, which will be calculated exclusively. The height outlier location is assumed to be an unevenness of the sapphire die and there are no other locations with a height above 20 µm nearby. The mean height and the standard deviation are estimated to be 19.46 µm and 1.07 µm without this outlier. Compared with the two adjacent nano-Cu bumps of 26.96 µm and 21.80 µm after the lift-off process, as indicated in Fig. 3, the height difference between the two nano-Cu bumps at different positions after bonding is much smaller. The NMP material is supposed to be compressible leading to an uniform standard height after bonding. As illustrated in Fig. 6b, the plane fitting of this flip chip was simulated using the measured data, showing the sapphire plane was relatively flat after bonding, indicating that nano-Cu paste can be beneficial as a bonding material to planarize the flip chip.

B. Electrical Characterization

This specimen was designed to be interconnected by nano-Cu bumps through the top and bottom Au patterns, hence, the electrical resistivity is important for evaluating the 3D interconnects. The schematic of the electrical measurement setup is shown in Fig. 7a, indicating in the top right box, that it was a simplified four-point measurement method using four-probes to inspect the electrical contacts between the top die and bottom substrate. A forced current was applied through needle 1 and needle 2, and the voltage differences were measured by needle 3 and needle 4, the interconnection path following the red arrow. To induce the forced current, a DC voltage sweep was performed from -2 V to 2 V. The Cu interconnects resistances, consisting of contact resistance between Au patterns and nano-Cu bumps as well as the resistance of nano-Cu bumps, can be estimated in (1).

$$R_{Cu} = \frac{V_{plus}\text{-}V_{min}}{I_{Force}} - \rho_{Au}\frac{l_{line}}{A} \quad (1)$$

Where ρ_{Au} is the gold electrical resistivity, which is approximately 2.44×10^{-8} Ω•m^{-1} at room temperature, and A is the cross-sectional area of the Au line, calculated as 3×10^{-11} m^2.

The Cu interconnects resistances will be derived by subtracting the total resistance of each interconnecting Au line from the resistance measured using the four-points method. Following the white dashed line, we placed needle 3 and needle 4 in the same position on each interconnect to ensure repeatability of measurements, and then obtained V_{plus} and V_{min}, respectively. The distance between needle 3 and needle 4 that current flows through the Au line, denoted by l_{line}, can be estimated in the design layout. Fig. 7b represents the Cu interconnects resistances of each of the 24 interconnects, each consisting of two nano-Cu bumps. The interconnects yield was measured to be 24 out of 24 interconnects, and the mean and standard deviation of the 24 measured Cu interconnects resistances were 117.45 Ω and 6.84 Ω, respectively. The mean interconnects resistances of one nano-Cu bump was 58.73 Ω. The measured resistance of nano-Cu bumps is more significant than that of a bulk Cu. It can be attributed that the drying was performed in air leading to oxidation and subsequent incomplete sintering.

IV. Conclusion and Outlook

In summary, a novel method to bond sapphire to silicon was developed by applying Cu nanoparticles paste joints at low temperature. The nano-Cu paste was stencil-printed using a lithographic defined photoresist mask. The NMP enables the 3D integration of sapphire and silicon bonding. The NMP sintering process for bonding occurred at a low temperature of 280°C and low pressure of 9MPa. The Cu nanopaste had a porous structure that was compressible after bonding, enabling the uniformity of the height of the flip chip. For one 3D interconnect structure consisting of four contact resistances between nano-Cu bumps and Au lines and two nano-Cu bumps resistances, the Cu interconnects resistances were estimated to be 117.45 ± 6.84 Ω. The flip chip interconnects were repeatable, with all 24 interconnects being valid after nano-Cu patterning and specimen bonding.

To further improve the performance of the flip chip, the reduction of resistance by sintering with forming gas to provide a reducing atmosphere will be investigated. Furthermore, since drying in air causes oxidation problems, the drying process can be improved, for example, by drying in a vacuum oven. In order to study the sintering degree of Cu NMP and the reliability of bonded flip chip, the shear test of sapphire to silicon integration will be investigated. After the shear test, the deformed sheared surface can be inspected to observe the sintered Cu NMP. Furthermore, to increase the evenness of patterned nano-Cu bumps after photolithographic stencil printing, the spreading process can be improved by automated printing, and the amount of Cu nanopaste can be controlled to fill only the contact opening areas.

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