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DOI
10.1109/ISCAS58744.2024.10558071

Publication date
2024

Document Version
Final published version

Published in
ISCAS 2024 - IEEE International Symposium on Circuits and Systems

A GaN Driver with Almost Constant dv/dt during Miller Plateau for V-I Overlap Loss Reduction

Yunzhe Yang[1,2], Qiujin Chen[1], Zaitian Yang[1], Sijun Du[2], Mo Huang[1*]
[1]State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China
[2]Department of Microelectronics, Delft University of Technology, Delft, The Netherlands
*Email: mohuang@um.edu.mo

2024 IEEE International Symposium on Circuits and Systems (ISCAS) | 979-8-3503-3099-1/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISCAS58744.2024.10558071

***Abstract*—When driving a GaN switch, the maximum transition speed of drain-source voltage (peak *dv/dt*) should meet specification. But reducing the peak *dv/dt* usually exacerbates V-I overlap loss. This work presents a GaN driver for buck converter featuring: 1) voltage-controlled peak *dv/dt*; 2) almost constant *dv/dt* during Miller Plateau (MP) for reducing V-I overlap loss. We analyze why a constant *dv/dt* minimizes V-I overlap loss under a peak *dv/dt* specification, how to maintain a constant *dv/dt* during the MP period, and propose an implementable solution. We use a sensing block to judge whether the peak *dv/dt* violates the specification, and an adaptive searching scheme to find out the key parameters for the targeted constant *dv/dt*. We designed the layout with a 180-nm SOI process, and simulation results show that the peak *dv/dt* is well under control. It saves up to 33.99% V-I overlap loss when compared with the conventional constant current driver scheme.**

***Index Terms*—GaN, buck converter, *dv/dt*, Miller Plateau, V-I overlap loss, EMI**

I. Introduction

With low turn-on resistance and small parasitic capacitance, Gallium Nitride (GaN) power switches draw significant attention in high-speed DC-DC converters. Fig. 1(a) shows a buck converter with GaN switches, and Fig. 1(b) shows the turn-on transient waveforms of the high-side switch M_H. The gate current I_G from the gate driver first charges the C_{GS}, raising V_{GS} to the threshold voltage V_{TH} and turning on M_H. After that, the drain current I_D increases to its maximum value. Then, the V_{DS} drops. This V_{DS} dropping period is defined as the Miller Plateau (MP) period. We use *dv/dt* to define the absolute value of the slew rate of V_{DS} during the MP period. Clearly, the GaN switch has a V-I overlap loss when turned on. Therefore, it is favorable to increase the *dv/dt* value, reducing the V-I overlap loss during the MP period. However, a high *dv/dt* would cause electromagnetic interference (EMI) issues [1]. The peak *dv/dt* should be kept within a value (dv/dt_{MAX}) for certain applications [2]. Consequently, it is pivotal to reduce the V-I overlap loss without violating the dv/dt_{MAX}.

The *dv/dt* is mainly determined by the charging and discharging speed of C_{GD} [3]. Previous works [3], [4], [5] and [6] proposed gate drive schemes to control the *dv/dt*. Take the charging phase as an example. One method in [3] is to reduce the gate current I_G to extend the MP period, thus suppressing *dv/dt*, shown as "Reduced I_G" in Fig. 1(c). Clearly, it increases the V-I overlap loss. Works from [4], [5] and [6] used large

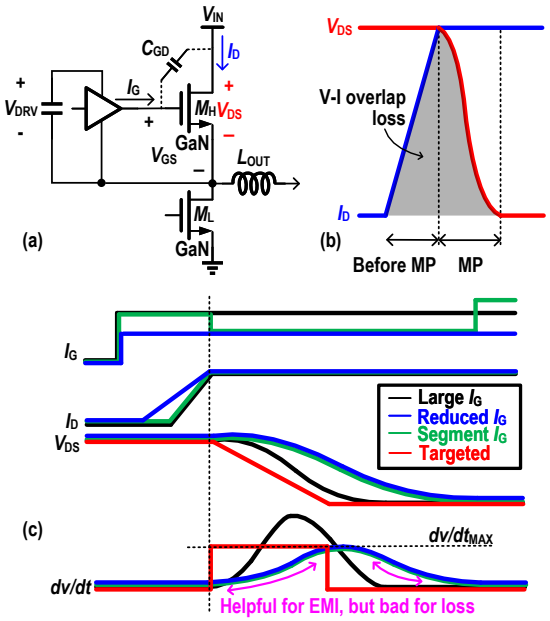

Fig. 1. (a) Diagram of a buck converter with GaN switches; (b) its V-I overlap loss; (c) waveform in different cases: Large I_G; Reduced I_G [3]; Segment I_G [4] [5] [6]; and Target waveform.

I_G before MP, and reduced I_G during MP, known as "Segment I_G" in Fig. 1(c). However, their V-I overlap loss becomes larger than the "Large I_G" in a conventional design due to the extension of V-I overlap time. And their peak *dv/dt* value cannot be adjustable. [7] proposed a GaN driver with Gaussian V_{DS} waveform in MP for an optimum EMI performance. Still, it is not helpful to the V-I overlap loss.

We notice that the *dv/dt* with a constant I_G during the MP period from previous works does not hold a constant value. Its peak value usually occurs in the middle of the MP period, as shown in Fig. 1(c). Previous works aimed at reducing the peak *dv/dt*, yet making the *dv/dt* at the begin and end of the MP period even smaller. This is not helpful for a smaller peak *dv/dt*, but inevitably exacerbates the V-I overlap loss.

In this paper, our targeted scheme keeps *dv/dt* close to the dv/dt_{MAX} during the MP period ("Targeted" in Fig. 1(c)), minimizing the V-I overlap loss without violating the EMI requirements. We organize the paper as follows. Section II analyses how to reduce V-I overlap loss in MP under a *dv/dt* specification. Section III presents the implementation. Section

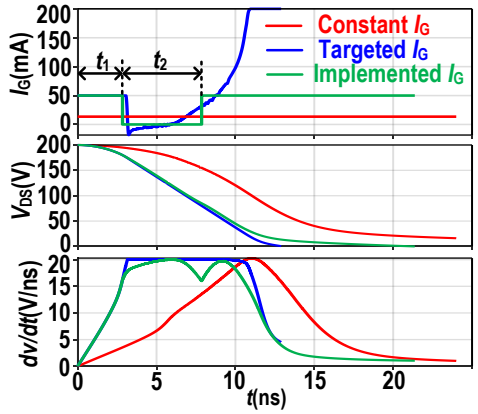

Fig. 2. Caculated V_{DS} and *dv/dt* with difference I_G curves, from a Matlab model.

IV gives the simulation results, and Section V draws the conclusion.

II. V-I Overlap Loss Reduction under dv/dt_{MAX}

A constant $dv/dt = dv/dt_{MAX}$ on Fig. 1(c) should minimize the V-I overlap loss. Obviously, such constant *dv/dt* should be achieved with a specific I_G curve during the MP period.

To find out which I_G shape generates the targeted *dv/dt*, we analyze the relationship between I_G and *dv/dt* in the MP period, based on a buck converter as shown in Fig. 1(a). During the turn-on period of the high side switch M_H, we have [8]:

$$dv/dt = \frac{g_{FS}(V_{GS} - V_{MP})}{C_{OSS\_HS} + C_{OSS\_LS}}, \quad (1)$$

$$\frac{dV_{GS}}{dt} = \frac{I_G}{C_{ISS\_HS}} - \frac{g_{FS}C_{RSS\_HS}(V_{GS} - V_{MP})}{C_{ISS\_HS}(C_{OSS\_HS} + C_{OSS\_LS})}, \quad (2)$$

where g_{FS}, C_{OSS_HS}, C_{ISS_HS} and C_{RSS_HS} are the transconductance, output capacitance, input capacitance and reverse transfer capacitance of M_H, respectively. C_{OSS_LS} is the output capacitance of M_L. V_{GS} and V_{MP} are gate-source voltage and MP voltage of M_H.

To calculate the transient waveforms during the MP period, we build a mathematical model on MATLAB based on the partial differential equations (1) and (2). Fig. 2 shows the calculation results of I_G, V_{DS} and *dv/dt*. "Target I_G" is calculated from making *dv/dt* (eq. (1)) = dv/dt_{MAX}. We include a constant I_G case for comparison, which shares the same peak *dv/dt* as the target one. Simulation results show that the targeted I_G reduces V-I overlap loss during the MP period by 46.9%.

However, such a complex shape of "targeted I_G" is difficult to implement. We propose to use a pulse I_G instead of the target one, shown as a "Implemented I_G" in Fig. 2. t_1 and t_2 are two important parameters of the implemented I_G: t_1 represents the period of the high I_G, starting from the MP period, while t_2 is the period of I_G = 0 afterward. The *dv/dt* from the implemented I_G is almost constant during the MP period, as expected. The V-I overlap loss from the implemented I_G is only 7.4% larger than the targeted one.

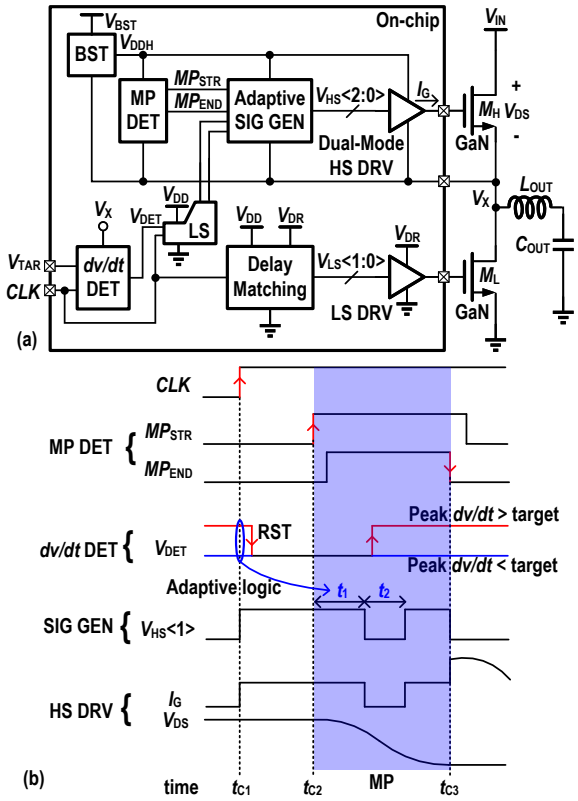

Fig. 3. (a) Architecture of the buck converter system, and (b) key transient waveforms.

III. Implementations

A. Architecture

Fig. 3(a) shows the block diagram of the buck converter consisting of the proposed gate drive chip, two off-chip GaN switches M_H and M_L and other off-chip components. We use the bootstrap (BST) block to generate V_{DDH} as the power supply in the floating voltage domain, and the level shifters (LS) to convert signals from the low-voltage to the floating-voltage domain. Fig. 3(b) gives the key waveforms. The rising edge of the clock signal *CLK* comes at t_{C1}, where I_G rises from 0 to the implemented value as shown in Fig. 2. The MP detector (MP DET) senses the begin and end time of the MP period, represented by the rising edge of MP_{STR} and falling edge of MP_{END}, at t_{C2} and t_{C3}, respectively. The peak *dv/dt* detector (*dv/dt* DET) compares the peak *dv/dt* with the dv/dt_{MAX} (proportional to a voltage V_{MAX}) within the MP period (between t_{C2} and t_{C3}), and outputs V_{DET}. V_{DET} = "0" means the peak $dv/dt < dv/dt_{MAX}$, whereas V_{DET} = "1" means it is $> dv/dt_{MAX}$. The adaptive signal generator (Adaptive SIG GEN) uses V_{DET} at t_{C1} (representing whether the peak $dv/dt < dv/dt_{MAX}$ in the last switching cycle) to generate V_{HS}<1> featuring t_1 and t_2, as explained later in Section III-C. Then, the V_{DET} signal is reset. A dual-mode high-side driver (HS DRV) generates the targeted I_G shape according to V_{HS}<1>.

B. Peak dv/dt Detector and MP Detector

Fig. 4(a) shows the peak *dv/dt* detector block, where the switching node V_X is sensed by an RC low-pass filter (R_{DET}

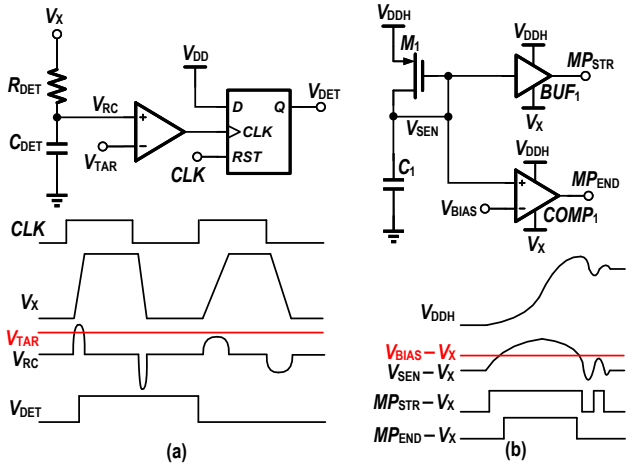

Fig. 4. Schematic and working waveforms of (a) peak *dv/dt* detector, and (b) MP detector.

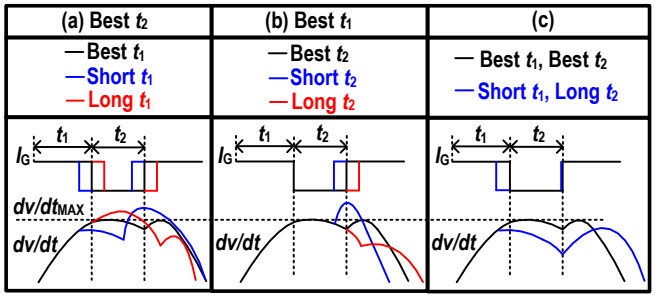

Fig. 5. Waveform of $I_{\rm G}$ and *dv/dt* with (a) short/long t_1 and best t_2, (b) best t_1 and short/long t_2, and (c) short t_1 and long t_2.

and $C_{\rm DET}$). The output voltage $V_{\rm RC}$ of the RC filter is

$$V_{\rm RC} = R_{\rm DET}C_{\rm DET}dv/dt. \tag{3}$$

Therefore, $V_{\rm RC}$ is proportional to *dv/dt*. After that, we use a high-bandwidth comparator to determine whether the instantaneous $V_{\rm RC}$ is larger than $V_{\rm MAX}$, which represents whether the *dv/dt* is larger than $dv/dt_{\rm MAX}$. The result of the comparator output is latched by the cascading DFF. We reset the DFF at the beginning of every switching period (after $t_{\rm C1}$).

Fig. 4(b) shows the schematic and working waveforms of the MP detector block [5]. The RC low-pass filter consisting of M_1 and C_1 makes $V_{\rm SEN}$ rise with *dv/dt*. The rising of $V_{\rm SEN}$ flips the low-$V_{\rm TH}$ buffer BUF_1 output $MP_{\rm STR}$. Subsequently, once $V_{\rm SEN}$ drops below $V_{\rm BIAS}$, the comparator $COMP_1$ output $MP_{\rm END}$ drops. Thus, the rising edge of $MP_{\rm STR}$ and the falling edge of $MP_{\rm END}$ represent the begin and end time of MP, respectively.

C. Adaptive Signal Generator

To control $V_{\rm HS}<1>$, we should determine the values of the key parameters t_1 and t_2, to which the resultant *dv/dt* is highly sensitive. We define the "best" t_1 and t_2 to have the smallest V-I overlap without violating the $dv/dt_{\rm MAX}$. As shown in Fig. 5(a), if t_1 deviates from the best value, the peak *dv/dt* exceeds $dv/dt_{\rm MAX}$. With respect to the t_2 inaccuracy, as shown in Fig. 5(b), if t_2 is shorter, the peak *dv/dt* exceeds the $dv/dt_{\rm MAX}$. If it is longer, a higher V-I overlap loss occurs. Another case not violating the $dv/dt_{\rm MAX}$ is short t_1 and long t_2 (Fig. 5(c)). This leads to a higher V-I overlap loss as well.

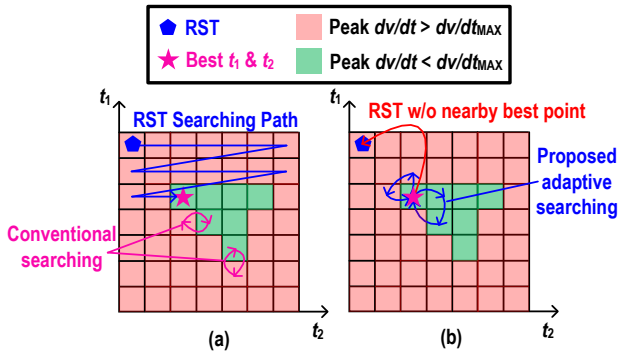

Fig. 6. Searching algorithm (a) at reset, and (b) after reset.

From Fig. 5, we conclude that there are three cases suppressing the peak *dv/dt* within $dv/dt_{\rm MAX}$: 1) best t_1 and t_2, 2) best t_1 and long t_2, and 3) short t_1 and long t_2. Then, Fig. 6(a) summarizes the peak *dv/dt* value under the t_1 and t_2 coordinate: the green lattices represent that it is smaller than $dv/dt_{\rm MAX}$, while the red ones indicate that it is larger. However, as analyzed in Fig.5, only the top left lattice in green achieves the lowest V-I overlap loss.

Note that our implemented MP detector only gives bipolar result whether $dv/dt > dv/dt_{\rm MAX}$ or not. Using conventional searching schemes may find the non-optimum lattice, as shown in Fig. 6(a). Consequently, we propose a new searching algorithm to ensure finding out the top left lattice in green. We reset the t_1 and t_2 initial values at the top left corner as shown in Fig. 6(a), a.k.a. longest t_1 and shortest t_2. Subsequently, we use a 2-D searching algorithm, searching t_2 first and then t_1, with a minimum 250-ps time resolution. In this sequence, the first green lattice found should be the best point. The algorithm at reset may take a long time.

After finding the best t_1 and t_2, we use another searching algorithm as presented in Fig. 6(b), monitoring the *dv/dt* continuously. The algorithm only searches the adjacent t_1 and t_2 values, shortening the searching time greatly. If the algorithm does not converge after the adjacent searching, we reset t_1 and t_2 and perform the reset searching as in Fig. 6(a) again.

D. Dual-Mode High-Side Driver

Fig. 7(a) gives the schematic of the dual-mode high-side driver, and Fig. 7(b) shows its working waveforms. It has two pull-up drivers: a current driver and a voltage driver. The current driver, controlled by the $V_{\rm HS}<1>$, is activated before and during the MP period. It works as a switched current source for the targeted $I_{\rm G}$. However, after the MP period, the $I_{\rm G}$ should be much larger to quickly pull up the $V_{\rm GS}$ and save the loss. Consequently, we use the voltage driver controlled by the $V_{\rm HS}<2>$. The pull-down driver controlled by the $V_{\rm HS}<0>$ discharges $V_{\rm GS}$ every period.

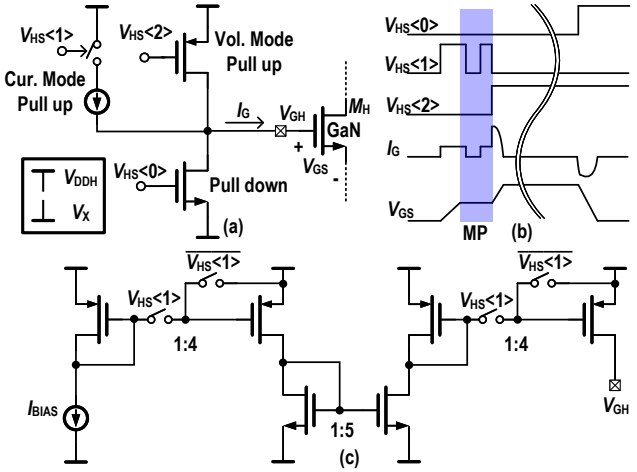

Fig. 7. (a) Schematic of high-side driver, (b) working waveforms of high-side driver, and (c) schematic of pull-up current driver.

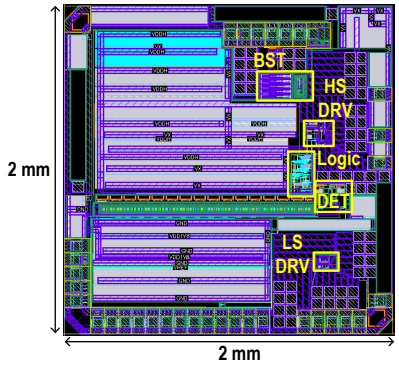

Fig. 8. Layout of the proposed GaN driver.

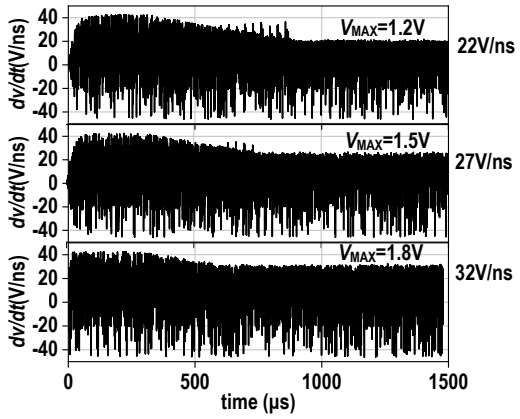

Fig. 9. Simulated transient results of *dv/dt* under three different V_{MAX}s.

Fig. 7(c) shows the schematic of the current driver. We use an on-chip bandgap reference to generate bias current I_{BIAS}, and amplitude it with 3-stage current mirrors. And four switches are inserted to control the output current.

IV. Simulation Results

The proposed driver IC was designed with a 0.18-μm silicon-on-insulator SOI process. It integrates the building blocks in Fig. 3(a). Fig. 8 shows its top layout, taking an active area of 2.7mm^2.

We simulate the DC-DC converter with 200-V input and 26-V output voltages, at 13-A load current and 1-MHz switching frequency. GaN switches are EPC2207 [9]. Fig. 9 shows the simulated transient waveforms under three different V_{MAX}. The original peak *dv/dt* is around 42V/ns. When V_{MAX} is 1.2V, 1.5V and 1.8V, the peak *dv/dt* in the steady state is reduced to 22V/ns, 27V/ns and 32V/ns, respectively. The algorithm converges within 1ms for the three cases. This verifies the proposed scheme.

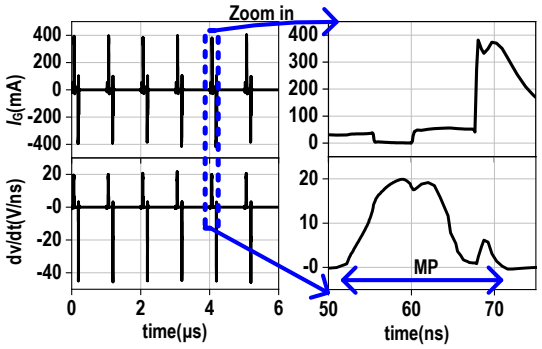

Fig. 10. Simulated transient waveforms in the steady state, where the *dv/dt* is almost constant during the MP period.

TABLE I
V-I Overlap Loss Saving Percentage in Different *dv/dt*s

Peak *dv/dt* (V/ns)	22	27	32
Loss in this work (μJ/cycle)	20.70	19.77	18.27
Loss in constant I_G (μJ/cycle)	31.36	26.12	22.21
Loss Saved (%)	33.99	24.31	17.74

Fig. 10 gives the zoomed-in transient waveforms in the steady state when V_{MAX} is 1.2V. As seen, the I_G curve almost fits to that in Fig. 2. The resultant *dv/dt* is almost constant during the MP period, as expected. Table I shows under different peak *dv/dt*s, the simulated V-I overlap loss with proposed driver, with constant I_G driver, and the saving percentage. The proposed driver saves 17.74% – 33.99% V-I overlap loss.

V. Conclusion

Reducing peak *dv/dt* for reduced EMI demands a better optimization of the V-I overlap loss. The key of saving the loss is to implement a specific I_G that keeps an almost constant $dv/dt = dv/dt_{MAX}$ during the MP period. We implement the proposed scheme, verified by the simulation results.

Acknowledgment

This work was supported in part by the Natural Science Foundation of China under Grant 61974046, in part by the Science and Technology Development Fund, Macau, SAR, under Grant 0041/2022/A1, and Grant SKL-AMSV(UM)-2023-2025; in part by the Research Plan of Shenzhen, Hong Kong, and Macau under Grant SGDX20210823103805040; and in part by the Research Committee of University of Macau under Grant MYRG2022-00004-IME.

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