ZVS Turn-on integrated Triangular Current Mode Three-phase AC-DC PFC for EV On-board Chargers

Jian Sun

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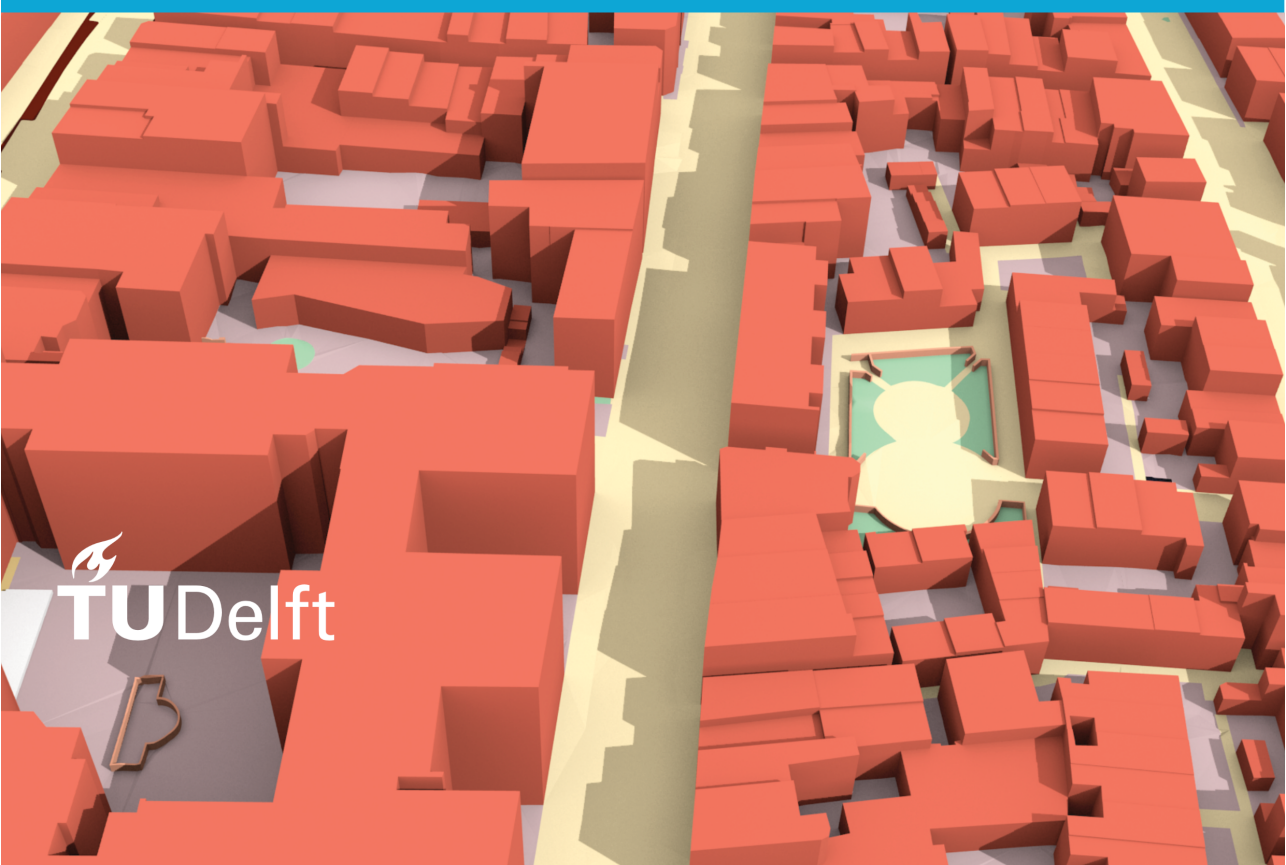

ZVS Turn-on integrated Triangular Current Mode Three-phase AC-DC PFC for EV On-board Chargers

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ABSTRACT

An efficient, compact, and lightweight three-phase AC-DC power factor correction (PFC) converter becomes a necessity for the On-board chargers (OBCs) of the electric vehicle (EV) in conventional grid-to-vehicle (G2V) and vehicle-to-grid (V2G) charging scenarios. The commercially available OBCs have very limited power density despite the moderate efficiency under specific power levels.

In this dissertation, the integrated triangular current mode (iTCM) control is implemented to improve the power density (kW/L) and specific power (kW/kg) of the three-phase PFC converter (the front stage of OBCs) while maintaining high efficiency. Zero voltage switching (ZVS) turn-on is realized in the iTCM control with a higher switching frequency to reduce the LCL filter size without sacrificing the efficiency.

By adding an LC branch between the bridge leg and the mid-point of the DC link, the high-frequency and low-frequency current is split to minimize the inductor loss and to achieve a better inductor design. Analytical modeling and simulation in PLECS are firstly conducted to verify the idea of iTCM. Besides, the capacitor-current feedback active damping method is implemented to prevent instability from the LC and LCL filters. Finally, the designed 11 kW three-phase AC-DC PFC converter, including the input LCL filter, achieves an efficiency of 98.61%, a power density of 6.5 kW/L and a specific power per weight of 0.72 kW/kg.

The proposed three-phase iTCM control is validated in a 3 kW SiC MOSFET-based AC-DC converter. The current and voltage waveform of iTCM, TCM and CCM is verified in the hardware platform with (DSP)-TMS320F28379D. The efficiency of the iTCM control achieves 96.38%, which improves by around 1% compared to CCM at the same power density level.

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1

INTRODUCTION

1

1.1. BACKGROUND

In 2021, the global sale of Electric Vehicles (EVs) reached 6.75 million compared to 3.24 million in 2020, as shown in Figure 1.1. It has a remarkable annual growth rate of 108%, the highest growth since 2012, though the world is still not out of the COVID-19 pandemic. The global EV market share increased from 4.2% to 8.3% in 2021, which almost doubled. In Europe, the EV share increased from 10% to 17%, while in China, the share increased from 5.5% to 13.3% [1] [2].

There are multiple reasons why people switch to EVs featuring higher efficiency, zero green gas emission, etc. One of the biggest reasons is the government's preferential policies including the purchase subsidy. What's more, in Shanghai, EVs can get the license plate directly without spending much time and money on the lottery, compared to gasoline cars.

However, many car buyers are still concerned about the short lifetime of the battery, the limited driving range and the long charging time. With the rapid development of battery technology, charging technology, especially power electronics and the building of charging stations, these problems are gradually mitigated.

The conductive charging is the most commonly used charging method among the current charging technology. One of the conductive charging methods is DC charging, which is also called fast charging. It has a very high power level and can charge an EV battery in a short time. For example, Tesla Model 3 has a peak charging power of 150 kW, and it only takes 13 minutes to charge the battery to fulfill a 200 km driving range [3]. However, DC fast charging needs a sizable converter and would cause a significant fluctuation to the grid, so it can only be implemented in fast-charging stations with a strong grid.

The other method of conductive charging, which is the most commonly used, is AC charging. The charging place of AC charging can take place at your home or workplace with a one-phase or three-phase home grid. The AC charging has more availability since the on-board charger is installed inside the EV. Moreover, AC charging is a key to the future Vehicle-to-Grid (V2G) charging. V2G is defined as using EV batteries to feed electricity to or store electricity from the grid. In the future, when more and more electricity is produced by renewable energy, such as wind energy or solar energy, V2G charging becomes a feasible solution to shape the power peak or regulate frequency. [4].

Bidirectional on-board chargers (OBCs) always take an essential role in daily home charging as well as future V2G charging. In today's automotive industry, the maximum power rating of OBCs reaches 40 kW, but in most commercial EVs, the power rating is around 7 kW for single-phase and 11 kW for three-phase [5].

OBCs have two main configurations, as shown in Figure 1.2. The two-stage configuration consists of a bidirectional AC-DC power factor correction (PFC) converter and a DC-DC converter with the electrical isolation. The PFC converter can be used to regulate the DC bus voltage while shaping the grid currents for a good power quality and harmonics performance, while the DC-DC part can provide a wide range of DC output voltage for fitting different batteries or different loads. The two-stage OBCs are used by most commercial manufacturers, as shown in Figure 1.3 [5].

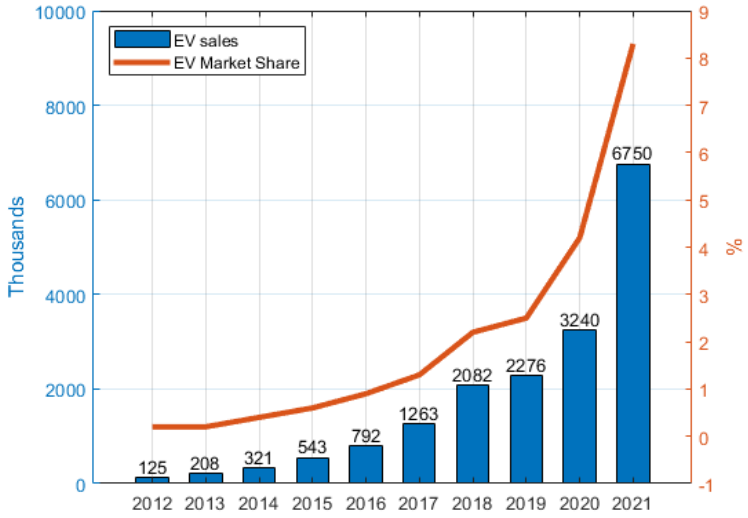


Figure 1.1: Global Electric Vehicle sales and market Share from 2012 to 2021 including plug-in hybrid EVs and battery EVs

1.2. PROBLEM DEFINITION

As the front-end stage of power conversion, the PFC converter plays a vital role in OBCs. It provides a controllable DC voltage for the back-end stage DC-DC converter, regulates the current to meet the IEEE harmonics standards when connected to the grid and provides a high power factor (>0.99). Thus, the three-phase PFC converter with high efficiency is a necessity for daily charging, especially for future V2G charging. Since it is on board, the weight and volume of OBCs must be taken into consideration, besides their efficiency.

Take the three-phase full-bridge PFC converter as an example; it normally operates at continuous current mode (CCM) at a low switching frequency (around 10 kHz). This leads to a relatively low and thus a higher efficiency. Nowadays, the highest efficiency of PFC converters can reach 99% in some applications without considering the inductor loss [5]. However, CCM with a low switching frequency needs a larger LCL filter to meet the current harmonics requirement for the grid-connected topology [6]. The volume and weight of the LCL filter always take up the largest part of the converter, sometimes even more than 80% [6]. Thus, PFC operating at CCM with low switching frequency often has a low power density (kW/L) and specific power (kW/kg). For example, one OBC from Eaton only has a power density of 2 kW/L. In commercial applications, all manufacturers are making an effort to increase the power density of OBCs. In US, OBCs power density target for year 2025 is 4.6 kW/L [5].

To improve the power density and specific power of the PFC converter, the switching frequency must be increased to get a smaller LCL input filter. However, improving switching frequency means increasing the turn-on and turn-off switching loss of semi-

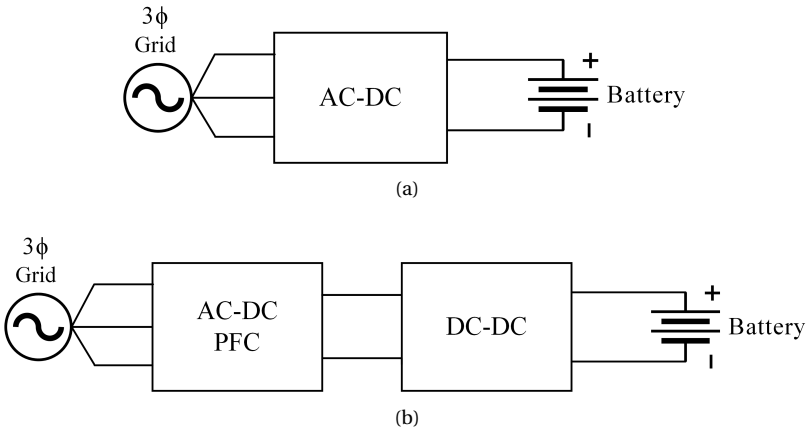


Figure 1.2: Two configurations of EV OBCs (a) Single-stage configuration. (b) Two-stage configuration.

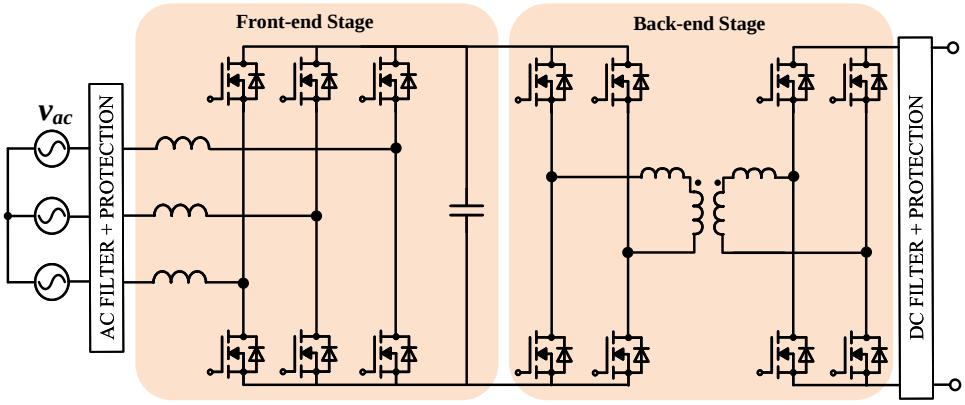


Figure 1.3: Example of a two-stage high power OBC configuration suitable to G2V and V2G charging

conductors, which will reduce the total efficiency. Therefore, it becomes a trade-off between efficiency and power density or specific power when designing the PFC converter for OBCs.

To achieve a high efficiency, power losses of semiconductors should be minimized. Considering the semiconductor loss, turn-on switching loss takes more than 70% of the total loss[6]. In contrast, the turn-off switching and conduction loss only take up a small part, especially for wide-band-gap semiconductors like SiC MOSFET [6]. Furthermore, the turn-off loss is negligible compared to the turn on loss for the next generation WBG device. Thus, soft turn-on switching is necessary to minimize the power losses and improve the efficiency.

1.3. RESEARCH OBJECTIVE

The three-phase AC-DC PFC converter for OBCs is desired to be efficient, compact and lightweight. However, the high-efficient converter normally operates at CCM with a low switching frequency, where a large and heavy input filter is needed. Besides, increasing the switching frequency can reduce the size of the input filter but would cause significantly higher loss. Thus, improving the power density and the specific power while maintaining high efficiency is an essential and challenging topic.

This thesis aims to design a three-phase AC-DC PFC converter as the front-end for OBCs and develop a soft turn-on method to make it more efficient, compact and lightweight. The specific requirements of the PFC converter are:

1. Ensure high efficiency
2. Ensure high power density
3. Ensure high specific power

1.4. RESEARCH PLAN

Depending on the research objective, the research plan for this thesis topic is:

1. Perform a literature review of three-phase bidirectional PFC and choose a suitable topology
2. Perform a literature review of soft switching method and do the simulation via PLECS
3. Compare different soft switching methods by efficiency, power density and specific power
4. Develop a suitable soft switching method for OBCs PFC and conduct the experiment validation

1.5. THESIS OUTLINE

The thesis mainly consists of a literature review, mathematical modelling, simulation and experiment validation, which are divided into six chapters.

Chapter 1: Introduction

This chapter pointed out the motivation and requirements of this thesis, and it clearly shows the importance of the high-efficient PFC converter for OBCs on EV charging. This thesis aims to design a three-phase PFC with high efficiency, power density and specific power.

Chapter 2: Literature review

A literature review of the three-phase bidirectional AC-DC PFC converter as well as the zero-voltage-switching method that can be applied to the PFC converter is presented in chapter 2. By considering the pros and cons, the topology and soft switching method is determined for this dissertation.

Chapter 3: integrated Triangular Current Mode of three-Phase AC-DC PFC

Chapter 3 presents the basic concept of the three-phase grid-connected AC-DC PFC converter with iTCM control for OBCs. The single-phase iTCM control is discussed first. Then, the three-phase iTCM control is proposed and modeled in detail. Improved Bounded-iTCM control and Sinusoidal-iTCM control are also introduced to limit the switching frequency and to prevent EMI and practical issues. Finally, the close-loop control with capacitor-current feedback active damping method for the iTCM control is implemented.

Chapter 4: System Loss Modelling

This chapter modeled the semiconductor losses and inductor losses of the three-phase iTCM control. The SiC MOSFETs (C3M0120090J) are used in the modeling. Since ZVS turn-on is achieved in iTCM; only conduction loss and turn-off loss are considered. A specific procedure of inductor loss calculation is also illustrated in this chapter.

Chapter 5: Magnetic Design

The most significant improvement of the iTCM control is a better inductor design compared to the TCM control. The inductor design optimization procedure is introduced in this chapter. Different core dimensions with multiple materials are swept to seek the optimal design point. Powder iron core, ferrite core, litz wire and solid wire are discussed in this chapter. Finally, CCM, TCM and iTCM modeling results are compared and analyzed.

Chapter 6: Simulation and Experiment validation

In chapter 6, the simulation is conducted via PLECS to verify the idea of the three-phase iTCM control. Moreover, the iTCM idea is also realized and verified on the hardware platform with the DSP TMS320F28379D. Due to the practical restrictions, a 3kW converter prototype is used for the experimental validation, and the magnetic core is chosen as ferrite core from TDK instead of powder iron core from Magnetics. The experiment results of the iTCM, TCM and CCM control are summarized and compared.

Chapter 7: Conclusion and future work

In the final chapter, the conclusion and summary of each chapter are given. The future work and extension are also discussed based on the accomplished job and judgment.

2

LITERATURE REVIEW

2.1. THREE-PHASE BIDIRECTIONAL PFC CONVERTERS

The two-stage OBCs are the most popular topology in the automotive industry. The front-end stage is a grid-connected AC-DC PFC converter connected to the power grid via an AC input filter. The single-phase bidirectional PFC topologies such as two-phase boost interleaved totem pole PFC or three-phase boost interleaved totem pole PFC are not discussed in this dissertation [7] [8] [9]. The three-phase PFC converters, full-bridge, T type and NPC, are preferred for V2G operation.

2.1.1. THREE-PHASE FULL-BRIDGE PFC CONVERTER

The three-phase full-bridge PFC converter is the most popular choice for OBCs due to its simplicity, as shown in Figure 2.1(a). The body diodes of the MOSFETs ensure the possibility of bidirectional current. This topology is suitable for V2G operation and Vehicle-to-load (V2L) operation (bypassing one of the phases). BYD has developed this topology for their commercial applications with SiC MOSFETs, achieving 98.3% efficiency at an 11kW power level. The switching frequency range is 60-140kHz, and the output DC voltage is 700V [5].

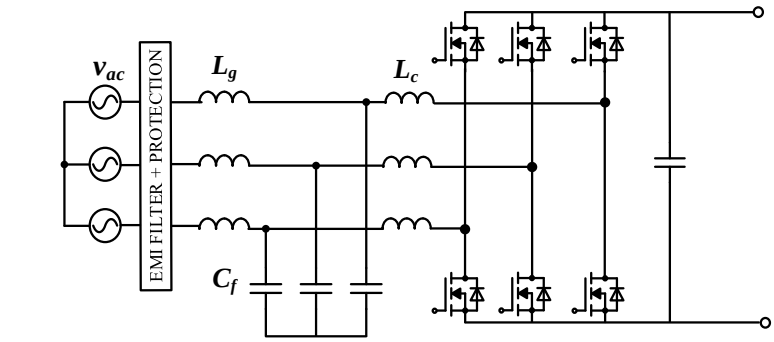
2.1.2. THREE-PHASE T-TYPE PFC CONVERTER

The three-phase T-type PFC converter is also a feasible topology for bidirectional applications, as shown in Figure 2.1(b). Compared to the three-phase two-level topology, the T-type PFC converter has the advantage of lower conduction and switching losses. Moreover, the semiconductor components operate at lower voltage stress, which means lower voltage rating and cheaper MOSFETs or IGBT can be used. One typical application of this topology using Si IGBT achieving 99% efficiency at a 10kW power level is reported in [10]. However, six additional switches are needed in this topology, and the control becomes more complicated.

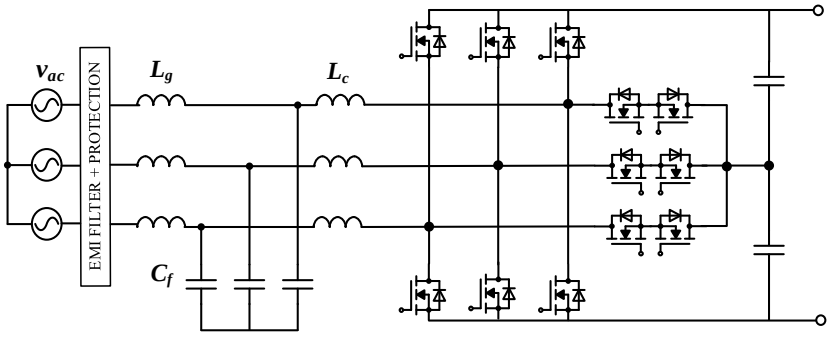
In general, the current commercial applications of the bidirectional PFC converters can achieve an efficiency of 98%, sometimes up to 99%. The WBG semiconductors are widely used in these applications. The modulation method of the totem pole topology is either Continuous Current Mode (CCM) or Critical Conduction Mode (CRM). However, for the three-phase full-bridge developed by BYD and T-type PFC converter in [10], the modulation method is not mentioned.

2.2. ZVS TURN-ON METHOD

As discussed in Chapter 1, increasing switching frequency is a typical way for the PFC converters to reduce the input filter size and thus improve the power density and specific power. However, the switching loss will be extraordinarily increased, where the turn-on switching loss takes up the most prominent part. Thus, the soft-switching turn-on method is necessary for the PFC converters to improve the power density and specific power while maintaining high efficiency. The state-of-art control methods like the critical conduction mode (CRM) control and the triangular current mode (TCM) control are good alternatives to achieve soft switching by zero-voltage-switching (ZVS) turn-on.



(a)



(b)

Figure 2.1: The most commonly used bidirectional PFC converters; (a) Three-phase full-bridge topology; (b) Three-phase T-type topology.

2.2.1. CRITICAL CONDUCTION MODE CONTROL

The critical conduction mode (CRM) control is a common method to achieve soft turn-on switching for the AC-DC PFC converters [6]. Compared to normal CCM control, the AC side current i_{ac} drops to zero and then increases to a certain value during each switching period, as the blue line shows in Figure 2.2 (b). The average value of the AC current is i_{avg}, as the red line presents in Figure 2.2 (b), which depends on the input power.

Taking one phase of the PFC converter as an example, the schematic is shown in Figure 2.2, where L_{c} is the boost inductor on the AC side, v_{ac} is the AC side voltage, and V_{dc} is the DC link voltage. The parasitic capacitor of the upper switch S_{11} and the lower switch S_{11} is denoted as C_{S1} and C_{S2}, respectively.

The current and voltage waveform of the CRM control in one switching period is il-

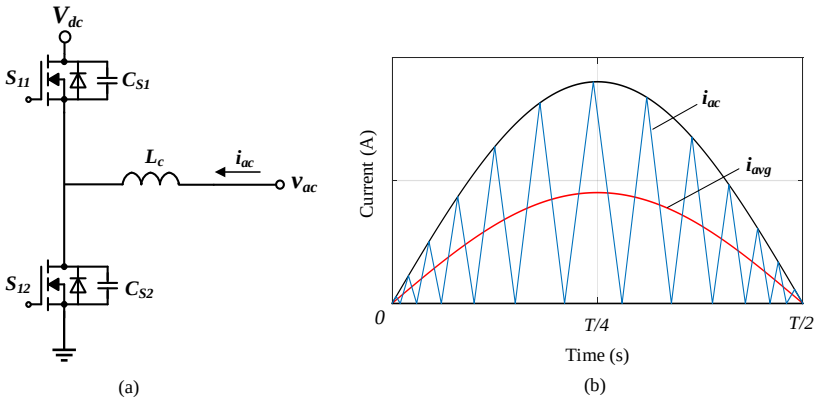


Figure 2.2: (a) One phase leg schematic of the bidirectional AC-DC PFC converters for the CRM control illustration. (b) Triangular current waveform of the CRM control in the positive period (Only take few switching period as illustration)

lustrated in Figure 2.3. Since the switching frequency is normally at several kilo-Hertz, which is larger than the main frequency (50 Hz), it is assumed that the input AC voltage $v$ac is constant in each switching period. The operation can be divided into four intervals.

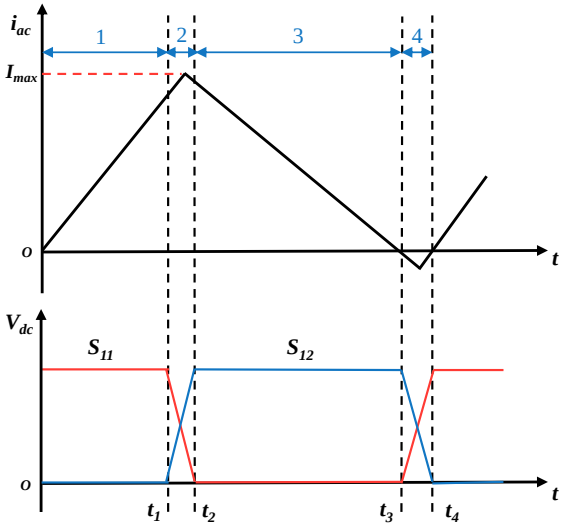


Figure 2.3: The input current waveform and the voltage waveform of semiconductors in the CRM control in one switching period

1. Interval 1 (0 - t_1): The lower switch S_{12} is on. The input voltage v_{ac} is applied on the boost inductor L_c. The input current increases linearly from 0 to a certain value. S_{12} is turned off at the end of interval 1.

2. Interval 2 (t_1 - t_2): Since S_{12} has been turned off, the resonant occurs between the two parasitic capacitors C_{s1}, C_{s2} and the boost inductor L_c. The current i_{ac} increases to I_{max} until the voltage of C_{s2} reaches v_{ac}, then it drops. During the resonance, C_{s2} is charged to V_{dc}, while C_{s1} is discharged to 0 so that the anti-parallel diode of S_{11} conducts. At t_2, S_{11} is turned on at zero voltage, which means soft turn-on switching is achieved. This resonance occurs extremely faster, which means the interval 2 shown in Figure 2.3 should be much shorter.

3. Interval 3 (t_2 - t_3): After S_{11} is turned on, the voltage applied on the boost inductor becomes $V_{dc} - v_{ac}$. Then, the current i_{ac} decreases linearly. S_{11} is turned off when i_{ac} drops to zero.

4. Interval 4 (t_3 - t_4): The same resonance occurs again after turning off S_{11}. C_{s1} is charged while C_{s2} is discharged. However, when $v_{ac} > V_{dc}/2$, the minimum voltage of C_{s2} during resonance is $2v_{ac} - V_{dc}$. ZVS is not achieved when turning on S_{12}. The voltage of C_{s2} can only be discharged to zero when $v_{ac} < V_{dc}/2$. Only in this condition can ZVS turn-on of S_{12} be achieved.

2.2.2. TRIANGULAR CURRENT MODE CONTROL

Due to the ZVS limitation of the CRM control, the triangular current mode (TCM) control has been proposed in many papers and is considered as the state-of-art method to achieve soft turn-on switching [11] [12].

Taking one phase leg of the PFC converter as an example, the schematic and the current waveform are shown in Figure 2.4. The only difference is that the input current i_{ac} will reverse in every switching cycle to a certain value, denoted as I_{zvs} in Figure 2.4 (b). This reversal current I_{zvs} makes the voltage of the parasitic capacitor drop to zero. It ensures that the anti-parallel diode conducts before turning on the switch so that ZVS is fully achieved in the whole period.

The current and voltage waveform of the TCM control in one switching cycle is illustrated in Figure 2.5. It is also assumed that the input AC voltage v_{ac} is constant in each switching cycle. The operation can be divided into four intervals.

1. Interval 1 - 2 (0 - t_2): The same as the CRM control.

2. Interval 3 (t_2 - t_3): After S_{11} is turned on, the current i_{ac} decreases linearly reaches a certain value I_{zvs} at the opposite direction. S_{11} is turned off at t_3.

3. Interval 4 (t_3 - t_4): The resonance occurs between the two parasitic capacitors C_{s1}, $C_{s2}$and the boost inductor L_c after turning off S_{11}. Because of the reversal current I_{zvs}, C_{s2} is discharged to zero so that the anti-parallel diode of S_{12} conducts before turning on S_{12}. ZVS turn-on is completely achieved.

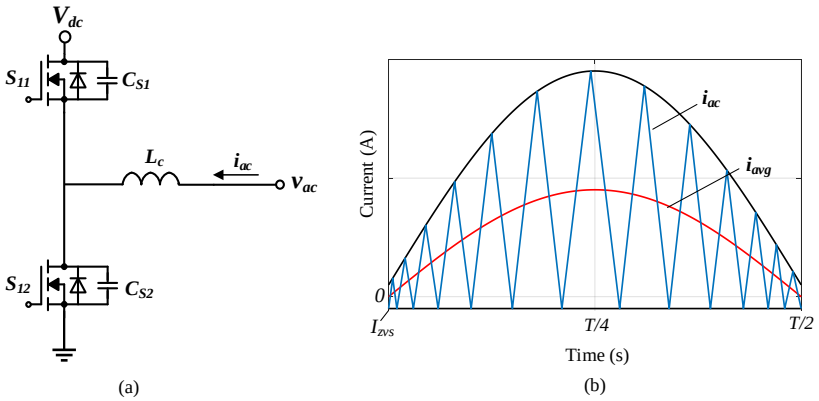


Figure 2.4: (a) One phase leg schematic of the bidirectional AC-DC PFC converters for the TCM control illustration. (b) Triangular current waveform of the TCM control in the positive period (Only take few switching period as illustration)

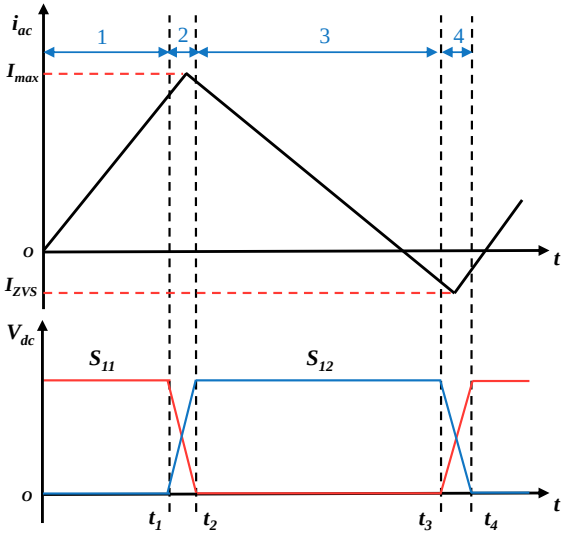


Figure 2.5: The input current waveform and the voltage waveform of semiconductors in the TCM control in one switching period

The biggest advantage of TCM compared to CRM is that ZVS is fully achieved in the whole period. Moreover, there are other soft switching methods like adding extra components, which will increase the physical complexity and most likely will also impair the gain of power density and specific power [13] [14]. Thus, this dissertation uses the state-of-art TCM method for the AC-DC three-phase PFC converters of OBCs.

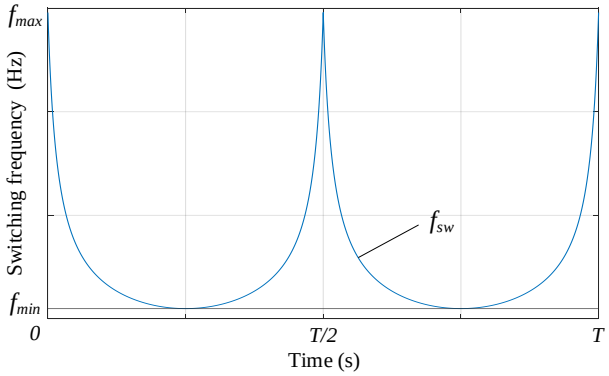


Figure 2.6: The switching frequency variation of TCM control in one main period

2.2.3. THREE-PHASE PFC TOPOLOGIES UNDER TCM CONTROL

The previous analysis of the TCM control is based on the one-phase leg of the PFC converters. However, it cannot be directly applied to the three-phase two-level full-bridge applications. First of all, the switching frequency f_{sw} is not constant and varies with time in the whole period, as shown in Figure 2.6. Moreover, the switching frequency of the three phases are not synchronized since the input voltage and current have a 120° phase shift. Thus, the three phases should be operated independently with the aforementioned TCM control, which is not applicable in conventional two-level converters.

Different topologies have been proposed to overcome this problem, as shown in Figure 2.7. L_c is the boost (converter-side) inductor as discussed previously, while L_g is the gird-side inductor. The two-level full-bridge converter is connected to the power grid via an LCL filter to meet the grid-connected current harmonic requirements [5]. P and N represent the neutral point of the grid and the filter, respectively, while O represents the mid-point of the DC link. The state of S_1 and S_2 determines three different topologies.

1. Topology 1: Simple two-level full-bridge converter with S_1 and S_2 closed.
2. Topology 2: S_1 is closed but S_2 is open.
3. Topology 3: Both S_1 and S_2 are closed.

COUPLED THREE-PHASE TOPOLOGY UNDER TCM CONTROL

Topology 1 demonstrates a coupled three-phase converter, where only two phases can operate independently. Thus, an improved TCM + Discontinuous current mode (DCM) + Clamped modes control is proposed in [12] [15] [16].

The main period is divided into 12 sectors based on the three-phase input voltage. Each switching period can be divided into 8 intervals. For example, in the first sector ($\omega t = 0 - 30°$), the three-phase current (i_a i_b and i_c) waveform in one switching period is shown in Figure 2.8. The AC voltage is considered constant in each switching period since the switching frequency is much larger than 50 Hz (greater than 20 times).

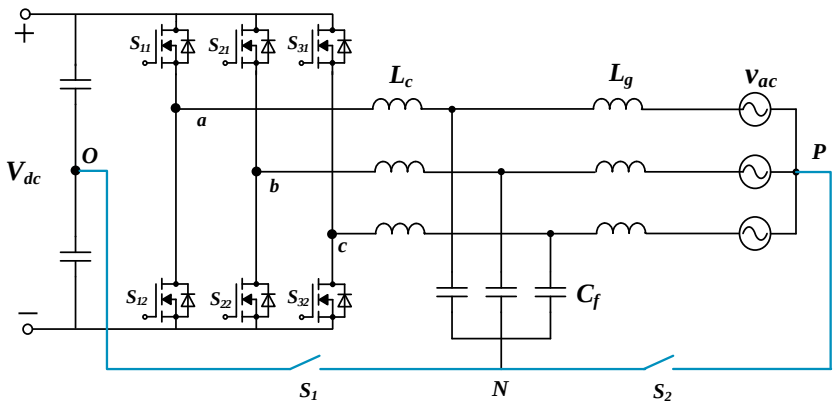


Figure 2.7: Three-phase PFC converters allowing the usage of the TCM control

Interval 1 (0 - t_1): All the lower switches (S_{12} S_{22} and S_{32}) are on. i_a and i_c increase linearly. Due to the negative voltage v_b, i_b decreases linearly. The slopes of current are:

$$di_a/dt = v_a/L_c \tag{2.1}$$

$$di_b/dt = v_b/L_c \tag{2.2}$$

$$di_c/dt = v_c/L_c \tag{2.3}$$

S_{32} is turned off at t_1.

Interval 2 (t_1 - t_2): Resonance occurs between the two parasitic capacitors of S_{31}, S_{32} and inductor L_c. The parasitic capacitor of S_{31} is discharged to zero so that the anti-parallel diode conducts, and S_{32} is turned on at t_2 under zero voltage.

Interval 3 (t_2 - t_3): S_{12} S_{22} and S_{31} are turned on. The current i_c starts to decrease. The slope of the three-phase current becomes:

$$di_a/dt = (v_a + V_{dc}/3)/L_c \tag{2.4}$$

$$di_b/dt = (v_b + V_{dc}/3)/L_c \tag{2.5}$$

$$di_c/dt = (v_c + V_{dc}/3)/L_c \tag{2.6}$$

S_{12} is turned off at t_3.

Interval 4 (t_3 - t_4): Resonance occurs in phase A. The parasitic capacitor of S_{11} is discharged to zero, and S_{11} is turned on at t_4 under zero voltage.

Interval 5 (t_4 - t_5): S_{11} is turned on. i_a starts to decrease. The slope of the three-phase current becomes:

$$di_a/dt = (v_a - V_{dc}/3)/L_c \tag{2.7}$$

$$di_b/dt = (v_b + 2V_{dc}/3)/L_c \tag{2.8}$$

$$di_c/dt = (v_c - V_{dc}/3)/L_c \tag{2.9}$$

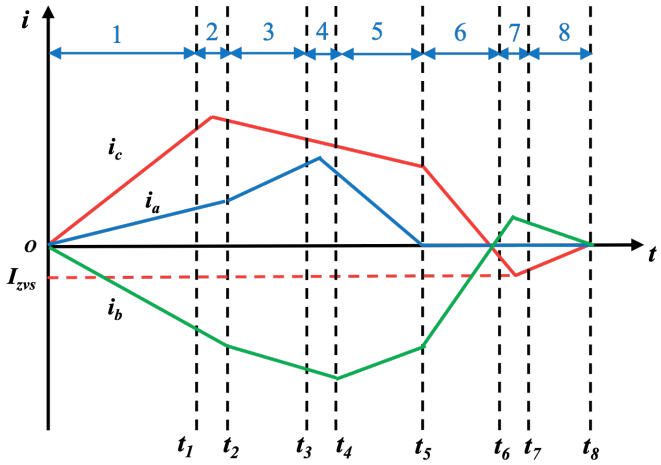


Figure 2.8: Three-phase current waveform under TCM + DCM + Clamped modes control in one switching period of sector 1 ($\omega t = 0 - 30°$)

Since v_a is the smallest value, i_a drops to zero first. Then, S_{11} is turned off at t_5.

Interval 6 (t_5 - t_6): Only S_{22} and S_{31} conduct now, so the current slope becomes:

$$di_b/dt = -di_c/dt = (V_{dc} + v_b - v_c)/2L_c \tag{2.10}$$

i_c drops to zero and then to a negative value I_{zvs}, ensuring that the parasitic capacitor of S_{32} can be discharged to zero voltage. S_{31} is turned off at t_6.

Interval 7 (t_6 - t_7): The same resonance process occurs, and S_{32} is turned on at t_7 under zero voltage.

Interval 8 (t_7 - t_8): Only S_{22} and S_{32} conduct now, so the current slope becomes:

$$di_b/dt = -di_c/dt = (v_b - v_c)/2L_c \tag{2.11}$$

i_b and i_c reach zero at the end of interval 8, and this switching period is over.

During this switching cycle, phases A, B and C operate at DCM, clamped mode and TCM, respectively. The operation mode of the three phases varies based on the absolute value of input voltage. The phase with the largest voltage value operates at clamped mode, while that with the smallest voltage value operates at DCM [6]. The switching frequency of the three phases is synchronized.

However, this method requires significant computational resources and complicated control. Besides, extra current zero-crossing detection (ZCD) device is needed in Topology 1.

DECOUPLED THREE-PHASE TOPOLOGY UNDER TCM CONTROL

A more straightforward way for three-phase TCM control is to decouple the three phases by connecting the AC neutral point and the midpoint of the DC link [17] [18] [19] [20]. Topology 2 and Topology 3 are two examples. In these two topologies, three phases are

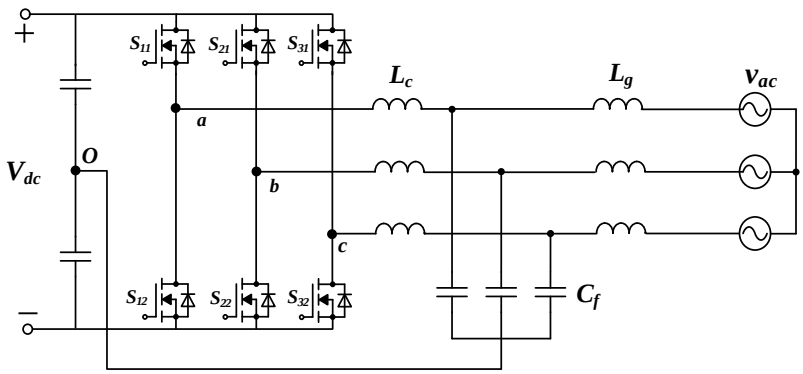


Figure 2.9: The chosen topology of three-phase PFC converters under the TCM control

decoupled so that they can operate independently. Thus, the TCM control discussed in 2.2.2 can be used directly.

However, topology 3 usually is not preferred in practical applications. The first reason is that the neutral point of the AC grid is not always available. Moreover, zero sequence current can flow so that third harmonic injection PWM (THIPWM) and discontinuous PWM (DPWM) are not possible for implementation, which limits the modulation index. Thus, in this dissertation, topology 2 is selected for three-phase TCM control analysis, as shown in Figure 2.9. The basic operation is the same as discussed in 2.2.2, and the only difference between the three phases are phase shifted by 120° accordingly.

3

BASIC CONCEPT AND OPERATION PRINCIPLE

3.1. INTRODUCTION

IN the TCM control introduced in Chapter 2, the semiconductor current reaches a certain value in the opposite direction in each switching cycle, which makes the voltage of the parasitic capacitance drop to zero during the resonance period. It ensures that the anti-parallel diode conducts before turning on the switch so that fully ZVS is achieved.

The TCM control is the state-of-the-art and commonly used method to achieve zero turn-on loss during the whole switching period [21]. Compared to CCM, TCM operation almost eliminates the turn-on loss. Compared to critical conduction mode (CRM), TCM operation can achieve ZVS over the whole switching period, further leading to a smaller turn-on loss. However, in the PFC applications, the filter inductor current in TCM has a large ripple, containing both the low-frequency and the high-frequency components, resulting in the higher inductor loss and conduction loss.

To minimize the inductor loss and achieve a better inductor design, the integrated triangular current mode (iTCM) control is proposed in [22] [23] [24]. The basic idea of the iTCM control is to split the high-frequency and low-frequency current by adding an extra LC branch to the converter output. The high-frequency current will flow into the LC branch due to its high-pass characteristic, while the low-frequency current will flow through the AC-side boost inductor. Then, the inductor can be optimally designed to minimize the inductor losses. The inductor with low-frequency current can be designed by powder iron core with solid wire, while the inductor with high-frequency current can be designed by ferrite core with litz wire to minimize the total inductor losses.

3.2. SINGLE-PHASE ITCM PFC CONVERTERS

The single-phase AC-DC PFC converter topology under the iTCM control has been developed in [22] [23]. In this section, the idea of the single-phase iTCM control will be briefly introduced.

The schematic of the single-phase AC-DC PFC converter for the iTCM control is shown in Figure 3.1(a). It consists of two switching legs, each containing two SiC MOSFETs with integrated anti-parallel diodes.

The right switching leg is operated synchronously with the grid frequency which is 50 Hz in the Netherlands. When $v_{ac} > 0$, the lower switch (S_{22}) conducts. When $v_{ac} < 0$, the upper switch (S_{21}) conducts. The left switching leg is operated under iTCM control, switching frequency up to several kilo-Hertz. Since the switching frequency f_{sw} >>50 Hz, the input AC voltage can be considered a constant value in each switching cycle.

The AC side is connected to the grid via an input LCL filter (L_c, L_g and C_f), EMI filter and protection circuit. The AC side voltage can be expressed as:

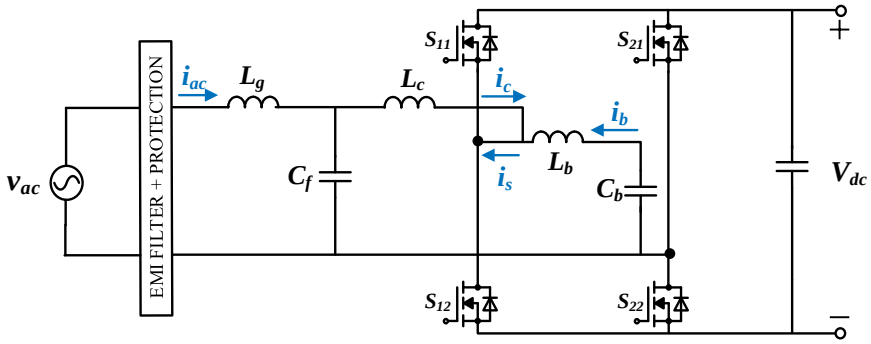
$$v_{ac}(t) = \hat{v}_{ac} \sin(\omega t) \tag{3.1}$$

where $\hat{v}_{ac}$ is the input peak voltage, ω is the grid angular frequency.

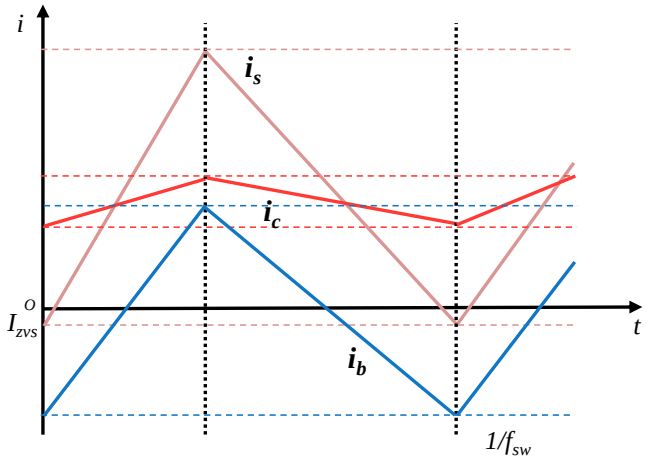
In the PFC converter, the input current $i_{ac}(t)$ is in phase with the input voltage, which is expressed as:

$$i_{ac}(t) = \hat{i}_{ac} \sin(\omega t) \tag{3.2}$$

where $\hat{i}_{ac}$ is the input peak current, and it is determined by the input power P, which can be expressed as:



(a)

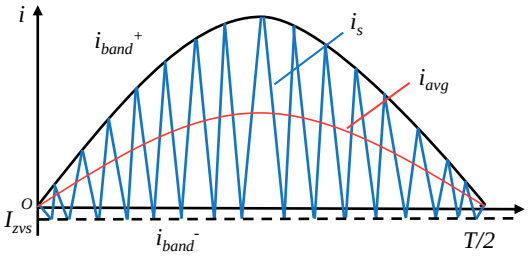


(b)

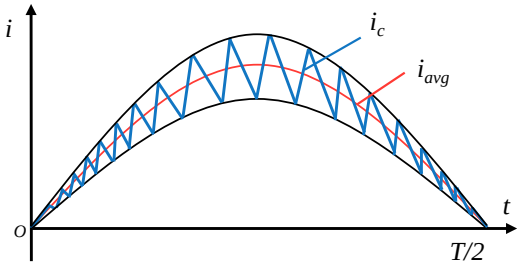
Figure 3.1: (a) Single-phase AC-DC PFC converter with an additional LC branch allowing the usage of iTCM control of OBCs; (b) Current waveform in one switching period ($1/f_{sw}$) for illustrating the idea of iTCM control

$$\hat{i}_{ac} = \frac{2P}{\hat{v}_{ac}} \tag{3.3}$$

The LC branch (L_b and C_b) is added between the two legs in the TCM control, as shown in Figure 3.1(a). The semiconductor current i_s is split into two parts because of the added LC branch. Due to the high-pass characteristic of the LC circuit, most of the high-frequency current (i_b) flows through L_b, which stays within the circuit. Only low-frequency current with a small ripple (i_c) flows through L_c to the grid-side. The current i_s flowing into the semiconductors remains the same as the conventional TCM control,



(a)



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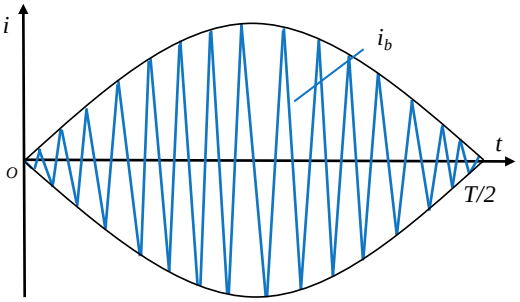
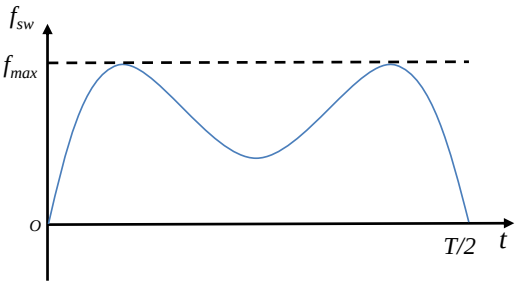


(c)



(d)

Figure 3.2: (a) The semiconductor current i_s in TCM or iTCM with reversal current I_{zvs}; (b) The L_c current with a small ripple; (c) The LC branch current i_b with most high-frequency component; (d) The switching frequency (f_{sw}) of the TCM or iTCM (Taking few switching periods in one positive half main-frequency period as illustration)

ensuring fully ZVS turn-on. The illustration of this current integration in one switching cycle is depicted in Figure 3.1(b). The most desirable case happens when the average current of $i_b = 0$, and only i_c contributes to the active input power [22].

Take the positive half period (S_{22} conducts) as an example; when S_{12} conducts, the current i_s increases linearly, which is expressed as:

$$\Delta i_s(t) = \frac{1}{L} v_{ac}(t) \cdot t_{on}(t) \tag{3.4}$$

where $\Delta i_s(t)$ is the current ripple of the semiconductor current, $t_{on}(t)$ is the on time of S_{12}, L is the equivalent boost inductance, which is expressed as:

$$L = 1/(\frac{1}{L_c} + \frac{1}{L_b}) \tag{3.5}$$

When S_{11} conducts, the current i_s decreases linearly as:

$$\Delta i_s(t) = \frac{1}{L}(v_{ac}(t) - V_{dc}) \cdot t_{off}(t) \tag{3.6}$$

The switching frequency f_{sw} of the single-phase iTCM control varies with time in order to keep a constant reversal current I_{zvs}, as shown in Figure 3.2(d). By combining Equation 3.4 and 3.6, the switching frequency f_{sw} of the single-phase iTCM control can be calculated as:

$$f_{sw} = \frac{1}{L\Delta i_(t)} \frac{v_{ac}(t)(V_{dc} - v_{ac}(t))}{V_{dc}} \tag{3.7}$$

The average value of the semiconductor current i_s is the input current i_{ac}. Besides, a constant reversal current must be obtained to achieve fully ZVS turn-on. Thus, i_s is a triangular current with a large current ripple, which can be expressed as:

$$\Delta i_s(t) = 2|I_{zvs}| + 2\hat{i}_{ac}|\sin(\omega t)| \tag{3.8}$$

The switching frequency can be further expressed as:

$$f_{sw} = (\frac{1}{L_c} + \frac{1}{L_b}) \frac{\hat{v}_{ac}^2 |\sin(\omega t)|}{2|I_{zvs}|\hat{v}_{ac} + 4P|\sin(\omega t)|} \frac{V_{dc} - \hat{v}_{ac}|\sin(\omega t)|}{V_{dc}} \tag{3.9}$$

However, the switching frequency f_{sw} becomes zero when the input voltage equals zero in the single-phase iTCM control, which is undesirable and inapplicable. Thus, the switching frequency f_{sw} is limited by f_{min}. For example, in [22], f_{min} is set to 35 kHz.

The value of L_c and L_b should be well-designed for the current distribution. The parameter r is introduced as the peak-to-peak current ripple of i_c in the percentage of the input peak current ($\hat{i}_{ac}$) to determine the inductance of L_c and L_b [22]. The coefficient r varies from 0 to 200 %. When $r = 200$ %, the control scheme becomes equivalent to the TCM control since the value of L_b becomes 0. The inductance of L_c is first determined by:

$$L_c = \frac{\hat{v}_{ac}^2}{2r f_{min} P}\left(1 - \frac{\hat{v}_{ac}}{V_{DC}}\right) \tag{3.10}$$

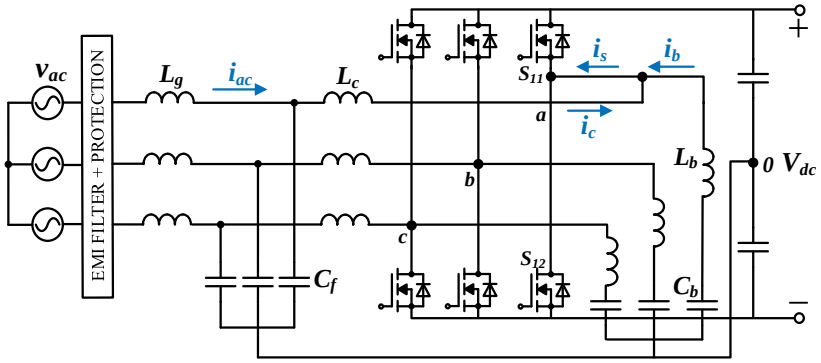


Figure 3.3: The chosen topology of three-phase AC-DC PFC converters allowing the usage of the iTCM control

Then, by subtracting Equation 3.9 and 3.10, the branch inductor L_b is calculated as:

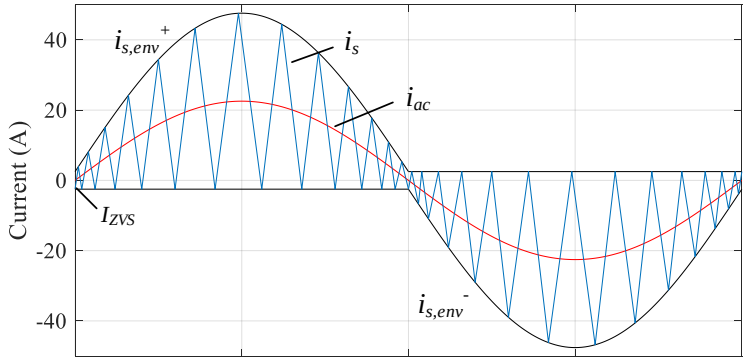
$$L_b = \frac{\hat{v}_{ac}^2}{2P(2-r)+2I_{zvs}\hat{v}_{ac}}\left(1-\frac{\hat{v}_{ac}}{V_{DC}}\right)\frac{1}{f_{min}} \tag{3.11}$$

The idea and mathematical calculation of single-phase iTCM control is introduced in this section. However, according to the literature study, the iTCM control method is only used in DC/DC converters or single-phase AC-DC PFC applications[22] [25]. It has not been applied to the utility grid (230V RMS and 50 Hz in the Netherlands). Besides, only the single-phase iTCM topology is proposed, which is not desirable when connecting to the three-phase power grid as OBCs. The three-phase AC-DC PFC converter is necessary as the front stage of OBCs when using V2G or V2X operation.

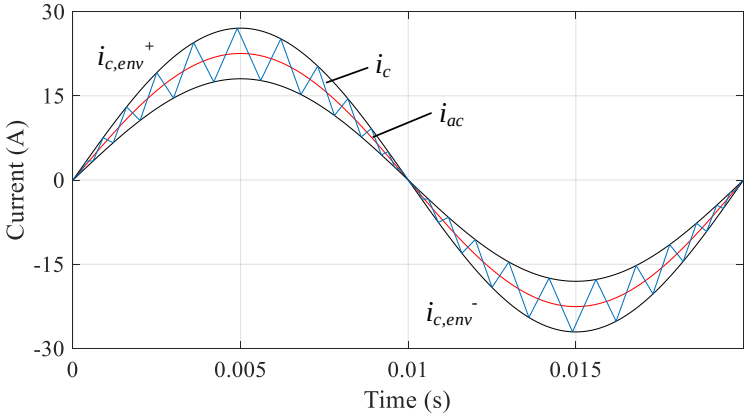
3.3. THREE-PHASE iTCM PFC CONVERTERS

In this section, the iTCM control method will be extended to three-phase applications. First of all, the topology of the three-phase AC-DC PFC converter under the iTCM control is chosen based on the three-phase TCM topology discussed in Chapter 2 topology 2, as shown in Figure 3.3.

The iTCM three-phase topology is a three-phase full-bridge two-level AC-DC PFC converter with the added three-phase LC branch in the Y connection. The AC-side is connected to the three-phase power grid via an input LCL filter to the current harmonic requirement. The DC midpoint and AC neutral point of the capacitor are connected to ensure that the three phases are decoupled, and each phase can operate independently. Independent operation must be guaranteed in the three-phase iTCM control since the switching frequency f_{sw} of each phase has a 120° phase shift, as shown in Figure 3.5 [26]. Simple sinusoidal PWM (SPWM) method can be used in this topology, and it can be extended to space vector PWM (SVPWM) or third harmonic injection PWM (THIPWM) [26].



(a)



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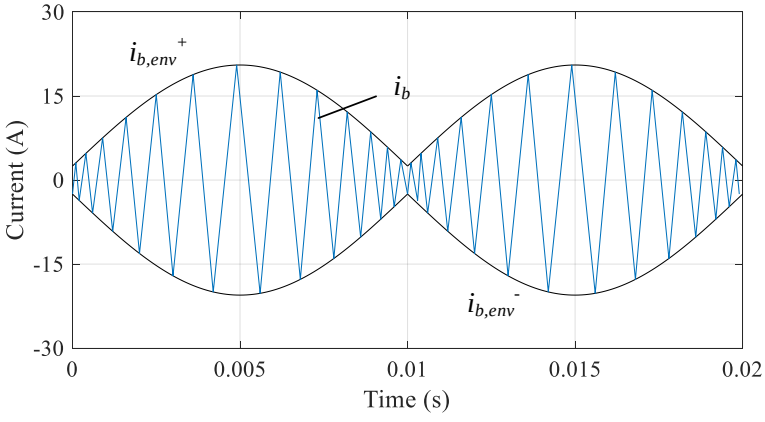
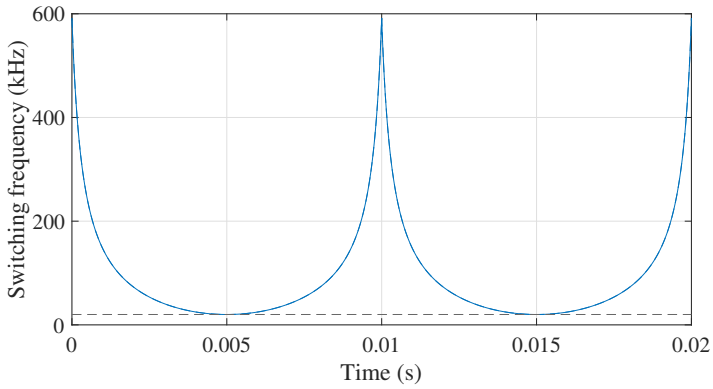
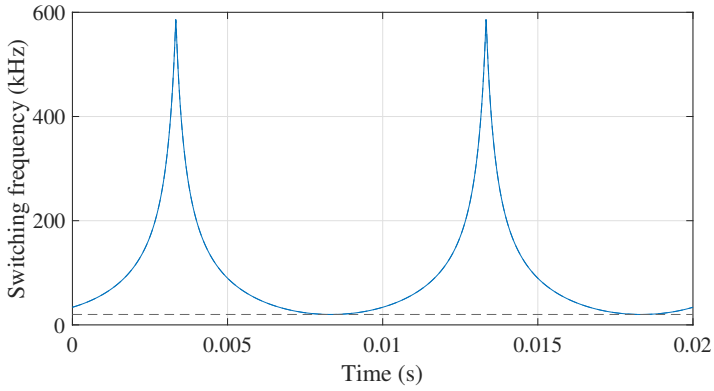


(c)

Figure 3.4: The current waveform of the iTCM control; (a) The semiconductor current i_s; (b) The boost inductor current i_c with a small ripple; (c) The LC branch current i_b with high-frequency component; (Taking just one-phase and few switching periods in one positive half main-frequency period as illustration)



(a)



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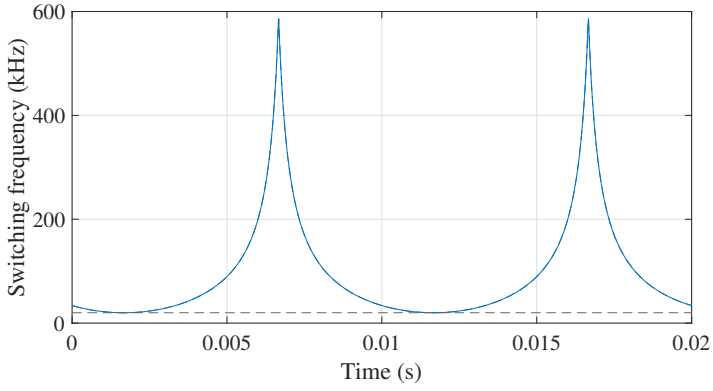


(c)

Figure 3.5: The switching frequency f_{sw} of the three-phase iTCM control with a 120° phase shift; (a) Phase A; (b) Phase B ; (c) Phase C.

3.3.1. SYSTEM DESIGN

The three-phase input voltage can be expressed as:

$$\begin{cases} v_{ac,a}(t) = \hat{v}_{ac} \sin(\omega t) \\ v_{ac,b}(t) = \hat{v}_{ac} \sin(\omega t - 2\pi/3) \\ v_{ac,c}(t) = \hat{v}_{ac} \sin(\omega t + 2\pi/3) \end{cases} \tag{3.12}$$

where $v_{ac,a}(t)$, $v_{ac,b}(t)$ and $v_{ac,b}(t)$ are the input AC voltage of phase A, B and C respectively, ω is the grid frequency.

Considering a constant DC side voltage V_{dc}, the modulation index can be defined as:

$$M = \frac{\hat{V}_{ac}}{V_{dc}/2} \tag{3.13}$$

The current of each phase is in phase with the voltage in PFC converters, so the three-phase current can be expressed as:

$$\begin{cases} i_{ac,a}(t) = \hat{i}_{ac} \sin(\omega t) \\ i_{ac,b}(t) = \hat{i}_{ac} \sin(\omega t - 2\pi/3) \\ i_{ac,c}(t) = \hat{i}_{ac} \sin(\omega t + 2\pi/3) \end{cases} \tag{3.14}$$

where $i_{ac,a}(t)$, $i_{ac,b}(t)$ and $i_{ac,b}(t)$ are the input AC current of phase A, B and C, respectively.

Switching frequency

Taking phase A in Figure 3.3 as an example, i_s, i_c, i_b and i_{ac} are the semiconductor current, the boost inductor current, the LC branch current and the input AC current, respectively. It is assumed that the positive direction of the current is from the grid to the converter in the following analysis.

The semiconductor current i_s is the triangular current with a large current ripple to ensure the fully ZVS operation, the same as the single-phase iTCM control shown in Figure 3.4(a). The upper and lower envelope is denoted as $i^+_{s,env}$ and $i^-_{s,env}$, respectively. The average value of i_s is the required input current i_{ac}, as the red line shown in Figure 3.4(a).

In each switching cycle, the AC input voltage can be considered constant since the switching frequency is much larger than the main frequency. When S_{12} is on, the current i_s increases linearly. The current ripple of i_s is:

$$\Delta i_s(t) = \frac{1}{L}(V_{ac}(t) + V_{dc}/2) \cdot t_L(t) \tag{3.15}$$

where L is the equivalent boost inductor calculated by Equation 3.5, $t_L(t)$ is the on time of the lower semiconductor S_{12}.

When S_{11} is on, the current i_s decreases linearly. The current ripple of i_s is:

$$\Delta i_s(t) = \frac{1}{L}(V_{ac}(t) - V_{dc}/2) \cdot t_H(t) \tag{3.16}$$

where $t_H(t)$ is the on time of the upper semiconductor S_{11}. Since Δi_s in one switching cycle is constant, the on time of S_{11} and S_{12} can be expressed as:

$$t_{\mathrm{H}}(t) = \frac{2L\Delta i_{\mathrm{s}}(t)/V_{\mathrm{dc}}}{1 - M|\sin(\omega_{\mathrm{ac}} t)|} \tag{3.17}$$

$$t_{\mathrm{L}}(t) = \frac{2L\Delta i_{\mathrm{s}}(t)/V_{\mathrm{dc}}}{1 + M|\sin(\omega_{\mathrm{ac}} t)|} \tag{3.18}$$

The switching frequency of phase A can be calculated as:

$$f_{\mathrm{sw}}(t) = \frac{1}{t_{\mathrm{H}}(t) + t_{\mathrm{L}}(t)} = \frac{V_{\mathrm{dc}}}{4L\Delta i_{\mathrm{s}}(t)}[1 - M^2 \sin^2(\omega t)] \tag{3.19}$$

As discussed above, the semiconductor current i_{s} should guarantee a constant reversal current I_{zvs} and satisfy the input power in each switching cycle, so the current ripple Δi_{s} is expressed as:

$$\Delta i_{\mathrm{s}}(t) = 2I_{\mathrm{zvs}} + 2\hat{i}_{\mathrm{ac}}|\sin(\omega t)| \tag{3.20}$$

where $\hat{i}_{\mathrm{ac}}$ is the peak value of the input current, which can be calculated based on the input power:

$$\hat{i}_{\mathrm{ac}} = \frac{2P}{3\hat{v}_{\mathrm{ac}}} \tag{3.21}$$

where P is the three-phase input power.

Combining Equation 3.19, 3.20 and 3.21, the switching frequency of phase A in three-phase PFC converter under the iTCM control is expressed as:

$$f_{\mathrm{sw,a}} = \frac{\hat{v}_{\mathrm{ac}}^2\,(1/M - M\sin^2(\omega t))}{4I_{\mathrm{zvs}}\hat{v}_{\mathrm{ac}} + 8P/3\,|\sin(\omega t)|}\left(\frac{1}{L_{\mathrm{c}}} + \frac{1}{L_{\mathrm{b}}}\right) \tag{3.22}$$

The switching frequency of phase B and C only have a phase shift, which are expressed as:

$$f_{\mathrm{sw,b}} = \frac{\hat{v}_{\mathrm{ac}}^2\,(1/M - M\sin^2(\omega t - 2\pi/3))}{4I_{\mathrm{zvs}}\hat{v}_{\mathrm{ac}} + 8P/3\,|\sin(\omega t - 2\pi/3)|}\left(\frac{1}{L_{\mathrm{c}}} + \frac{1}{L_{\mathrm{b}}}\right) \tag{3.23}$$

$$f_{\mathrm{sw,c}} = \frac{\hat{v}_{\mathrm{ac}}^2\,(1/M - M\sin^2(\omega t + 2\pi/3))}{4I_{\mathrm{zvs}}\hat{v}_{\mathrm{ac}} + 8P/3\,|\sin(\omega t + 2\pi/3)|}\left(\frac{1}{L_{\mathrm{c}}} + \frac{1}{L_{\mathrm{b}}}\right) \tag{3.24}$$

Inductance (L_{c}, L_{b}) design

The current i_{s} is divided into two parts due to the added LC branch. The capacitance C_{b} in the LC branch blocks DC and low-frequency current so that most of the high-frequency current would flow through the LC branch (i_{b}), as shown in Figure 3.4(c). As a result, the low-frequency current with a small current ripple (i_{c}) flows through L_{c} to the grid, as shown in Figure 3.4(b). The inductance of L_{c} and L_{b} is properly designed to guarantee that the average value of i_{c} and i_{b} are i_{ac} and 0, respectively. The equation $i_{\mathrm{s}} = i_{\mathrm{b}} + i_{\mathrm{c}}$ is always valid in the iTCM control.

The parameter r is introduced as the peak-to-peak current ripple of i_{c} in the percentage of the input peak current ($\hat{i}_{\mathrm{ac}}$) to determine the inductance of L_{c} and L_{b} [22]. The maximum ripple of current i_{c} is:

$$\Delta i_{\mathrm{c,max}} = \frac{2P/3}{\hat{v}_{\mathrm{ac}}} \cdot r \tag{3.25}$$

The coefficient r varies from 0 to 200%. When r = 200 %, the control scheme becomes equivalent to the TCM control since the value of L_b becomes 0.

By only considering L_c, the ripple of the current i_c can be expressed as:

$$\Delta i_c(t) = \frac{1}{L_c}(V_{ac}(t) + V_{dc}/2) \cdot t_L(t) \tag{3.26}$$

where $t_L(t)$ is the on time of the lower semiconductor S_{12}.

$$\Delta i_c(t) = \frac{1}{L_c}(V_{ac}(t) - V_{dc}/2) \cdot t_H(t) \tag{3.27}$$

where $t_H(t)$ is the on time of the upper semiconductor S_{11}, and $t_H(t) + t_L(t) = 1/f_{sw}(t)$.

By combining Equation 3.26 and 3.27, the inductance Lc can be expressed as:

$$L_c(t) = \frac{1}{\Delta i_c(t) f_{sw}(t)}(V_{ac}(t) - \frac{V_{ac}^2(t)}{V_{dc}}) \tag{3.28}$$

Considering Equation 3.28, when $v_{ac}(t)$ reaches its maximum value, f_{sw} lies in its minimum value as shown in Figure 3.5(a), and $\Delta i_c(t)$ becomes maximum. Thus, L_c is finally determined by:

$$L_c = \frac{\hat{v}_{ac}}{2P/3\ f_{min}\ r} \cdot \frac{(V_{dc}/2)^2 - \hat{v}_{ac}^2}{V_{dc}} \tag{3.29}$$

where f_{min} denotes the minimum value of switching frequency, as the dash line indicates in Figure 3.5. L_b can be subsequently subtracted from Equations 3.22 and 3.29 and can be expressed as:

$$L_b = \frac{1}{f_{min}} \frac{\hat{v}_{ac}}{2I_{zvs}\hat{v}_{ac} + 4P/3 - 2P/3\ r} \frac{(V_{dc}/2)^2 - \hat{v}_{ac}^2}{V_{dc}} \tag{3.30}$$

Capacitance (C_b) design

The capacitor C_b needs to be well-designed to block the DC and low-frequency current so that most of the high-frequency component flows into the LC branch as expected. First of all, it will draw some reactive power at low frequency and reduce the total power factor so that the value of C_b should be small. Moreover, C_b should be large enough to keep the resonance frequency of the LC branch smaller than the switching frequency f_{sw} to get an inductive behaviour, which is a necessity to achieve ZVS turn-on [23]. The LC resonant frequency $\omega_{LC,res}$ is chosen as 40000 rad/s in this paper, and hence the value of C_b can be determined by

$$\omega_{LC,res} = \frac{1}{\sqrt{L_b C_b}} < \omega_{min} \tag{3.31}$$

where $\omega_{min} = 2\pi f_{min}$.

The admittance of the LC branch is:

$$Y = \frac{i_b}{v_t} = \frac{sC_b}{s^2 L_b C_b + sR_D C_b + 1} \tag{3.32}$$

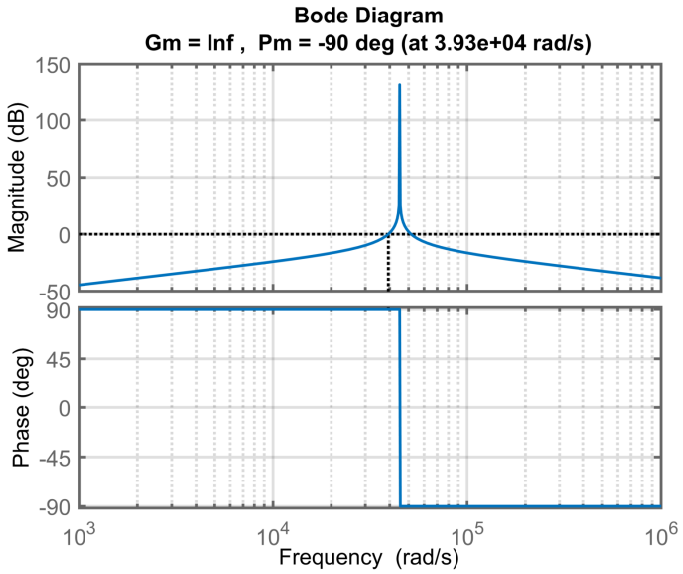


Figure 3.6: Bode diagram of the transfer function of LC branch to determine the value of C_b

Table 3.1: Individual current odd harmonic limits for 120V - 69kV, $I_{SC}/I_L < 20$ system (IEEE 519 - 2014)

I_{SC}/I_L	Harmonics values are in % of maximum current I_{max}					TDD
	$3 \le h < 11$	$11 \le h < 17$	$17 \le h < 23$	$23 \le h < 35$	$35 \le h \le 50$	
<20	4.0	2.0	1.5	0.6	0.3	5.0

The Bode diagram of this transfer function is shown in Figure 3.6. If the switching frequency is close to the resonance frequency $\omega_{LC,res}$, this will lead to considerable oscillation in the system. Since the minimum switching frequency is 20 kHz in this dissertation, the LC resonance frequency $\omega_{LC,res}$ is chosen to 40000 rad/s in this dissertation.

Inductance (L_g) design

The grid-side inductance L_g is designed to meet the current harmonics standard, such as IEEE 519 - 2014 [27]. The odd harmonics limit is shown in Table 3.1, which is expressed as:

$$I_{IEEE519,odd} = cI_{max} \tag{3.33}$$

where c is the harmonics values shown in Table 3.1. The even harmonics $I_{IEEE519,even}$ are limited to 1/4 of the odd harmonics.For the harmonics larger than 50, it is limited to 0.3% and 0.75% of the fundamental current for odd and even harmonics in this calculation.

The attenuation of the LCL filter is:

$$\mathrm{Att}(\omega) = \frac{1}{L_\mathrm{T}} \cdot \frac{\omega_\mathrm{res}^2}{\omega \left|\omega^2 - \omega_\mathrm{res}^2\right|} \tag{3.34}$$

where ω_res is the resonant frequency of the LCL filter, as:

$$\omega_\mathrm{res} = \sqrt{\frac{L_\mathrm{c} + L_\mathrm{g}}{L_\mathrm{c} L_\mathrm{g} C_\mathrm{f}}} \tag{3.35}$$

The total inductance of the LCL filter L_T has to attenuate the critical current harmonic below the standard current limit I_IEEE519.

$$L_\mathrm{T,crit} = \frac{\omega_\mathrm{res}^2 V_\mathrm{crit}}{\omega_\mathrm{crit} \left|\omega_\mathrm{crit}^2 - \omega_\mathrm{res}^2\right| I_\mathrm{IEEE519}} \tag{3.36}$$

where V_crit is the critical voltage harmonic of the converter side voltage V_t, ω_crit is the critical frequency.

Since L_c has already determined by the Equation 3.29, L_g can be obtained by:

$$L_\mathrm{T,crit} = L_\mathrm{c} + L_\mathrm{g} \tag{3.37}$$

For a certain power rating and switching frequency range, the total needed inductance $L_\mathrm{T,crit}$ would be the same. However, L_c varies with the parameter r, so L_g can only be obtained after determining r. In the following analysis in Chapter 5, it can be seen that L_g is not needed in some cases. However, L_g remains due to efficiency and power density reasons, which will be further discussed in Chapter 5.

3.3.2. RESONANCE INTERVAL ANALYSIS

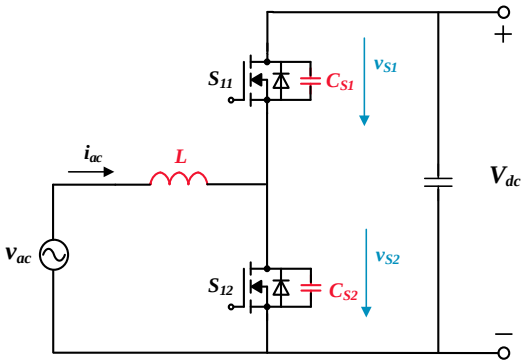
The current i_s goes to the reversal direction at a certain value in each switching cycle, indicated as $|I_\mathrm{zvs}|$. Then, the anti-parallel diode of the semiconductor conducts before the control turns on the switch so that fully ZVS turn-on is achieved. I_zvs is the desired turn-off current of semiconductors to fully discharge the parasitic capacitance so that the anti-parallel diodes can conduct before turning on.

As discussed in Chapter 2.2.2, the resonance occurs at interval 2 and interval 4 in the TCM control. In the iTCM control, the boost inductor L is the parallel of L_c and L_b, calculated by Equation 3.5. By taking the boost inductor L instead of L_c and L_b, the resonance circuit of one phase-leg can be simplified as shown in Figure 3.7(a).

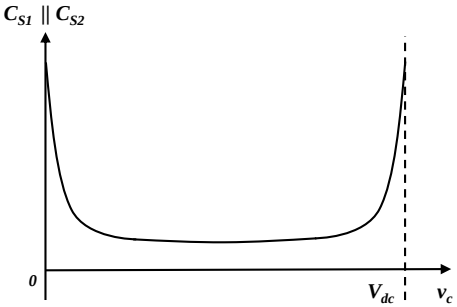
This resonance circuit can be considered as a series LC circuit, and the equivalent capacitance C_eq is the parallel of C_s1 and C_s2.

$$C_\mathrm{eq} = C_\mathrm{s1} + C_\mathrm{s2} \tag{3.38}$$

The MOSFET parallel capacitance C_s1 or C_s2 is nonlinear. When the voltage across the capacitor is small (close to 0), the capacitance is very large. As the voltage increases, the capacitance drops. Thus, the parallel capacitance C_eq is shown as Figure 3.7(b).



(a)



(b)

Figure 3.7: (a) One phase resonance circuit of interval 2 and 4 (as discussed in Chapter 2) in the iTCM control; (b) Parallel connection of the nonlinear anti-parallel capacitors, where v_c is the voltage across the parasitic capacitor of the turned-off semiconductor.

Interval 2

When S_{12} is turned off, the resonance occurs between the two parasitic capacitance C_{s1}, C_{s2} and the equivalent boost inductor L. The initial voltage of C_{s1} and C_{s2} are 0 and V_{dc}, respectively. Since the equivalent capacitance C_{eq} is large in the beginning, the voltage v_{s2} increases slowly. As v_{s2} rising, the C_{eq} drops so that the voltage slope increases. When v_{s2} nearly reaches V_{dc}, C_{eq} increases again, and the voltage slope decreases again.

The inductor current i_{ac} keeps increasing until v_{s2} exceeds the input voltage v_{ac}. When the voltage across the boost inductor L becomes negative, the inductor current i_{ac} drops.

During the series LC resonance, the voltage of the capacitor v_{s1} can be expressed as:

$$v_{s1}(t) = V_{ac} - (V_{ac} - V_{c0})\cos\omega_0(t - t_0) + Z_0 I_{L0}\sin\omega_0(t - t_0) \tag{3.39}$$

where V_{ac} is the AC voltage during the resonance (Assumed to be constant since the resonance period is short enough), V_{c0} is the initial capacitor voltage ($-V_{dc}$ in interval

2), I_{L0} is the initial boost inductor current, ω_0 is the angular resonance frequency, which is calculated by:

$$\omega_0 = \frac{1}{\sqrt{LC_{eq}}} \tag{3.40}$$

Z_0 is the resonant impedance, which is expressed as:

$$Z_0 = \sqrt{\frac{L}{C_{eq}}} \tag{3.41}$$

By Equation 3.39, it can be seen that the voltage $v_{s1}(t)$ will drop to zero during the resonance. When v_{s1} drops to zero, the anti-parallel diode conducts due to the positive current direction, and then S_{11} can be turned on under ZVS.

Interval 4

When S_{11} is turned off, the resonance occurs between the two parasitic capacitance C_{s1}, C_{s2} and the equivalent boost inductor L as well. The initial voltage of C_{s1} and C_{s2} are V_{dc} and 0, respectively. Since the equivalent capacitance C_{eq} is large in the beginning, the voltage v_{s1} increases slowly. As v_{s1} rising, the C_{eq} drops so that the voltage slope increases. When v_{s2} nearly reaches V_{dc}, C_{eq} increases again, and the voltage slope decreases again.

The inductor current i_{ac} keeps decreasing at the revesal direction until v_{s1} is smaller than the input voltage v_{ac}. When the voltage across the boost inductor L becomes positive, the inductor current i_{ac} increases again.

During the series LC resonance, the voltage of the capacitor v_{s2} can be expressed as:

$$v_{s2}(t) = V_{ac} - (V_{ac} - V_{c0})\cos\omega_0(t - t_0) + Z_0 I_{L0}\sin\omega_0(t - t_0) \tag{3.42}$$

where V_{c0} is the initial capacitor voltage (V_{dc} in interval 4), I_{L0} is the initial boost inductor current (negative in interval 4). Thus, Equation becomes:

$$v_{s2}(t) = V_{ac} - (V_{ac} - V_{dc})\cos\omega_0(t - t_0) - Z_0 I_{L0}\sin\omega_0(t - t_0) \tag{3.43}$$

When $2V_{ac} < V_{dc}$, $v_{s2}(t)$ will drop to zero during the resonance, and then the parallel diode conducts before turning on S_{12}. ZVS turn-on is achieved in this case.

When $2V_{ac} > V_{dc}$, $v_{s2}(t)$ will not drop to zero if the $Z_0 I_{L0}\sin\omega_0(t - t_0)$ part is neglected (The worst case ($i_{ac} = 0$) should be considered). In order to let $v_{s2}(t)$ drop to zero during resonance, I_{L0} must be a negative value. This is the main difference between the CRM control and the TCM control, which means the negative initial inductor current will make the parasitic capacitor voltage drop to zero.

Method 1: Mathematical calculation of interval 4

The minimum initial current of the boost inductor I_{L0} that makes the minimum value of $v_{s2}(t)$ equals zero can be mathematically calculated by Equation 3.43 when $2V_{ac} > V_{dc}$. First of all, the derivation of Equation 3.43 is:

$$v'_{s2}(t) = \omega_0(V_{ac} - V_{dc})\sin\omega_0(t - t_0) - \omega_0 Z_0 I_{L0}\cos\omega_0(t - t_0) \tag{3.44}$$

Assuming $t_0 = 0$, let $v'_{s2}(t) = 0$, then

$$\tan\omega_0 t = \frac{Z_0 I_{L0}}{(V_{ac} - V_{dc})} \tag{3.45}$$

In the PFC converters with MOSFET, the value of the boost inductance L is around dozens to hundreds of μH, while the parasitic capacitance is in the level of pF. In general, $Z_0 I_{L0} > V_{ac} - V_{dc}$. Thus, when

$$\omega_0 t = \arctan \frac{Z_0 I_{L0}}{(V_{ac} - V_{dc})} \quad (\frac{\pi}{2} < \omega_0 t < \pi) \tag{3.46}$$

$v_{s2}(t)$ gets its minimum value. By taking Equation 3.46 into Equation 3.43, the minimum initial boost current that makes the $v_{s2}(t)$ drop to zero is calculated as:

$$I_{L0} = \frac{\sqrt{V_{dc}(2V_{ac} - V_{dc})}}{Z_0} \tag{3.47}$$

Thus, by combining Equation 3.41 and 3.47, the reversal constant current ensuring fully ZVS I_{zvs} can be calculated as:

$$I_{zvs} = -\sqrt{\frac{C_{eq} V_{dc}}{L}(2V_{ac} - V_{dc})} \tag{3.48}$$

where C_{eq} is the equivalent output capacitance of each half-bridge semiconductors (assuming that the upper and bottom switches are the identical), and can be expressed as:

$$C_{eq} = C_{s1} + C_{s2} = \frac{2}{V_{dc}} \int_0^{V_{dc}} C_{ds}(v_{ds})\, \mathrm{d}v_{ds} \tag{3.49}$$

where C_{ds} is the nonlinear output capacitance of each semiconductor, v_{ds} is the drain to source voltage when measuring C_{ds}. Both of the data can be obtained from the semiconductor datasheet.

Method 2: Analytical modeling of interval 4

In [7], u-Zi diagram has been proposed to analyze the minimum turn-off current needed to fully discharge the parasitic capacitance of the switch which will turn on. The voltage and current waveform of interval 4 is shown in Figure 3.8.

In interval 4, when S_{11} is turned off, C_{s1} is discharged from V_{dc} to 0, while C_{s2} is charged from 0 to V_{dc}. To fully discharge C_{s2}, the needed charge Q_c is:

$$Q_c = \int_0^{V_{dc}} C_{ds}(v_c)\, d v_c \tag{3.50}$$

Beside, the same charge is needed to charge C_{s1}. To simplify the analysis, it is assumed that the voltage applied to the equivalent capacitor v_c is [28]:

$$v_c(q_c) = \begin{cases} V_{dc}, & \text{if } q_c > Q_c \\ 0, & \text{else} \end{cases} \tag{3.51}$$

where q_c is the charge in the equivalent capacitance C_{eq}.

Considering the interval T_y, as shown in Figure 3.8, I_{zvs} can be expressed as:

$$Q_c = \frac{I_{zvs} T_y}{2} \tag{3.52}$$

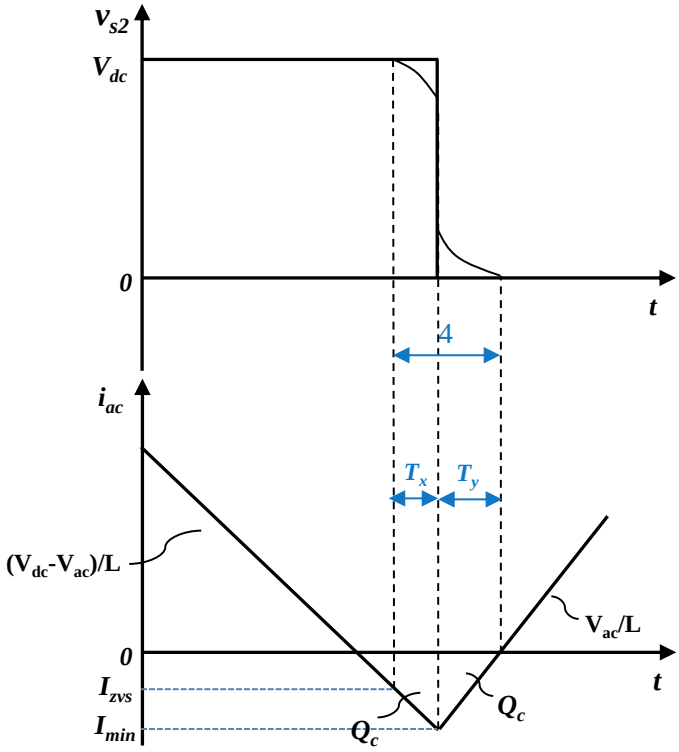


Figure 3.8: The simplified current and voltage waveform of interval 4 resonance period for the iTCM control (T_x and T_y are very short, I_{zvs} and I_{min} can be considered as the same value)

where T_y is calculated by:

$$L\frac{di}{dt} = L\frac{I_{zvs}}{T_y} = v_{ac} \tag{3.53}$$

By combining Equation 3.49, 3.50, 3.52 and 3.53, I_{zvs} can be calculated as:

$$I_{zvs} = -\sqrt{\frac{C_{eq}V_{dc}}{L}(2V_{ac} - V_{dc})} \tag{3.54}$$

Both Method 1 and 2 can obtain the same result. In the main cycle, the minimum required ZVS turn-on current is obtained when the input voltage is at its peak value, so:

$$I_{zvs} = \begin{cases} -\sqrt{\frac{C_{eq}V_{dc}}{L}(2\hat{v}_{ac} - V_{dc})} & \text{if } 2\hat{v}_{ac} \geq V_{dc} \\ 0 & \text{if } 2\hat{v}_{ac} < V_{dc} \end{cases} \tag{3.55}$$

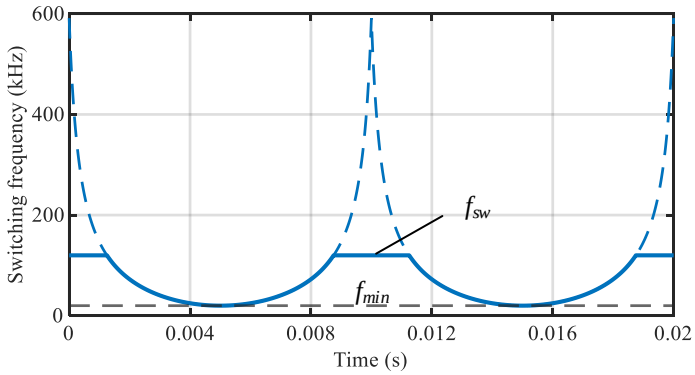


Figure 3.9: The switching frequency f_{sw} with a maximum 120 kHz limitation (the solid line) of the Bounded-iTCM control

3.3.3. FREQUENCY LIMITATION

The waveform of the iTCM switching frequency f_{sw} is shown in Figure 3.5. However, the variation is quite large, which is from 20 kHz to 591 kHz in this case. This will pose a great challenge to the practical implementation as well as to the design of the EMI filter [26]. Basically, there are two ways to limit the maximum frequency.

Bounded-iTCM

The switching frequency is limited within 120 kHz (f_{max} = 120 kHz) as the solid line shown in Figure 3.9, which is called the Bounded-iTCM control. Thus, the switching frequency f_{sw} becomes:

$$f_{sw}(t) = \begin{cases} f_{max} \cdot r & \text{if } r < 1 \\ f_{max} & \text{if } r \geq 1 \end{cases} \tag{3.56}$$

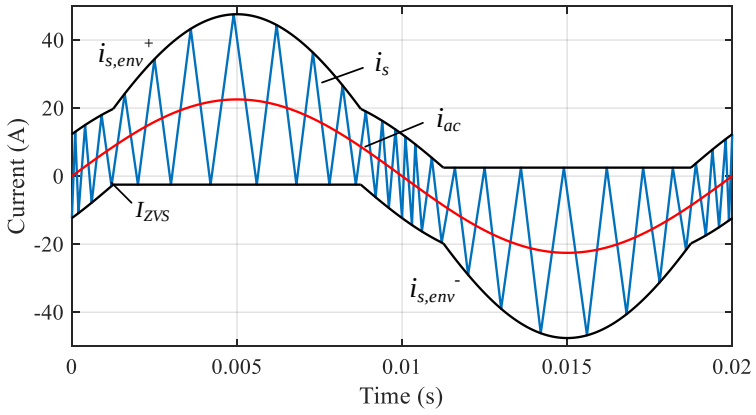
where r is the ratio between f_{sw} and f_{min}, expressed as:

$$r = \frac{f_{sw}(t)}{f_{max}} = \frac{1}{f_{max}} \frac{\hat{v}_{ac}^2 \, (1/M - M\sin^2(\omega t))}{4 I_{zvs} \hat{v}_{ac} + 8P/3 \, |\sin(\omega t)|} \left(\frac{1}{L_c} + \frac{1}{L_b}\right) \tag{3.57}$$

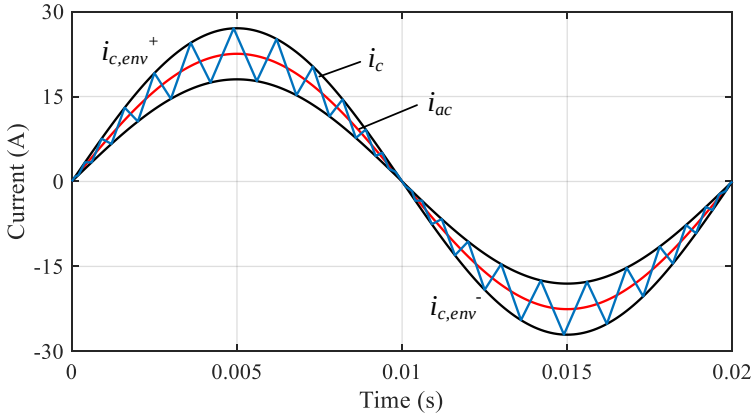
The ripple of $i_s(t)$ becomes:

$$\Delta i_s(t) = \begin{cases} 2I_{zvs} + 2\hat{i}_{ac}|\sin(\omega t)| & \text{if } r < 1 \\ (2I_{zvs} + 2\hat{i}_{ac}|\sin(\omega t)|) \cdot r & \text{if } r \geq 1 \end{cases} \tag{3.58}$$

Under the Bounded-iTCM control, ZVS turn-on is still achieved, but the reverse current is not constant due to the frequency limitation, as the i_s waveform shown in Fig. 3.10(a). This causes a larger current ripple, a larger turn-off current, and a higher turn-off loss compared to the case without frequency limitation. Since the turn-off loss of the WBG semiconductors is much smaller than the turn-on loss, and due to the fact the switched current is naturally smaller and close to the zero-crossing of the phase current, the trade-off is acceptable. With the switching frequency limitation, the current i_c and i_b



(a)



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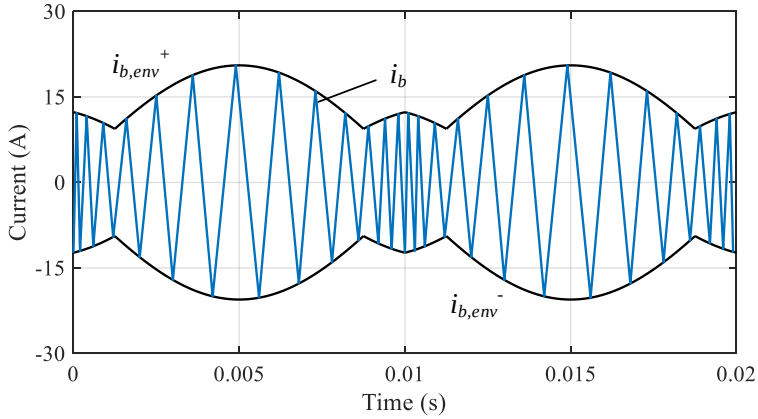


(c)

Figure 3.10: The current waveform of the Bounded-iTCM control with a maximum 120 kHz switching frequency limitation; (a) The semiconductor current i_s; (b) The boost inductor current i_c with a small ripple; (c) The LC branch current i_b with high-frequency component; (Taking just one-phase and few switching periods in one positive half main-frequency period as illustration)

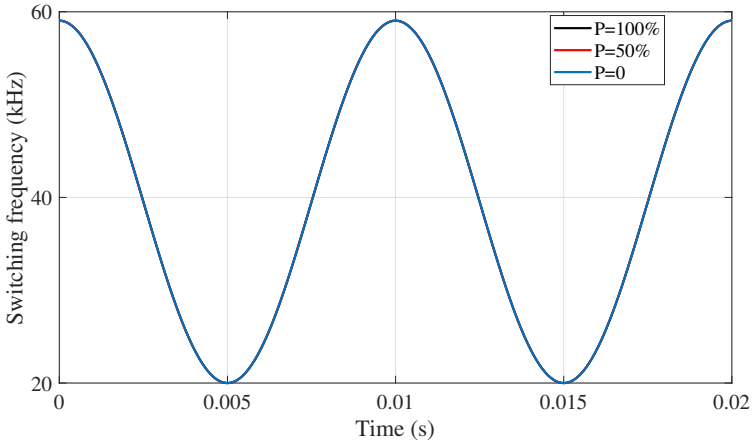


Figure 3.11: The switching frequency f_{sw} of the Sinusoidal-iTCM control

are shown in Figure3.10(b) and 3.10(c), respectively. This Bounded-iTCM control is the simplest way to limit the maximum switching frequency.

Sinusoidal-iTCM

The sinusoidal-iTCM control was introduced in [26] to limit the maximum switching frequency while maintaining ZVS turn-on. The idea is to create a constant sinusoidal current band of $i_s(t)$ instead of Equation 3.20:

$$\Delta i_s(t) = 2I_{zvs} + 2\hat{i}_{ac} \tag{3.59}$$

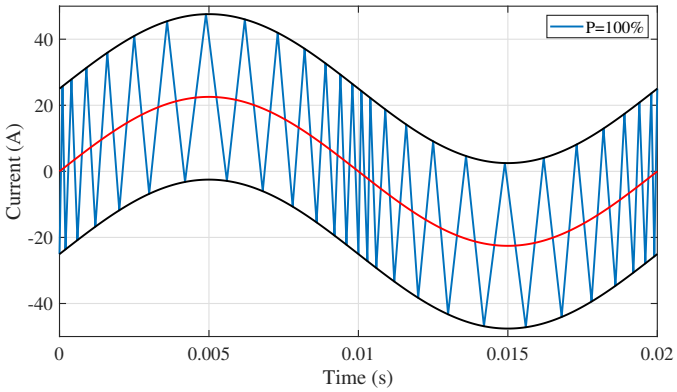
Taking Equation 3.59 into 3.19, the switching frequency of Sinusoidal-iTCM is expressed as:

$$f_{sw} = \frac{\hat{v}_{ac}^2\,(1/M - M\sin^2(\omega t))}{4I_{zvs}\hat{v}_{ac} + 8P/3}\left(\frac{1}{L_c} + \frac{1}{L_b}\right) \tag{3.60}$$

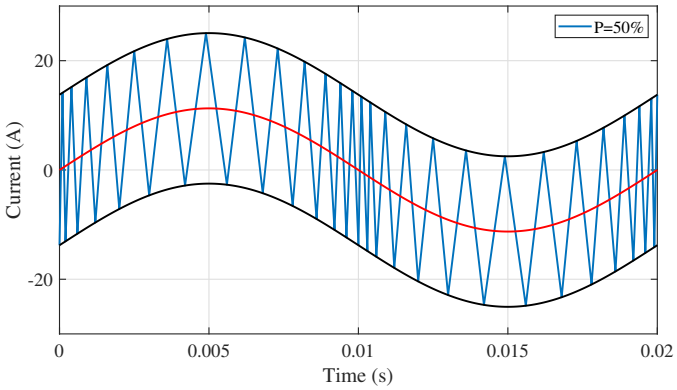
The waveform of the switching frequency f_{sw} and the semiconductor current i_s under the Sinusoidal-iTCM control are shown in Figure 3.11 and 3.12, respectively. It can be seen that the current ripple of the Sinusoidal-iTCM control is larger than the Bounded-iTCM control in general, which would cause higher switching loss and a larger input filter. However, the biggest advantage of the Sinusoidal-iTCM control is that the current band and the switching frequency maintains the same at different load conditions, which means it can handle various charging power without adjustment. In the Bounded-iTCM control, the switching frequency should be adjusted When the EV battery is charging at a different power level.

3.3.4. MODULATION METHOD

The previously analysis is based on the Sinusoidal PWM (SPWM), but the aforementioned three-phase iTCM topology still leaves the possibility for THIPWM, SVPWM or DPWM.



(a)



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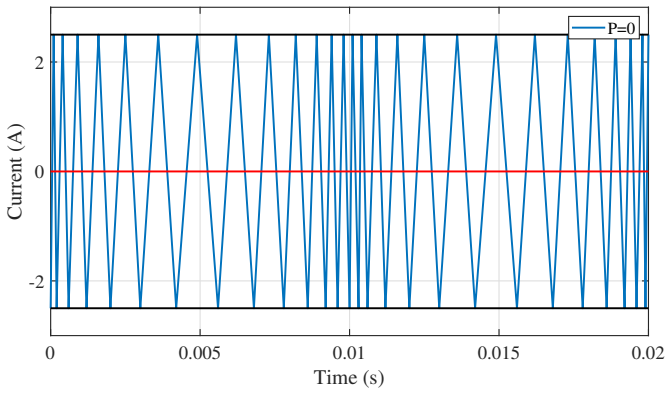
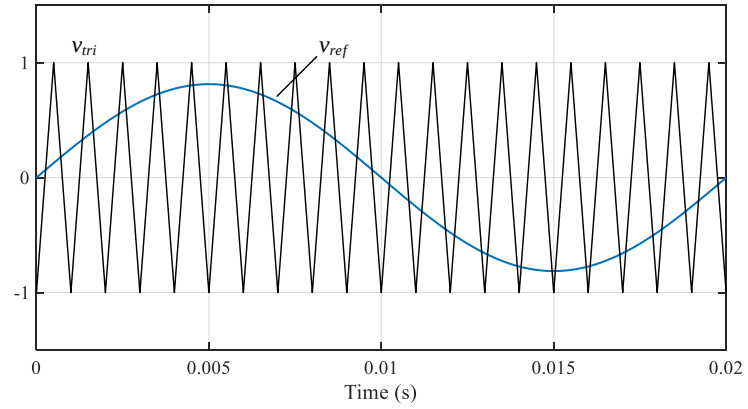
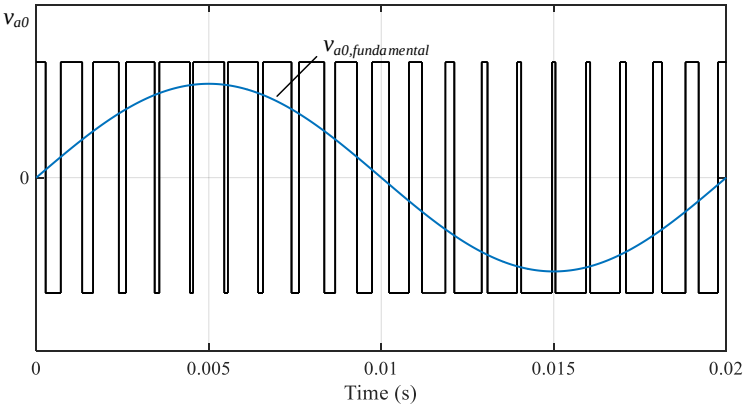


(c)

Figure 3.12: The semiconductor current i_s waveform of the Sinusoidal-iTCM control; (a) i_s under full load condition P=100%; (b) i_s under part load condition P=50%; (c) i_s under zero load condition P=0; (Taking just one-phase and few switching periods in one positive half main-frequency period as illustration)



(a)



(b)

Figure 3.13: SPWM; (a) Control signal and reference signal; (b) Output voltage of phase a v_{a0} and its fundamental component;(Taking f_{sw}=1000Hz as illustration)

SINUSOIDAL PWM

In the SPWM modulation, a sinusoidal reference signal v_{ref} is compared with a triangular wave v_{tri} to generate gate signals. The reference signal v_{ref} is a sinusoidal wave, of which the amplitude and frequency are the modulation index M and the grid frequency (50Hz) respectively. The frequency of the comparative triangular wave is f_{sw}, which is much larger than 50Hz. Normally, the triangular wave is symmetric, and its signal value of from -1 to 1.

The waveform of phase A is shown in Figure 3.13. When $v_{ref} > v_{tri}$, the upper switch is on while the lower switch is off. Phase A is connected to the positive DC bus. When $v_{ref} < v_{tri}$, the upper switch is off while the lower switch is on. Phase A is connected to

the positive DC bus. Thus, the voltage of phase A (v_{a0}) is shown in Figure 3.13(b).

In three phases, three sinusoidal reference waves ($v_{ref,a}$, $v_{ref,b}$, and $v_{ref,c}$) is expressed as:

$$v_{ref,a}(t) = M\sin(\omega t) \tag{3.61}$$

$$v_{ref,b}(t) = M\sin(\omega t - 2\pi/3) \tag{3.62}$$

$$v_{ref,c}(t) = M\sin(\omega t + 2\pi/3) \tag{3.63}$$

where M is the aforementioned modulation index. These three reference signals are compared with three triangular waves, of which the switching frequency is $f_{sw,a}$, $f_{sw,b}$ and $f_{sw,c}$ respectively.

The fundamental frequency component (the blue line shown in Figure3.13(b)) of the output voltage is:

$$(\hat{V}_{a0})_1 = M\frac{V_{dc}}{2} \qquad \text{if } M \le 1 \tag{3.64}$$

THIRD-HARMONIC INJECTION PWM

SPWM is simple to implement but the DC link voltage is not fully occupied. However, the maximum modulation index can be increased by adding a common mode third-harmonic component. This common mode component will not affect the grid side line voltage, since it will be cancelled between phases. The reference voltage becomes:

$$v_{ref,a+3}(t) = M\sin(\omega t) + M_3\sin(3\omega t) \tag{3.65}$$

$$v_{ref,b+3}(t) = M\sin(\omega t - 2\pi/3) + M_3\sin(3\omega t) \tag{3.66}$$

$$v_{ref,c+3}(t) = M\sin(\omega t + 2\pi/3) + M_3\sin(3\omega t) \tag{3.67}$$

The third-harmonic component will not influence v_{ref} when $\omega t = 2k\pi/6$ because sin(3(2k)π/6)=0 for all integer k.

$$\frac{dv_{ref,a+3}(t)}{d\omega t} = M\cos\omega t + 3M_3\cos 3\omega t = 0 \tag{3.68}$$

which for k=1 and $\omega t = \pi/3$, $M_3 = M/6$.

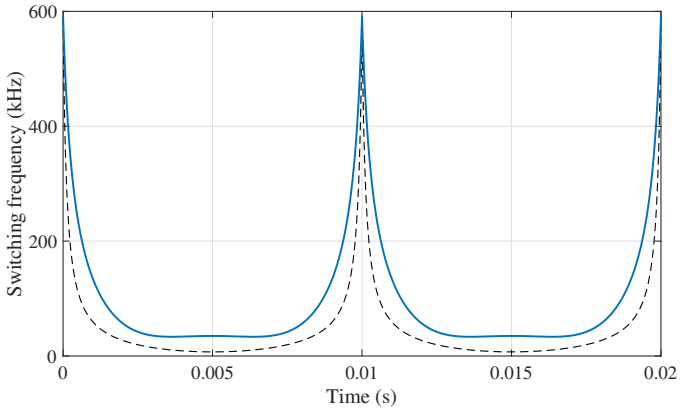
Then, the maximum modulation index becomes:

$$|v_{ref,b+3}(t)| = |M\sin(\omega t) + \frac{M}{6}\sin(3\omega t)| = 1 \tag{3.69}$$

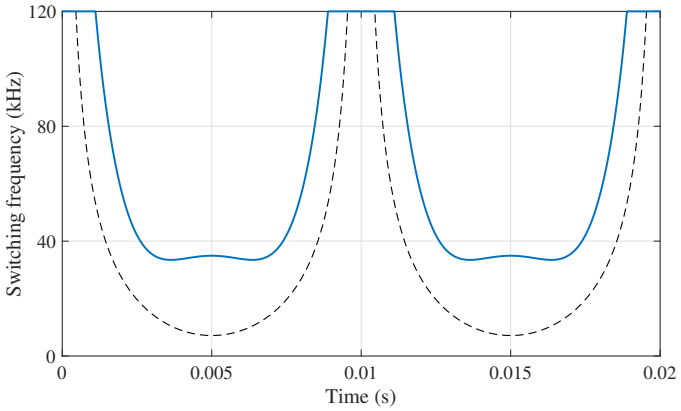
which occurs when $M = 2/\sqrt{3} = 1.15$. The modulation index M can be increased by 15% without going to over-modulation region.

For THIPWM in the iTCM control, only the switching frequency has to be adjusted to obtain the same current waveform. Equation 3.22 3.23 and 3.24 are modified as:

$$\begin{aligned} f_{sw,a} = &\frac{V_{dc}}{8L}\frac{1}{36\,(I_{zvs} + \hat{i}_{ac}|\sin(\omega t)|)}[36 - 36M^2\sin(\omega t)^2 \\ &- M^2\sin(3\omega t)^2 - 12M^2\sin(\omega t)\sin(3\omega t)] \end{aligned} \tag{3.70}$$



(a)



(b)

Figure 3.14: (a) The switching frequency of the iTCM control with third-harmonic injection PWM; (b) The switching frequency of the iTCM control with third-harmonic injection PWM (maximum 120kHz limitation); (The dash line is the switching frequency of the iTCM control with SPWM)

$$f_{\mathrm{sw,b}} = \frac{V_{\mathrm{dc}}}{8L} \frac{1}{36\,(I_{\mathrm{zvs}} + \hat{i}_{\mathrm{ac}}|\sin(\omega t - 2\pi/3)|)} [36 - 36M^2 \sin(\omega t - 2\pi/3)^2 - M^2 \sin(3\omega t - 2\pi)^2 - 12M^2 \sin(\omega t - 2\pi/3)\sin(3\omega t - 2\pi)] \tag{3.71}$$

$$f_{\mathrm{sw,c}} = \frac{V_{\mathrm{dc}}}{8L} \frac{1}{36\,(I_{\mathrm{zvs}} + \hat{i}_{\mathrm{ac}}|\sin(\omega t + 2\pi/3)|)} [36 - 36M^2 \sin(\omega t + 2\pi/3)^2 - M^2 \sin(3\omega t + 2\pi)^2 - 12M^2 \sin(\omega t + 2\pi/3)\sin(3\omega t + 2\pi)] \tag{3.72}$$

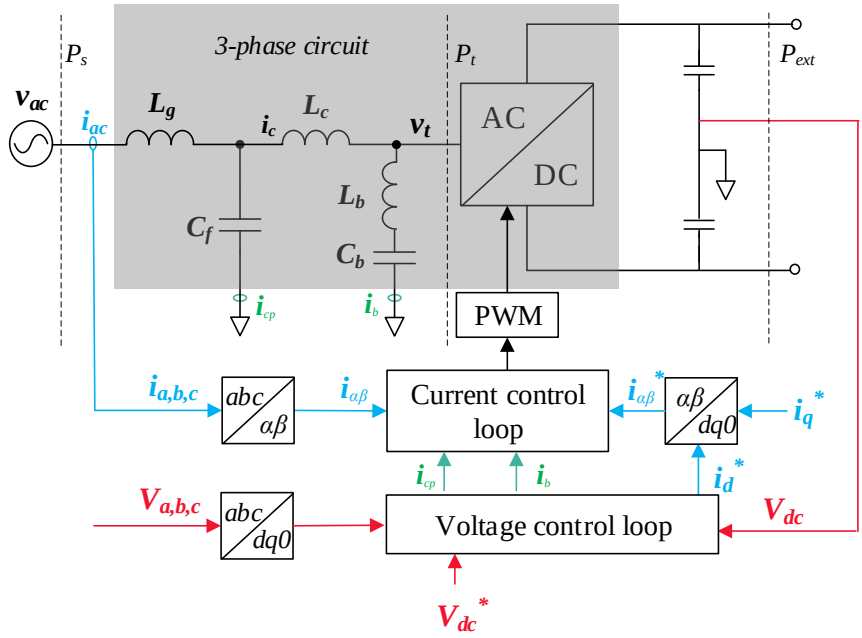


Figure 3.15: Control block diagram of the iTCM three-phase AC-DC PFC converter

The waveform of the switching frequency under THIPWM is shown in Figure 3.14. The current waveform keeps the same, as shown in Figure 3.4 and 3.10. ZVS turn-on is still achieved.

3.4. CLOSE-LOOP CONTROL

The close-loop control of the iTCM control is not discussed and implemented in the previous research. Resonance of the added LC branch would cause instability problem when merged with the LC input filter. In [22], only passive damping method (adding large resistors) is applied to suppress the LC branch resonances. This method is simple and reliable but at the cost of extra high losses, weight and volume. Thus, an active damping method must be developed to stabilize the system.

The control diagram of the three-phase iTCM PFC converter is shown in Figure 3.15. The close-loop control consists of an outer voltage loop and an inner current loop. The capacitor current feedback active damping method is also implemented to stabilize the system.

3.4.1. CURRENT CONTROL LOOP

The dynamic of the AC-side LCL filter is:

$$L_c L_g C_f \frac{d^3 i_{ac}}{dt^3} + L_c \frac{d i_{ac}}{dt} + L_g \frac{d i_{ac}}{dt} - L_c C_f \frac{d^2 v_{ac}}{dt^2} = v_{ac} - v_t \tag{3.73}$$

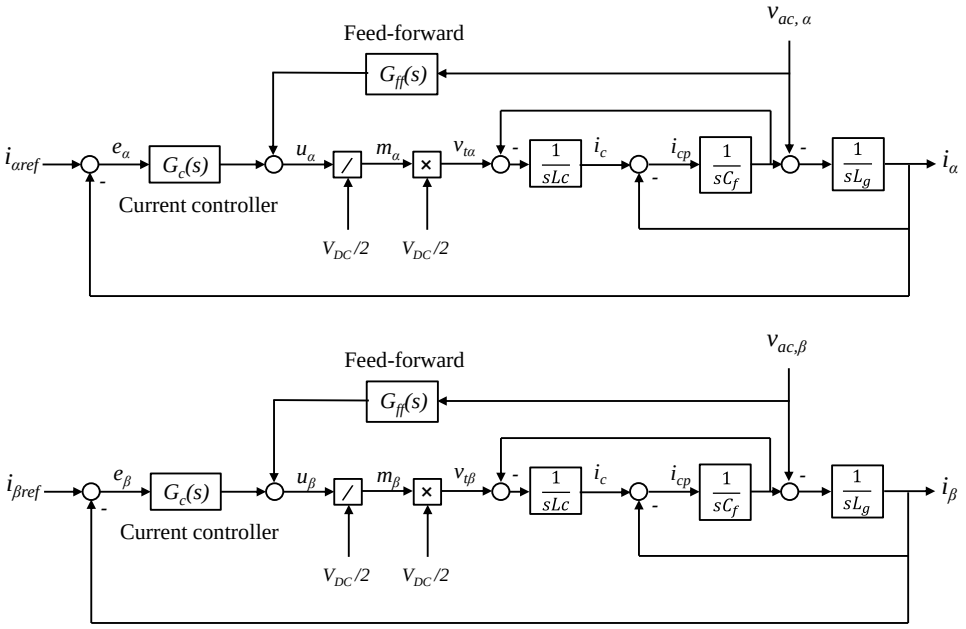


Figure 3.16: The current-loop control block diagram in the $\alpha\beta$ frame of the iTCM three-phase AC-DC PFC converter

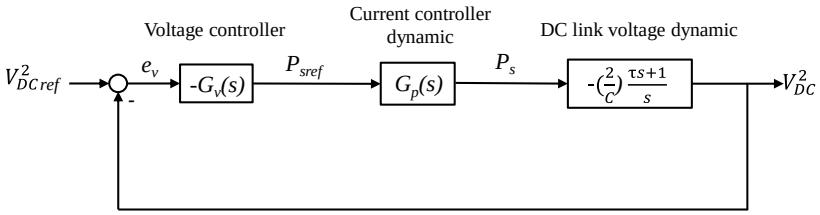


Figure 3.17: The DC link voltage-loop control block diagram of the iTCM three-phase AC-DC PFC converter

The grid-side current can be expressed as:

$$i_{\mathrm{ac}} = \frac{1}{s^3 L_{\mathrm{g}} L_{\mathrm{c}} C_{\mathrm{f}} + sL_{\mathrm{g}} + sL_{\mathrm{c}}} v_{\mathrm{t}} - \frac{s^3 L_{\mathrm{c}} C_{\mathrm{f}} + 1}{s^2 L_{\mathrm{q}} L_{\mathrm{c}} C_{\mathrm{f}} + sL_{\mathrm{g}} + sL_{\mathrm{c}}} v_{\mathrm{ac}} \tag{3.74}$$

Splitting Equation 3.73 into real and imaginary part, the dynamic of $\alpha\beta$ frame becomes:

$$L_{\mathrm{c}} L_{\mathrm{g}} C_{\mathrm{f}} \frac{d^3 i_{\mathrm{ac},\alpha}}{dt^3} + L_{\mathrm{c}} \frac{d i_{\mathrm{ac},\alpha}}{dt} + L_{\mathrm{g}} \frac{d i_{\mathrm{ac},\alpha}}{dt} - L_{\mathrm{c}} C_{\mathrm{f}} \frac{d^2 v_{\mathrm{ac},\alpha}}{dt^2} = v_{\mathrm{ac},\alpha} - v_{\mathrm{t}\alpha} \tag{3.75}$$

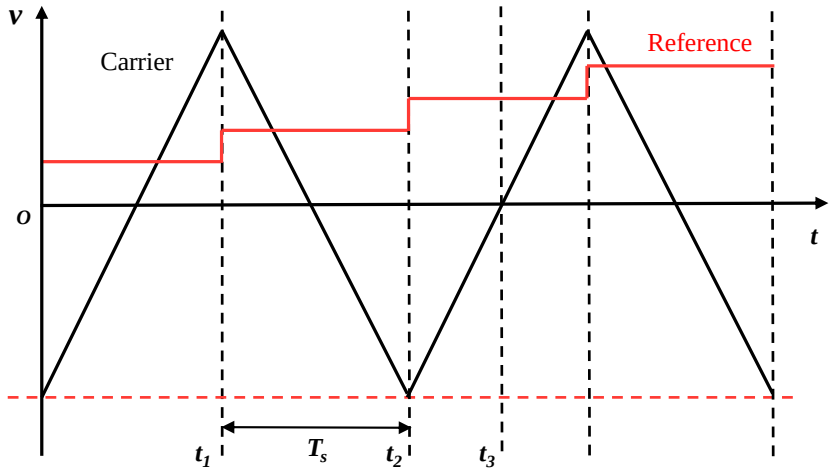


Figure 3.18: Computation and PWM delays in the digital control

$$L_c L_g C_f \frac{d^3 i_{ac,\beta}}{dt^3} + L_c \frac{d i_{ac,\beta}}{dt} + L_g \frac{d i_{ac,\beta}}{dt} - L_c C_f \frac{d^2 v_{ac}}{dt^2} = v_{ac,\beta} - v_{t\beta} \tag{3.76}$$

The control block diagram of the current-loop is shown in Figure 3.16. The α frame control and the β frame control are implemented based on Equation 3.75 and 3.76, respectively, The two frames are decoupled. Since v_{ac} is sinusoidal, $v_{ac,\alpha}$, $v_{ac,\beta}$, $i_{\alpha ref}$ and $i_{\beta ref}$ are also sinusoidal. Therefore, PR (proportional resonance) controller is applied to track the sinusoidal signal. The transfer function of PR controller $G_C(s)$ is:

$$G_c(s) = K_{pi} + \frac{2K_{ii}s}{s^2 + \omega_0^2} \tag{3.77}$$

where K_{pi}, K_{ii} are the PR controller coefficients, and ω_0 is the grid angular frequency. Since this transfer function will get a infinite gain at ω_0, a more practical controller is introduced to damp the resonant frequency, leading to:

$$G_c(s) = K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{3.78}$$

where ω_c is the cut-off frequency. In this case, the gain is not infinite but still enough for damping. Besides, the increased bandwidth will stand the grid frequency deviations.

Feed-forward compensation is used to obtain better dynamic performance of the controlled system, as shown in Figure 3.16. At the start-up instant, the output of the PR controller is zero, and the generated AC voltage starts from v_{ac} under the condition of $G_{ff}(0)$=1. Moreover, if $G_{ff}(s) \approx 1$, the dynamic of the converter system is decoupled from the AC grid system in the frequency range over which the AC system has considerable energy. Thus, the voltage difference is fully determined by the PR controller.

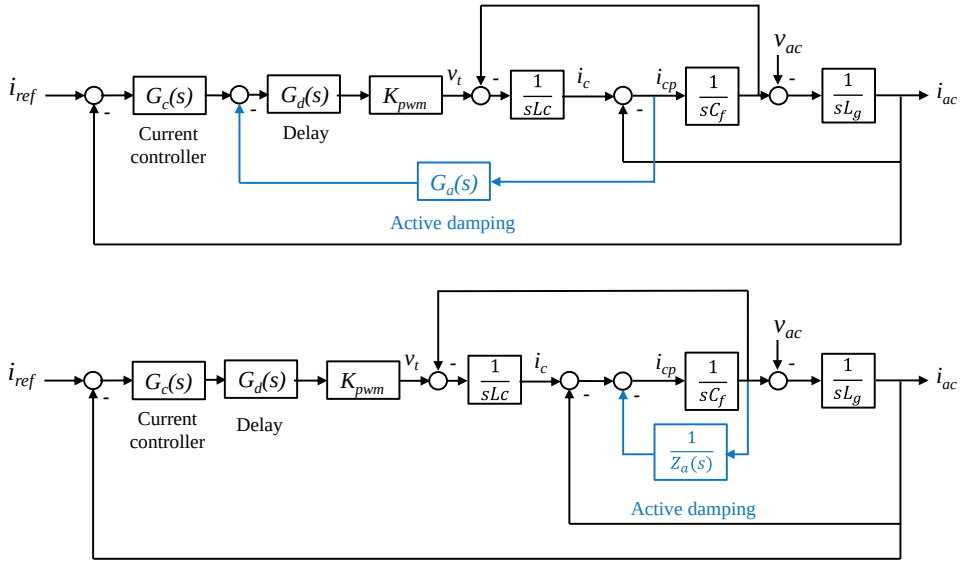


Figure 3.19: Block illustration of the capacitor current feedback active damping method

3.4.2. VOLTAGE CONTROL LOOP

Since the DC side is not connected to a voltage source in real applications, the power port needs regulated DC link voltage. The dynamic of the DC voltage is derived in [29], which is expressed as:

$$\frac{dV_{DC}^2}{dt} = \frac{2}{C}P_{ext} - \frac{2}{C}\left[P_s + \left(\frac{2L_cP_{s0}}{3\hat{v}_{ac}^2}\right)\frac{dP_s}{dt}\right] + \frac{2}{C}\left[\left(\frac{2L_cQ_{s0}}{3\hat{v}_{ac}^2}\right)\frac{dQ_s}{dt}\right] \tag{3.79}$$

where C is the DC link capacitor, P_s and Q_s denote the real power and the reactive power of the AC side, P_{ext} is the DC side external power, P_{s0}, Q_{s0} and P_{ext0} are the steady-state value by replacing all the derivative component to zero.

In the PFC converter, the reactive power Q_s is set to zero. The transfer function of V_{dc} and P_s becomes:

$$G_v(s) = -\left(\frac{2}{C}\right)\frac{\tau s + 1}{s} \tag{3.80}$$

where the time constant τ is

$$\tau = \frac{2L_cP_{s0}}{3\hat{v}_{ac}^2} = \frac{2LP_{ext0}}{3\hat{v}_{ac}^2}. \tag{3.81}$$

The control diagram of the voltage control loop is shown in Figure 3.17. A PI controller is used to control the DC link voltage, of which the transfer function is:

$$G_v(s) = K_{pv} + \frac{K_{iv}}{s} \tag{3.82}$$

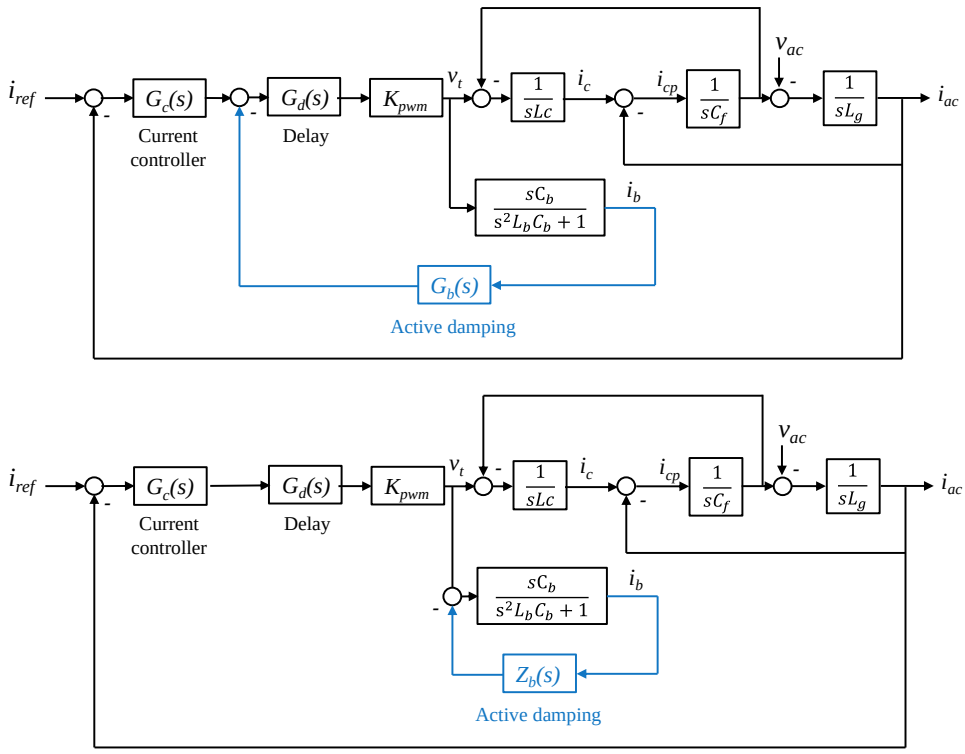


Figure 3.20: Block illustration of the LC branch current feedback active damping method

where K_{pv}, K_{iv} are the PI controller coefficients.

Normally, the bandwidth of the voltage controller should be designed adequately larger than the inner current (power) controller, so the transfer function $G_p(s)$ can be considered as 1 in the voltage control loop.

3.4.3. CAPACITOR CURRENT FEEDBACK

The capacitor-current-feedback control is one of the active damping methods used for damping the input LCL filter. The capacitor current is fed back to the current loop by a proportional gain, which can be considered as a virtual resistor parallel to the capacitor [30] [31] [32].

The digital control contains two delays - computation delay and PWM delay. Assuming the digital control is asymmetric regular sampled, the current i_g is sampled at the beginning and in the middle of each switching cycle, as shown in Figure 3.18. The sampling frequency f_s is twice of the switching frequency f_{sw}. Thus, the samping time T_s can be expressed as:

$$T_s = 0.5\ T_{sw} \tag{3.83}$$

The current is sampled at time t_1, and the PWM reference is updated after one sampling time T_s at t_2. This computation delay is expressed as:

$$G_{d0}(s) = e^{-sT_s} \tag{3.84}$$

After the reference is updated, it will be held on and compared to the triangular wave, and then generate duty cycle at t_3. This PWM delay is maximum half sampling time, which can be expressed as (assumed to be half sampling time in this case):

$$G_h(s) = \frac{1 - e^{-sT_s}}{s} \approx T_s e^{-0.5sT_s} \tag{3.85}$$

The total time delay $G_d(s)$ can be expressed as:

$$G_d(s) = G_{d0}(s) + G_h(s) = e^{-1.5sT_s} \tag{3.86}$$

The block diagram of current control loop with capacitor current feedback is shown in Figure 3.19. The capacitor current is fed to the loop via an active damping coefficient. Due to the time delay, it can be seen as an impedance $Z_a(s)$ parallel to the capacitor C_f as shown in Figure 3.21. The active damping transfer function is often chosen as constant value:

$$G_a(s) = K_a \tag{3.87}$$

Assuming that the capacitor current is synchronous sampled, the virtual impedance is:

$$Z_a(s) = \frac{L_c}{K_a K_{pwm} C_f} e^{1.5sT_s} \triangleq R_a e^{1.5sT_s} \tag{3.88}$$

where R_a is the equivalent resistance.

Taking $s = j\omega$ into Equation 3.88, it becomes:

$$Z_a(s) = R_d \left[\cos(1.5\omega T_s) + j\sin(1.5\omega T_s)\right] =\triangleq R_{eq}(\omega) // jX_{eq}(\omega) \tag{3.89}$$

where

$$R_{eq}(\omega) = \frac{R_a}{\cos(1.5\omega T_s)} \tag{3.90}$$

$$X_{eq}(\omega) = \frac{R_a}{\sin(1.5\omega T_s)} \tag{3.91}$$

The real part $R_{eq}(\omega)$, which is the resistor part, becomes negative when the resonance frequency is between $\frac{1}{6}f_s$ and $\frac{1}{2}f_s$. However, the sampling frequency is twice of maximum switching frequency, which is 240kHz in this case. The resonance frequency is below $\frac{1}{6}f_s$.

Applying the same method, the current i_b can be fed back to the main loop damping the LC branch resonance, as shown in Figure 3.20. The LC branch current is fed to the loop via an active damping coefficient. Due to the time delay, it can be seen as an impedance $Z_b(s)$ series to the LC branch as shown in Figure 3.21. The active damping transfer function is often chosen as constant value:

$$G_b(s) = K_b \tag{3.92}$$

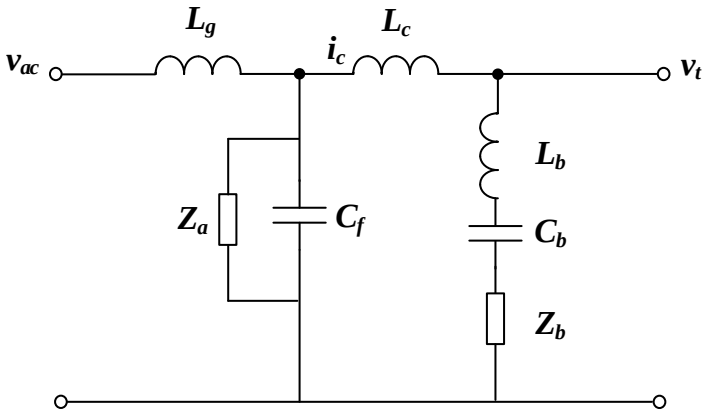


Figure 3.21: The equivalent circuit of the current feedback active damping method

Considering the time delay, the virtual impedance is:

$$Z_{\mathrm{b}}(s) = K_{\mathrm{b}} K_{\mathrm{pwm}} e^{-1.5sT_s} \triangleq R_{\mathrm{b}} e^{-1.5sT_s} \tag{3.93}$$

where R_{b} is the equivalent resistance.

Taking $s = j\omega$ into Equation 3.93, it becomes:

$$Z_{\mathrm{b}}(s) = R_{\mathrm{b}} \left[\cos(1.5\omega T_{\mathrm{s}}) - j\sin(1.5\omega T_{\mathrm{s}})\right] \triangleq R_{\mathrm{eqb}}(\omega) - jX_{\mathrm{eqb}}(\omega) \tag{3.94}$$

where

$$R_{\mathrm{eqb}}(\omega) = R_b \cos(1.5\omega T_s) \tag{3.95}$$

$$X_{\mathrm{eqb}}(\omega) = R_b \sin(1.5\omega T_s) \tag{3.96}$$

4

System Loss Modeling

4.1. INTRODUCTION

In this chapter, the proposed three-phase iTCM AC-DC PFC converter is mathematically modeled. The system specification for the analytical modeling is shown in Table 4.1. The semiconductor used for modeling and further experiment is the Silicon Carbide (SiC) MOSFETs (C3M0120090J [33], where four devices in parallel per switch are selected). The equivalent output capacitance C_{eq} is calculated based on Equation 3.54: $C_{eq} \approx 355\ pF$. The minimum turn-off current I_{zvs} for ensuring ZVS can be calculated by Equation 3.47, resulting in 2.05 A. To maintain a safety margin, I_{zvs} is chosen as 2.5 A.

In the following modeling and simulation, the simplest Bounded-iTCM control is used. The minimum switching frequency is preset to be 20 kHz, while the maximum switching frequency is limited by 120kHz due to the practical constraint and EMI issues.

By choosing a random r between 0-200%, the equivalent boost inductance L that needed for ZVS can be calculated by Equation 3.5, 3.29 and 3.30, which is 67.62 μH. The parameter r will be lately determined by the inductor modeling results. SPWM is adopted in this paper for both analytical modeling and simulation.

4.2. SEMICONDUCTOR LOSS MODELING

In the semiconductor loss modeling, the voltage in every switching cycle is assumed to be constant since the switching frequency f_{sw} is larger enough compared to main frequency f_0 [34].

4.2.1. SWITCHING LOSS

In general, the switching loss of the semiconductor can be expressed as:

$$P_{sw} = \frac{1}{2\pi}\int_0^{2\pi} f_{sw}(\omega t) E_{sw}\left(V_{sw}, I_{sw}(\omega t)\right) \mathrm{d}\omega t \tag{4.1}$$

where E_{sw} is the switching energy (it can be turn-on energy, turn-off energy or diode reverse recovery energy), and it is a function of the switching voltage V_{sw} and switching current I_{sw}. The temperature rising is not considered in the analytical modeling.

The switching energy E_{sw} (turn-on, turn-off or diode reverse recovery) of MOSFETs is expressed as:

$$E_{sw}\left(I_{sw}\right) = a + b|I_{sw}| + c|I_{sw}|^2 \tag{4.2}$$

where a, b and c are the polynomial coefficients of the switching energy [34]. For the selected MOSFET, the polynomial coefficients are shown in Table 4.2. It is extracted from the measured switching energy results for the same device in [34] by double-pulse test, which is more accurate than the datasheet.

In the iTCM control, the switching frequency f_{sw} and I_{sw} are both variables. Considering the paralleled four devices, the switching loss P_{sw} of each paralleled MOSFET can be expressed as [35]:

$$P_{sw} = \frac{V_{dc}}{2\pi V_b}\int_0^{2\pi} f_{sw}(\omega t)\ E_{sw}(I_{sw}(\omega t)/N_p) \mathrm{d}\omega t \tag{4.3}$$

where V_b is the reference voltage for measuring the switching energy that can be obtained from the datasheet, and N_p is the number of MOSFETs in parallel used per switch.

Table 4.1: System specifications

PARAMETER	V_{ac}	P (3ϕ)	f_0	V_{dc}	M
VALUE	230 V rms	11 kW	50 Hz	800 V	0.8132

Table 4.2: Polynomial coefficient of switching energy for SiC MOSFET C3M0120090J (per device) tested under V_b = 600 V

Coefficient	Turn-on Energy (E_{on}+E_{rr})	Turn-off Energy (E_{off})
a (μJ/A^2)	0.074	0.53
b (μJ/A)	10.43	5.36
c (μJ)	18.84	1.18

In the iTCM control, turn-on switching loss is eliminated by the reversal current I_{zvs}, so only the turn-off loss should be considered.

$$P_{sw,off} = \frac{V_{dc}}{2\pi V_b} \int_0^{2\pi} f_{sw}(\omega t)\, E_{sw,off}(I_{sw,off}(\omega t)/N_p) \mathrm{d}\omega t \tag{4.4}$$

4.2.2. CONDUCTION LOSS

The conduction loss P_{con} of each paralleled MOSFET is calculated as [36]:

$$P_{con} = R_{ds}(I_{s,rms}/N_p)^2 \tag{4.5}$$

where R_{ds} is the equivalent on-state resistance of each paralleled MOSFETs, $I_{s,rms}$ is the RMS value of current i_s flowing through the active switch. R_{ds} can be obtained from the MOSFET datasheet.

the RMS value of the semiconductor current during one switching period $i_{s,rms}$ can be calculated by [37]:

$$i^2_{s,rms} = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_s^2(t) \mathrm{d}t \tag{4.6}$$

Considering the triangular shape, Equation 4.6 can be rearranged as:

$$i^2_{s,rms}(t) = \frac{1}{3}\left[{i^+_{s,env}}^2(t) + i^+_{s,env}(t) i^-_{s,env}(t) + {i^-_{s,env}}^2(t)\right] \tag{4.7}$$

where $i^+_{s,env}(t)$ and $i^-_{s,env}(t)$ are the upper envelope and the lower envelope, respectively, which can be expressed as:

$$i^+_{s,env}(t) = |I_{zvs}| + 2\hat{i}_{ac} \sin(\omega t) \tag{4.8}$$

$$i^-_{s,env}(t) = -|I_{zvs}| \tag{4.9}$$

Thereafter, the RMS current $I_{s,rms}$ can be calculated by integrating Equation 4.7 over one main-frequency period [35], resulting in:

$$I_{s,rms} = \sqrt{\frac{1}{3}\left(2\,\hat{i}_{ac}^2 + \frac{4}{\pi}\,\hat{i}_{ac}\,I_{zvs} + I_{zvs}^2\right)} \tag{4.10}$$

If the I_{zvs}=0, the rms current is $\sqrt{\frac{2}{3}}\hat{i}_{ac}$. Compared to CCM, the conduction loss in the iTCM mode is increased around 33% if the current ripple in CCM is neglected. Due to the existence of I_{zvs} as well as the frequency limitation, the conduction loss is increased even further.

4.3. INDUCTOR LOSS MODELING

The modeling of the inductor loss is equally vital as semiconductor loss in the iTCM control since the large current ripple would cause saturation problems and higher inductor losses.

4.3.1. CORE LOSS

The core loss is mainly comprised of three parts: hysteresis loss, eddy-current loss and residual loss. Hysteresis loss is linear with the frequency. Eddy-current loss is caused by the changing magnetic field, and it depends on the geometry and the conductivity. Residual loss is due to the movement of the thermal equilibrium, especially when the frequency is relatively high.

The basic approach for the core loss modeling is the Steinmetz Equation (SE):

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{4.11}$$

where P_v is the average core loss per unit volume, f is the current frequency, $\hat{B}$ is the maximum flux density, k, α and β are the so-called Steinmetz coefficients which is material dependent and can be derived from the core datasheet [38].

However, the SE method is not valid for non-sinusoidal flux waveforms, and DC bias is not considered. Moreover, it is only valid in a limited frequency range. Thus, the improved Generalized Steinmetz Equation (iGSE) is proposed to calculate the core loss of any flux waveforms, which is expressed as [39]:

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha} dt \tag{4.12}$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{4.13}$$

and ΔB denotes the peak-to-peak amplitude flux density, k, α, β are the same parameters in the Steinmetz Equation. Note that ΔB will vary in time according to the evolution of the input voltage which will cause different current ripple values. Thus, the instant loss calculated in each switching period is summed up, and then averaged in a grid time period.

In power electronic applications, especially in the three-phase AC-DC converter, the flux waveform of the boost inductor is often made up of a high-frequency (switching frequency) component and a low-frequency (main frequency) component. Referring to B-H curve, it shows a major loop and some minor loops. The major loop denotes the high-frequency component, while minor loops denote the low-frequency components.

The flux waveform can generally be divided into two parts: rising and falling parts. The rising part represents the path from the lowest point to the highest point, while the falling part represents the path from the highest to the lowest. Since the analysis of the rising and falling parts are the same, the rising process is taken as an example. During the rising part, there are many minor loops, which means the scope can be either positive or negative, but it is rising in general [40]. The flow chart of the core loss calculation considering the splitting of the minor loop is shown in Figure 4.1. Thus, the loss of the major and minor loops can be calculated independently. By adding all loops loss together, the total core loss can be obtained by [41]:

$$P_{\text{tot}} = \sum_i P_{\text{i}} \frac{T_{\text{i}}}{T} \tag{4.14}$$

where P_{i} is the loss calculated by Equation 4.12 of each loop, T_{i} is the time of each loop, and T is the main period.

This iGSE calculation method can be used in any flux waveform rather than only sinusoidal wave. Moreover, the coefficients from SE can also be used without further adjustment.

4.3.2. WINDING LOSS

The other main part of inductor losses is the winding loss, which is the ohmic loss caused by eddy current. The two main components of winding loss are skin effect loss and proximity effect loss. The skin effect is caused by self-induced eddy current, while the proximity effect is caused by external-induced eddy current.

SKIN EFFECT

The AC current flows through the conductor will induce an alternating magnetic field according to Ampere's law:

$$\oint \boldsymbol{H} \mathrm{d}\boldsymbol{l} = \iint \boldsymbol{J} \mathrm{d}\boldsymbol{A} \tag{4.15}$$

where H is the magnetic field strength, J is the current density.

According to Faraday's law, an inside electric field will be induced due to the changing magnetic field, which then induces current. The induced current will cancel out the original current in the center of the conductor while enhancing it on the surface of the inductor. Thus, most current flows close to the conductor's surface, and the final current density decreases from the surface to the center [41].

$$\oint \boldsymbol{E} \mathrm{d}\boldsymbol{l} = -\frac{\mathrm{d}}{\mathrm{d}t} \iint \boldsymbol{B} \mathrm{d}\boldsymbol{A} \tag{4.16}$$

where E is the electric field strength, B is the flux density,

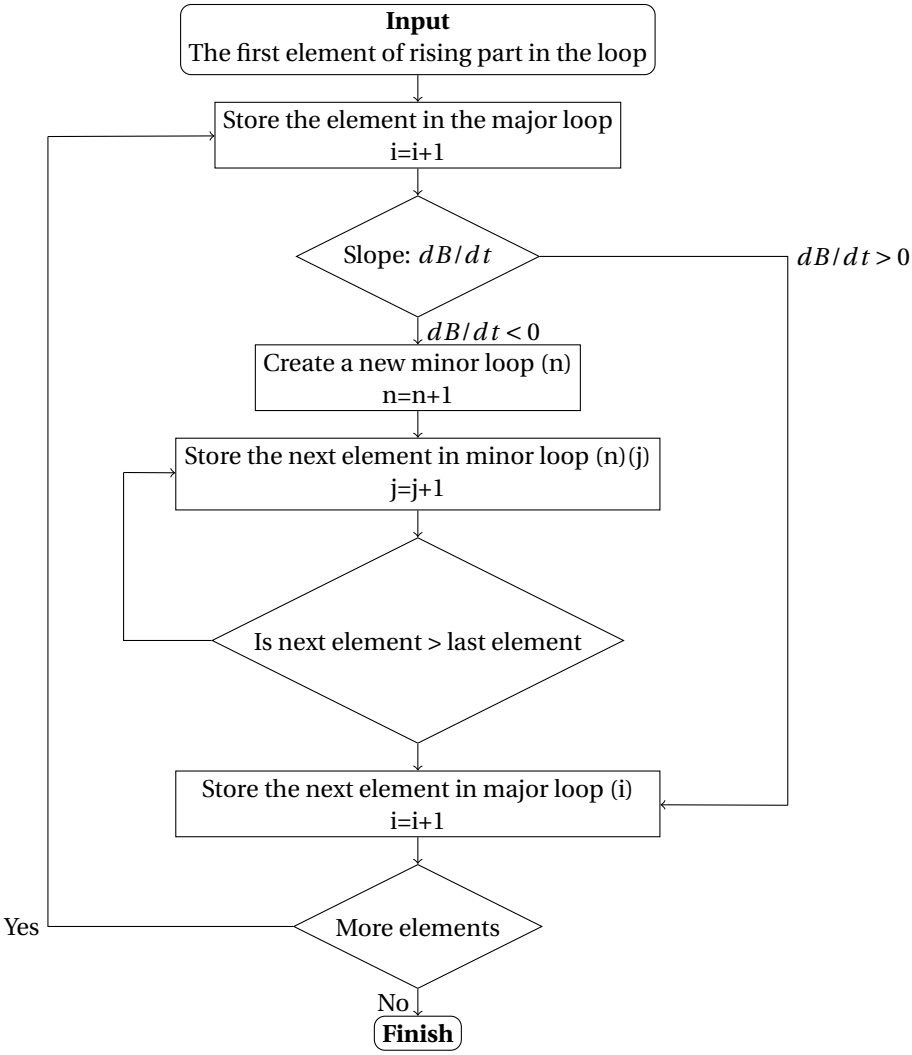


Figure 4.1: Flow chart of the core loss calculation considering the minor loop splitting (Taking the rising part as illustration)

The skin depth is defined as the distance from the surface of the conductor to where the current density decreases to its 1/e, which can be expressed as:

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \tag{4.17}$$

where σ denotes the conductivity of the conductor, μ_0 denotes the permeability of vacuum, f denotes the frequency of the current.

The skin effect loss P_S of per unit length solid round conductors is:

$$P_S = F_{R/S}(f) \cdot R_{DC} \cdot \hat{I}^2 \tag{4.18}$$

where $\hat{I}$ is the maximum current flowing through the conductor, R_{DC} is the DC resistance of the conductor per unit length, which can be expressed as:

$$R_{DC} = \frac{4}{\sigma \pi d^2} \tag{4.19}$$

where d is the diameter of the conductor.

$F_{R/S}$ is the ratio between DC and AC resistance, which can be calculated by:

$$F_R = \frac{\xi}{4\sqrt{2}} \left(\frac{\mathrm{ber}_0(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{ber}_0(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} - \frac{\mathrm{bei}_0(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{bei}_0(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_1(\xi)^2 + \mathrm{bei}_1(\xi)^2} \right) \tag{4.20}$$

where ξ can be calculated by:

$$\xi = \frac{d}{\sqrt{2}\delta} \tag{4.21}$$

For litz wire with a number of strand n, the skin effect loss calculation can be adapted to:

$$P_{S,\mathrm{Litz}} = n\, F_{R/S}(f)\, R_{DC} \left(\frac{\hat{I}}{n} \right)^2 \tag{4.22}$$

PROXIMITY EFFECT

The proximity effect of one conductor is caused by the changing magnetic field of the neighbouring conductors. It will induce external eddy current to the conductor. This would cause current crowding of the original conductor.

The proximity effect loss P_P can be calculated as:

$$P_P = R_{DC} \cdot G_{R/S}(f) \cdot \hat{H}_e^2 \tag{4.23}$$

where $\hat{H}_e$ is the magnitude of the external magnetic field, $G_{R/S}(f)$ is calculated by:

$$G_R = -\frac{\xi \pi^2 d^2}{2\sqrt{2}} \left(\frac{\mathrm{ber}_2(\xi)\,\mathrm{ber}_1(\xi) + \mathrm{ber}_2(\xi)\,\mathrm{bei}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} + \frac{\mathrm{bei}_2(\xi)\,\mathrm{bei}_1(\xi) - \mathrm{bei}_2(\xi)\,\mathrm{ber}_1(\xi)}{\mathrm{ber}_0(\xi)^2 + \mathrm{bei}_0(\xi)^2} \right) \tag{4.24}$$

For the litz wire, the magnetic field consists of external and internal parts. The external magnetic field $\hat{H}_e$ is generated by other neighbouring conductors, while the internal

magnetic field $\hat{H}_\mathrm{i}$ is generated by the neighbouring strands within the conductor [41]. The proximity effect loss calculation is adapted to:

$$P_\mathrm{P,Litz} = n\, G_\mathrm{R/S}(f)\, R_\mathrm{DC} \left(\hat{H}_\mathrm{e}^2 + \hat{H}_\mathrm{i}^2\right) \tag{4.25}$$

Finally, the winding loss can be obtained by summing up skin effect loss P_S and proximity loss P_P.

5

MAGNETIC DESIGN

5.1. INTRODUCTION

To obtain a compact, lightweight and high-efficient PFC converter design for OBCs, the inductor L_g, L_c and L_b should be optimally designed to obtain a minimum inductor loss as well as volume and weight.

The most commonly used cores are powder iron core and ferrite core. Powder iron core has a high saturation flux density, low hysteresis and eddy current losses and excellent inductance stability under both DC and AC conditions, which is suitable for power inductors as input filters. Ferrite core has high permeability and comparatively low power losses at high frequency, which is desirable in designing the inductor in the LC branch [22][41]. Litz wire with thin strand diameter, which highly eliminates skin effect losses, is suitable for high-frequency applications. However, litz wire typically has a low filling factor (chosen as 0.8 in the following design), which is not desirable for a high-frequency inductor design. Thus, solid copper wire with a high filling factor is better for the L_g design.

5.2. INDUCTOR DESIGN

As discussed before, L_g and L_c are designed by powder iron core with solid wire, while L_b is designed by ferrite core with litz wire. For the chosen core from Magnetics, the dimension and material data can be obtained from the datasheet [42] [43]. Based on the dimension data and system specifications shown in Table 4.1, the number of turns, reluctance, airgap length and wire diameter can be determined.

5.2.1. NUMBER OF TURNS

Powder iron core has a relatively high saturation flux density (B_{sat}) of up to 1.2 T, so the ungapped Toroid powder core is chosen for L_c and L_g design. The number of turns N is calculated by:

$$N = \sqrt{\frac{L l_e}{\mu_0 \mu_r A_e}} \tag{5.1}$$

where L is the inductance value, l_e is the flux path length, A_e is the cross-sectional area of the chosen core, μ_0 is the air permeability, and μ_r is the relative permeability.

Ferrite core has lower saturation flux density (B_{sat}< 0.5 T), so the gapped core (EE, UU) is a necessity for L_b design. The number of turns is determined by the maximum saturation flux density B_{sat} as:

$$N = \frac{L I_{max}}{0.8 B_{sat} A_e} \tag{5.2}$$

where I_{max} is the maximum current flowing through the inductor L, and 0.8 is the safety coefficient to avoid saturation.

$$L = \frac{N^2}{R} \tag{5.3}$$

where R is the total reluctance of the magnetic circuit, which consists of the core reluctance R_c and the air gap reluctance R_g.

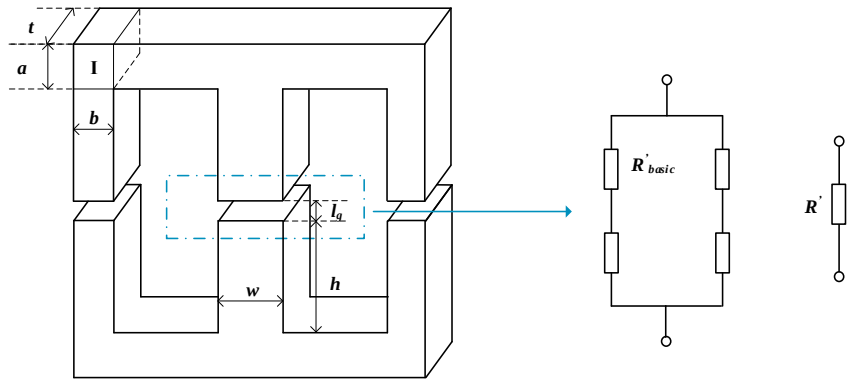


Figure 5.1: A more accurate modeling of calculation reluctance (Taking EE core as illustration)

5.2.2. RELUCTANCE

The core reluctance R_c is calculated as:

$$R_c = \frac{l_e}{\mu_0 \mu_r A_e} \tag{5.4}$$

When calculating the reluctance of the cross-sectional area, the flux path length l_e is adapted to:

$$l_e = \frac{2\pi}{4} \cdot \frac{(a+b)}{4} = \frac{\pi}{8}(a+b) \tag{5.5}$$

The cross-sectional area A_e is adapted to:

$$A_e = \frac{t(a+b)}{2} \tag{5.6}$$

A general method of calculating the air gap reluctance R_g is expressed as:

$$R_g = \frac{l_g}{\mu_0 A_g} \tag{5.7}$$

where l_g is the air gap length, A_g is the cross section of air gap.

However, this air gap reluctance calculation method does not consider the fringing flux, so it is only valid for relatively small air gap length. An accurate air gap calculation is proposed in [44], which is used in this modeling. In EE or UU core, the dimension of the cross-section is square. The air gap reluctance calculation by only considering the 2D dimension is shown in Figure 5.1. For this type of air gap, the equivalent model can be divided into four reluctance R'_{basic}, which are calculated by:

$$R'_{basic} = \frac{1}{\mu_0 \left[\frac{w}{l_g} + \frac{2}{\pi} \left(1 + \ln \frac{\pi h}{2 l_g} \right) \right]} \tag{5.8}$$

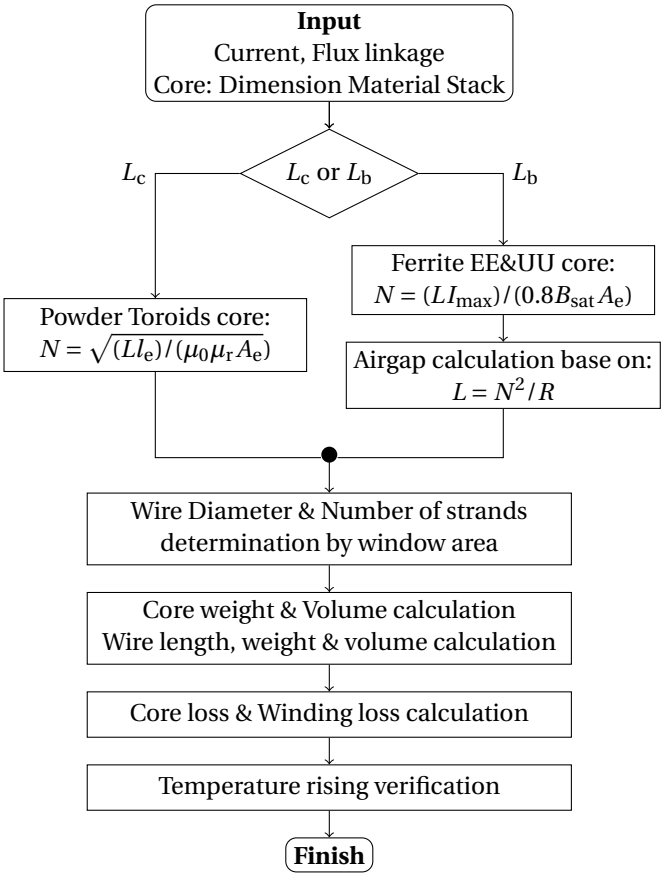


Figure 5.2: Inductor design procedure of the three-phase iTCM PFC converter. The core material is chosen from Magnetics. Core dimension, material and number of stacks are swept to get an optimal result

Considering the 3D case, the fringing factor is defined as the factor that describes how much reluctance decreases caused by fringing effect. The fringing factor of the y-axis is calculated as:

$$\sigma_y = \frac{R'}{\frac{l_g}{\mu_0 b}} \tag{5.9}$$

where $\frac{a}{\mu_0 b}$ is the idea airgap reluctance by considering the fringing effect.

The fringing factor of the x-axis is calculated as:

$$\sigma_x = \frac{R'}{\frac{l_g}{\mu_0 t}} \tag{5.10}$$

Thus, the air gap reluctance can be finally calculated as:

$$R_g = \sigma_x \sigma_y \frac{l_g}{\mu_0 \cdot t \cdot b} \tag{5.11}$$

The total reluctance of the magnetic circuit can be obtained by summing up all the core and air gap reluctance. Based on the calculated total reluctance by Equation 5.3, the needed air gap length l_g of the inductor can be obtained.

5.2.3. WIRE DIAMETER

The wire diameter d is determined by the number of turns N and the window area A_w.

$$d = \sqrt{\frac{A_w}{N}} - 2d_o \tag{5.12}$$

where d_o is the isolation distance of two wires (set to 0.1mm in this case).

Since the maximum switching frequency is up to 120 kHz, so litz wire AWG #40 is chosen to minimize the skin effect loss. The diameter of single conductor d_i=0.0799 mm for AWG #40 litz wire. The number of strands n is calculated based on the window area of the selected core, considering a filling factor of 0.8 for the litz wire bundle.

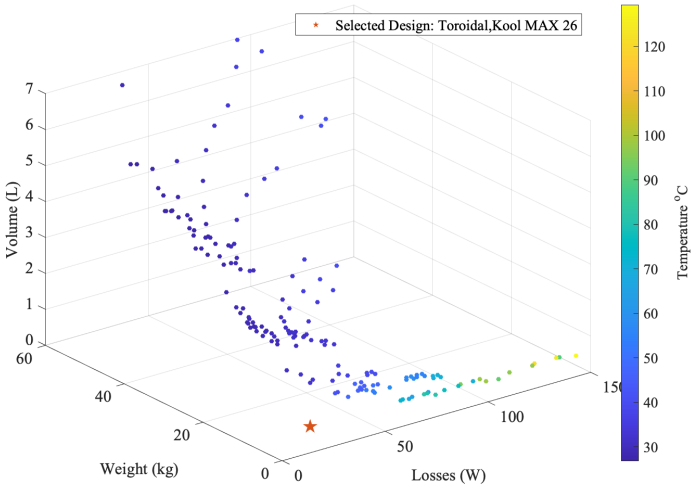
$$n = \frac{0.8d^2}{d_i^2} \tag{5.13}$$

5.2.4. TEMPERATURE RISING

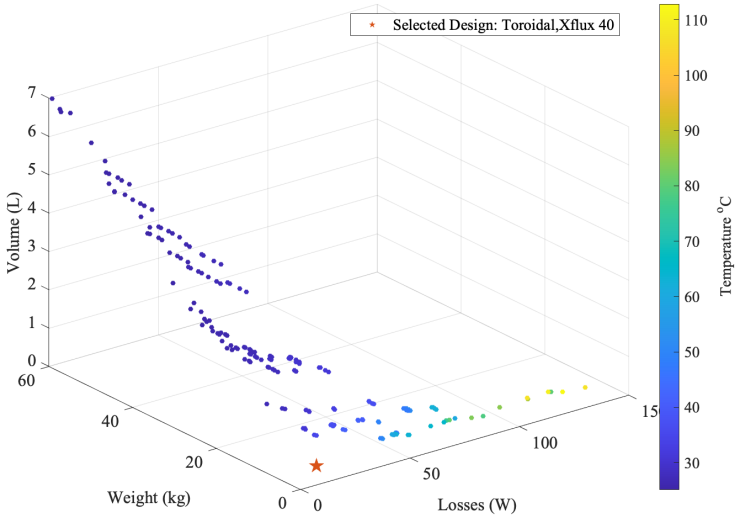
Meanwhile, the maximum temperature should be limited to an acceptable value, e.g., 80..130 °C. The temperature rising can be simply calculated as:

$$\Delta T = P_{loss} \cdot R_{sa} \tag{5.14}$$

where R_{sa} is the thermal resistance of the inductor, P_{loss} is the inductor loss that calculated in Chapter 4.



(a)



(b)

Figure 5.3: 3D Pareto plots for the merits of Volume, weight and loss for the inductor design of the studied three-phase recifier operating with iTCM (r=0.4, f_{min}=20kHz). The magnetic core dimensions, material, stacks from Magnetics are swept to derive an optimal design which is shown as star. The temperature rising of each design is shown in the color bar. Toroids powder core for L_c design with 36 material, maximum 2 stacks swept.

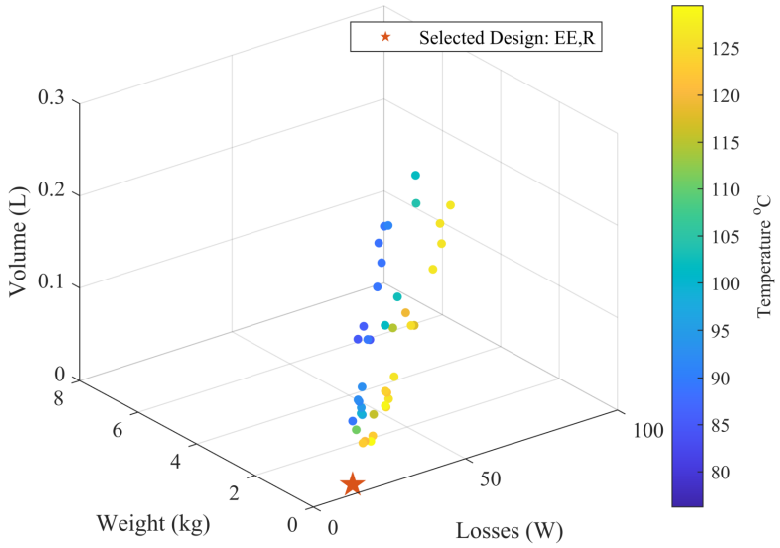


Figure 5.4: 3D Pareto plots for the merits of Volume, weight and loss for the inductor design of the studied three-phase recifier operating with iTCM (r=0.4, f_{min}=20kHz). The magnetic core dimensions, material, stacks from Magnetics are swept to derive an optimal design which is shown as star. The temperature rising of each design is shown in the color bar. EE&UU ferrite core for L_c design with 3 material (P,R,F), maximum 2 stacks swept

Table 5.1: Optimal results from Pareto plot for L_c L_g and L_b designs

f_{min}=20kHz, r=80%	L_c	L_g	L_b
Core Material	Kool MAX 26	Xflux 40	R
Core Code	'OD55337A2'	'OD55778A2'	'0R43520EC'
Core Type	Toroid	Toroid	EE
Number of Stacks	1	2	2
Number of Turns (N)	83	41	28
Airgap length(mm)	0	0	1.6
Wire	AWG #40	Solid	AWG #40
Core loss (W)	7.41	0.38	14.38
Winding loss (W)	22.65	13.64	10.02
Inductor loss (W)	30.06	14.02	24.4
Total weight (kg)	8.57	6.32	0.4131
Total volume (cm^3)	756.93	862.86	713.85

5.3. INDUCTOR DESIGN OPTIMIZATION

The inductor is always the bulkiest part of converters. In order to improve the power density of the whole system, minimization of the volume of the inductor is vital. Besides, the inductor loss take a considerable part of the total loss (especially under the TCM or iTCM control), so optimising the design of the inductor is quite important for improving efficiency [45].

The inductor design procedure is shown in Figure 5.2. All the core data used for modeling are from "Magnetics". For the toroid powder core, 18 different core dimensions, 36 core materials and a maximum of 2 stacks are scaled to seek the optimization design of the inductor. For ferrite EE and UU core, 36 core dimensions, 3 materials (R, F, P) and maximum 2 stacks are scaled.

The main goal is to design the inductor with lower loss as well as lower weight and volume. The volume/loss and weight/loss optimization results are obtained from the Pareto plot results, as summarized in Table 5.4.

The aforementioned parameter r will be determined based on the Pareto results. It is scaled from 0-100% for the inductor design optimization. As shown in Table 5.4, the inductor loss is not affected too much when $0.2 \leq r \leq 0.8$. When r is small, the value of L_c is larger, but the current flowing through L_c is closer to sinusoidal. Finally, r is selected as 0.8 to obtain a lower weight and volume of the filter. The inductance of L_c and L_b are 187.82μH and 105.68 μH, respectively. The Pareto plot for the design of L_c and L_b with $r = 0.8$ are shown in Figure 5.3(a), 5.3(b), respectively. The optimal inductor core and wire selection are summarized in Table 5.1.

5.4. COMPARISON OF CCM TCM AND ITCM

To verify the advantage of the proposed three-phase PFC converter with the iTCM control, the same models are also implemented to the CCM and the TCM control.

5.4.1. SYSTEM SPECIFICATIONS OF CCM AND TCM

The basic system specifications of CCM and TCM are the same as the iTCM control, as shown in Table 4.1.

The switching frequency range of the TCM control is from 20kHz to 591kHz. Due to the EMI and practical issues, the same Bounded-TCM control method is implemented, and the switching frequency is limited to 120kHz as well. To fulfill the ZVS turn-on in the TCM control, the value of the boost inductor L_c can be calculated by Equation 3.29 by choosing $r = 2$, which is 67.63μH for an 11kW system.

The CCM control switching frequency is 20kHz and 97.6kHz for one low-frequency case and one high-frequency case. The value 97.6kHz is the effective mean switching frequency of the conventional iTCM or TCM control.

The LCL filter design of TCM and CCM are the same as we discussed in Chapter 3. Taking CCM at 20Hz as an example, the total inductance needed for the filter is 1.348 mH, as shown in Figure 5.5. In this case, the resonance frequency is chosen as one-third of the switching frequency, which is 6.67kHz. L_c and L_g can be obtained by Equation 3.35 after choosing the resonance frequency.

For the iTCM control, the calculated total inductance for the LCL filter is around 733

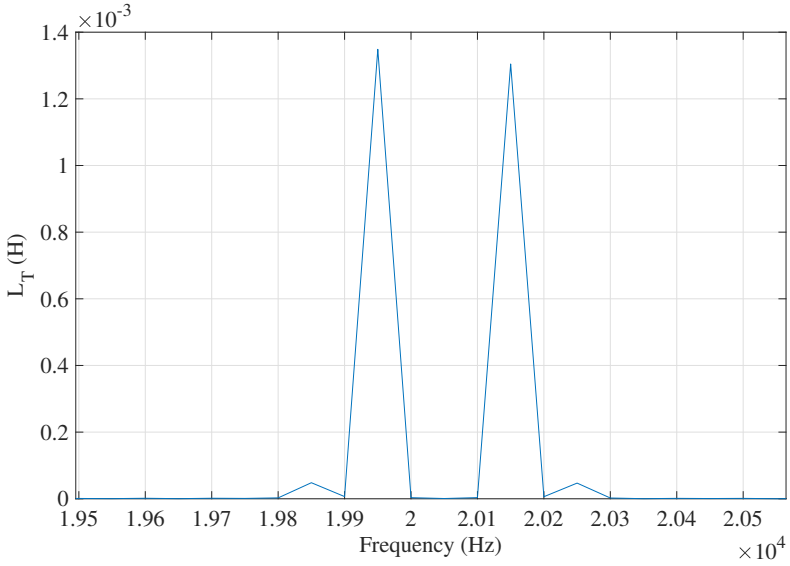


Figure 5.5: Total inductance needed for the input LCL filter (An example for CCM at 20kHz)

μH. Thus, for r<0.2, L_g is no longer needed. However, this dissertation does not consider these choices since the inductor loss, weight, and volume is not the desired result.

5.4.2. COMPARISON OF THE THREE MODES

The results of semiconductor loss, inductor loss and inductor weight and volume modeling are summarized in Table 5.2. All the results are extracted from the derived Pareto plots. Figure 5.6 shows the benchmark results considering the merits of efficiency, power density and specific power.

The efficiency of the rectifier operating with CCM at 20 kHz is the highest, while TCM leads to an efficiency of 98.54%. The power density and specific power are improved from 1.96 kW/L to 5.16 kW/L and 0.24 kW/kg to 0.56 kW/kg, respectively. It has been proved that increasing the switching frequency to reduce the LCL input filter is limited and impractical since it will lead to extremely high hard switching loss at a higher switching frequency.

Surprisingly, the efficiency of TCM is not improved compared to CCM at 97.6 kHz. The main reason is that for the selected MOSFETs (C3M0120090J), the switching energy is already extremely low, and the on-state resistance is quite large, as shown in Table 5.3. The TCM or iTCM control would eliminate turn-on loss, but the turn-off loss and conduction loss increase. Especially for the conduction loss, the RMS value is increased by at least 33% after setting I_{zvs} to 0. Moreover, the large current ripple causes high inductor loss at the converter-side inductor. Thus, the increased loss part is larger than the eliminated turn-on loss. The power density and specific power of the TCM are also slightly larger than those of CCM at 97.6 kHz, which is because a larger input filter is needed. Thus, the TCM control is more applicable for semiconductors with higher switching en-

Table 5.2: Total loss, weight and volume of the three-phase rectifier operating with CCM at 20kHz, CCM at 97.6kHz, TCM and iTCM with maximum frequency of 120 kHz. Note that only the inductor weight is take into consideration.

	Total loss (W)	Weight (kg)	Volume (cm^3)
iTCM (20-120kHz)	153.52	15.31	1691.18
TCM (20-120kHz)	163.16	26.04	3029.02
CCM (20kHz)	74.19	45.63	5600
CCM (97.6kHz)	159.91	19.68	2127.8

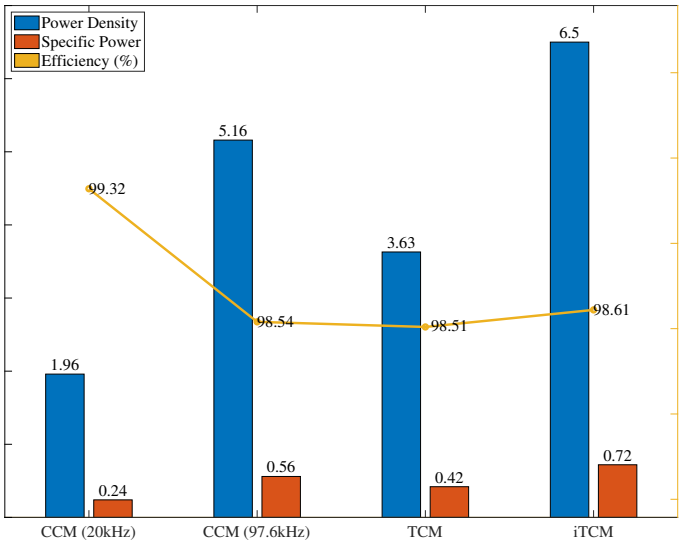


Figure 5.6: Efficiency. power density and specific power comparison for the three-phase rectifier operating with CCM at 20kHz, CCM at 97.6kHz, TCM and iTCM with maximum frequency of 120 kHz

ergy but lower on-state resistance. For the MOSFETs in hand, the turn-on loss is extremely low so that CCM is slightly better than TCM.

The iTCM control improved the power density and specific power to 6.5 kW/L and 0.72 kW/kg, respectively. Compared to CCM at 20 kHz, the efficiency is sacrificed by 0.71%, but the power density and specific power improved 3.3 and 3 times. The efficiency is not improved too much as we expected, with only a 0.1% improvement compared to TCM or CCM at 97.6 kHz due to the significantly low switching energy of the MOSFETs.

The power density and specific power of iTCM has not improved a lot compared to CCM at 97.6 kHz due to the additional LC branch, which increases the weight and volume in contrast.

Table 5.3: semiconductor loss modeling results with C3M0120090J Four in Parallel under CCM (20kHz and 97.6kHz), TCM and iTCM with switching frequency limitation. Note that the efficiency calculation shown here only consider the semiconductor losses

Mode	**Switching frequency (kHz)**	**P_{on} (W)**	**P_{rr} (W)**	**P_{off} (W)**	**P_{con} (W)**	**P_{loss} (W)**	**Efficiency(%)**
iTCM/TCM	20-591.48	0	0	49.45	36.52	85.97	99.22
iTCM_limit	20-120	0	0	47.71	37.31	85.02	99.23
iTCM_limit	20-60	0	0	47.65	42.19	89.84	99.18
iTCM_limit	20-20	0	0	51.93	126.74	178.67	98.38
CCM	20	15.78	0.80	7.81	25.16	49.55	99.55
CCM	97.6	78.05	3.98	37.49	25.13	144.65	98.69

Table 5.4: Inductor modeling optimization results from Pareto plot
for CCM (20kHz and 97.6kHz), TCM and iTCM with maximum switching frequency of 120kHz

iTCM (20-120kHz)	$L_c(\mu H)$	$L_b(\mu H)$	$C_b(\mu F)$	$L_g(\mu H)$	Loss (W)	Weight(kg)	Volume (cm^3)	THD (%)	TDD (%)
r=0.1	1502.52	70.81	9.00	0	67.87	22.8	3167.23	0.41	1.61
r=0.2	751.26	74.31	8.20	0	44.51	20.06	2494.39	0.65	3.19
r=0.3	500.84	78.18	8.00	232.16	53.12	23.78	3332.38	0.68	0.87
r=0.4	375.63	82.47	7.5	357.37	68.5	15.31	1691.18	0.68	0.87%
r=0.5	300.50	87.26	7	432.5	67.96	15.6	2180.14	0.68	0.84
r=0.6	250.42	92.64	6.80	482.58	65.67	17.71	2410.93	0.68	0.82
r=0.7	214.65	98.73	6.30	518.35	65.25	17.33	2363.54	0.68	0.82
r=0.8	187.82	105.68	6.00	545.18	66.53	16.15	2225.05	0.67	0.82
r=0.9	166.95	113.67	5.60	566.05	66.8	16.19	1658.65	0.67	0.82
r=1	150.25	122.98	5.00	582.75	61.45	24.83	3097	0.67	0.83
TCM (20-120kHz)	67.63	0	0	833	78.14	26.04	3029.02	0.52	0.64
CCM (20kHz)	699	0	0	649	24.64	45.63	5600	0.6	0.62
CCM(97.6kHZ)	159.93	0	0	113.57	15.26	19.68	2127.8	0.32	0.3

6

SIMULATION AND EXPERIMENT VALIDATION

6.1. SIMULATION RESULTS

THE simulation is conducted to verify the idea of the iTCM control and close-loop control via PLECS. The parameters used for the simulation are the same as the system specifications in Table 4.1. The aforementioned parameter r is selected as 0.4 just as an example. The Bounded-iTCM control and the Sinusoidal- iTCM control are verified in the simulation. The simulation circuit via PLECS is shown in Figure 6.1.

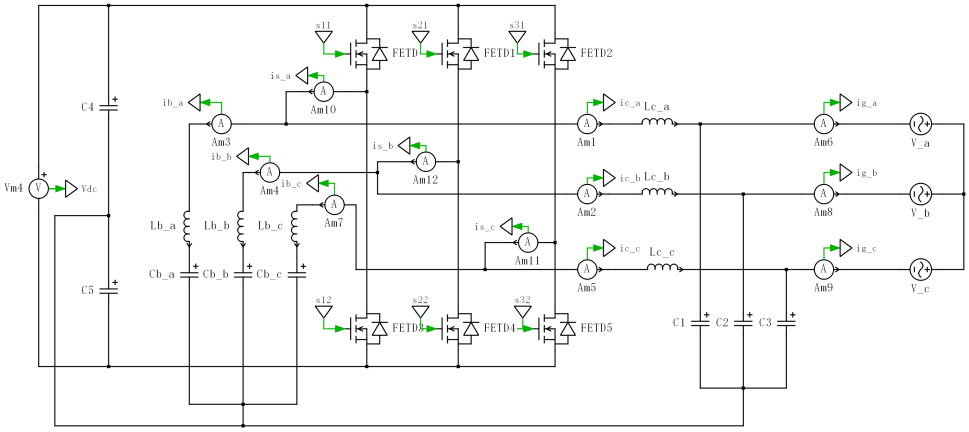


Figure 6.1: The simulation circuit of the iTCM control in PLECS

6.1.1. THE BOUNDED-ITCM CONTROL

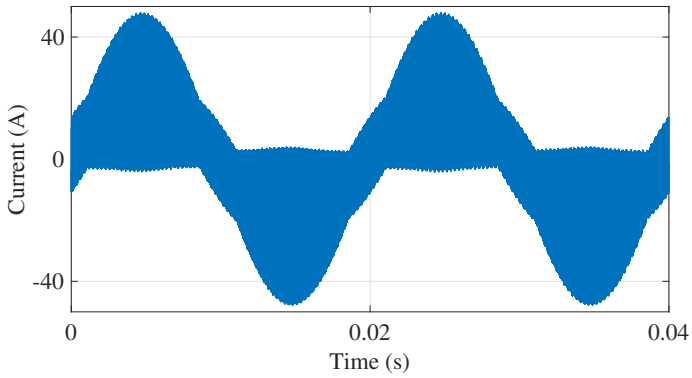
The simulation results of the aforementioned Bounded-iTCM control are shown in Figure 6.2 and 6.3.

Figure 6.2(a), 6.2(b) and 6.2(c) show the semiconductor current i_s, the converter-side current i_c and the LC branch current i_b, respectively. The semiconductor current i_sm is split into a low-frequency component i_c, and a high-frequency component i_b due to the added LC branch.

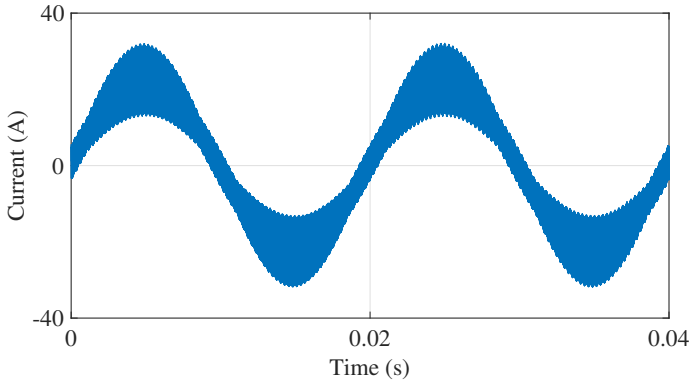
The low-frequency current satisfies the input power and the high frequency current flows through the LC branch, which stays within the circuit by the midpoint. The additional inductor L_b is well-designed so that the high-frequency current is split correctly.

Figure 6.3(a) shows several switching cycles of the semiconductor current i_s. It can be seen that ZVS turn-on is achieved since the semiconductor current is reversed to -2.5 A at each switching period. However, in the limited frequency region, the reversal current goes even larger, as shown in Figure 6.3(b). ZVS is still achieved in this region but the larger reversal current scarifies the efficiency because of the larger turn-off current and the higher RMS current.

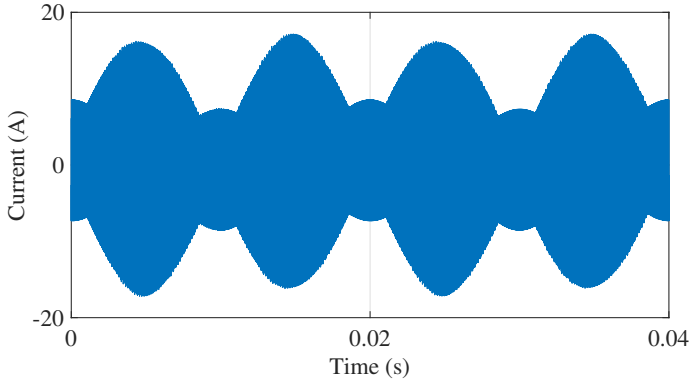
Figure 6.3(c) shows the switching frequency of the Bounded-iTCM control. The switching frequency is limited to 120 kHz, as discussed in Chapter 3.



(a)

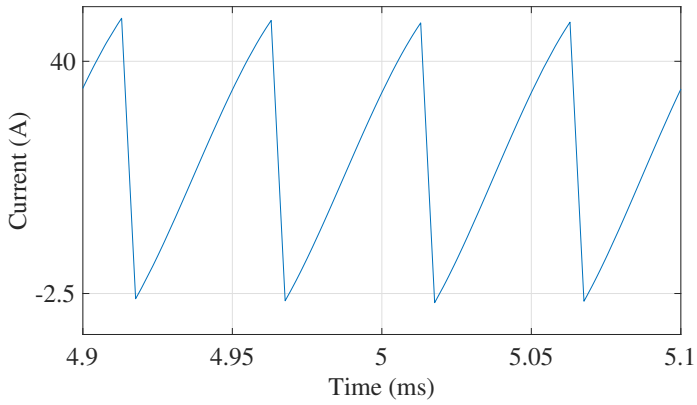


(b)

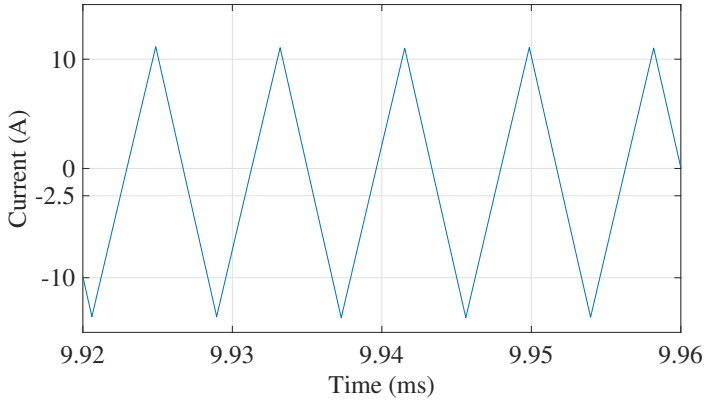


(c)

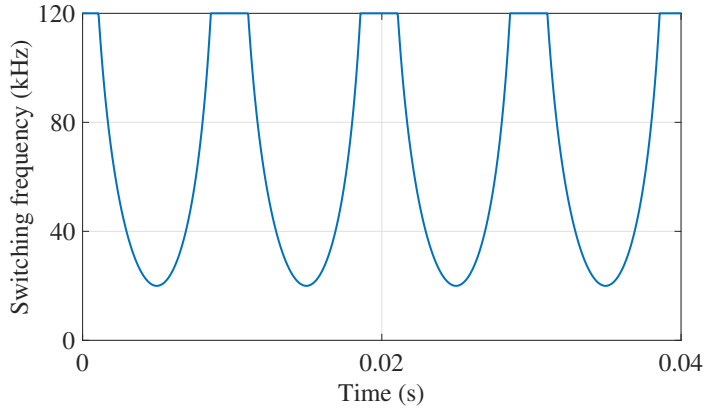
Figure 6.2: The simulation results of current waveform for the Bounded-iTCM control with a maximum 120 kHz switching frequency limitation; (a) The semiconductor current i_S; (b) The converter-side current i_C ; (c) The LC branch current i_b



(a)

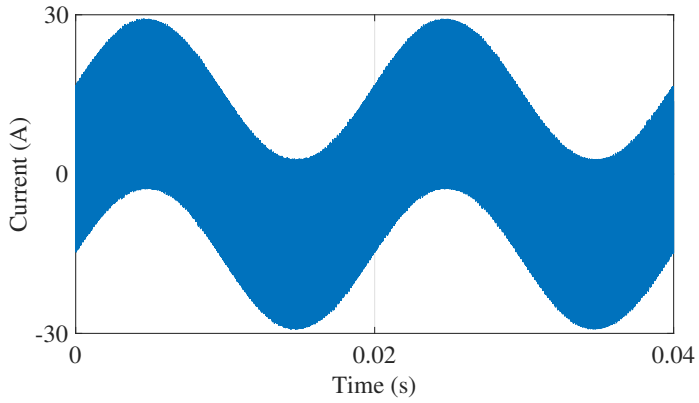


(b)

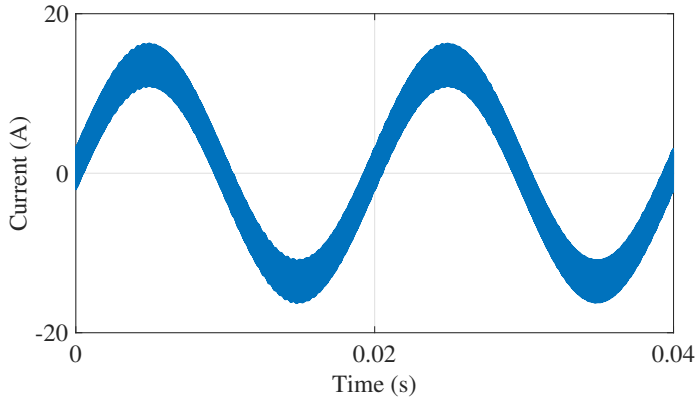


(c)

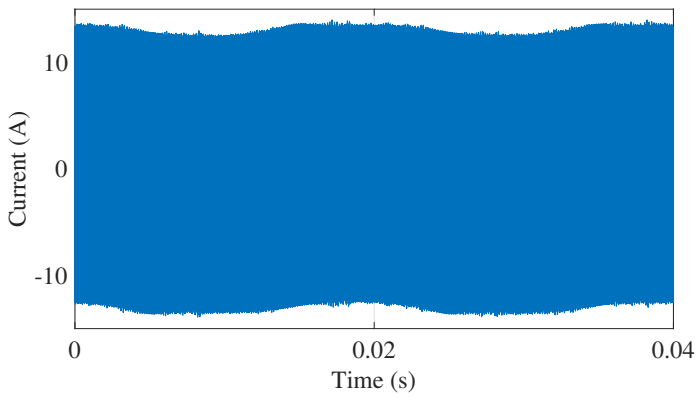
Figure 6.3: The simulation results of the Bounded-iTCM control with a maximum 120 kHz switching frequency limitation; (a) Several switching cycles illustration of the constant reversal current region; (b) Several switching cycles illustration of the limited-frequency region; (c) The switching frequency of the Bounded-iTCM control in one main period



(a)



(b)



(c)

Figure 6.4: The simulation results of current waveform of the Sinusoidal-iTCM control; (a) The semiconductor current i_s; (b) The converter-side current i_c ; (c) The LC branch current i_b

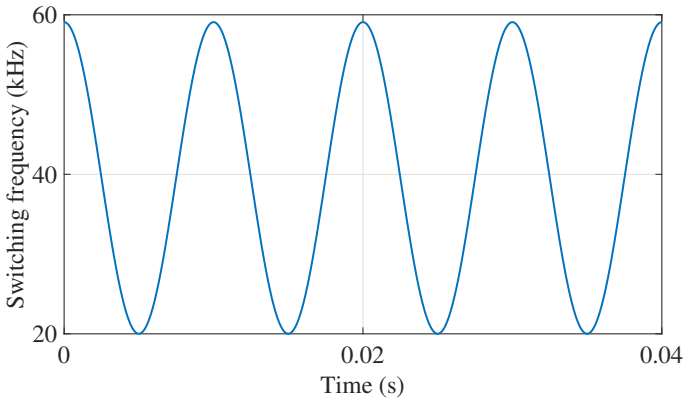


Figure 6.5: The simulation results of switching frequency for the Sinusoidal-iTCM control

6.1.2. THE SINUSOIDAL-ITCM CONTROL

The simulation results of the aforementioned Sinusoidal-iTCM control are shown in Figure 6.4 and 6.5.

Figure 6.4(a), 6.4(b) and 6.4(c) show the semiconductor current i_s, the converter-side current i_c and the LC branch current i_b, respectively. The semiconductor current i_s is split into a low-frequency component i_c and a high-frequency component i_b. The current ripple remains constant in the Sinusoidal-iTCM control, which is much larger than the ripple in the Bounded-iTCM control. ZVS turn-on is achieved in the main cycle, but the efficiency would be lower than the Bounded-iTCM control.

Figure 6.5 shows the switching frequency of the Sinusoidal-iTCM control. As discussed in Chapter 3, the switching frequency is calculated by Equation 3.60. The switching frequency keeps the same under different load conditions, which is the biggest advantage of the Sinusoidal-iTCM control.

6.2. EXPERIMENT VALIDATION

6.2.1. EXPERIMENT SETUP

To validate the advantage of the proposed iTCM control, the experiment based on the digital signal processor (DSP)-TMS320F28379D has been conducted under CCM, TCM and iTCM. The prototype used in the experiment is a three-phase two-level full-bridge AC-DC converter. The semiconductor device is Si Carbide MOSFET (C3M0120090J [33], four paralleled as one switch), the same as in the analytical modeling. The YOKOGAYA DLM4058 oscilloscope and the YOKOGAYA WT500 power analyser are used in this experiment.

Due to the limits of the prototype, a 3 kW prototype is chosen instead of 11 kW in the analytical modeling. The boost inductor L_c in CCM, TCM, iTCM and the branch inductor L_b in iTCM are chosen as the ferrite core instead of the powder iron core. The ferrite core would not be saturated since the peak current is quite lower compared to 11 kW. The litz wire is used in all inductors. Thus, only the waveform and the efficiency are measured

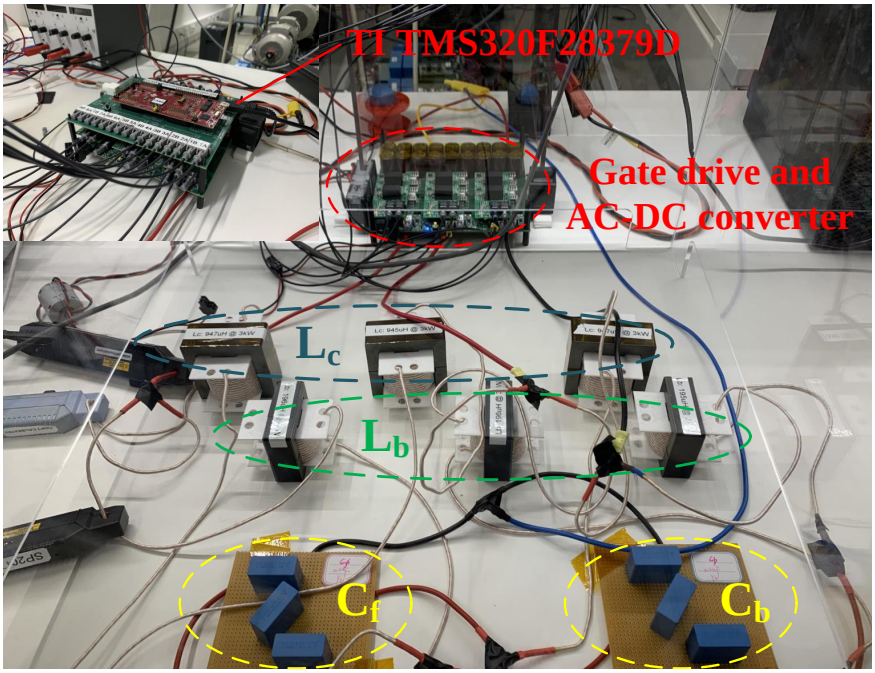


Figure 6.6: Experimental setup.

and compared in the experiment. Moreover, the ZVS turn-on current under the power rating of 3 kW is recalculated by Equation 3.55, which is 1.5 A.

All the parameters have been redesigned to fulfill the 3 kW power rating. The system specification of the experiment is shown in Table 4.1. The ferrite core is chosen from TDK, and the material is N87, of which the Steinmetz coefficients are shown in Table 6.1.

Due to the adjusted power rating, the minimum switching frequency of the TCM or the iTCM control is changed to 27.5 kHz. The maximum switching frequency is also limited to 120 kHz manually, as discussed in Chapter 3. By analytical calculation, the mean value of the switching frequency is 75 kHz. Thus, the CCM control is tested under 75 kHz for comparison.

Table 6.1: Coefficients in the improved Generalized Steinmetz Equation (iGSE) for the core material N87 used in the experiment: $P = k_o * (B^{\beta}) * (f^{\alpha}))P : [W/cm3], B : [T], f : [Hz]$

Coefficient	Value
α	1.2386
β	2.0155
k_o	1.0225e-5

Table 6.2: Optimal results from Pareto plot for the inductor design in the experiment

	Inductor 1	Inductor 2	Inductor 3
Inductance	945μH	196μH	165μH
Core Material	N87	N87	N87
Core Code	'65/32/27'(1.5)	'55/28/21'(2)	'55/28/21'(2)
Core Type	EE	EE	EE
Number of Stacks	1	1	1
Number of Turns (N)	56	34	31
Airgap length (mm)	0.1	0.1	0.1
Number of strands (n)	600	600	600
Diameter per strand (mm)	0.07	0.07	0.07
Usage	iTCM L_c TCM L_g	iTCM L_b CCM L_g	TCM L_c CCM L_c

6.2.2. EXPERIMENT RESULTS

Figure 6.7 and 6.8 show the experiment results of the Bounded-iTCM control. Figure 6.7(a) shows the waveform of the three-phase semiconductor current i_s. Figure 6.7(b) shows several switching cycles of the semiconductor current of one phase. The semiconductor current waveform is the same as analyzed in Chapter 3. Moreover, the current i_s is reversed to around -2.1 A in the positive switching cycle, which means the ZVS turn-on is achieved in the main cycle. Figure 6.8(a) and 6.8(b) show the experiment waveform of the LC branch current i_b and the converter-side current i_c, respectively. The converter-side current i_c is a 50 Hz sinusoidal wave with a small ripple flowing to the grid, while most of the high-frequency current i_b flows through the LC branch with stays within the circuit.

Figure 6.9 and 6.10 show the experiment results of the TCM control. The switching frequency is limited to 120 kHz as well. Thus, the semiconductor current would be the same as that of the iTCM control. Figure 6.9(a) shows the waveform of the three-phase semiconductor current (converter-side current) i_c. Figure 6.9(b) shows several switching cycles of the semiconductor current of one phase. The current reaches - 1.6 A in the positive switching cycle. ZVS turn-on is fully achieved. Figure 6.10(a) shows the waveform of the three-phase grid-side current i_g. Figure 6.10(b) shows the waveform of the three-phase AC-side voltage.

Figure 6.11 shows the experiment results of the CCM control with a switching frequency of 75 kHz. Figure 6.11(a) and 6.11(b) show the waveform of the three-phase semiconductor current (converter-side current) i_c and the three-phase grid-side current i_g, respectively.

Table 6.3: The efficiency of the CCM, TCM and iTCM control for modeling and experiment results comparison

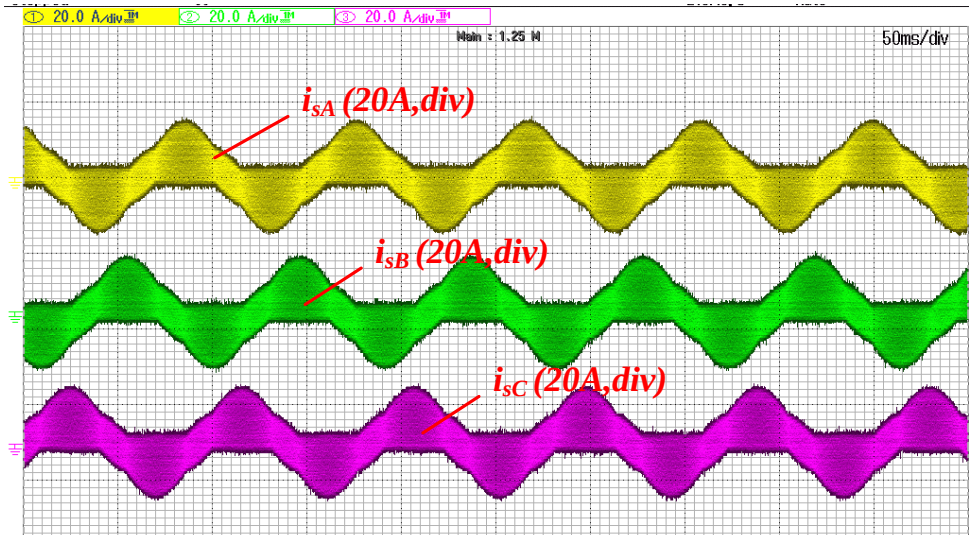
	P_{semi}	$P_{inductor}$	P_{total}	Efficiency (%)	Measurement (%)
iTCM	62.47	11.95	74.43	97.51	96.38
TCM	62.47	13.91	76.38	97.45	96.66
CCM	79.65	11.11	90.76	96.97	95.61

[a]P denotes the power loss.

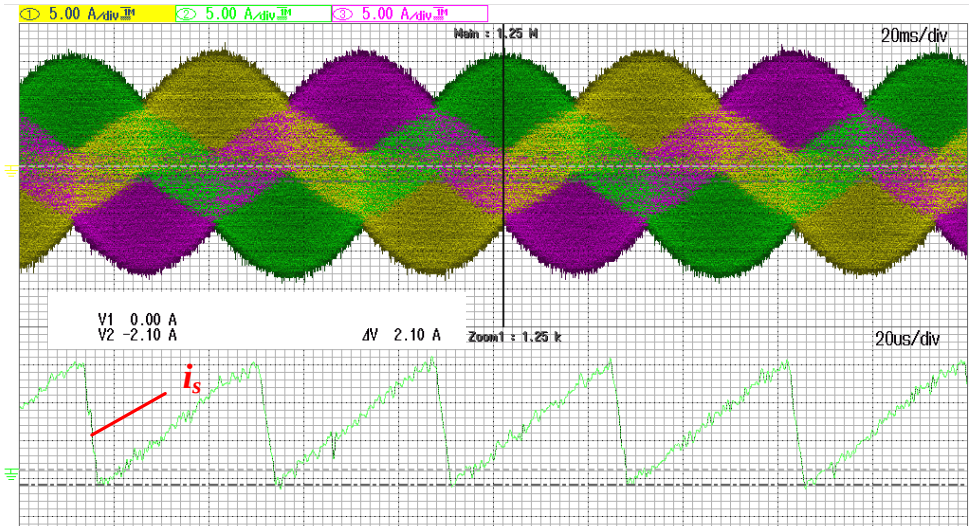
The efficiency of the three modes is shown in Figure 6.12 and summarized in Table 6.3. Table 6.3 also shows the analytical modeling efficiency results of the system for comparison, which contains the semiconductor loss modeling and the inductor loss modeling results.

First of all, the efficiency of the analytical modeling is larger than that of the experiment result of around 1%. The biggest reason is that the polynomial coefficients which model the switching energy are obtained from the double-pulse test in [46]. When the drain-source current is smaller than 3 A, the switching energy is not tested but estimated, which may cause larger errors. Moreover, the semiconductor junction temperature is much higher than that in the double-pulse test or the datasheet due to the higher power loss in the iTCM control. Besides, other losses, such as the capacitor loss, are neglected in the analytical modeling.

For the experiment results, the efficiency of iTCM, TCM and CCM is 96.38%, 96.66% and 95.61%, respectively. The efficiency of the iTCM control is improved by around 1% compared to CCM at 75 kHz. Regardless of the power density and the specific power, the efficiency improvement is quite large.

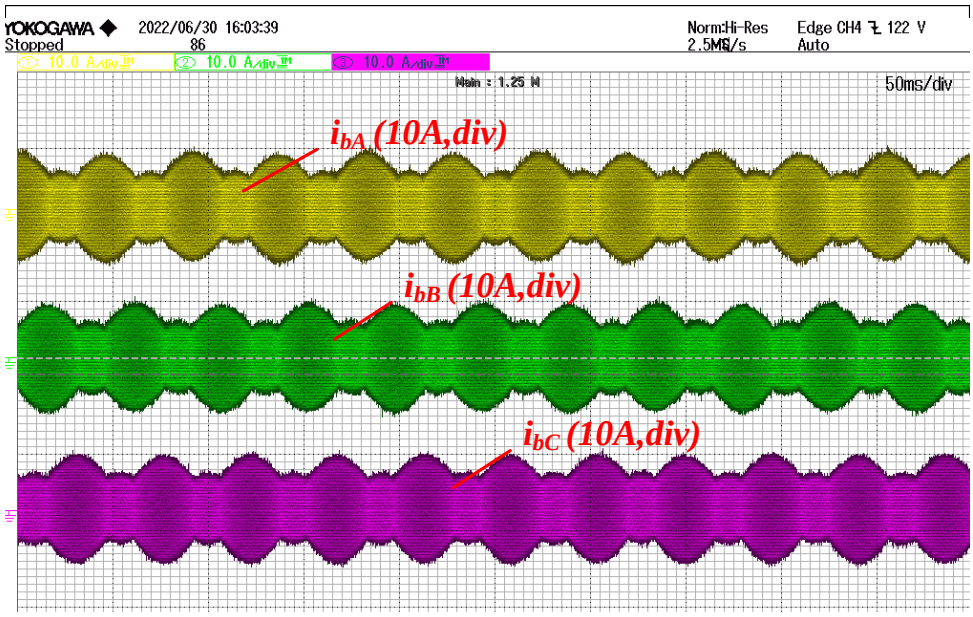


(a)

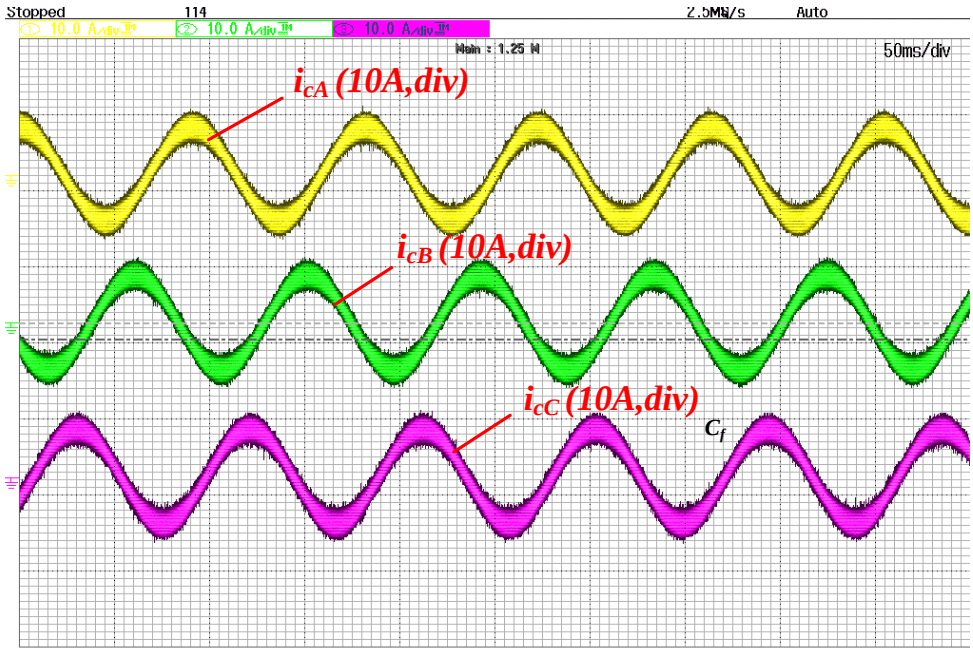


(b)

Figure 6.7: The experiment results of the Bounded-iTCM control; (a) Three-phase semiconductor current i_s ; (b) Several switching cycles of the semiconductor current i_s.

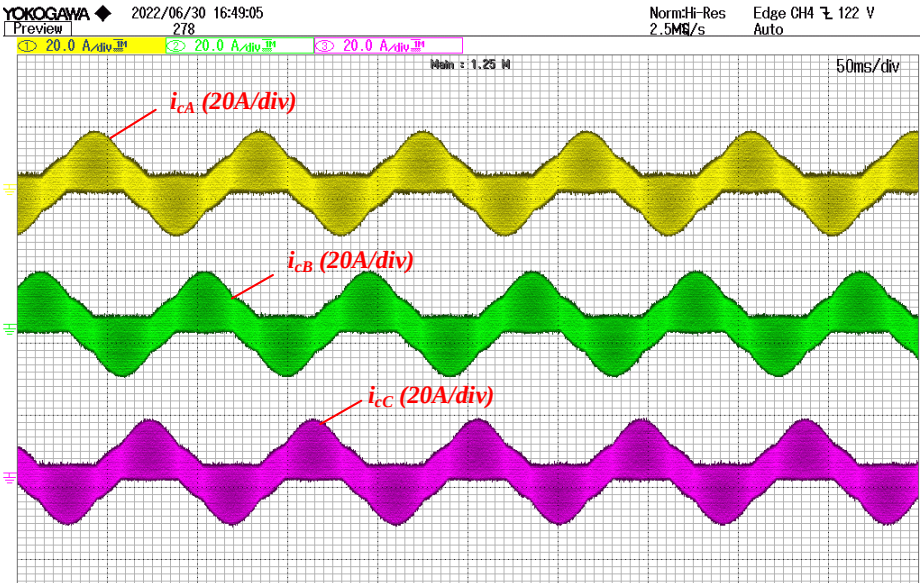


(a)

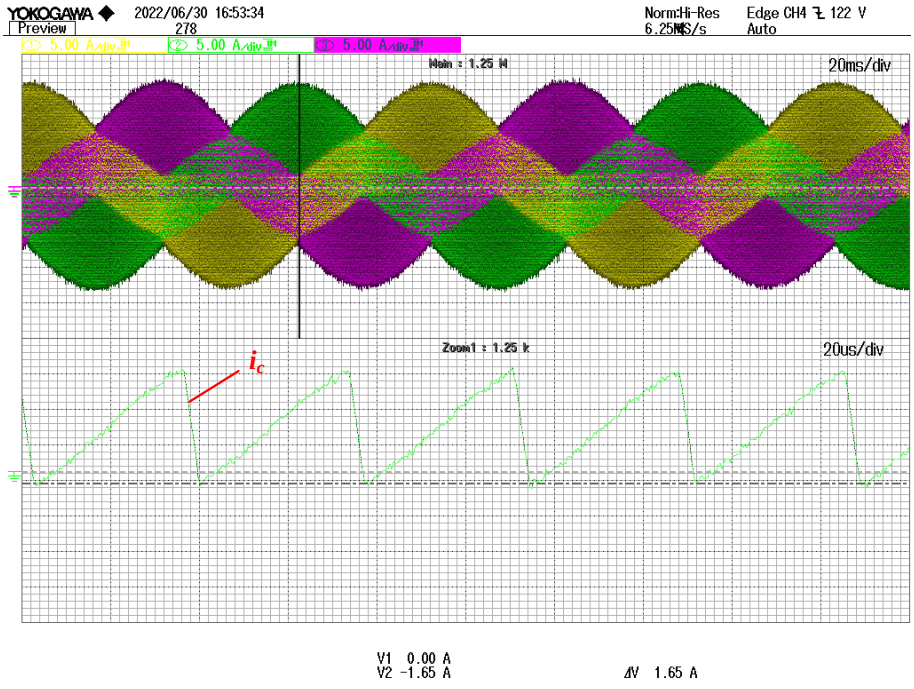


(b)

Figure 6.8: The experiment results of the Bounded-iTCM control; (a) Three-phase semiconductor current i_s ; (b) Several switching cycles of the semiconductor current i_s.

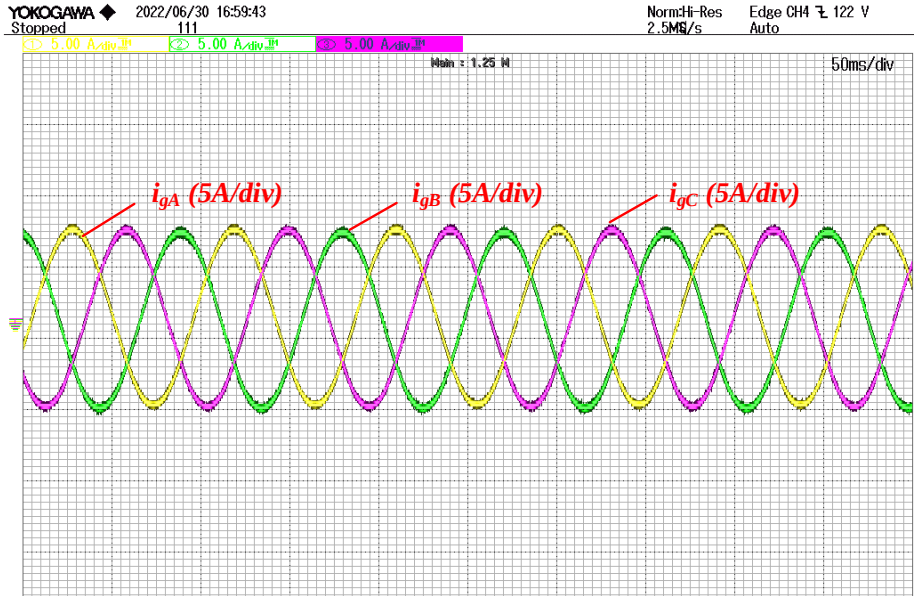


(a)

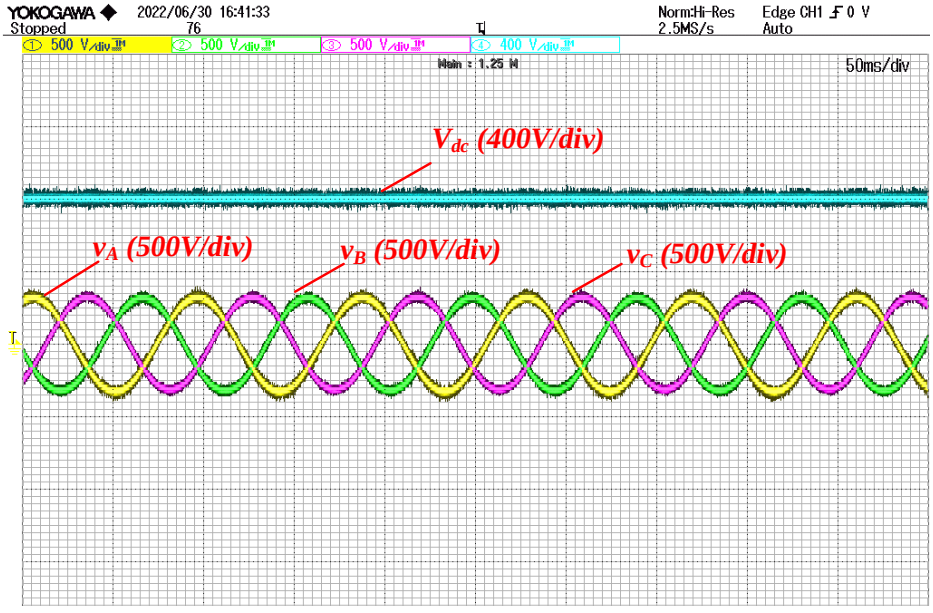


(b)

Figure 6.9: The experiment results of the TCM control; (a) Three-phase semiconductor current i_c ; (b) Several switching cycles of the semiconductor current i_c.

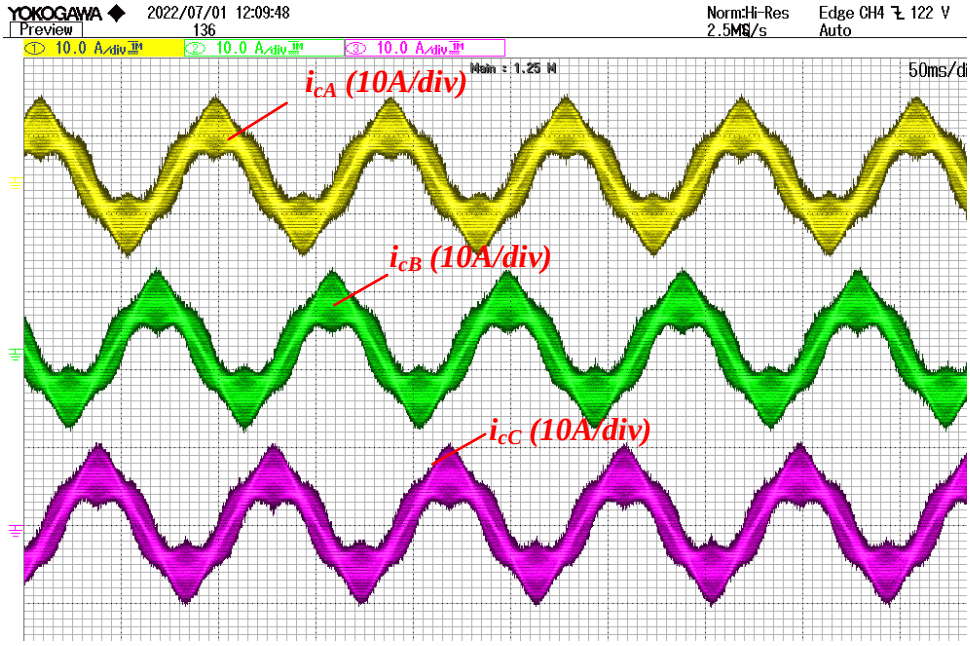


(a)

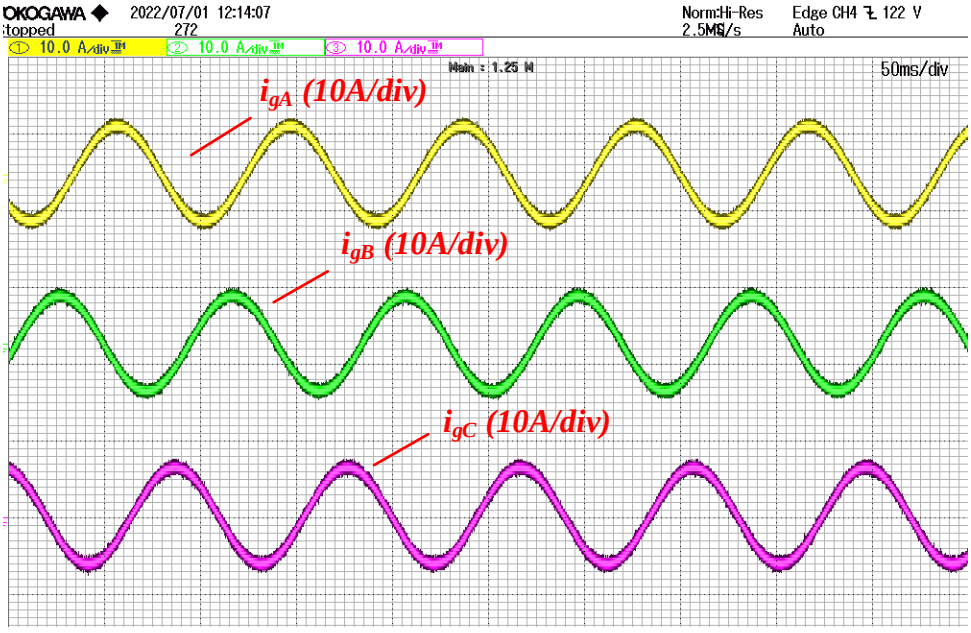


(b)

Figure 6.10: The experiment results of the TCM control; (a) Three-phase grid-side current i_g ; (b) Three-phase AC-side voltage v_{ac}.

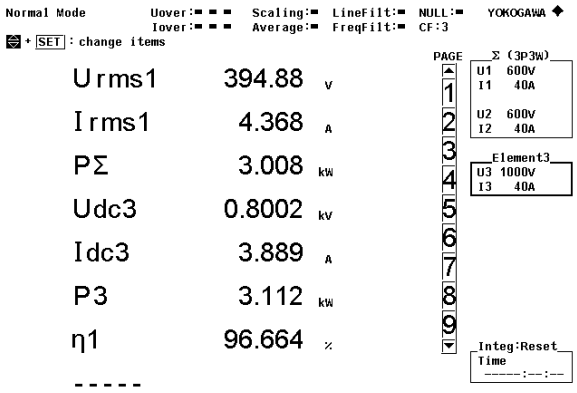


(a)

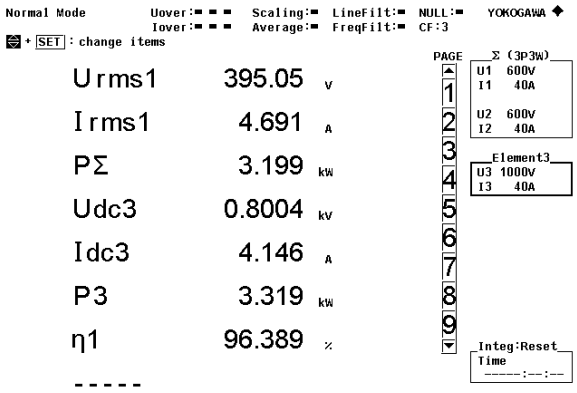


(b)

Figure 6.11: The experiment results of the CCM control; (a) The converter-side current i_c; (b) The grid-side current i_g.



(a)



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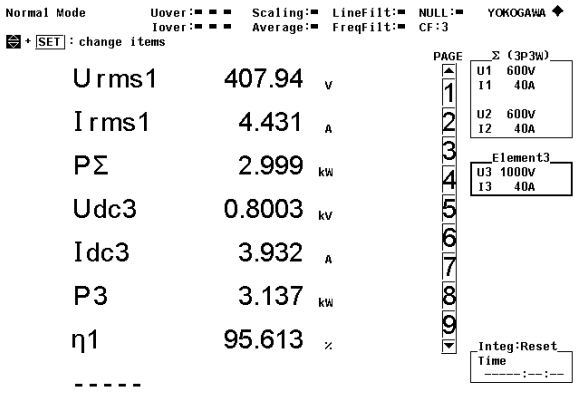

(c)

Figure 6.12: The experiment results of efficiency; (a) The iTCM control; (b) The TCM control; (c) The CCM control (75 kHz).

7

Conclusion and Future work

7.1. CONCLUSION

The iTCM control method applied to a three-phase AC-DC PFC converter has been proposed in this paper. ZVS operation in the iTCM strategy eliminates the turn-on switching loss but slight increases the turn-off switching and conduction losses. The inductor loss in iTCM is minimized due to the added LC branch, while the grid-side current ripple is highly reduced compared to the conventional TCM control.

By analytical modeling and simulation, iTCM is proven more efficient, highly compact and lightweight than TCM and CCM at the high switching frequency of 97.6 kHz. Compared with CCM at the low switching frequency of 20 kHz, the power density and specific power improved around 3 times but sacrificed efficiency by 0.71%, which is acceptable.

Dual-loop control with LCL capacitor and LC branch current feedback is proposed and implemented in PLECS to control the PFC converter in iTCM. The experimental test is conducted to verify the analytical modeling and simulation results. In the experiment, the iTCM control achieves an efficiency of 96.38%, which is higher than the CCM's efficiency at 75 kHz. Assuming the power density and the specific power are the same, the proposed iTCM control highly improves the system efficiency by 1%. Thus, to improve the power density and the specific power, the iTCM control is weighing more effective than increasing the switching frequency of CCM.

7.2. FUTURE WORK

Depending on the current conclusion, there are three recommendations for future work.

1. In this research, only bounded-iTCM control is discussed, but it can not handle different load conditions without changing the switching frequency. A possible solution is given as the Sinusoidal-iTCM control, but the optimal inductor design of this mode is not modeled. Analytically, it will cause more losses but has not been approved experimentally.

2. The experiment is only implemented at 3 kW power level due to practical limitations, and the inductor core is not chosen powder iron core and ferrite core from Magnetics as we modeled. In the future, it is better to verify it at 11 kW since the inductance value will drop with the increase of power rating, and it may give us further improvement.

3. The topology of the three-phase iTCM PFC converter also gives an idea of the input filter design for normal AC-DC converters. Due to the added LC branch, the grid-side inductor is not needed anymore when the ripple r is low, which is exactly the case at CCM.

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