Wafer Scale Flexible Interconnect Transfer for Hetrogeneous Integration

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DOI
10.1109/ECTC32862.2020.00133

Publication date
2020

Document Version
Accepted author manuscript

Published in
2020 IEEE 70th Electronic Components and Technology Conference (ECTC)

Wafer Scale Flexible Interconnect Transfer for Hetrogeneous Integration

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***Abstract*—A polymer-based wafer level integration technology suitable for miniaturized and multi-functional systems integration was developed and demonstrated in this work. Wafer scale flexible interconnects were firstly fabricated on one wafer, and then transferred to another wafer. Such transfer process involved wafer bonding and application of sacrificial materials. A sacrificial layer was firstly placed on the surface of the transfer wafer, and the sandwich interconnect structures were then manufactured on top of the sacrificial layer. With the help of sacrificial layer, the flexible interconnects were transferred to another wafer through wafer bonding process. Contact resistance structures were fabricated with the help of wafer bonding process, connecting and aligning metal contact layer on device wafer and metal layer embedded in transferred flexible interconnects. Such transferred contact resistance was measured through designed testing structures as a demo for wafer level heterogeneous integration**

Keywords—flexible interconnect, transferred interconnect, heterogeneous integration

I. INTRODUCTION

Advanced miniaturized and multifunctional packages bring critical challenges for semiconductor industry. [1] There are mainly two IC packaging concepts, namely system on chip (SOC) and system in a package (SIP). In SOC technology, all necessary electronic components are placed on a single integrated circuit (IC). While SIP integration allows chips or other components from different suppliers to be combined into highly functional products in their own respective technology flows. [2] Due to the limitations of wire bond and flip chip, self-aligned Wafer level Integration Technology (SAWLIT) has been introduced. [3]

Prior work SAWLIT was reported by H. Sharifi in 2007 [2]. Flexible interconnects in this work were directly fabricated on wafer with embedded components. However, their package temperature is limited to 200°C by PDMS. Since polyimide is more attractive than PDMS in semiconductor packaging due to high bending stiffness, high glass transition temperature, high thermal and chemical stability, low dielectric constant, and high mechanical strength [4], an appropriate SIP platform with flexible polyimide/aluminum/polyimide interconnects is presented in this work, with the help of wafer bonding , sacrificial materials [5], and lithography processes [6].

II. EXPERIMENT DESIGN

In this work, a sacrificial layer (Polycarbonate) was applied on silicon wafer (Transfer Wafer). After that, aluminum interconnects embedded in patterned polyimide were fabricated using spin-on, sputtering, and lithography technologies. The aluminum interconnects buried between polyimide layers were located in neutral plane, so the strain and stress can cancel each other when bending.

In the meantime, cavities were etched on the corresponding area of the device wafer and the devices were fixed in the cavities with the contact pads up. The contact pad and interconnects make contact with each other when the transfer wafer and the device wafer are aligned and bonded. The sacrificial layer was later sacrificed during the de-bonding processing, then the sandwich interconnect structures were transferred to the device wafer as well as connecting to the embedded devices.

The core of this theory is to realize electrical contact between the interconnect from transfer wafer and the contact pads on the devices (or on the device wafer). To simplify the prototype and verify this transferring interconnect theory, the cavities and the devices are removed from the design and aluminum contact pads are added on the corresponding places as replacement (shown in Fig. 1.). Theses rectangular pads were manufactured on the device wafer beforehand and to make contact with interconnect on transfer wafer after aligned bonding and de-bonding with silver glue. The contact status can then be measured with probe station by testing the places that was not covered by the transferred interconnects. The key of this prototype is to verify the feasibility of transfer and interconnect bonding. As in proving interconnect can be transferred with polyimide encapsulated and the contacts between interconnect and contact pads can transmit electric current.

To prove this theory, a mask has been designed as shown in Fig. 2. This design contains three types of structures. Fig. 2 (a) is a modified Daisy Ring structure with different sizes. The aluminum interconnects are designed to be encapsulated by two polyimide layers, forming the sandwich interconnect structures.

These sandwich interconnect structures are all manufactured on the transfer wafer on the sacrificial layer. Contact holes have been designed to check the electoral connection status as well as measure the reliability and resistivity of interconnect with probe station. The light blue layer is the aluminum contact pads that are manufactured on the device wafer.

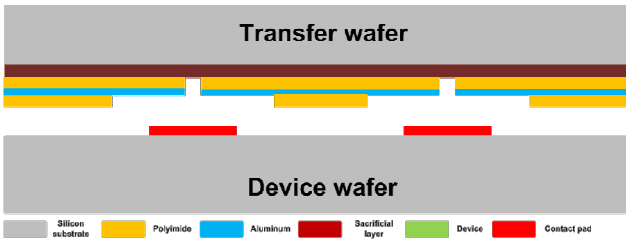


Fig. 1. Simplified crosssection of transferred flexible interconnect prototype.

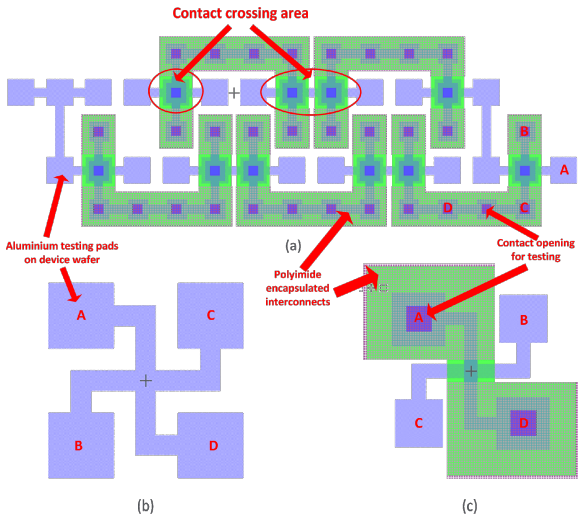


Fig. 2. Mask design of (a) Modified Daisy Ring structure (b) Greek sheet resistance testing structure (c) transfer contact resistance testing structure

After aligned wafer bonding, the crossed aluminum areas from both the interconnects on transfer wafer and the aluminum pads on device wafer come into contact. As aluminum interconnects suffer self-oxidation problems (a thin aluminum oxide would be formed itself after aluminum is sputtered), a conductive glue is applied between the aluminum contacting surfaces (including the Daisy Ring structures and the Greek sheet resistance testing structures). The conductive glue not only improves the contact condition of the two interconnects, but also helps with the interconnect transferring in the later processing steps.

Such Daisy Ring structure supplies multiple contact openings for electrical contact status checking. By measuring between A and B or between A and C, the contact status can be obtained (conductive or not). By measuring between C and D, the conductivity of interconnects in sandwich structure can be tested.

Greek sheet resistance testing structures are also added to the design as in Fig. 2(b). Sheet resistance is a ratio between the material resistivity and the layer thickness. It is usually measured by using four point probe (FPP) method.

These sheet resistance testing structures are also designed to be placed both on transfer wafer and on device wafer. Based on that, the aluminum interconnect thickness on polyimide and on silicon after the processing can be checked.

After the aligned bonding and transfer procedure, the crossing area comes into contact with conductive glue. By forcing a current into A-D and measuring a voltage drop between B-C, the contact resistance can be obtained and in turn, the conducting aluminum thickness can be calculated. Through this demo, the transferred interconnects are demonstrated for wafer level heterogeneous integration.

III. Experimental Results

A. *Transfer Wafer*

Sacrificial layer was fabricated by 20 wt% poly propylene carbonate (PPC) solution. The solution was produced by mixing PPC solids with solvent γ-Butyrolactone (GBL). The mixing required continuously stirring in the solution for 72 hours. The PPC solution was firstly spin coated on the substrate as sacrificial layer. After 2 hours baking in vacuum under 180 °C, most of the solvent (GBL) had been removed and a 3 μm layer of PPC was obtained.

To better understand the influence of PPC during processing, a PPC thermogravimetric analysis under 150 °C for 18 hours was carried out. According to the TGA result shown in Fig. 3, PPC only decomposed 6.2% through this soft baking procedure.

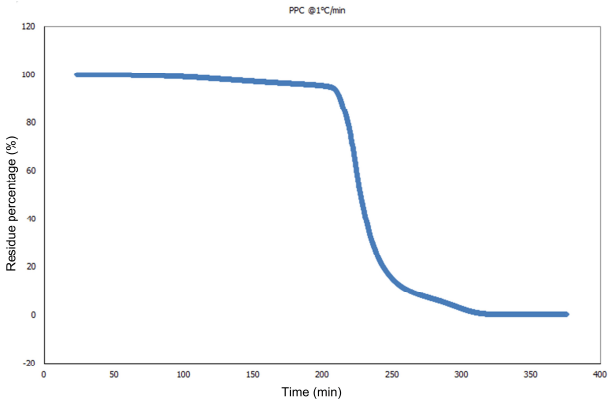


Fig. 3. TGA of PPC at 1 °C/min.

Directly on top of the sacrificial layer, two polyimide layers and embedded Al metal layer was processed. Polyimide plays an important role in the processing and two different kinds of polyimide were selected. One is Durimide A112, a polyimide precursor from Fujifilm. Such dissolved poly amic acid in a liquid status can be spin-coated, wet etching patterned and then cured to form a strong polyimide film. The other polyimide, Kapton® film, is a cured polyimide film which is able to be patterned by plasma dry etching. The differences between these two types of polyimide lead to different processing steps and transfer results.

Directly on top of the sacrificial layer, a 2.4 µm layer of Durimide A112 was spin coated with a speed of 2000 rpm/s for 45 s and soft baked for 3 min. Photoresist SPR 3012 was used for patterning and 1.5% TMAH solution was used as developer. As TMAH would start to damage the sacrificial layer (PPC) when polyimide is etched away and PPC is exposed in TMAH, the developing time was tested and selected with great care. In this case, the developing should last no longer than 1min 20 sec. After developing, a directly rinsing was demanded to rinse away the TMAH residues, which would damage PPC and uncured polyimide seriously.

Standard procedure to strip photoresist on uncured polyimide is to rinse it with acetone, IPA and water. But this standard procedure is not suitable for this case as PPC would dissolve in acetone rapidly. To complete photoresist stripping, ethanol was tested and selected instead, so that the PPC sacrificial layer is protected.

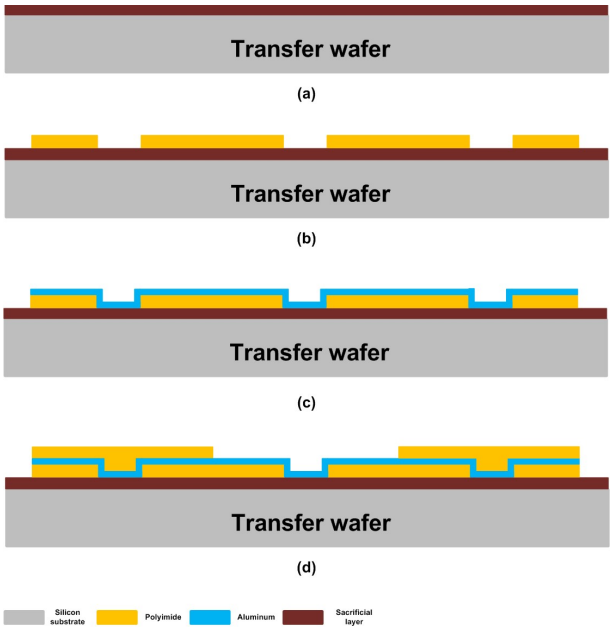


Fig. 4. Transfer wafer manufacturing process with Durimide A112.

Polyimide curing process is also tuned to protect the PPC layer. The standard curing step for Durimide A112 is 2 hours in vacuum under 400 °C. Polyimide polymerization requires higher temperature for a shorter time or lower temperature for a longer time. As a result, the patterned polyimide then was cured under 150 °C for 18 hours with vacuum, in order to protect the PPC sacrificial layer.

In step (c), aluminum interconnects were deposited and patterned on the cured polyimide film. A 2 µm layer of aluminum was deposited on the polyimide and PPC. A layer of 2 µm thickness of SPR 3027 photoresist was performed as masks for patterning and the aluminum dry etching was carried out in Trikon Omega with Cl2 and HBr plasma. This was followed by a full wafer exposure and 2 min ethanol rinsing to strip the photoresist.

Fig. 5 shows a microscope observation picture of aluminum interconnects on patterned polyimide. Some patterned polyimide structures were shifted during low temperature curing process, because polyimide has a low adhesion to the PPC surface and polyimide shrinks during the curing process. This shrinkage and low adhesion resulted in misplacement of the polyimide structures, which in return leads to misalignment between the polyimide structures and interconnect structures. Such misplacement distributed in a radios form. The structures in the wafer center show only within 10 µm misplacement. The further from center, the more serious the misplacement is. On the edge of the wafer, the structure misplacement could be up to 100 µm to 300 µm. This phenomenon was more obvious around the contact holes.

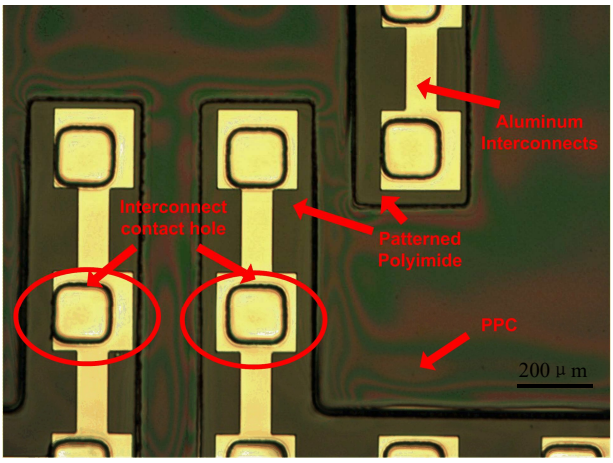


Fig. 5. Aluminum interconnects on patterned polyimide.

Due to such misalignment problems caused by shrinkage of Durimide A112, Kapton® film with 12.7 µm thickness is then selected as the first layer of polyimide. As a cured PI film, such material brings better protection to PPC sacrificial layer and less shrinkage of flexible structures. Kapton film shows a good chemical resistance, no known organic solvent, and a high temperature resistance, which opens more possibilities for high temperature applications.

In this process, PPC was firstly coated on the wafer as mentioned before. In this case, the layer of PPC is not only used as a sacrificial material, but also as an adhesive material. The Kapton® film was then cut into a fitted shape and put on the transfer wafer with PPC. AML bonder was applied for film attachment. The wafer was attached to the film in AML ramping from room temperature to 70 °C for 10 min in vacuum with a pressure of 500 N. The Kapton® film was then well attached to the wafer with the help of PPC and was compatible with all CMOS processing steps. As the thickness of the film is still too thick for the application, a uniform dry etching was performed to the film first. The etching was carried out in Trikon Omega dry etcher with an etching rate of 3.5 µm per 3 minutes. This plasma etch also removes PPC that was not covered by the Kapton® film. After a uniform etching for 6 min, a layer of 5.7

μm Kapton® film was remained on the wafer as illustrated in Fig. 6 (b).

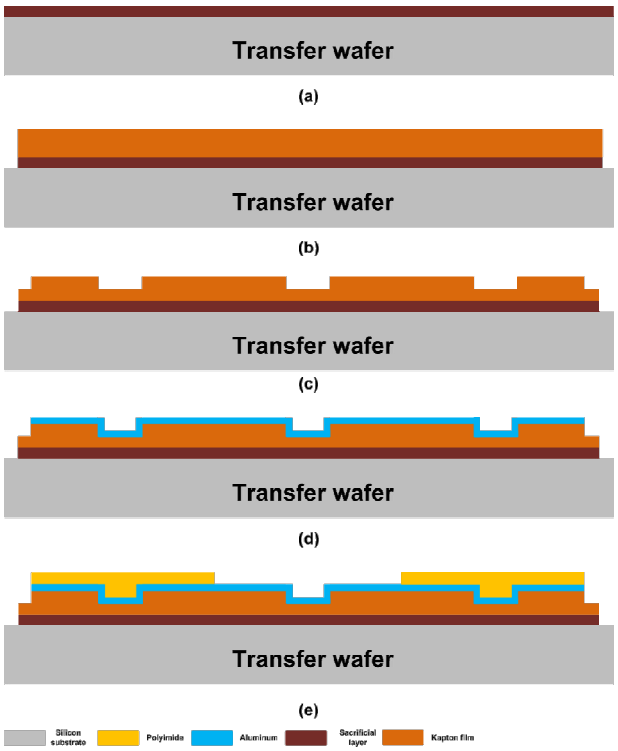
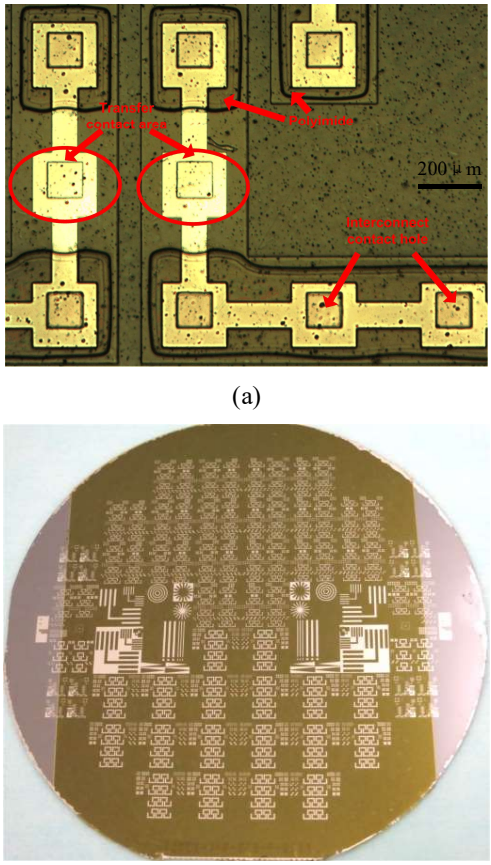


Fig. 6. Transfer wafer manufacturing with Kapton® film.

Unlike Durimide A112, Kapton® film cannot be patterned with wet etching. Dry etching with the same recipe as the uniform etching was selected for Kapton® film patterning. As this recipe also etches photoresist rapidly, so obviously photoresist is not suitable for its mask. Aluminum was then chosen as the hard mask for patterning Kapton® film. A layer of 500 nm aluminum was deposited on Kapton® film and patterned by photoresist and dry etching, thus forming an aluminum hard mask. Then, this aluminum hard mask was used to pattern Kapton® film under dry etching. Another 3.5 μm Kapton® film was etched and a thickness of 2.2 μm film was left as a protection layer for PPC as presented in Fig. 6 (c). Since the etching rate of Kapton® film cannot be precisely controlled, this thin layer was left to protect PPC from plasma and allowed later the aluminum interconnect land on Kapton® film but not on silicon substrate.

Similar to Durimide A112, a layer of 2 μm aluminum was deposited in CHA Solution Std and patterned by dry etching, as mentioned in step (d). Unlike Durimide, Kapton® film requires a lower processing temperature. The soft bake for photoresist had been reduced to 80 °C but under a longer time, e.g. 5 minutes. The hard bake after exposure was cancelled to avoid the high baking temperature. . The processing temperature should be kept under 80°C in the following steps, in order to avoid PPC decomposition. Although PPC doesn't decompose completely around 100 °C (0.876 % loss of PPC), the gas produced during decomposition (CO_2 and H_2O) has strong influence to the final demo. These gases between the Kapton® film and PPC will appear in a form of bubbles and influence the flatness of the film or even bring a dislocation of the whole film.

In step (e), a layer of 2.6 μm polyimide, Durimide A112, was coated and then patterned in the same way as introduced before. Before the low temperature curing, the four edges of the Kapton® film should be fixed by Kapton® tape. This procedure is to prevent the film from dislocation caused by polyimide shrinkage and PPC decomposed bubbles. After low temperature curing, the tapes were removed and the film is pressed again with AML bonder to remove the bubble under the film. It has been observed that after a longer time placement without any processing procedure, the result after curing of it had shown less bubbles or shrinkage.



(a)

(b)

Fig. 7. (a)Manufactured of the flexible interconnect with Kapton® Film; (b) Flexible interconnectss with Kapton Film on 4 inch wafer

Fig.7 presents a microscope picture of completed sandwich interconnect structure manufactured with Kapton® film and polyimide. The surface of the Kapton® film is relatively rough, with bubbles, holes and apophysis, which present as black dots in the microscope observation. The shiny parts are aluminum interconnects that manufactured on the patterned Kapton® film and the square holes in the middle are interconnect contact holes. After transferring and backside etching, aluminum interconnects in these contact holes will be exposed for measurements. The darker parts on the patterned Kapton® film are patterned polyimide, which act not only as protection layer for

interconnect, but also as adhesive layer for transferring. The interconnect areas that are not covered by polyimide, transfer contact areas, are intentionally left exposed for making contact with the contact pads on the device wafer after transferring.

B. Device Wafer

As already demonstrated in Fig. 1, device wafer was patterned contact pads on silicon substrate. These contact pads were designed to make contact with the transfer contact areas on transfer wafer after bonding and transfer process. To make sure the contact can be made, the thickness of the contact pads should be larger than the 2.6 µm thickness of the last layer of polyimide.

Therefore, a 4 µm of Al/Si layer was sputtered on the substrate in Trikon Sigma in Clean Room 100. Another 4 µm layer of photoresist SPR3027 was used as mask for patterning. Dry etching with Cl_2 and HBr was carried out in Trikon Omega. The mask photoresist was then tripped off by Tepla Plasma 300 and cleaning line (Fig. 8).

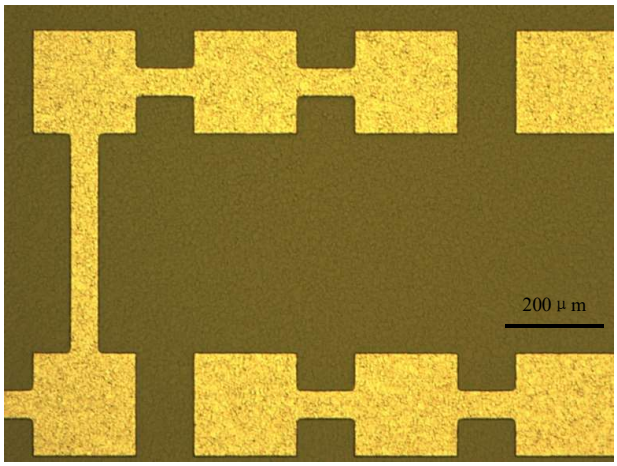
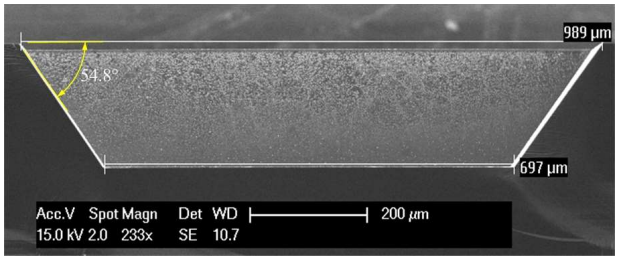


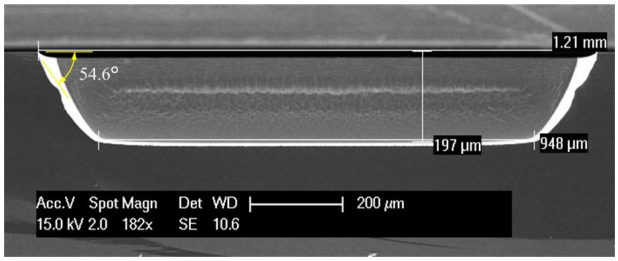
Fig. 8. Aluminum pads and interconnects on the device wafer.

Meanwhile, cavities for self-alignment were investigated in another separated silicon wafer by lithography and KOH etching. A comparison between wet etched and DRIE tapered cavities was made. Two test wafers were patterned with the reflector cavity mask. One wafer was etched in 33% KOH at 85 °C and the other used the DRIE etcher. Cross-sections of the resultant cavities are shown in Fig. 9. The KOH cavities have a smooth surface and form an inverted trapezoid, whereas plasma etched cavities have rounded edges and the sidewalls are rough. The taper angles in both cases are almost identical. Due to undercutting of the masking layer, the DRIE cavity expanded by more than 230nm, while the KOH cavity retained the patterned dimensions.

Precise locked components obtained by pick and place are possible to embed in such silicon cavities, e.g. LED dies. Devices fixed in the cavities will be connected to the transfer interconnects. For LED chip integration, the cavities then had to be lined with a reflective coating layer to enhance light extraction. A rough surface can act as a diffusive reflector and scatter light out of the cavity more efficiently. Aluminum was chosen as the reflector coating because of its high reflectivity and compatibility with the process flow. 250nm of Al were sputtered and patterned with the cavity mask using spray-coated negative resist to cover the Al inside the cavities. Furthermore, backside of device wafer can also be patterned. Backside etching of device wafer is possible to turn 2D devices into 3D by folding from the transferred flexible hinges. Demos will be presented in future works.



(a)



(b)

Fig. 9. Cavities comparison with KOH etching process (a) and DRIE process (b).

C. Interconnect Transfer

After curing the polyimide, the Kapton® tape that was used for fixing the Kapton® film should be removed. This removal could cause some Kapton® film detaching from PPC due to the stickiness of the tape. Therefore, an extra step to flatten the film was needed. The backside of another wafer was bonded with the transfer wafer under 70 °C for 10 min in vacuum with a pressure of 500 N. After the flattening, the transfer wafer was coated with primer VM652 and bonded with the device wafer that had conductive glue on its contact pads. The two wafers were aligned and bonded under 180 °C for 2 hours in vacuum with a pressure of 8000 N. (Fig. 10 (b))

After the bonding process, the bonded two wafers were moved to MEMS Lab for sacrificial layer removal. The sacrificing temperature was set to 250 °C for 2 hours. The sacrificial layer was removed after this process and the two wafers were separated, with the whole Kapton® film transferred from the transfer wafer to the device wafer (Fig. 10 (c)). This step should take more caution because a whole film transferring is much harder than patterned polyimide transferring, especially on the edges. So the separation should be really careful to make sure the whole film transferred to the device wafer successfully.

Different from processing with Durimide A112, Kapton® film wasn't etched through to PPC during the patterning process, so the contact openings are not exposed after the transferring. Therefore, another dry etching was performed. As it was no longer CMOS compatible with conductive glue, the etching was

carried out in Alcatel GIR300 F/Cl etcher in MEMS Lab. The etching used SF6 and O2 with a ratio of SF2:O2=10:85 under 50 °C for 35 min. Due to the ununiformed etching, 3 to 5 min of over etching was necessary. The contact openings were exposed then after the etching and the measurement could take place there, shown in Fig. 11 (b).

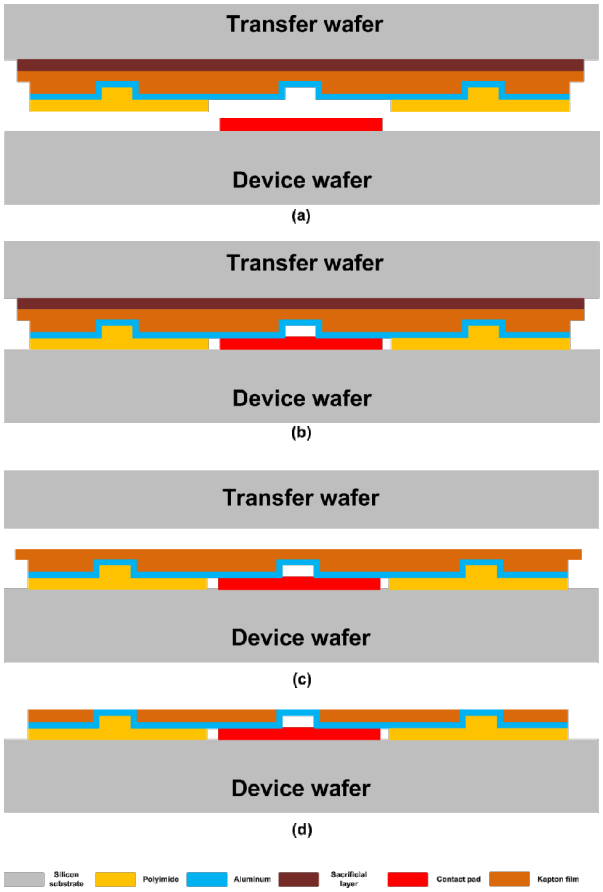


Fig. 10. Transferring flow for flexible interconnect with Kapton® film.

Fig. 11 shows transferred interconnect with Kapton® film. Fig. 11 (a) and (b) presents a large size of a partial modified Daisy Ring structure. Fig. 11 (b) is the transfer contact resistance testing structure. The dark black areas are where conductive glue was placed. After the bonding process, the glue was squeezed and the areas got expanded. The pictures indicate that the transfer contact areas from the sandwich structures were well bonded with the contact pads on the device wafer through the conductive glue. Unlike interconnects with Durimide A112, these interconnects with Kapton® film didn't have that much shrinkage problems and the surfaces were more flat. The polyimide structures are also well shaped because the PPC were protected by the Kapton® film and the polyimide patterning time didn't have to be balanced. But it can be well observed on the picture that the polyimide was under etched and shorter than the patterned Kapton® film, even though the polyimide was designed larger than the Patterned Kapton® film on the mask. This proved the wet under etching issue for polyimide patterning. Though Fig. 11 (c), it is clear that Kapton film has been fully transferred to device wafer, with very few voids.

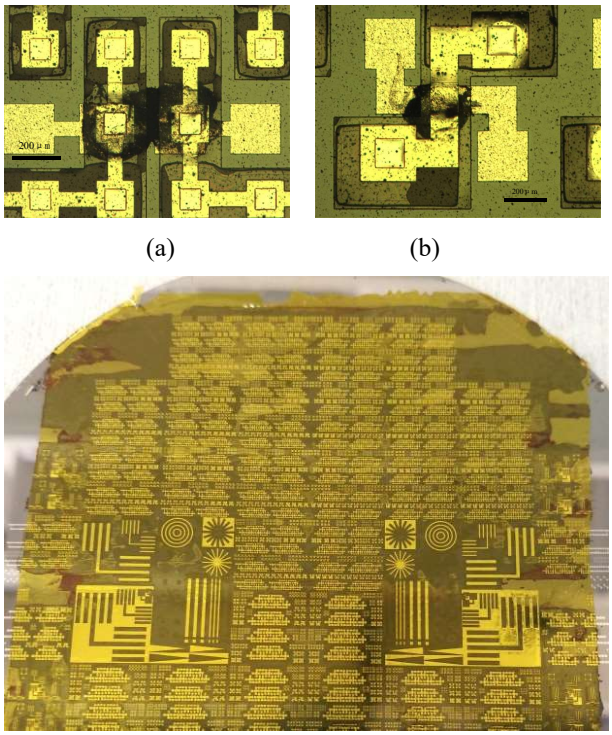


Fig. 11. Microscope observation of transferred flexible interconnect with Kapton® film. (a) Daisy ring structure; (b) Contact resistance structure; (c) Transferred interconnect on device wafer.

IV. RESISTANCE MEASUREMENT

The designed thickness for aluminum pads on device wafer was 4 μm but come out with a result of around 3.48μm. Through sheet resistance measurement, the calculated pad thickness was 3.42 μm. This 0.06 μm measurement deviation could because of the thin self- generated aluminum oxide layer on the aluminum pads, resistivity caused by conductive glue, and possible un-uniform aluminum sputtering on the substrate could also affect the measurement result.

Contact resistance structure was also measured, ranging from 2.14 Ohm/sq to 45.96 Ohm/sq. According to the result, this theory of transferred interconnect from one wafer to another has been proved due to an electrical connection has been observed between the transferred interconnect from the transfer wafer and the aluminum pads on the device wafer. However, the yield of contact through conductive glue need to be further improved. Soldering process, for instance, is worth for further investigation, since it is possible to combine with wafer bonding

For future work, to demonstrate the capabilities of this technology, components (capacitors, resistors, LED die, etc.) with different dimensions and bond pad locations will be integrated in silicon cavities, and then transferred from 2D to 3D with the help of polyimide/aluminum/polyimide flexible interconnects.

V. Conclusion

In this work, flexible interconnects were designed, transferred and tested for heterogeneous integration. Novel flexible interconnect fabrication concepts for heterogeneous integration is to fabricate embedded aluminum layer in between two polyimide layers.

The key processing procedure of such fabrication is to fabricate flexible interconnects on top of sacrificial layer. It has been demonstrated that polyimide precursor is not that compatible with PPC sacrificial material. The shrinkage and misalignment problem is unbearable. Kapton® film, however, has a better compatibility with PPC material and the transferred interconnect theory has been verified via contact resistance measurement. The final transferred interconnects were tested via contact resistance structures combined with metal layer on device wafer and transferred flexible interconnect fabricated on transfer wafer. Through contact resistance measurement, this transfer technique was demonstrated. Future work will be arranged related to device soldering during wafer bonding process.

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