DESIGN OF THE AIP FEEDING LINES FOR 6G APPLICATIONS IN A HIGH DEFINITION FAN-OUT TECHNOLOGY

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by

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This Master's graduation project contains confidential information containing certain technologies that cannot be disclosed in this publication. All sensitive information has been hidden in this version for publishing purposes.

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ABSTRACT

Since 2018, a race on 6G technology between many countries and institutions has started. As 6G mobile communication utilizes sub-THz frequency band, the antenna packaging requires higher level integration. Antenna in Package (AiP) is seen as a promising solution when it comes to the integration problem. At 100GHz operation frequency band, AiP is not only feasible but also mandatory for a high-density interconnect and efficient IC-antenna integration. Current packaging technologies such as LTCC, HDI, and E-WLB, and their feeding concepts limit the possibilities to achieve an optimum for the given silicon and antenna configuration, such as the complexity of the feeding network, the realizable thickness of metal or substrate material, and so on. To overcome these limitations, a novel high definition fan-out technology is investigated. This high definition fan-out technology enables complex-shaped vertical interconnects. Yet there is a lack of research focused on the performance of such interconnects as well as the impact of its manufacturing process on the RF performance.

This thesis work is aimed to provide a scope of how the high definition fan-out technology benefits the performance of an AiP by applying coaxial structure as an antenna feeding path in such a package. This new feeding concept is aimed to optimize the interface structure between the RF front end in silicon and the antenna array in the same package, to reduce the routing size, reduce the insertion loss between the antenna array and the silicon interface, and increase the isolation between the two adjacent feeds. An initial model is fully parameterized for performance improvements via tuning. A benchmark model built up by the traditional laminate technology with vias is compared with the performance of the proposed feeding structure regarding matching, insertion loss, and port isolation. The presented model achieves 0.25dB insertion loss, 25dB return loss and 80dB isolation. Compare to the benchmark model, on average, the model from the high definition fan-out technology has significantly decreased the insertion loss, and increased the channel isolation, while maintaining a similar return loss.

The impact of this high definition fan-out technology's manufacturing process on the model performance is discussed through parameters' sensitivity analysis and system robustness. The robustness analysis shows this feeding system has acceptable reliability if the manufacturing error can be restricted within 10%, and it has good reliability if the manufacturing error can be restricted within 5%.

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ABBREVIATION

MEO mid-earth-orbit

LEO low-earth-orbit

PCB printed circuit board

AoC antenna on chip

AiP antenna in package

LTCC low temperature co-fired ceramic

HDI high-density interconnect

E-WLB embedded wafer level ball grid array

CPW co-planar waveguide

MC mold compound

RDL redistribution layers

BCB benzocyclobutene

TEM transverse electromagnetic

PTH plating through hole

CMOS complementary metal–oxide–semiconductor

SIC substrate integrated cavity

GWG gap waveguide

SIW substrate integrated waveguide

WLAN wireless local area network

UWB ultra wide band

IPD Integrated passive device

EMC epoxy-based molding compound

MoM method of moments

FDTD finite difference time domain method

FEM finite element Method

FIT finite integration technique

1 INTRODUCTION

1.1 MOTIVATION

Looking back to the last four decades, mobile communication has been developed rapidly from the first generation (1G), where analog communication is applied to transfer only voice signals, to the fifth generation (5G), where the mmWave is utilized to realize high-speed data transmission.

Moving towards 2030 and beyond, due to the fast growth of new technologies such as virtual reality, vehicle-to-X network, unmanned aerial vehicle network, mid-earth-orbit (MEO), and low-earth-orbit (LEO) satellite network, and oceanic information network, the 5G communications would become insufficient [1]. The new application scenarios will require a much wider bandwidth and a larger area coverage, for which the higher frequency band needs to be applied.

Thus the sixth generation (6G) mobile communication is required to be investigated in order to meet the technical requirements of the new application scenarios. To obtain a wider bandwidth to increase data rates and network capacities, sub-terahertz spectrum above 90GHz will be applied for 6G mobile communication. However, with such a high operational frequency band, the electronic components on a mobile device and the manufacturing process will face several major challenges as well. As the signal wavelength is getting much smaller, the electronic components will need to be smaller correspondingly, furthermore, a higher level of component integration will be another important topic as well.

The traditional PCB technology can only reach a minimum trace width/gap around 100-200um, which will not be enough for signal transmission over 90GHz, thus seeking an alternative technology, which can provide a smaller size and better integration is crucial for both research and realization of 6G mobile communication. Antenna feeding, packaging, and inter-connections are all important factors that should be considered when it comes to an active integrated antenna system. This thesis will focus on realizing a high-performance antenna feed, regarding reflection and isolation, in a 6G mobile communication scenario.

At operation frequency bands above 100GHz, antenna on chip (AoC) or antenna in package (AiP) are not only feasible but also mandatory to realize higher integration. The AoC integrates antennas with front-end circuitry on the same chip manufactured using mainstream silicon technologies. However, AoC usually has very low radiation efficiency and very limited space on the chip, thus AoC is not an ideal solution in many cases [2] [1].

As a great alternative to AoC, AiP technologies can provide higher radiation efficiency and much wider bandwidth [1], which makes it more popular than AoC. AiP integrates chips and front-end circuits and makes them a surface mount chip-scale device, it can significantly increase the integration level.

From the manufacturing perspective, novel packaging technologies are also desired to adapt the high integration requirements. High definition fan-out (HDFO) technologies are promising fabrication technologies that can significantly reduce the routing size, however, it is still in the developing phase, so the performance, reliability and manufacturing error, etc. are mostly still unclear.

1.2 PROBLEM FORMULATION

This project is aimed to optimize the interface structure between the RF front end in silicon and the antenna array in the same package for 6G applications, to reduce the routing size and the insertion loss between the antenna array and the silicon pad, and the isolation between the different channels.

Current package technologies and their feeding concepts limit the possibilities to achieve an optimum for the given silicon and antenna configuration. To overcome these limitations, a novel HDFO technology will be used.

Currently, the research on AiP is mainly focused on LTCC, HDI, E-WLB, and so on, but they have limitations with respect to vertical integration. In most situations, only via interconnects are possible, which may cause more loss when higher frequencies are applied. In comparison, the HDFO technology provides more possibilities to create complex shaped vertical interconnects such as actual coaxial structures. Theoretically, a coaxial structure not only can provide better isolation on the signal path, it can also realize a more smooth impedance matching at the impedance discontinuous part, simply by tuning the dimension of the coaxial.

However, it is not yet clear how different variations in the manufacturing process of such a new fabrication method may impact the RF performance. The major challenges in the feed design in this technology that will be addressed in this thesis are (i) to model the feeding structure from the RF chip output to a patch-like antenna element for reliable performance under the impacts of the fabrication process, (ii) to evaluate the robustness of the system against small variations on the important dimensions of the model.

1.3 RESEARCH APPROACH

This thesis work is mainly divided into three parts, which are the literature study, the modelling, and the manufacturing impact study. A step-by-step overview can be seen in Figure 1.1.

The literature study contains a basic introduction to the current AiP technology, including the fabrication technology of LTCC, HDI, E-WLB, and HDFO. The regular antenna type and interconnect form are also briefly discussed in this section, and common concepts of antenna feeding in a package are explained.

A benchmark model designed by the traditional laminate method is used to compare the electrical performance with the HDFO model. The key performances to be focused on are the insertion loss, return loss, and isolation between two adjacent feeds. Followed by the benchmark model study, the actual HDFO feeding model is being parameterized. The AiP model of this thesis work is mainly operated in Ansys HFSS, the model is fully parameterized for tuning purpose. The main parameters involved in this process are the ones that directly affect the feeding impedance, key parameters can be seen in Table 3.2 in Chapter 3.

The model is tuned to meet the performance requirements before doing the investigation of the manufacturing impact. As the process uncertainties of the HDFO technologies are not known, this step is intended to give a general conclusion of the impact on the package performance of manufacturing tolerance according to this case study. To achieve this goal, sensitivity analysis and robustness analysis are performed. Sensitivity analysis is performed to provide a scope of how a single parameter of the model impacts the model performance, meanwhile, the robustness analysis represents a more realistic scenario where all the parameters have a small variation and their total influence on the performance.

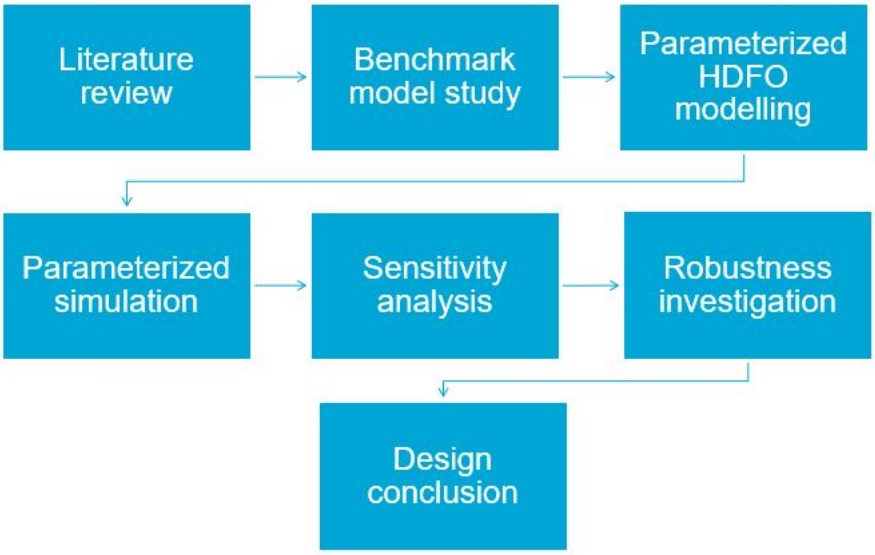


Figure 1.1: Thesis workflow

1.4 NOVELTY

The above mentioned work flow is intended to provide a clear vision of how HDFO technology improves performance of a particular AiP application through the case study of the AiP feeding model. The novelty of this thesis is addressed as follows,

- This work provides the first-time comparison between the tradition laminate and HDFO technology through a case study.
- This work provided first research of a coaxial feeding structure in AiP at 92GHz-100GHz.
- This work corrected an impedance deviation in co-planar waveguide (CPW) to coaxial transition in high frequency.
- This work provides a design reference for the feeding model regarding to operation frequency tuning.
- This work provides a general vision of the impact on the package performance of manufacturing tolerance. The manufacturers can also see this as an manufacturing error requirements.

1.5 STATE OF THE ART

1.5.1 AiP Technology

While 5G technology has gradually been applied in our daily applications, the research for 6G technology has been quickly initiated worldwide. One of the key concept to achieve high speed communication in 6G mobile communication is to utilize higher frequency bands, for example sub-THz band(100GHz-300GHz) and THz band(3THz - 10THz). Such high operation frequencies can provide much wider frequency band even than 5G [3].

Together with the benefits, high operation frequency also brings difficulties when it comes to packaging. Most of the traditional packaging methods are no longer applicable to sub-THz and THz radios. Sub-THz or 6G communications focus on heterogeneous package integration by incrementally advancing the system components such as precision antenna arrays, low-loss interconnects and waveguides and active devices[4]. A lot of challenges related to multi-mode excitation, radiation, reflection and loss, which affects the electrical performance significantly will appear. And most of these problems are associated with the dimension and integration level of the package. Thus it is very important in 6G applications to find a perfect solution to bring the RF packaging to a higher integration level.

One widely accepted and well-investigated solution for high packaging integration is Antenna-in-Package(AiP) technology. AiP technology has been widely adopted for 28GHz 39GHz 60GHz 5G applications, 60GHz gesture radars, 77GHz automotive radars, 94GHz phased arrays, 122GHz imaging sensors, and 300-GHz wireless links[2], more detailed description of most common AiP applications can be found in [2]. Apparently AiP technology holds a huge potential of being the solution for 6G mobile communications. An overview of the AiP technology can be seen in Figure 1.2.

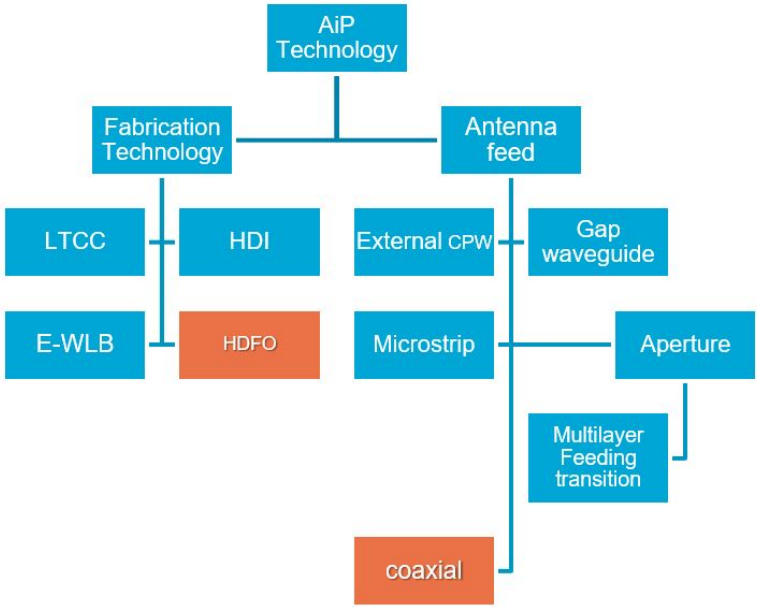


Figure 1.2: AiP Technology overview

AiP technology usually describes an RF package which contains an antenna (panel) with a transceiver die in a standard surface-mounted device. Three widely used AiP fabrication methods are low temperature co-fired ceramic (LTCC), high-density interconnect(HDI), and E-WLB (embedded wafer level ball grid array).

LTCC technology technology is a way to manufacturer multi-layer circuits from ceramic substrates. A typical LTCC device consists of multiple dielectric layers, screen-printed or photo-imaged low-loss conductors, embedded baluns, resistors and capacitors and via holes for interconnecting the multiple layers. A basic introduction for the process of LTCC technology can be seen in [2]. LTCC technology provides good thermal conductivity, high passive integration and low-loss substrate [2]. However there are some major problems that limits the capability of LTCC technology. During the firing process there is tape shrinkage of between 12% to 16% that usually occurs at X and Y dimensions. [5] Due to firing process, the printing screen is not reproducible with different characteristics after cooling, which remains the package producing process very expensive, thus it is difficult to realize mass production.

HDI technology offers the finest trace structures, the smallest holes and Blind Buried Vias. HDI technology allows sequential lamination with dielectric materials and conductor wiring for a higher density of routing. Compare to LTCC technology, it is more suitable for mass production due to its relatively low cost. However, there are some drawbacks of HDI technology as well, [6] gives a good explanation on the advantages and disadvantages of HDI PCB. Firstly, HDI PCB contains many via holes, which are sensitive regarding the shape and size, other components may give unwanted thermal stress on vias to cause inaccuracy on the performance; besides expansion of material in z-axis stresses the vias as well. Secondly, the aspect ratio(the division of material thickness by hole diameter [6]) of blind vias limits the dimension of the via holes as well as the material selection, to fulfill the limitation of aspect ratio, sometimes the manufacturers has to use very thin prepregs, it increases the complexity of the manufacturing process and also brings a negative impact on the reliability of the PCB. Furthermore, the fiber glass in the prepregs is another risky factor to the manufacturing process of placing via holes, the glass may cause a offset on the laser direction and lead to a change on the via hole shapes.

E-WLB is one of the fan-out wafer level technologies that is adaptive to modern semiconductor chips. E-WLB technology utilizes a wafer reconstruction process when the known good dies from the original device wafer are picked and placed on a carrier and then encapsulated with mold compound (MC) to make an artificial wafer. It eliminates the need for a laminate substrate and replaces it with copper redistribution layers (RDLs). Polymers, such as benzocyclobutene (BCB), are used for the electrical isolation between the metal layers. This technology is also a good alternative to realize mass production. The disadvantages of this technology are : inspection and repair difficult since visual inspection is restricted; mechanical stress between package and board is transmitted stronger than for other package technologies.

A more detailed summary about the trade off between the above mentioned 3 technologies can be found in [2].

	Advantages	Disadvantages
LTCC	Good integration, low loss substrate	Expensive, printing screen not reproducible
HDI	Low cost, variety choices for dielectric	Limited choices for metal material
EWLB	Low cost, good integration, high number of interconnects	Inspection and repair difficulty, high mechanical stress
HDFO	Good integration, flexible interconnectio	Structure offset

Table 1.1: Comparison Between the mentioned 4 types of AiP fabrication process

Antenna selection is another important consideration whiling designing AiP. Patch antenna (array) is one of the most widely used antenna type in AiP designing, the designing methodology of patch antenna aligning with AiP technology is well investigated and developed. Some examples can be seen in [7] [8] [9]. Patch antenna provides an easy surface mounting and high integration possibility.

Yagi-Uda antenna consists of parallel metal line driver, reflector, and director on a substrate, it creates an end-fire radiation pattern. Frid antenna consists of rectangular metal loops on a grounded substrate and fed against the ground at a proper point. Together with patch antenna, these are the three most widely used antenna types in AiP. Figure 1.3 [2] illustrates a comparison among these antennas.

Horn antenna is less common in AiP designing but it still provides practical value in some cases. A step-profiled corrugated horn antenna designed by Tajima et al.[10] operated at 300GHz turned out to provide great bandwidth(100GHz) [10].

Antennas	Description	Pros	Cons	Uses
Patch 	The patch antenna is a piece of metal on a grounded substrate and fed against the ground at a proper point.	• Compact • Lightweight • Low profile • Conformal • Polarization diversity • Multiband • Ease of ESD	• Narrow impedance bandwidth • Low power handling capability • Warpage	• Base station • Mobile phone • Radar • Imager • AR/VR
Yagi-Uda 	The Yagi-Uda antenna consists of parallel metal line driver, reflector, and director on a substrate.	• Compact • Lightweight • Low profile • Wide impedance bandwidth • Good front-to-back ratio	• Non Polarization diversity • Low power handling capability • Sensitive to its location on PCB	• Mobile phone
Grid 	The grid array antenna consists of rectangular metal loops on a grounded substrate and fed against the ground at a proper point.	• Compact • Lightweight • Low profile • Wide impedance bandwidth • High gain • Low cross polarization	• Narrow gain bandwidth • Low power handling capability • Pattern squint	• Radar

Figure 1.3: Most used antennas in AiP [2]

Besides antennas, another designing consideration that is critical to AiP performance is the interconnections. The typical ways to connect die and antenna panel are vias, bonding pads, traces and wires.

For horizontal interconnection in the same layer, traces such as CPW and microstrip are often used, transmission lines usually give very good performance with low loss.

For vertical interconnection in different layers, wires and vias are usually used. There are two major techniques to build wires and bumps, one is wire-bonding and the other one is flip-chip technique [2]. The wirebonding technique is proved to be robust and inexpensive through many practical applications already. Furthermore, it is also tolerant to chip thermal expansion, which makes it more reliable. The flipchip technique usually provides better electrical performance than the wire-bonding technique, since the bump usually has shorter length and bigger diameter.

A coax via is worth mention here since it is the most reliable vertical transition between traces on different layers[2]. The coax via is a group of vias distributed in a way that resembles a coaxial cable, in which a center via places in the middle that works as inner conductor while a few of ground vias placed around the center via that works as the outer conductor. Just like a coaxial cable, coax via supports the transmission of the dominant transverse electromagnetic (TEM) mode. The coax via should match not only the impedance but also the mode distribution of the connected lines [2].

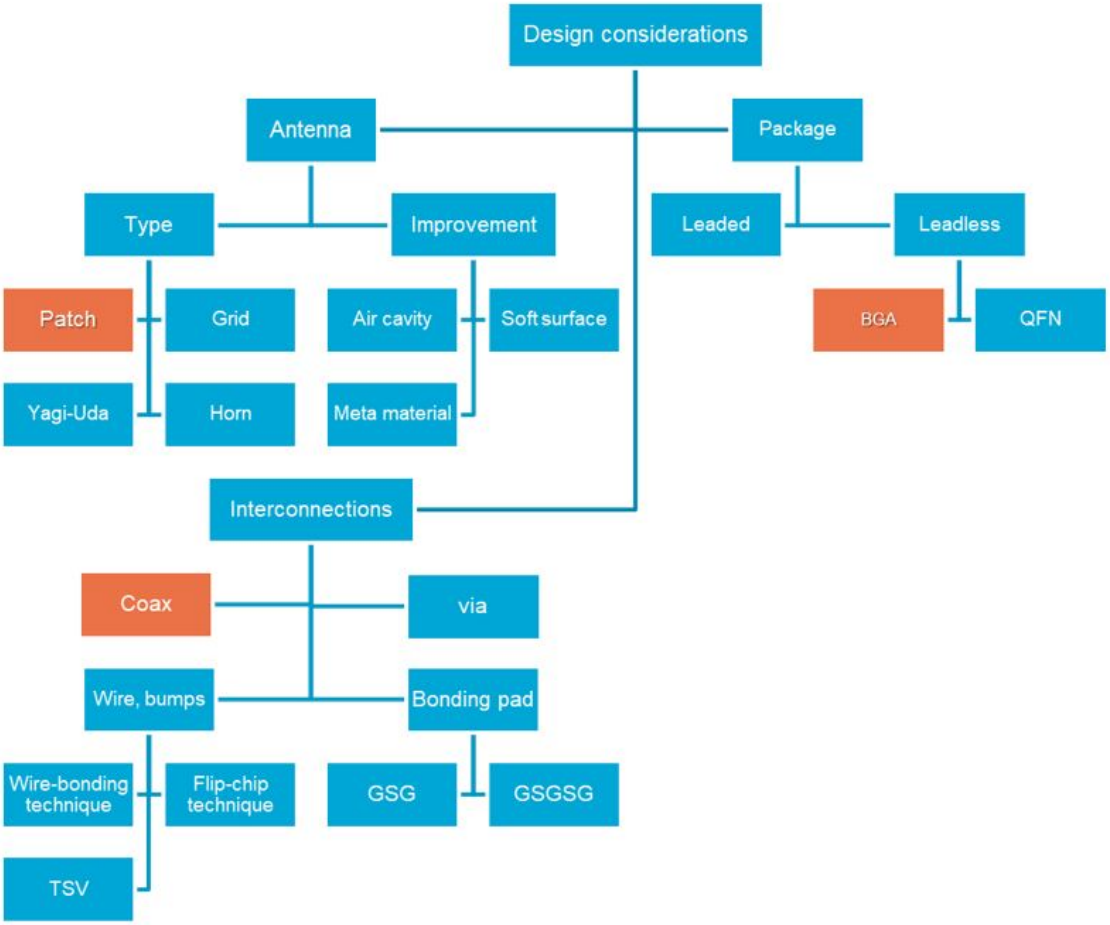


Figure 1.4: AiP design considerations

The coax via has been investigated in many literature including [11] [12], coax via has similar features and functions as a real coaxial line. However it is not easy to realize coaxial structure as interconnect in a package in the traditional technologies for mass production, thus a real coaxial interconnect would worth our attention when it is possible to manufacture.

A coaxial plating through hole (PTH) proposed in [13] have achieved performance improvement for a laminate PCB by replacing the normal PTH with coaxial structured PTH. Figure 1.5 shows the structure of conventional PTH and proposed coaxial PTH. The research shows coaxial PTH does provide a better impedance matching and lower insertion loss. This very recent study is a very strong proof that using actual coaxial structure as interconnect is of great potential benefits of improving the performance.

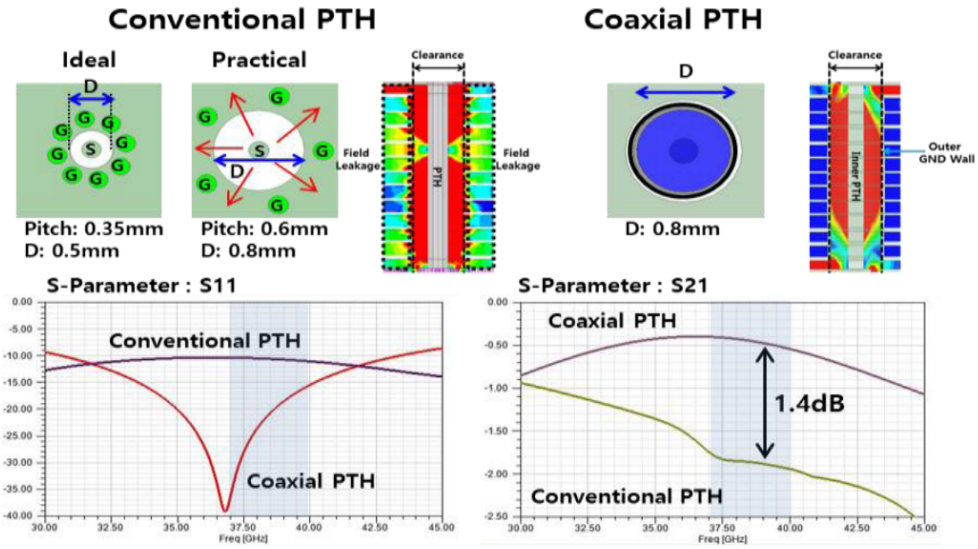


Fig. 3. Simulated performance of vertical transition (conventional vs. proposed). Impedance matching (S11) (left), insertion loss (S21) (right).

Figure 1.5: Coaxial PTH and coaxial via comparison[13]

1.5.2 Antenna Feeding Method in AiP

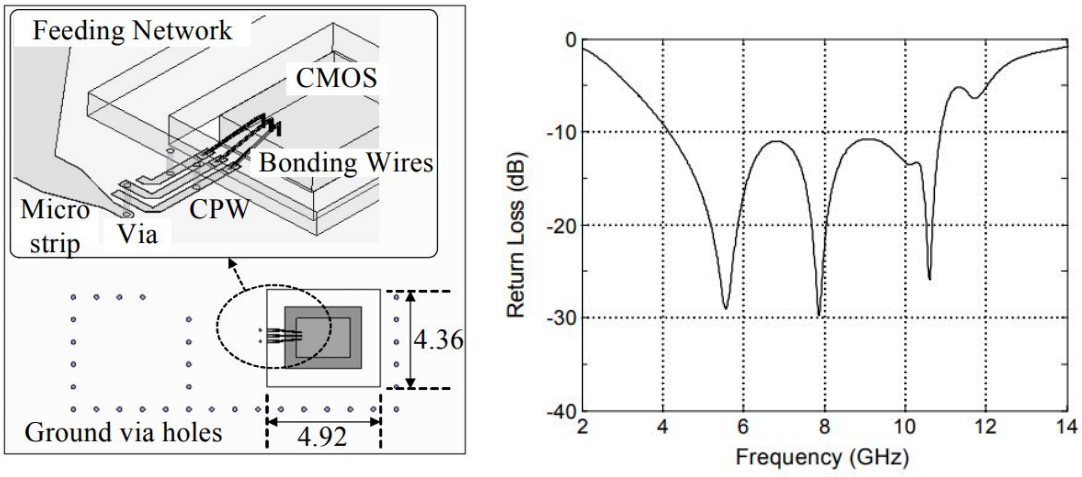
A variety of feeding structures applied in AiP technology can be found in recent research papers, they are usually a complex network which involves the combination of few interconnect methods such as wires, vias, and few transmission lines such as CPW, SIW, and microstrip. Typical feeding network concepts including pin/transmission line feeding network, aperture/slot feeding network and hybrid feeding network are discussed in this section. Table 1.2 illustrates the main pros and cons of each feeding method. A typical feeding network and their performance for each type have been briefly described below.

antenna feeding method	advantages	disadvantages
Pin/transmission line feeding	applicable for most cases, easy to achieve good matching	needs relatively larger space
aperture/slot feeding	simple structure, suitable for both low frequency and high frequency applications	channel isolation is low
hybrid feeding	easier to reach a larger bandwidth, good matching	complex structure

Table 1.2: Comparison between feeding methods

A. Pin/ transmission line feeding is one of the most common concept. It can be found in a lot of designs for example in [14], [15] [16] [17]. A bottom view if an LTCC package and feeding network proposed in [14] is shown in Figure 1.6a, this feeding network in Table1.3 is referred as A-1. The package has 3 layers, the antenna is placed on the

middle layer and the feeding network is placed on the bottom layer. Feeding network on the bottom layer consists of microstrip line, via, CPW and bonding wires. The CMOS die firstly connects to the CPW through bonding wires, then the signal transits to the feeding microstrip line by a via, antenna panel is then excited by the microstrip line. Bonding wires can be easily applied in this design due to the internal space difference in different layers. This package occupies a space of $20 \times 20 \times 1.3mm^2$. The operation frequency is between 4 to 10GHz. The calculated return loss is shown in Figure 1.6b, it has 3 resonant frequencies between 4GHz to 12GHz.



(a) Feeding network **(b)** Return loss

Figure 1.6: A typical feeding network in AiP[14]

Another typical example is an external CPW feeding with SIW structure proposed in [15], this feeding network in Table1.3 is referred as A-2. The configuration can be seen in the figure below. This design has a relatively less complex structure. The feeding network is completely placed underneath the antenna array, SIW and CPW are placed on the layer below the antenna array with a feeding line extension. In this way the feeding structure does not add extra space for the antenna array horizontally. The return loss of this design is shown in Figure 1.11.

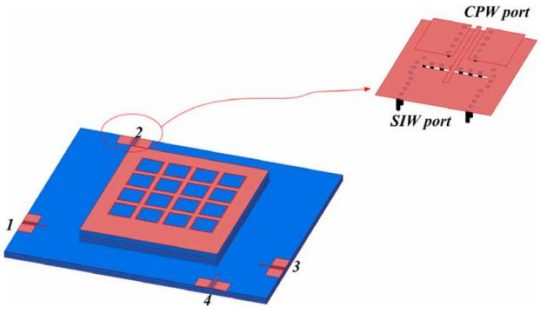


Figure 1.7: External feeding network [15]

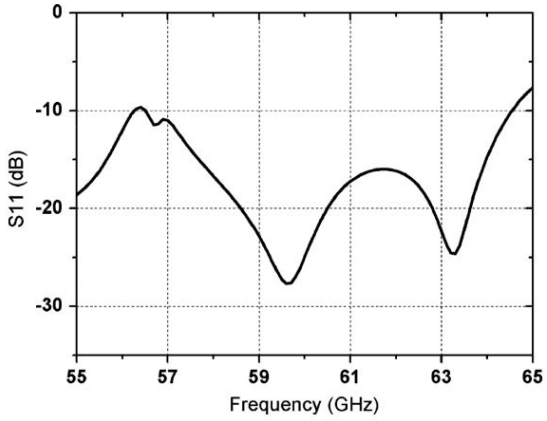


Figure 1.8: S11 performance of the external feeding network

B. Aperture coupled feeding network is another very popular feeding methods. This type of feeding network usually has a relatively simpler structure. [18] [19] [20] are three typical examples. The aperture feeding network proposed in [18] can be seen in Figure 1.9, this feeding network in Table1.3 is referred as B. This feeding network added a planar feeding transition above the feeding aperture, which provides a matching section from the aperture of the external waveguide to the radial line. Via fences are applied around the transition to suppress the leakage. This structure achieves S11 less than -10 dB over a wideband between 263 GHz to 273 GHz (approximately). Aperture feeding is suitable for both low frequency applications and high frequency applications. However it does not always guarantee a good isolation if there are multiple channels at close distance.

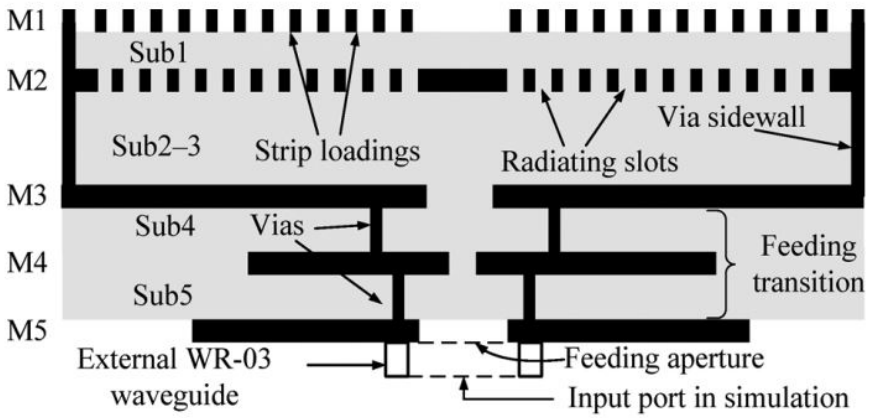
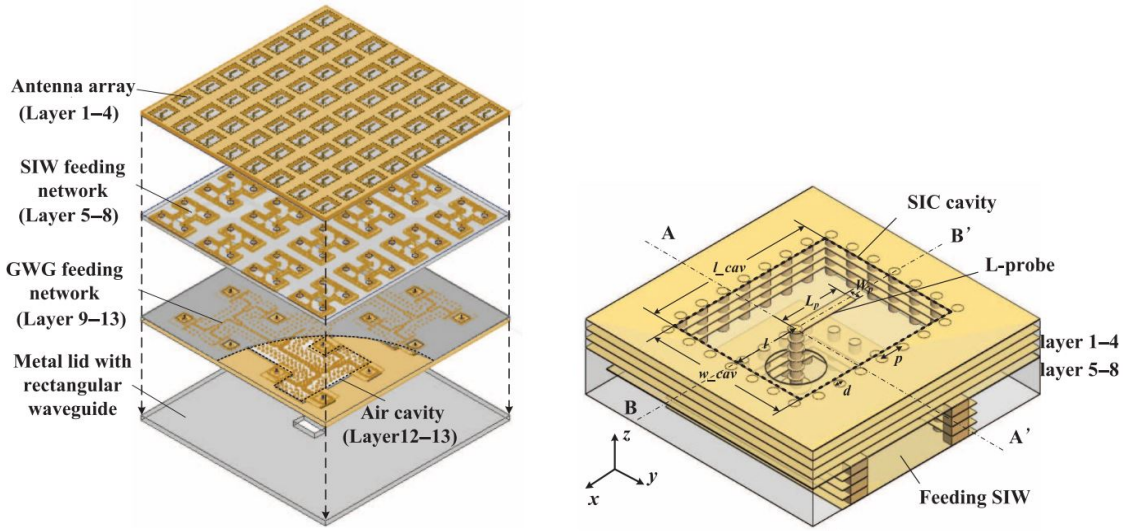


Figure 1.9: An aperture feeding network with extra transition structure

C. Hybrid feeding network usually includes multiple feeding structures on multiple layers in a package, it usually has more complexity and less feeding loss. [21] [22] are typical examples for hybrid feeding network. in [22], a vertical structured antenna array and feeding network based on multi-layer LTCC technology is proposed, this feeding network in Table1.3 is referred as C. This design uses substrate integrated cavity (SIC) antenna and a two layers feeding network. As shown in Figure 1.10a, the first layer of

feeding is gap waveguide (GWG) feeding network and the second feeding network is a substrate integrated waveguide (SIW) feeding network. The SIC is finally excited by a L-probe from the SIW network, as shown in Figure 1.10b. Each of the SIW section (Figure 1.10b) occupies an area of $1.8mm \times 1.5mm$. The return loss is of this feeding network is shown in Figure 1.11. As seen from this example model, the hybrid feeding network has relatively more complicated structure, and it is more suitable to packages that have more layers.



(a) overview of the feeding network **(b)** close-up view at the probe

Figure 1.10: A probe feeding network[22]

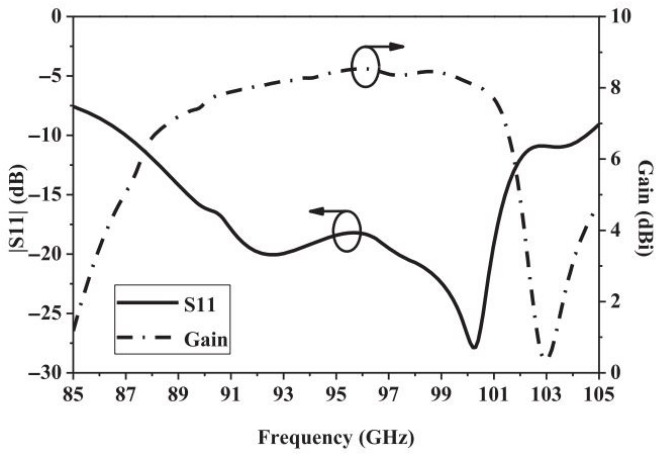


Figure 1.11: S11 performance of the probe feeding network[22]

Furthermore, another interesting feeding network design proposed in [23], for dual polarized patch antenna focused on high polarization isolation is worth mentioning here. This feeding network in Table1.3 is referred as D. There are three stacked patches placed in 3 layers to achieve dual-band operation. lower large patch fed by the middle patch operates the lower band(27.48GHz to 28.50GHz). the middle and upper patches together works on upper band(36.94 to 40.43GHz). To increase the polarization isolation

in the lower band, a shorting pin connecting the lower patch and ground is applied. The structure can be seen in Figure 1.12. This feeding network has very similar structure with the HDFO feeding model that will be discussed in the later chapters. They both aim to achieve a high isolation. However, the model in [23] utilizes vias while the HDFO model utilizes coaxial. The average isolation loss achieved in this model is about 25dB.

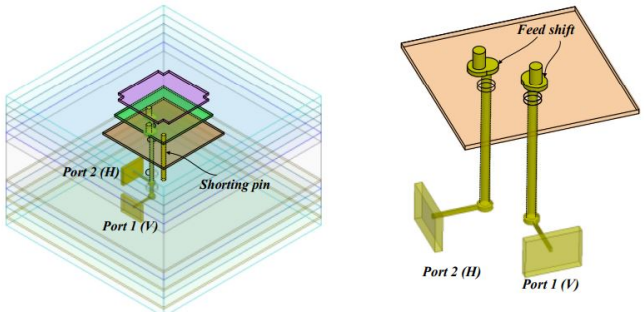


Figure 1.12: High polarization isolation feeding design[23]

A summary of the performance of above mentioned feeding methods in AiP can be seen in Table 1.3. Note that in this table, the performance (S11, bandwidth, isolation) refers to the performance of the package, not only the feeding the structure.

feeding method	S11 bandwidth(-10dB)	frequency band	complexity	isolation
A-1	6.73GHz	4.15Ghz-10.88GHz	medium	
A-2	10GHz	55GHz-65GHz	low	20dB-40dB
B	10GHz	263GHz-273GHz	low	
C	16GHz	87GHz-103GHz	high	
D	4.5GHz	27.5GHz- 28.5GHz, 37-40.5GHz	medium	25dB

Table 1.3: Performance comparison between the above method [14] [15] [18] [22] [23]

In conclusion, the pin/transmission line feeding network has relatively simple structure, but it can take more space in a package. The slot/aperture feeding are applicable for both low frequency and high frequency applications, but the isolation will not be as good. The hybrid feeding method usually achieves good matching and are more flexible to be tuned to have larger bandwidth, but the structure can have more complexity. In most AiP designs, the isolation loss between two polarization channels normally achieves 20dB - 40dB.

1.5.3 Limitations and Challenges

Research against AiP fabrication technology are mainly focused on LTCC technology, HDI technology and E-WLB technology, there is a lack of study on the new raising high definition fan-out technology.

While considering an AiP, the interconnects choosing is very important since it directly relates to the loss on the signal pass and the feeding method. The coax via seems to be a very promising structure as interconnect in a package according to many researches mention in previous section. However, instead of a coax via, a real coaxial structure will theoretically works even better, and this topic is worth investigating.

Besides the interconnect, the routing size is also another limitation for 6G application. The above mentioned feeding structure usually has a complex network. Built a simpler feeding structure and reduce the size to a suitable integration level for sub-Thz is another challenge.

1.6 THESIS STRUCTURE

The 2nd chapter gives a detailed description of the HDFO feeding model in HFSS and HFSS simulating mechanism, in order to validate and verify the reliability of the thesis work based on this model and this EM modeling tool.

The HDF model optimization process and results are given on Chapter 3, where the parameterized model has been described first, following with optimization method and results. In the end, the overall performance is compared with the benchmark model where the traditional laminate method is applied.

The 4th chapter investigated the impact of manufacturing tolerance on the model's electrical performance by giving the results of sensitivity analysis of each parameter and robustness analysis of the whole system. Sensitivity analysis provides the information of how a specific parameter impacts the feeding performance, while robustness analysis provides the information of how the parameters will affect the performance when all of the parameters have fluctuations at the same time.

In the end, conclusions regarding the overall performance of the HDFO based antenna feed on this thesis work is given on the 5th Chapter.

2 SIMULATION APPROACH

2.1 PHYSICAL MODEL DESCRIPTION

The HDFO technology explored in this thesis is a proprietary, non-disclosed technology. The aim of this thesis is to investigate the suitability of such technologies for AiP realisation for 100 GHz applications. Thus throughout this thesis, no detailed information on actual designs and sizes can be given.

The AiP feeding model based on the HDFO technology has a unique structure due to its manufacturing process as described in the previous chapter. Every part of the feeding path has one inside dielectric layer and one outside copper layer. The copper layer always covers the top and side of the dielectric layer but does not always cover the bottom.

The main material used in this AiP model involves copper, EMC, and dielectric material. The main substrate material used in this package is one of the epoxy-based molding compound materials, EMC.

The chip is designed by NXP SiGe technology, the top layer of the die faces up to the 1st layer coaxial feeding network, a microstrip is placed between two vertical interconnects to increase the flexibility with respect to the antenna feeding point. An illustration for the overall structure of this feeding network can be seen in Figure 2.1

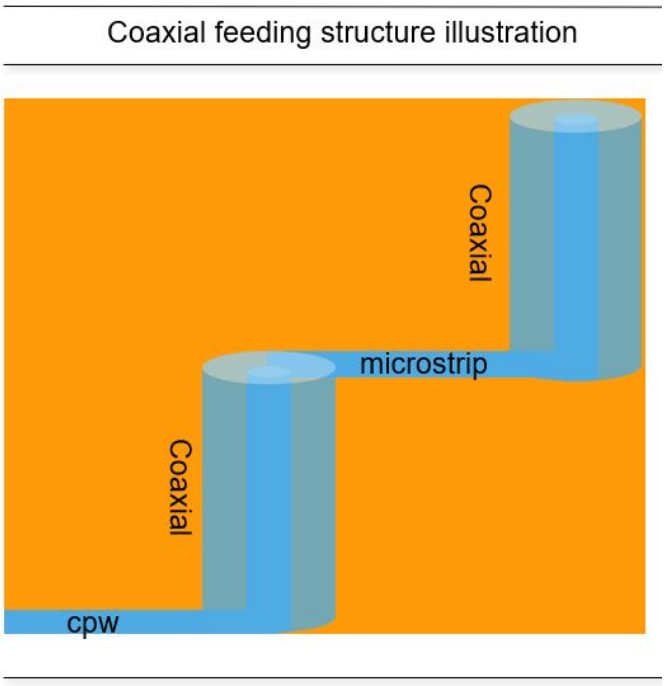


Figure 2.1: Feeding network illustration

2.2 HFSS MECHANISM

2.2.1 HFSS solver

The most commonly used EM simulation solvers are mainly based on 4 modeling techniques: the method of moments(MoM), the finite difference time domain method(FDTD), the finite element Method(FEM), and the finite integration technique (FIT). A general introduction of the above-mentioned methods as well as some other modeling approaches and the software where it is applied can be found in [24].

Among the most popular EM simulation software, Ansys HFSS uses a 3-D full-wave frequency domain electromagnetic field solver based on the finite element method (FEM). FEM is a method based on solving partial differential equations. It is most commonly formulated based on a variational expression. It subdivides space into elements, for example, tetrahedron. Fields inside these elements are expressed in terms of a number of basic functions, for example, polynomials. These expressions are inserted into the functional of the equations, and the variation of the functional is made zero. This yields a matrix eigenvalue equation whose solution yields the fields at the nodes [24]. The accuracy of FEM is discussed in [25], [26]. In general, the FEM method gives quite an accurate field calculation results.

2.2.2 Meshing Approach

In HFSS, the initial mesh is generated by default using geometry as tetrahedral mesh elements. These mesh elements in combination with the adaptive mesh procedure create a geometrically conformal, and electromagnetically appropriate mesh for any arbitrary HFSS simulation.

HFSS uses tetrahedral mesh elements to make elements calculation. However it cannot fully represent the volume of a true surface structure, thus a volume perturbation technique to automatically correct for the reduced volume represented by the mesh, an introduction of such a volume perturbation can be found in[27].

Additionally, HFSS provides a lambda refinement function, which is a meshing process, where all the tetrahedrons are smaller than a certain fraction of wavelength, it provides a minimum mesh density over all objects. In this model, the target fraction value is 0.3333. The meshing elements of different simulations involved in this project varies due to the difference of the components' dimension. The number of meshing elements is usually between 150,000 to 230,000.

2.3 HFSS MODELLING

2.3.1 General description of HFSS model

The parameterized model is built on AnsysHFSS. The package contains antenna feeding, chip, and a few other silicons behind the chip. The chip and other structures below the chip are simplified to material boards. The chip interface is simplified to CPW as the input of the feeding network.

The first layer coaxial connects the signal trace, a coplanar waveguide from the chip to the second coaxial layer through a via. The following layers of the coaxial interconnect are straight forward to each other, with a small center offset in between each other due to manufacturing reasons. A micro-strip line is applied between the two coaxial interconnects, to make feeding point tuning on the patch antenna easier and more flexible. The second coaxial interconnect connects to the antenna.

Table 2.1 lists the used materials in the em simulation. Copper material is used in the model as main conductor material, such as on signal trace of CPW and microstrip line, the outer conductor of coaxial feeding. PEC material only used for port settings.

	Material	Applied Part
1	copper	signal trace, coaxial conductor
2	Core	via core material
3	EMC	feeding coaxial dielectric
4	PEC	GND

Table 2.1: Main material used in the model

2.3.2 Port verification

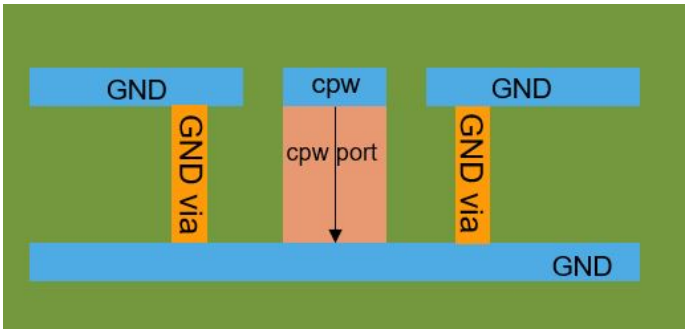
For each channel in this feeding network, one port locates in the end of CPW from chip and the other one in the end of the last layer of coax.

Even thought, most of the time a wave port will be applied to a transmission line, in this case a lumped port is more suitable for this CPW end. The lumped port applied here firstly can provide an accurate input impedance of 50Ohms to give a good representation for the chip input, secondly it avoids the parasite field that can be created by a metal cap when Wave port is applied. The lumped port at the CPW end can be seen in Figure 2.2a.

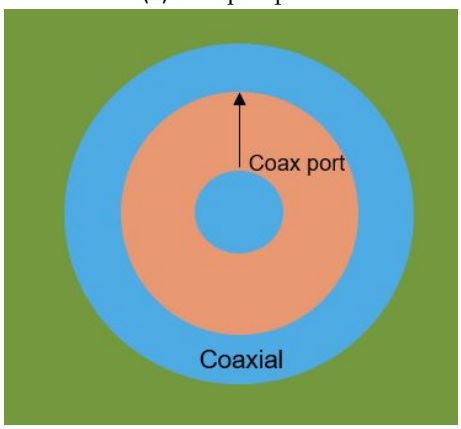
For the coax feeding, firstly the electromagnetic modes need to be considered. The feeding coax roughly has a dimension of inner conductor diameter d, outer conductor diameter D, the dielectric material has relative permittivity of ϵ_r. The cutoff frequency of the second propagation mode - TE11 can be calculated as follow,

$$\lambda_c = \pi(\frac{D+d}{2}\sqrt{\mu_r\epsilon_r}) \qquad f_c = \frac{c}{\lambda_c} \tag{2.1}$$

The cutoff frequency for a coaxial structure in such a dimension is around 500GHz, which is far beyond the operation frequency. The only propagation mode is TEM mode in this case, thus no higher order mode needs to be considered. A simple wave port is applied at the cross-section of the coaxial end. The wave port at the coaxial end can be seen in Figure 2.2b.



(a) Lumped port



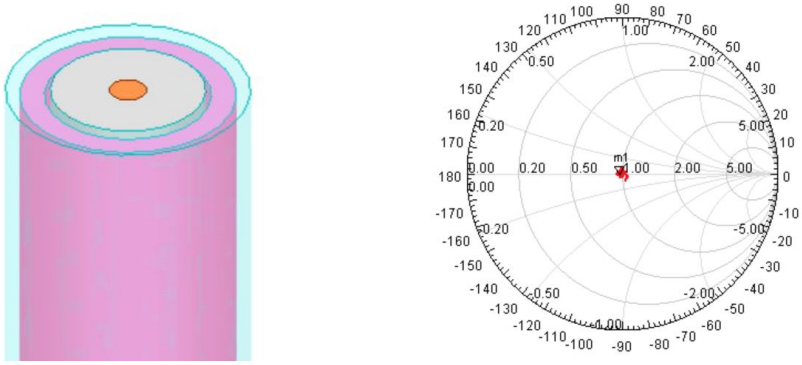
(b) Wave port

Figure 2.2: Two port types

To verify HFSS provides field results without major errors, a single coaxial cable with the same dimension as the coaxial port mentioned above is simulated and calculated at the same time to compare the impedance results. For a coaxial cable with inner conductor diameter d, outer conductor diameter D, dielectric constant ϵ_r its impedance can be calculated as,

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu_0\mu_r}{\epsilon_0\epsilon_r}}ln(\frac{D}{d}) \tag{2.2}$$

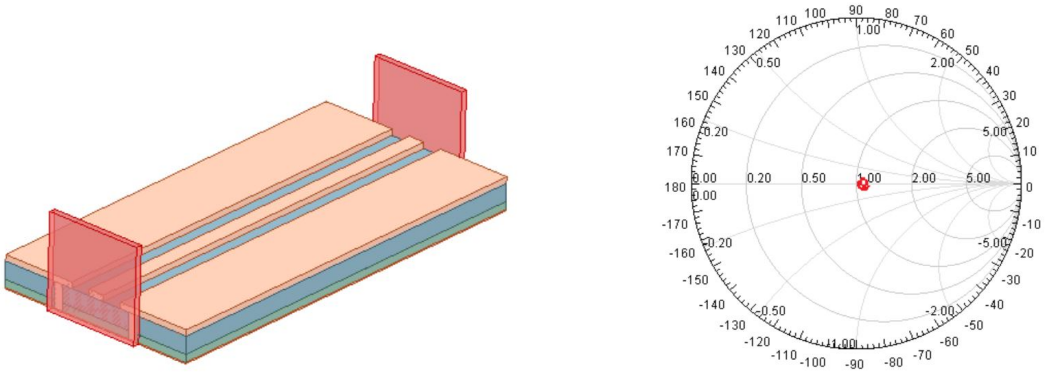
Such a coaxial cable is built in HFSS, as seen in Figure2.3a, this coaxial follows the same layer-by-layer structure as in the feeding model, the simulation in HFSS also shows the impedance nicely matches at 50Ohms, as seen in Figure2.3b. For Since the major parts of the feeding model is of such a coaxial structure, we can say that this simulation environment gives a reliable results. Regarding the impedance expectation, an derivation is observed when the signal passes through CPW to coaxial, it will be discussed in Chapter 3.



(a) coaxial model structure **(b)** S11

Figure 2.3: Impedance verification model of coaxial

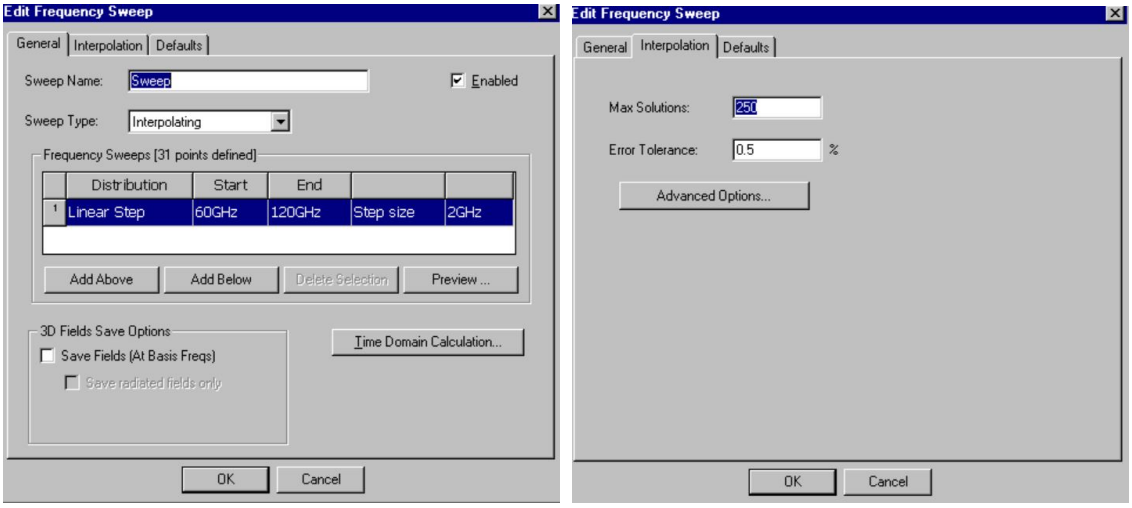
Similarly, an identical CPW model as on the chip is calculated and simulated. The HFSS model can be found in Figure 2.4a. The model follows the same substrate structure and dimensions, same signal trace width and gap width. However, the signal trace length is set to a larger value to in order to show a clear impedance results. From the S11 result in Figure 2.4b, the impedance is matched to 50Ohms.



(a) CPW model structure **(b)** S11

Figure 2.4: Impedance verification model of CPW

2.3.3 Simulation Setup



(a) (b)

Figure 2.5: HFSS analysis setup

The operation frequency band is between 92GHz to 100GHz, which is the main interval this work is focused on, however, the simulation is set from 60GHz to 120Ghz to observe the model behavior in a larger bandwidth. Due to the big amount of simulations that need to be done in this thesis work, most of the simulation uses sweep-type Interpolating to achieve the best time efficiency. The adaptive solution frequency is set to 100GHz(the maximum operation frequency) to guarantee the mesh size is appropriate for all the frequencies since the sweep type is interpolating. The Lambda refinement, as introduced in the previous section, is applied to reach a good meshing size automatically.

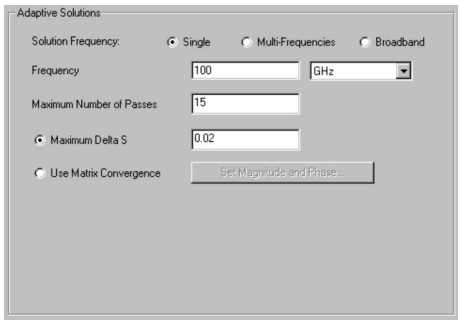


Figure 2.6: Adaptive solution set up

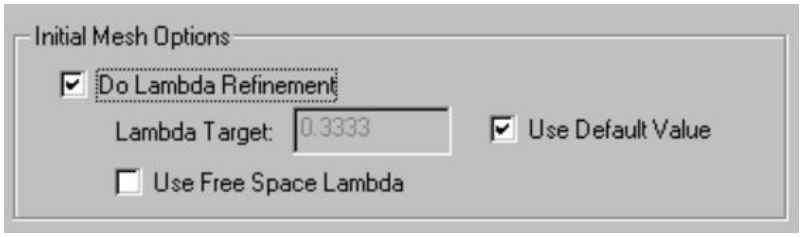


Figure 2.7: Lambda refinement

The simulation accuracy is determined by interpolating error tolerance. The interpolating sweep generates a solution for the S-matrix over the defined frequency range. The solver chooses the appropriate frequency points at which the field solution is calculated. HFSS does this by choosing appropriate frequency points at which to solve for the field solution, it continues to choose frequency points until the full sweep solution lies within a certain error tolerance. In short, the error tolerance value is the maximum relative difference allowed between two successive interpolation solutions. Error tolerance of 0.5% is used in this thesis work.

2.4 SUMMARY

In this chapter, the general HDFO model description including the layer distribution and feeding structure is given. The EM model is built in AnsysHFSS environment. The port verification has been justified for both the coaxial port and CPW port. The applied meshing method is lambda refinement, which is a adaptive meshing method. Simulation setup in HFSS has been introduced.

3 MODELING AND ANALYSIS

3.1 BENCHMARK MODEL AND RESULTS

The benchmark model is illustrated here to provide a performance comparison to the HDFO model. This benchmark model is designed by the traditional laminate method with vias as interconnect method. An overview of this benchmark model can be seen in Figure 3.1. The height of each layer remains the same, via is used to connect chip and antenna, a few vias are placed around the connecting via to form a coax via structure, which is one of the best interconnect methods as discussed in Chapter 1.

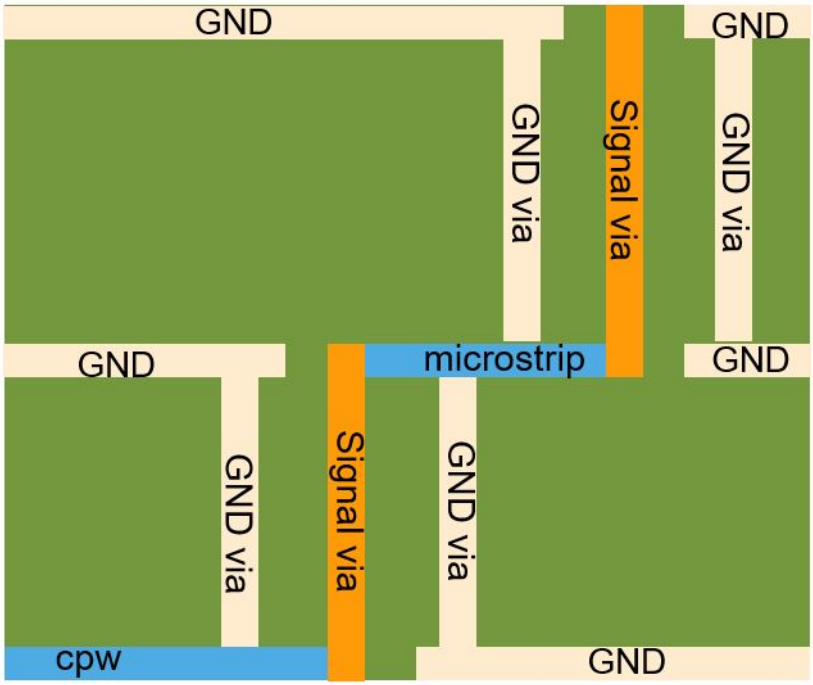


Figure 3.1: Benchmark model

Figure 3.2 shows the S parameter of one channel in this benchmark model. Return loss is above 25dB at the frequency range from 92GHz to 100GHz, and the insertion loss is around 0.45 to 0.5dB at almost all frequency band. Figure 3.3 shows the isolation between 2 of the adjacent feeds, the isolation is roughly around 39dB between the feeds. Although the return loss and insertion loss of the benchmark model seem fine, the

isolation does not look good enough yet. A detailed performance goal can be found in Section 3.2.2.

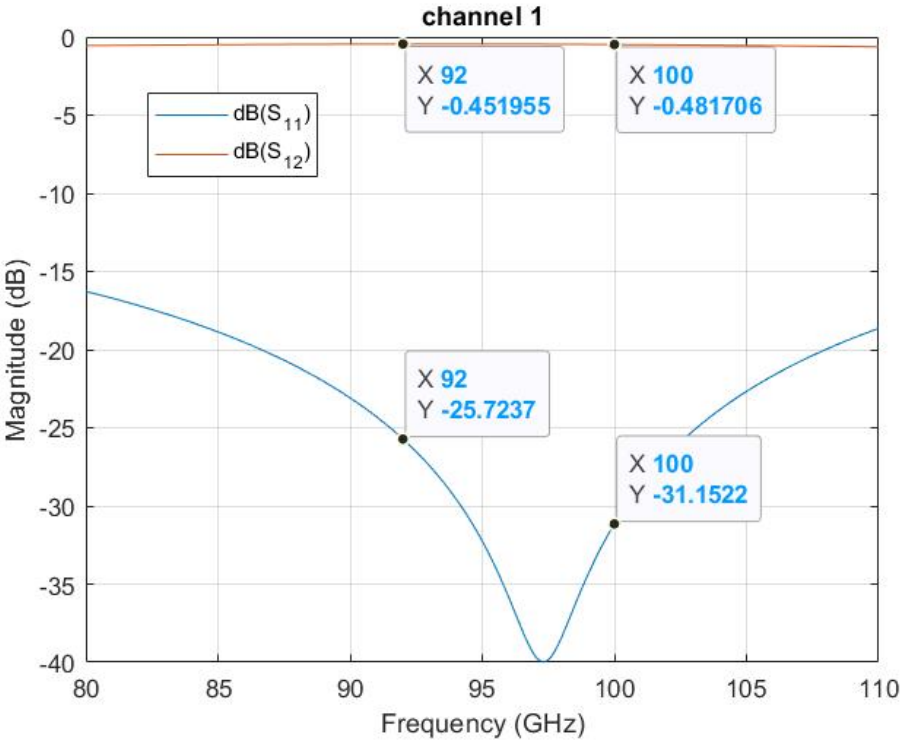


Figure 3.2: Benchmark model S parameter, channel 1

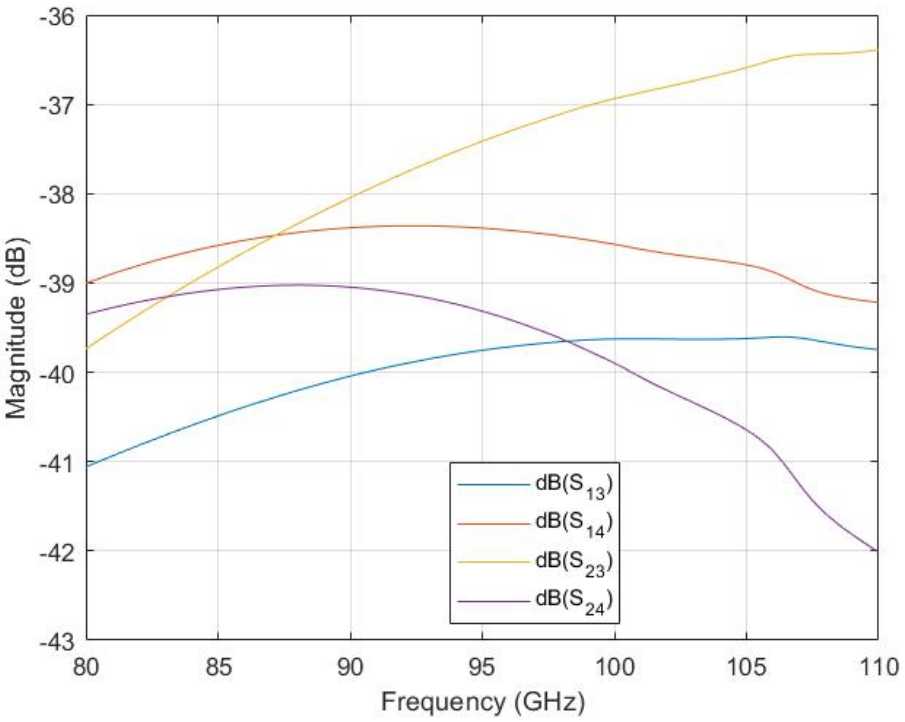


Figure 3.3: Isolation

3.2 PROPOSED PARAMETERIZED MODEL

3.2.1 Model Description

The parameterized model built on AnsysHFSS contains an antenna feeding structure, chip, and a few other silicon layers underneath the chip. The antenna feeding structure is described in the previous chapter.

The chip and other silicon layers below the chip are simplified to material boards. In this chapter, only the chip part is introduced since only this part is relevant to the feeding performance investigation. A detailed description of coaxial feeding network structure has been introduction in Section 2.3.1. This section will be more focused on the model parameterization.

This parameterized model contains many variables, all of the variables used in this model are described in the following tables.

Table 3.1 lists the parameters that are expected to have a fixed value but are also critical to the performance, they will be used in the next chapter for sensitivity analysis.

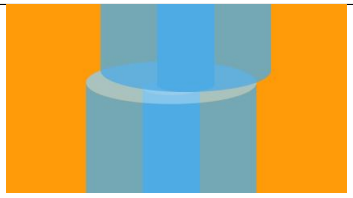
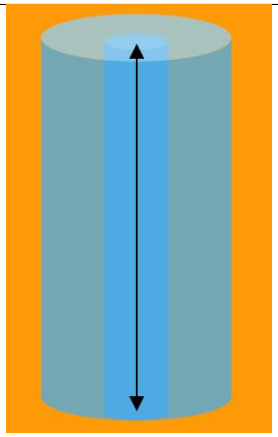
Name in the thesis	Description	Illustration
Xab, Yab	offset between a-th and b-th layer at x axis and Y axis	
Lx	thickness of x-th layer	
hc	copper thickness	

Table 3.1: Variable list: key parameters part 1

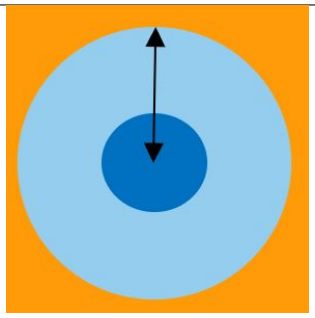
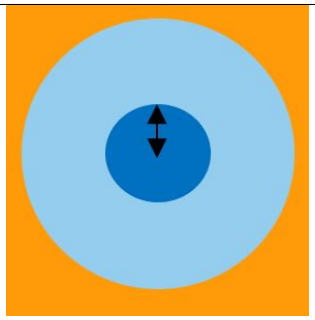
Name in the thesis	Description	Illustration
tracewidth	Microstrip trace width	
traceradius	Microstrip end pad radius	
spreadwidth_core	via pad	
spreadwidth	via landing pad	
Rx	Outer conductor radius of x-th layer	
rx	Inner conductor radius of x-th layer	

Table 3.2: Variable list5: key parameters part2

3.2.2 Design Requirements and Limitations

This package is designed to be applied in 6G mobile communication, the center frequency is 96GHz with 8GHz bandwidth, thus the modeling performance will be investigated from 92GHz to 100Ghz. The purpose of this thesis work is to reach good matching, high isolation, and minimum loss.

A exact value of the required the insertion loss, return loss of the feeding path should be constrained by many other factors such as input signal power. minimum output signal power, signal loss on chip, antenna gain and so on. According to these value, the exact number of the loss budget that is allowed at this feeding structure can be calculated. However, since the other numbers are unknown, we cannot provide a precisely calculated requirements. Normally, for a complete network, a 10dB return loss, 10% reflected power is good enough. So as part of the full package, a higher standard is applied to this part, the matching performance of this feeding network is expected to reach under -20dB. Similarly, the insertion loss is expected to reach less than 0.5dB. From Section 1.5.2, the isolation between ports from different feeding paths are normally achieved at around 20-40dB, thus a higher isolation loss of 50dB is expected in this feeding network. A summary of the electrical performance requirements can be seen in the table below.

	frequency band	insertion loss	matching	isolation
requirements	92-100 GHz	$\leq 0.5dB$	$\leq -20dB$	$\geq 50dB$

Table 3.3: Modelling performance requirements

While investigating the performance of this AiP model by optimizing its dimensions, the dimension limitation is also a critical factor to be considered. The dimensions of certain parts of this model are restricted by manufacturing ability and the dimension of the antenna panel. The minimum via diameter is limited due to manufacturing process. The maximum value of outer conductor diameter on the top layer is limited by the antenna dimension.

3.3 OPTIMIZATION OF PARAMETER VALUES

The optimization process of this AiP feeding model is divided into 2 blocks. Firstly only the coaxial feeding structure is optimized to make sure the coaxial feeding itself has the minimum loss, this result then will provide a starting value for the second block of the optimization process, which is the chip to feeding optimization, where the chip interface is involved. For each parameter, a separate sets of simulation was performed.

According to the variable introduction in section 3.2, Table 3.2 lists all the variables that are critical to the model performance and can be adjusted in this design. Thus the variables from Table 3.2 is used in this optimization process.

3.3.1 Feeding Tuning

For feeding optimization, only the coaxial part is involved in this process. The critical parameter in this section is listed in Table 3.2, as these parameters have a direct impact on the impedance of the coaxial layers.

To have a good impedance match between the feeding and antenna panel, the feeding line needs to be tuned to 50Ohms. All coaxial layers have the same structure, thus the initial value of the inner conductor radius and outer conductor radius of all coaxial layer has been set to the values according to calculation.

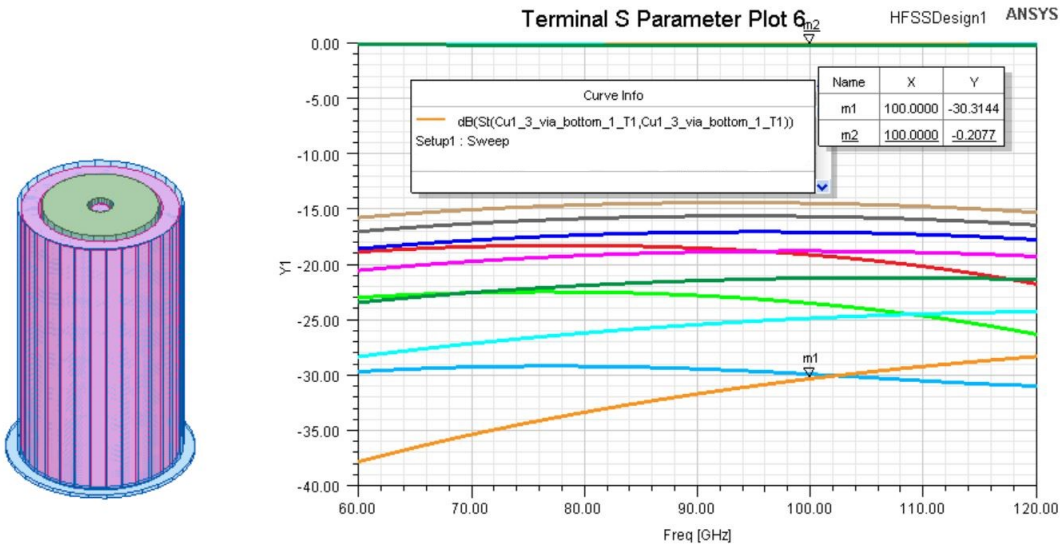
The coaxial feeding dimension can be calculated as follows,

$$\frac{R}{r} = 10^{\frac{Z_0 \times \sqrt{\epsilon_r}}{138}} \tag{3.1}$$

where R is outer conductor radius,r is inner conductor radius, $Z_0 = 50Ohms$, ϵ_r is the relative permittivity of dielectric material.

In this way, the initial value of r and R are set for all the coaxial layers. To verify this result, a parametric study for the coaxial performance has been shown in Figure 3.4, where a single layer coaxial feeding structure same as the original model has been applied, and

the inner conductor radius has been set to r. The outer conductor radius ranged from 80%R to 130%R. The simulation results show that the optimum performance occurs when the outer conductor radius is R.



(a) coaxial structure **(b)** parametric sweep for the coaxial dimension

Figure 3.4: Single coaxial optimization

Thus the initial values of each variable in Table 3.2 are set according to the calculation and optimization results. In addition to the coaxial conductor dimensions, other structures that affect the feeding impedance are the microstrip line width ('trace width'), the contacting point area between the end of the microstrip line, and the coaxial inner conductor('trace radius'), and the metal spread size on the coaxial outer conductor('spread width'), and the metal spread size on the coaxial inner conductor('spread width core').Based on the coaxial dimension we determined earlier, the next step is to find the optimum value of these four parameters.

To perform the optimization, a few sets of parametric sweeps have been applied to the key parameters. The range is defined around the initial value in an interval that does not affect the structure, hence no insertion between materials.

The tuning of the above-mentioned parameters is done by a parametric sweep near the initial value. Figure 3.5, Figure 3.6, Figure 3.7, Figure 3.8, Figure 3.9, show the parametric sweep of these key parameters. This tuning process is aimed to find good initial values based on the performance of the coaxial structure, excluding the feeding and chip transition, the performance given in this section is not the finally performance of the full feeding network. A similar parametric sweep for these parameters will be performed again when the chip to coaxial transition is added.

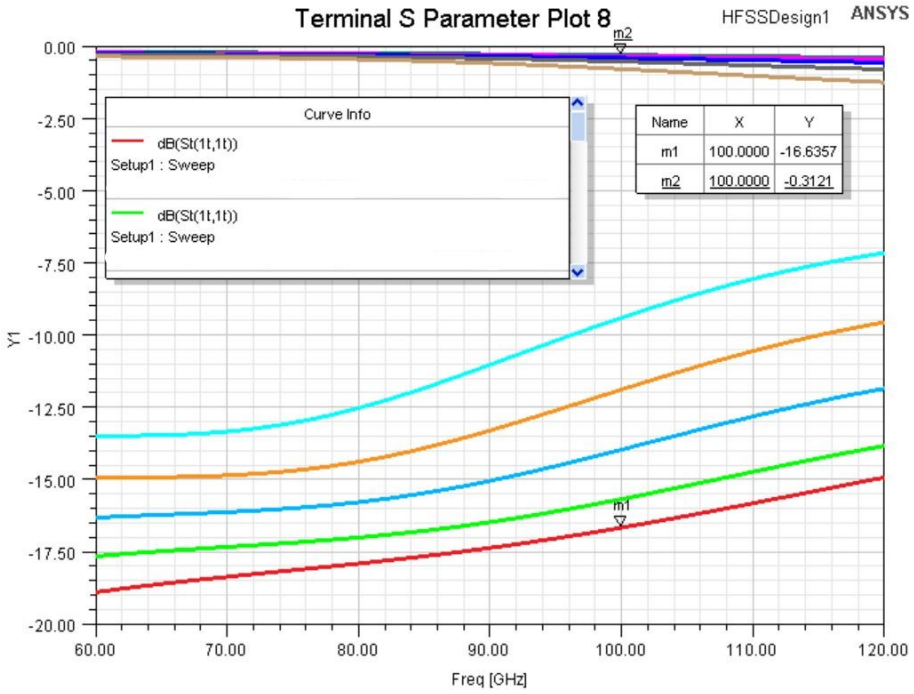


Figure 3.5: ”spread width core” parametric sweep

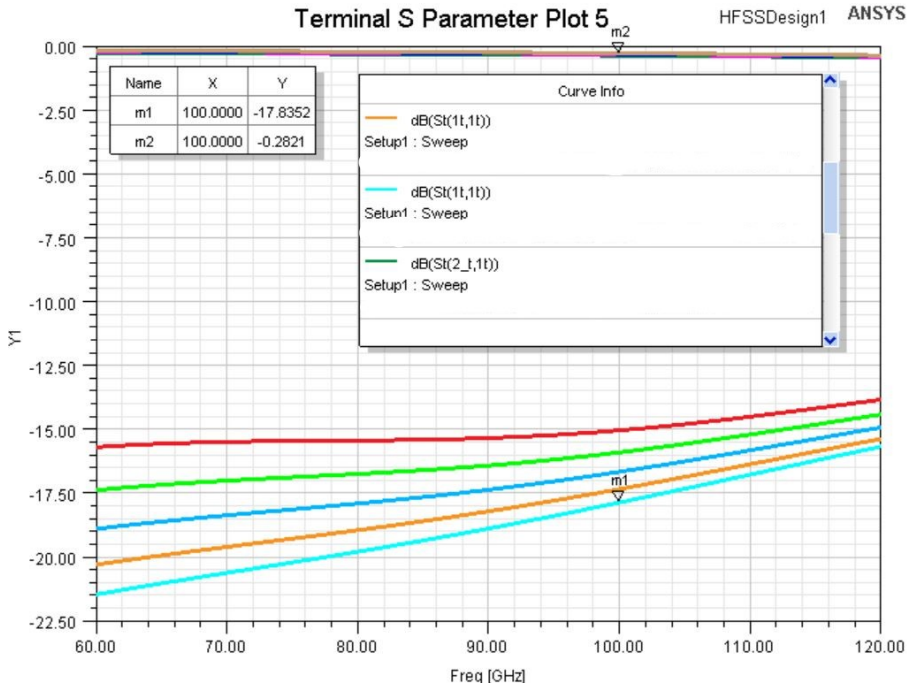


Figure 3.6: ”spreadwidth” parametric sweep

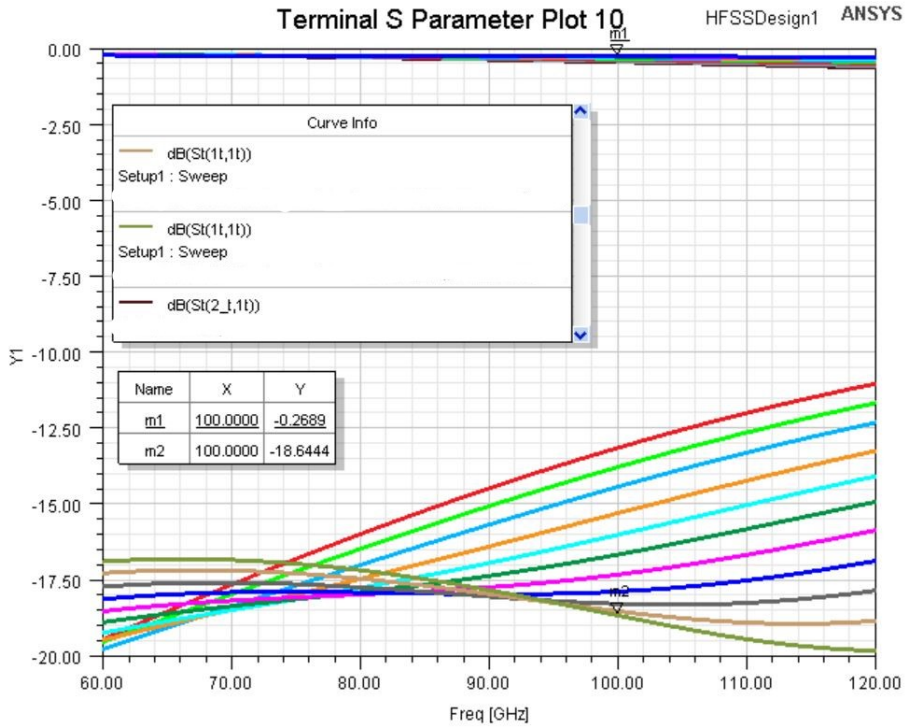


Figure 3.7: ”tracewidth” parametric sweep

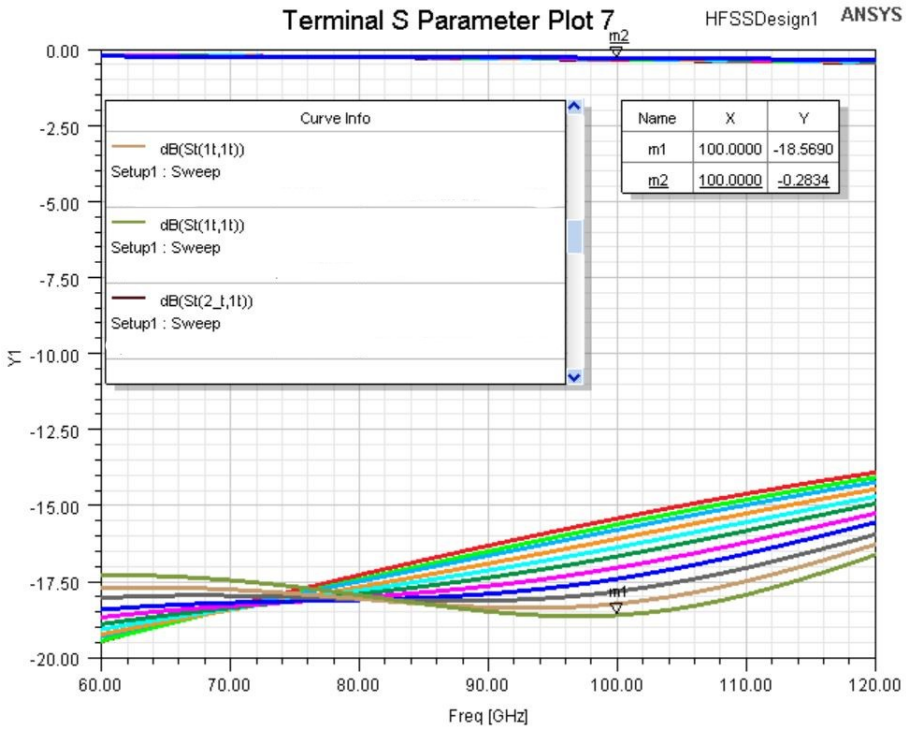
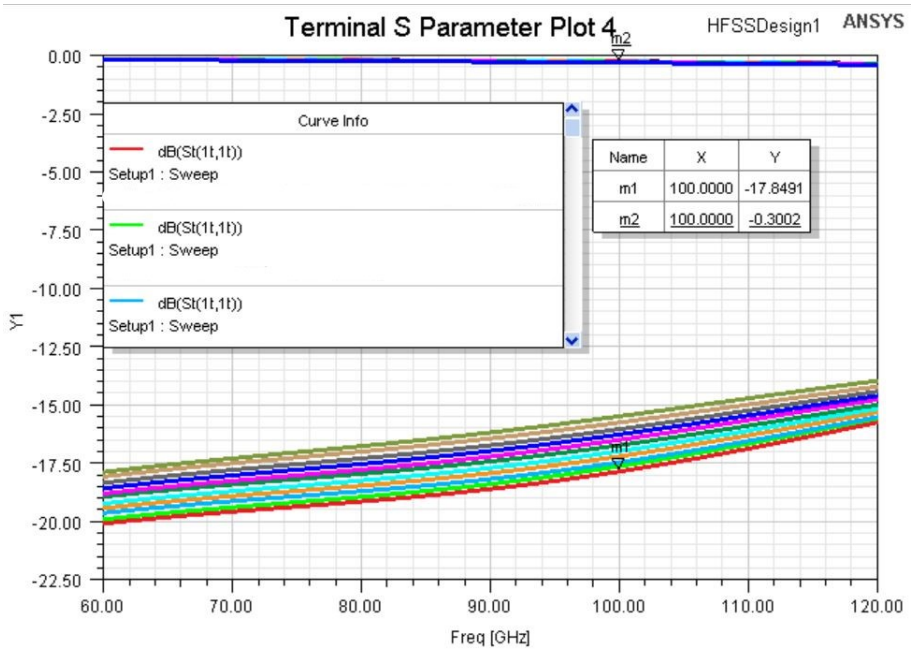
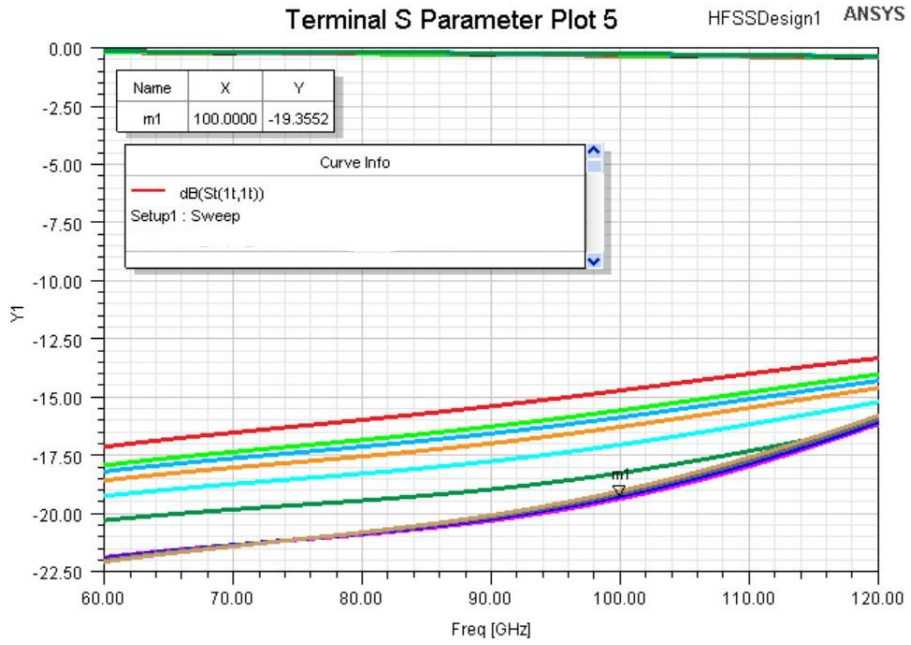


Figure 3.8: ”traceradius” parametric sweep



(a) Inner conductor radius rx



(b) Outer conductor radius Rx

Figure 3.9: Coaxial dimension sweep of x-th layer

3.3.2 Chip to Feeding Optimization

Optimized coaxial feeding need to be connected with the chip to check the overall performance, thus this section will be based on the optimization results from last section, to investigate how to reach better performance.

Effective transition from CPW to coaxial has been investigated by many engineers. In most of the cases with lower frequency band, a direct transition between CPW to coaxial both in horizontal or vertical orientation will not cause severe loss. Two examples can be seen in Figure 3.10 and Figure 3.11.

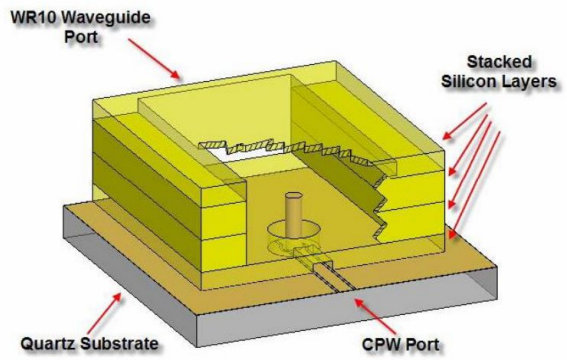


Figure 3.10: A vertical CPW to coaxial transition (75-110GHz) [28]

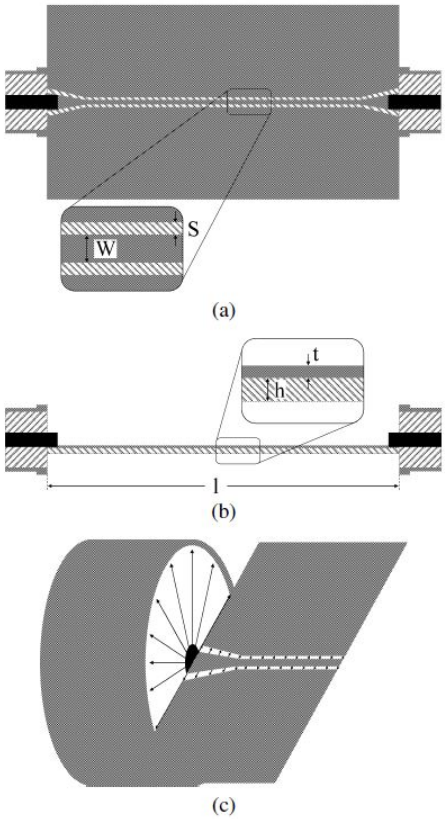


Figure 3.11: A horizontal CPW to coaxial transition (up to 20GHz) [29]

The transition between chip CPW to feeding coaxial is taken place on the first layer by a via, as shown in Figure 3.13. The orange bars are vias connecting between feed and chip. The CPW port is set as a lumped port instead of a wave port. Even though in most cases, a direct transition between CPW and coaxial works very well, this AiP package has shown a different result. The direct transition has shown a very strong loss according to S parameter results as shown in Figure 3.12.

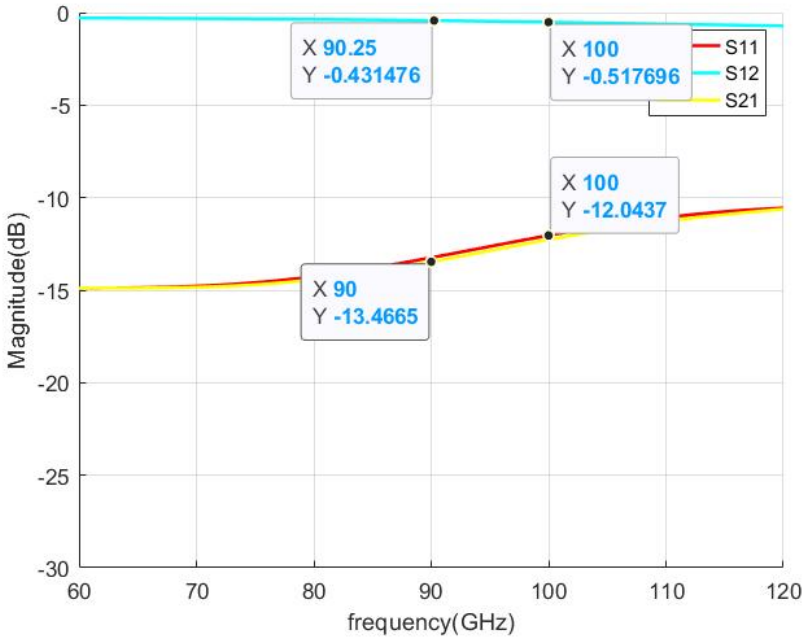


Figure 3.12: 50ohms feed to 50ohms CPW transition performance

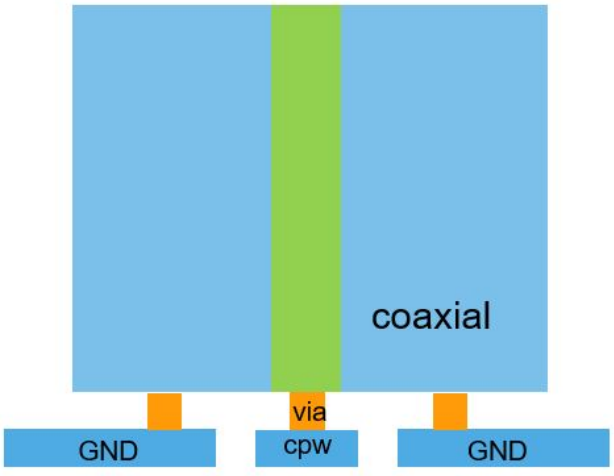


Figure 3.13: Transition between chip and 1st coaxial layer

This loss in the transition part is caused by an impedance mismatch between two structures. The chip CPW has a 50Ohms characteristic impedance, and the optimized coaxial

feeding also has the same characteristic impedance. However, the space between the chip to the feed, or the height of the connecting via is very small. At the operation frequency between 92GHz to 100GHz, due to the skin effect, current concentrates in the outer skin of the conductor, thus the area over which the current can flow in the conductor decreases, which increases the resistance. In another way, the parasite capacitance will show a very significant impact as well due to the very small space between conductors. These two phenomena both contribute to the change of impedance at this transition part significantly, that's why we can no longer expect that in this situation, two 50ohms components can have a smooth transition without too much loss.

Due to the complexity of the structure, it is very hard to find the exact impedance of this transition part. However, by tuning the size of the first coaxial feeding layer and performing simulation on the whole model, the impedance of this transition part is found to be around 72Ohms. A very significant improvement can be seen in the 72Ohms model compared to the 50 ohms model, as shown in Figure 3.14.

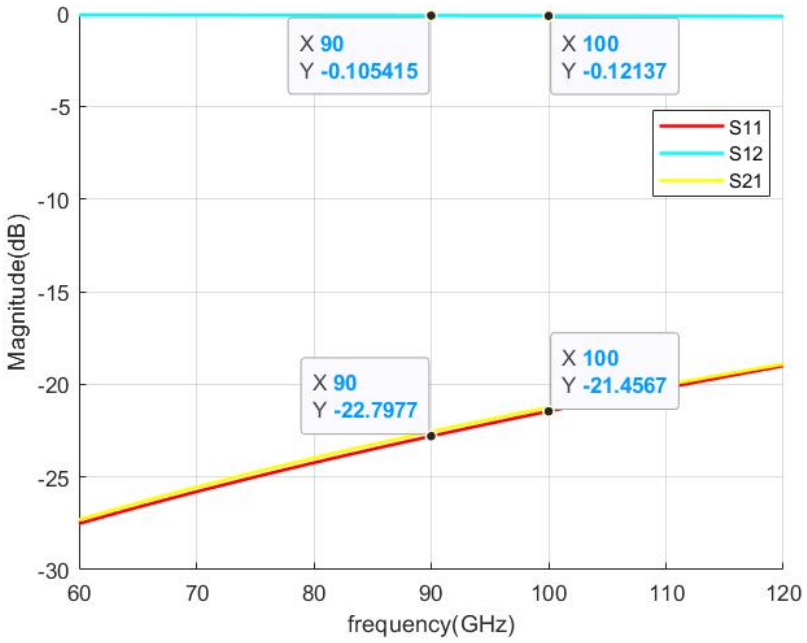


Figure 3.14: 72ohms feed to 50ohms CPW transition performance - insertion loss and reflection coefficient

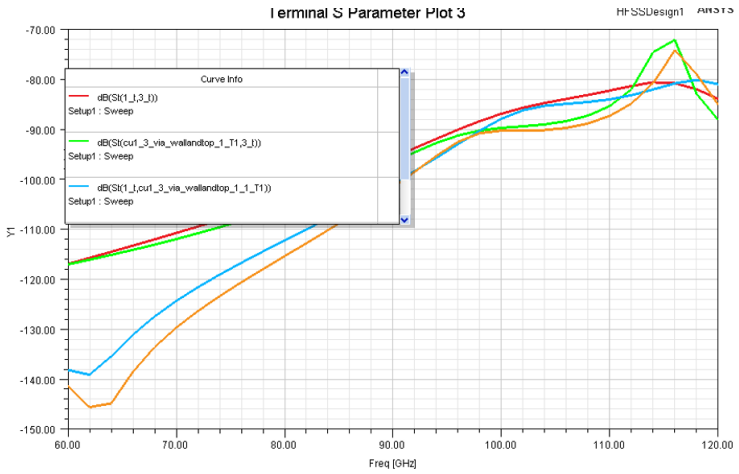
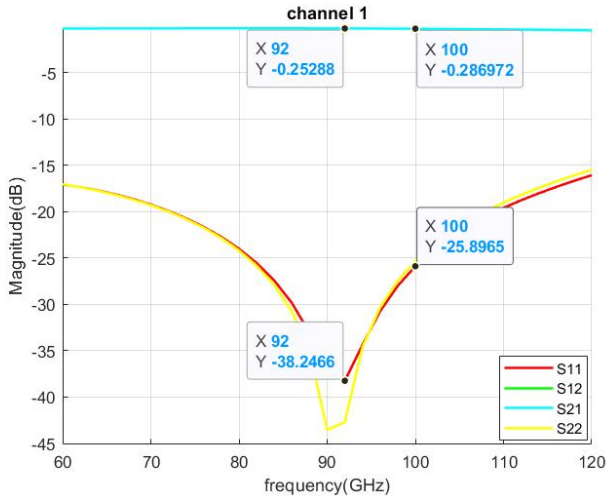


Figure 3.15: 72ohms feed to 50ohms CPW transition performance - isolation between adjacent feeds

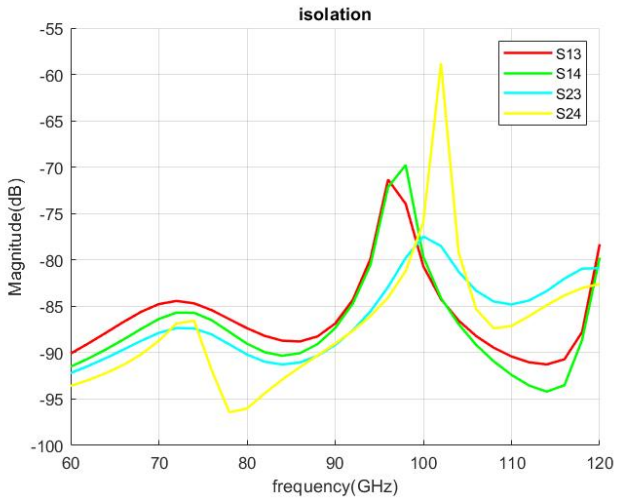
After getting a smooth transition between the chip and the feed, the other layers' dimension also needs to be tuned accordingly since the 1st layer coaxial now has a different impedance. By repeating the same optimization process as described in the last section, the optimized dimension of each layer can be determined. A final model with high isolation, low insertion loss, and low return loss has been achieved.

Note that this is not the theoretically optimized model and performance. The selection for the 1st coaxial layer is very tricky due to the design limitations. To reach 72Ohms impedance at this layer, "r1" should be even smaller and "R1" should be even larger, however, the available space limits the selection range of "R1" while the manufacturing ability limits the selection range of "r1". Concerning these limitations, "r1" and "R1" has been set to an impedance of 71Ohms instead of 72Ohms.

3.4 RESULTS OF THE OPTIMIZED MODEL AND COMPARISONS



(a) channel 1



(b) isolation

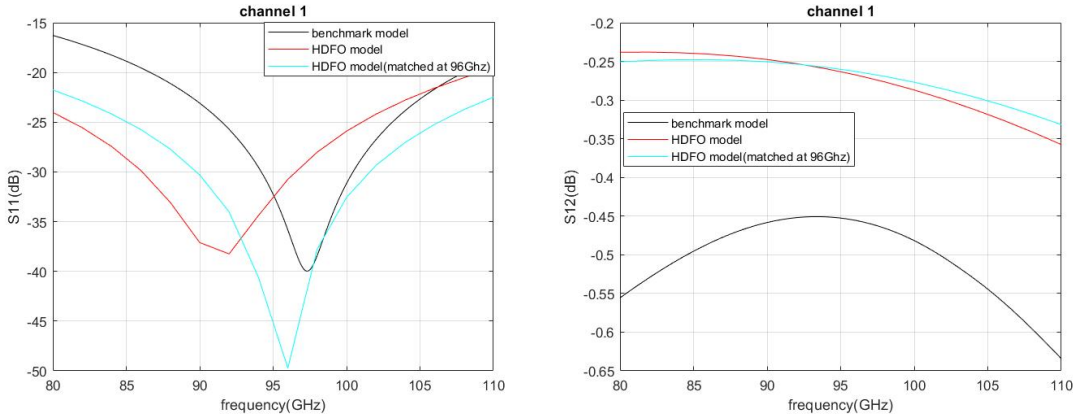
Figure 3.16: HDFO model performance

From 92GHz to 100GHz, the complete model shows very good isolation between two channels of around -70dB, an insertion loss of around -0.23dB, and a reflection coefficient of around -25dB, as shown in Figure 3.16.

Figure 3.17 shows the S11 and S12 comparison on channel 1 between benchmark model and HDFO model. The red and black plots in Figure 3.17a and Figure 3.17b compare the benchmark model and the best results achieved in HDFO model, they have similar performance in S11, but HDFO model gives lower insertion loss. However, the benchmark model and the HDFO model do not match at the same frequency, so the blue plots are provided to give a more fair comparison where the HDFO model is matched at 96GHz. This result is achieved by changing one of the layer thickness, which does not apply for the design since the layer thickness are restricted, thus this result is only used for comparison purpose. This two figures still show a good improvement on both S11

and S12 compare to the benchmark model. Figure 3.18 shows the isolation on HDFO model is much better than in benchmark model, the isolation loss has been improved for around 40dB. Additionally, the HDFO model also achieves larger bandwidth compare to the benchmark model.

In conclusion, Compare with the benchmark model, the HDFO model achieved much better isolation between 2 adjacent feeds and lower insertion loss, while the reflection coefficient remains similar. A numerical level comparison can be seen from Table 3.4. Furthermore, the HDFO model achieves much better isolation between ports compare to the feeding model proposed in [23], where the isolation loss was merely 25dB. More detailed description of the model can be found in Section 1.5.2.



(a) S11 **(b)** S12

Figure 3.17: Performance comparison of channel 1

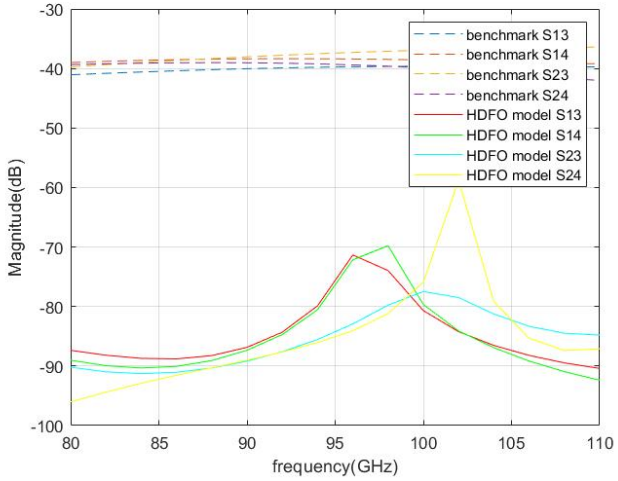


Figure 3.18: Adjacent feeds isolation comparison

	insertion loss			reflection coefficient			isolation		
	92GHz	100GHz	average	92GHz	100GHz	average	92GHZ	100GHz	average
coax via model (benchmark)	0.45dB	0.5dB	0.47dB	-25dB	-25dB	-27dB	40dB	40dB	40dB
coaxial model (HDFO	0.25dB	0.27dB	0.26dB	-35dB	-26dB	-30dB	85dB	80dB	80dB

Table 3.4: Performance comparison between benchmark model and HDFO model

3.5 SUMMARY

A benchmark model built in traditional laminate technology provides return loss of above 25dB at the frequency range from 92GHz to 100GHz, insertion loss of around 0.45 to 0.5dB, and isolation of around 39dB between the two adjacent feeds. Parameterized HDFO model shows more flexibility regarding to impedance tuning and matching. The HDFO design achieves 0.25dB insertion loss, 25dB return loss and 80dB isolation. Significant improvements on insertion loss (0.2dB), isolation (40dB) and bandwidth have been made compare to the benchmark model. In conclusion, the high definition fan-out technology is of great benefits regarding the matching, insertion loss and channel isolation, compare to traditional laminate technology with coax via feeding design.

4 IMPACT OF MANUFACTURING TOLERANCE

As the accuracy and errors of the manufacturing process for the HDFO technology are yet unknown, this chapter is intended to give a general conclusion of the impact on the package performance of manufacturing tolerance. Sensitivity analysis and robustness analysis are applied in this chapter.

4.1 SENSITIVITY ANALYSIS

4.1.1 Critical Parameters and Range Definition

Sensitivity analysis provides information on how a specific parameter impacts feeding performance. Sensitivity analysis is performed on the variables listed on Table 3.1 and Table 3.2. Table 3.1 lists the variables that are defined by the overall package design but will have a small fluctuation due to the manufacturing process; while Table 3.2 lists the variables that are optimized in this thesis work, but their values may be altered during the manufacturing process and cause potential performance degradation. All these key parameters are divided into 4 categories: coaxial feeding dimension, layer thickness, copper thickness and layer offset. The sensitivity analysis results of the 4 categories will be discussed separately.

The sensitivity analysis range is usually defined around the optimum value, with approximately $\pm 50\%$ variation, this variation changes slightly for different parameters according to their actual value. The range for 1st layer dimension is selected differently, the outer conductor diameter of the 1st layer is selected towards a higher value, since in reality it is wanted to be larger to get better impedance matching as introduced in Section 3.3.2.

4.1.2 Coaxial Feeding Dimensions

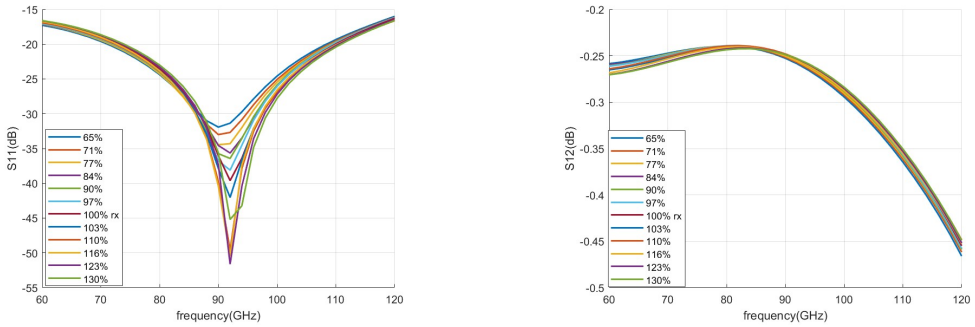
As discussed in the last chapter, the inner and outer conductor dimensions can directly affect the model performance. This section will discuss in detail how and how much each of these dimensions applies an impact on the feeding model performance.

It is obvious that the model performance is less sensitive to some of the dimensions, A example can be seen in Figure 4.1. their variations do not cause an severe performance degrading.

At the same time, some parameters show failure at some variations. These failures are all caused by structure disconnection when their value is too small or too big that exceed the available space. The material overlapping cuts off the signal path, thus failure occurs.

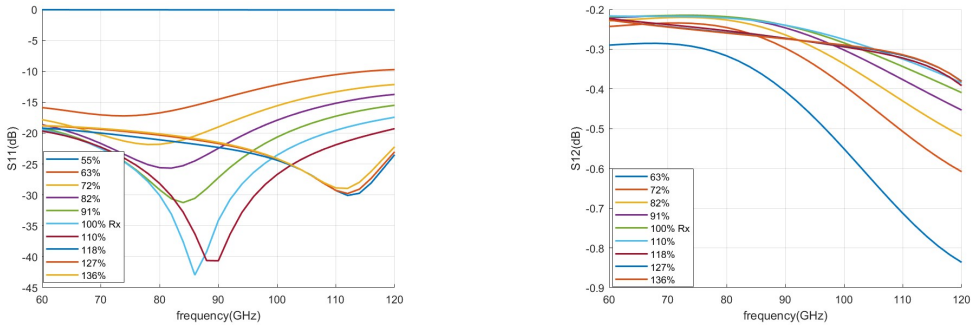
This mainly happens with the coaxial outer conductor radius. A example can be seen in Figure 4.2

The other dimensions are able to provide an acceptable performance in the given range. Their impact mainly shows on the resonant frequency shift. The first coaxial shows a particular clear relation between its value and the resonant frequency, as seen in Figure 4.3. The following discussion about this topic can be found in Section 4.3.



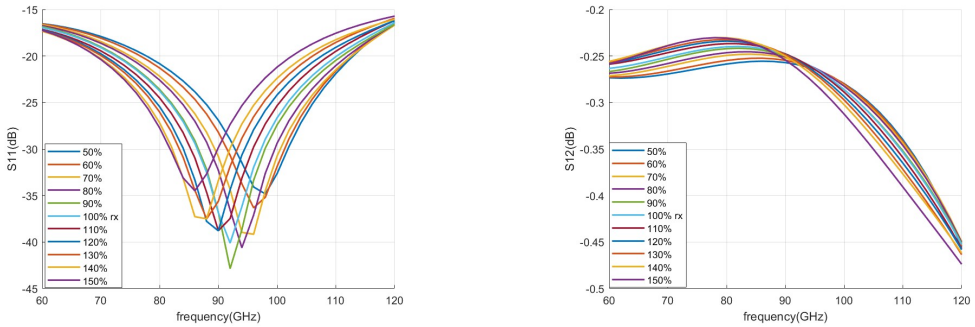
(a) rx vs s11 **(b)** rx vs s12

Figure 4.1: Sensitivity analysis results on rx, x=b



(a) Rx vs s11 **(b)** Rx vs s12

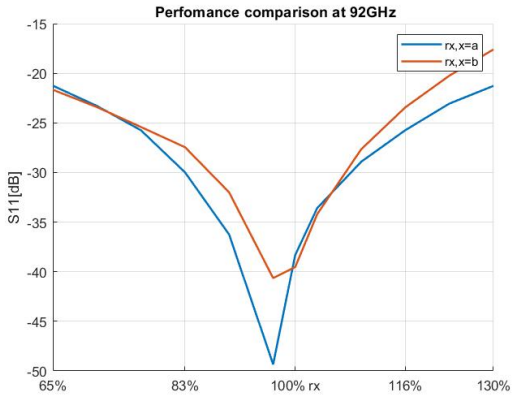
Figure 4.2: Sensitivity analysis results on Rx, x=a



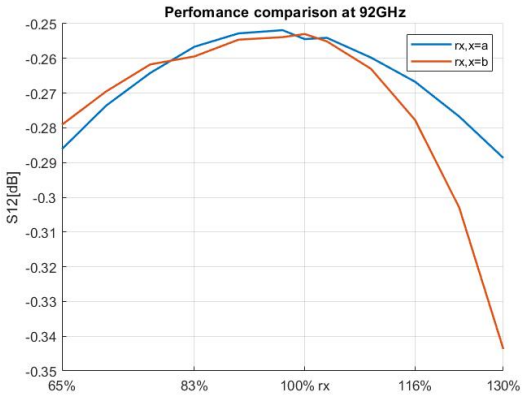
(a) rx vs S11 **(b)** rx vs S12

Figure 4.3: Sensitivity analysis results Rx, x=1

Longitudinal comparison between two of the coaxial layers dimension at three frequencies(92GHz, 96GHz, 100GHz) has been made due to their numerical similarities, as shown in Figure 4.4 and Figure 4.5. The comparison has been made for coaxial inner conductor radius rx and outer conductor radius Rx separately. Here we use symbol a and b to represent the different layer. It can be seen that the a-th layer dimensions "ra" and "Ra" make much lower performance degrading than the b-th coaxial layer dimensions "rb" "Rb". This can be seen particularly in between the outer conductor radius comparison.



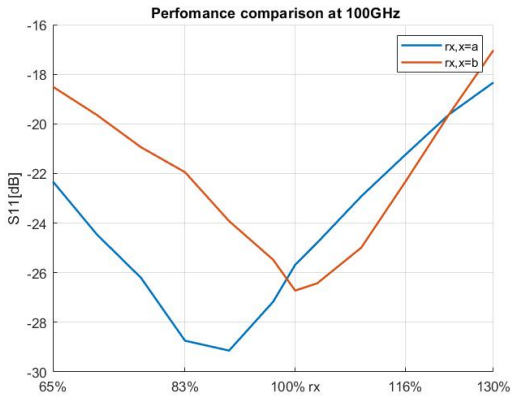
(a) S11 at 92GHz



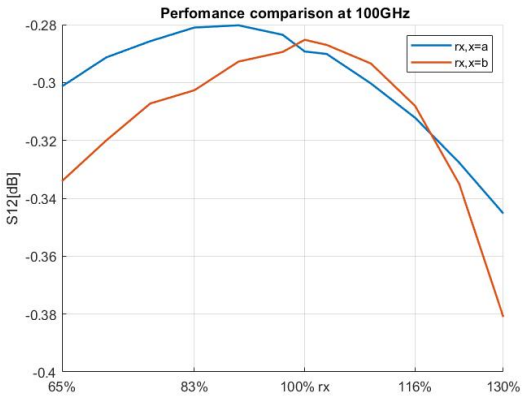
(b) S12 at 92GHz

(c) S11 at 96GHz

(d) S12 at 96GHz

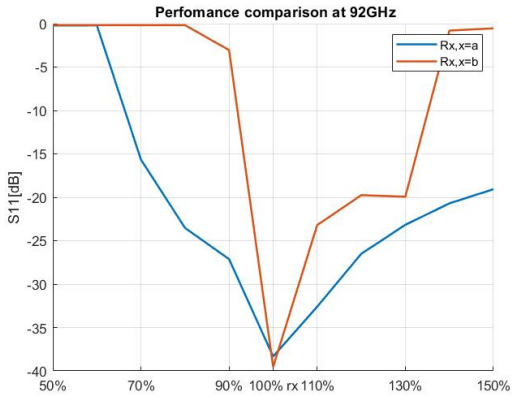


(e) S11 at 100GHz

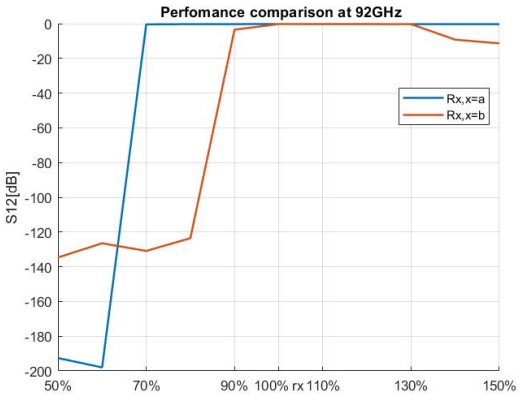


(f) S12 at 100GHz

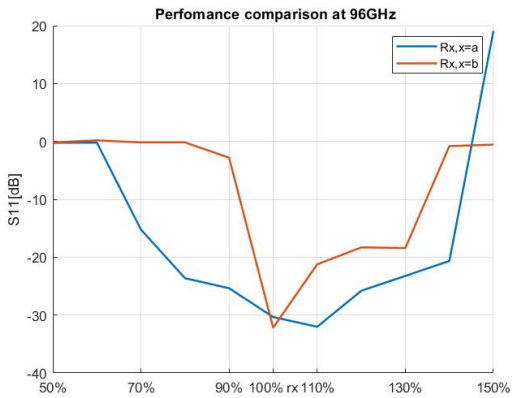
Figure 4.4: Longitudinal comparison among "ra" "rb"



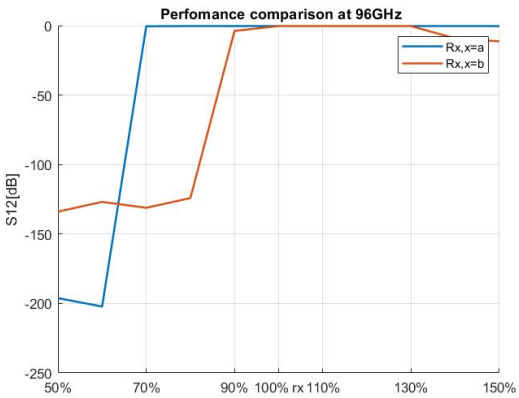
(a) S11 at 92GHz



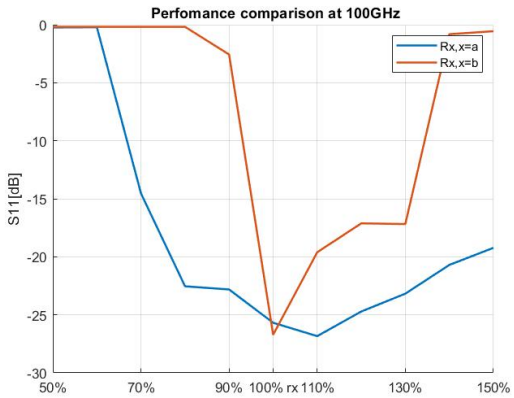
(b) S12 at 92GHz



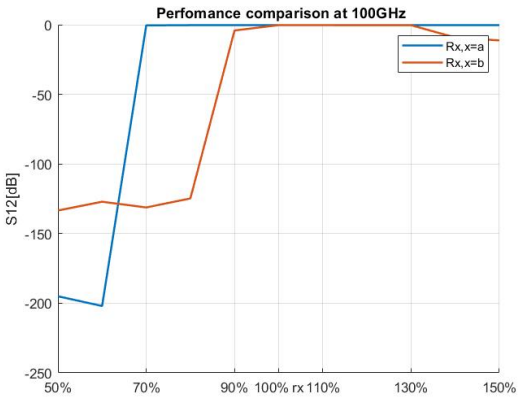
(c) S11 at 96GHz



(d) S12 at 96GHz



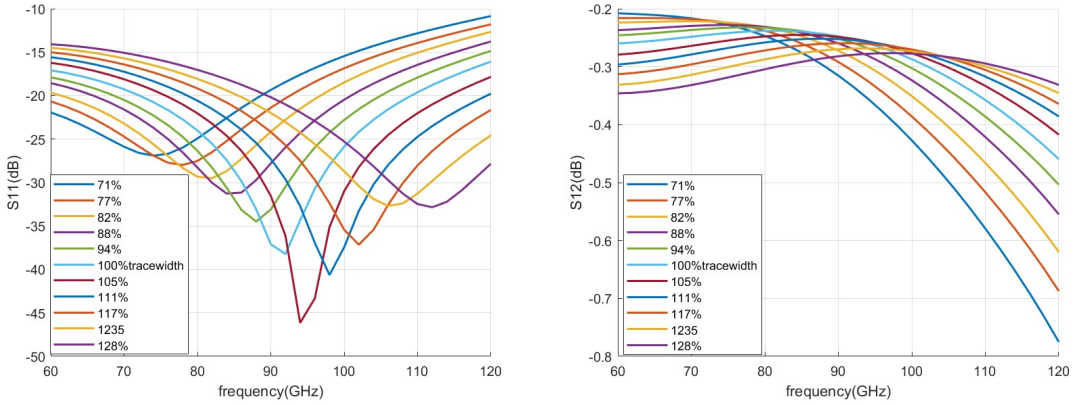
(e) S11 at 100GHz



(f) S12 at 100GHz

Figure 4.5: Longitudinal comparison among ”Ra” ”Rb”

The last key parameter in coaxial is the width of the microstrip between the 4th and 5th layer, ”tracewidth”. Similar to ”R1”, the variation of ”tracewidth” still provides acceptable performance at all ranges, but it has also a clear relationship with the matching frequency, following discussion about this topic can be seen in Section 4.3.



(a) S11 (b) S12

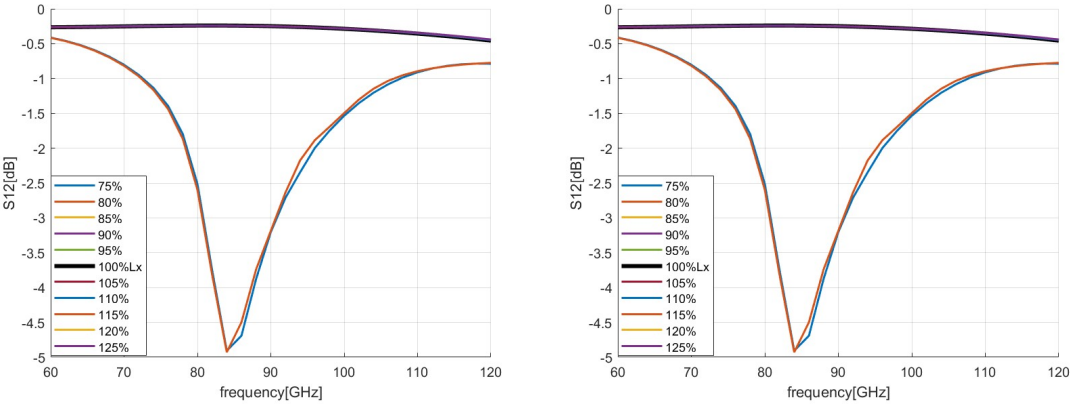
Figure 4.6: Sensitivity analysis results on "tracewidth"

4.1.3 Layer Thickness

The layer thickness has also been considered in the sensitivity analysis. The thickness of each layer is determined by the other components on the layer and their application purpose, However, the manufacturing process may cause a small deviation in the thickness of each layer.

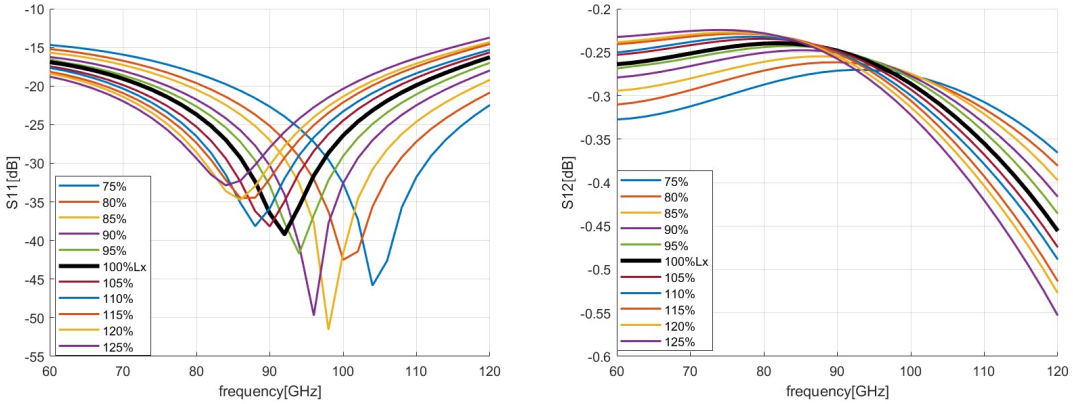
From the sensitivity analysis results, we can conclude that the model performance is more sensitive on the layer thickness of first layer and the layers for which the microstrip connects. At the same time, the model performance is less sensitive on the other layers' thickness.

Figure 4.7, Figure 4.8, Figure 4.9 show the model performance results of layer thickness sensitivity analysis at all frequency ranges. Figure 4.7 and Figure 4.8 are the examples of sensitive layer thickness. A follow-up discussion can be found in Section 4.3. Figure 4.9 is the example of less sensitive layer thickness.



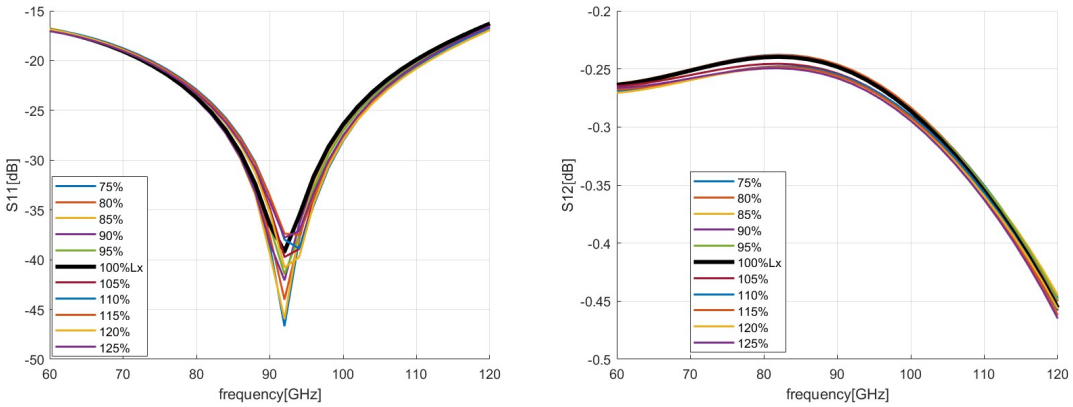
(a) S11 (b) S12

Figure 4.7: Sensitivity analysis results on "Lx, x=a"



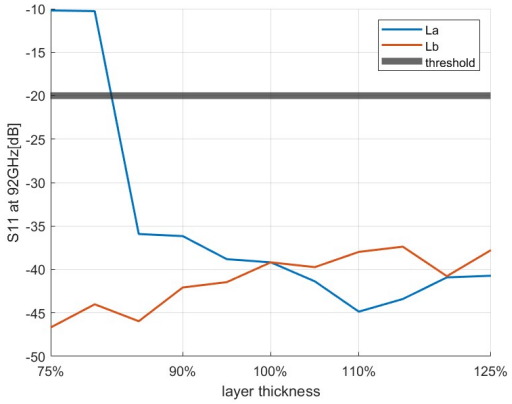
(a) S11 **(b)** S12

Figure 4.8: Sensitivity analysis results on "Lx, x=b"

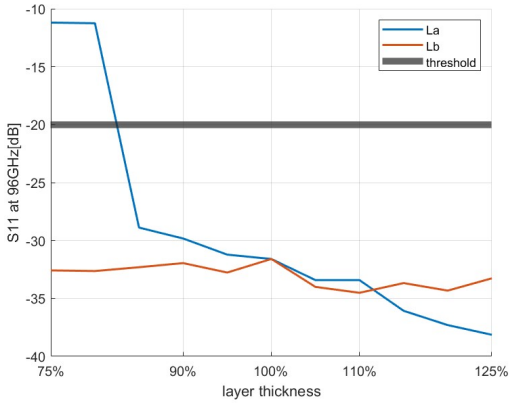


(a) S11 **(b)** S12

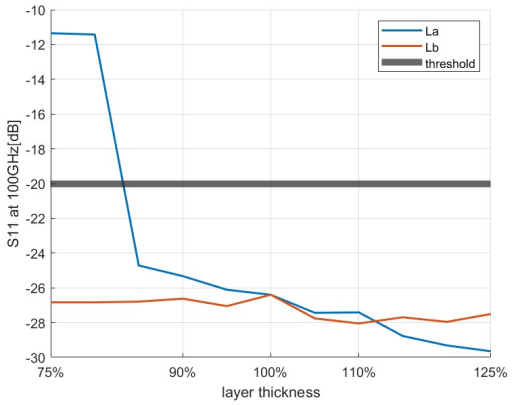
Figure 4.9: Sensitivity analysis results on "Lx, x=c"



(a) s11 at 92GHz

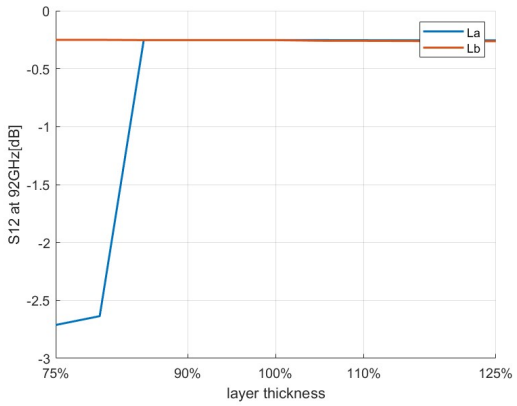


(b) s11 at 96GHz

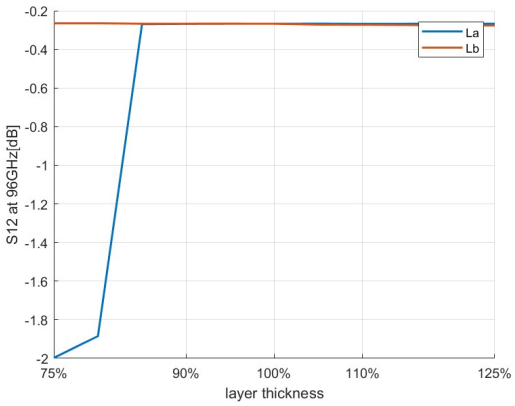


(c) s11 at 100GHz

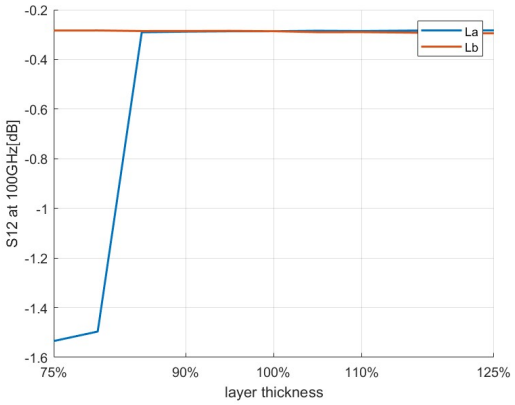
Figure 4.10: Return loss comparison for 'Lx, x=a', 'Lx, x=b'



(a) s12 at 92GHz



(b) s12 at 96GHz



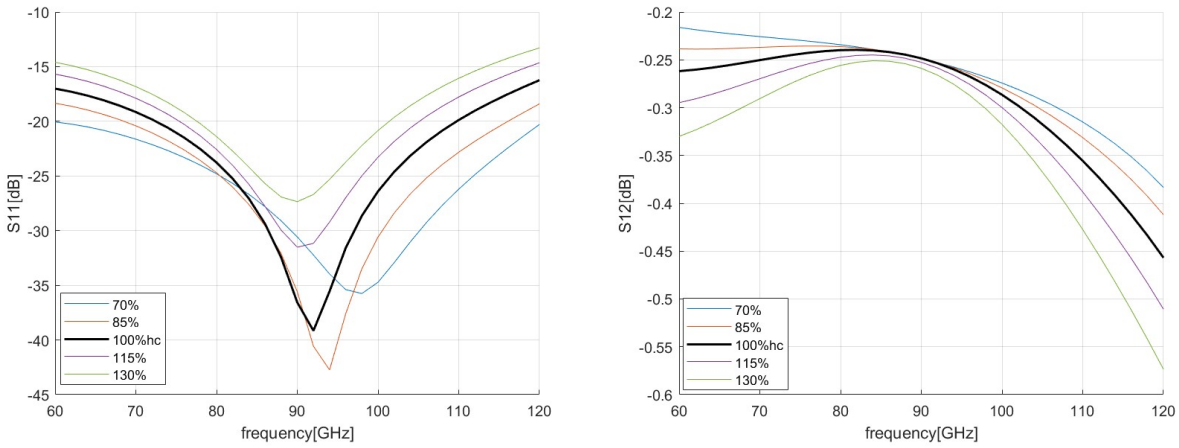
(c) s12 at 100GHz

Figure 4.11: Insertion loss comparison for 'Lx, x=a', 'Lx, x=b'

Longitudinal comparison among the thickness of layer La and Lb at three frequencies(92GHz, 96GHz, 100GHz), as shown in Figure 4.10 and Figure 4.11. In this case a = 1 represents for the 1st layer. It can be seen that the 1st layer thickness has much more impact on the performance, as they could cause failure when their value is smaller than certain value(85% of the designed value). At the same time, the other layer's dimension has smaller impact compare to it.

4.1.4 Copper Thicknessness

Copper layer thickness is another uncertainty where manufacturing error can be involved, which might lead to performance degradation. A range from -30% to $+30\%$ is considered for the sensitivity analysis. Figure 4.12 shows the S parameter of the model in the sensitivity analysis. The copper thickness variation does affect the model performance obviously, but the performance remains acceptable within this variation range.

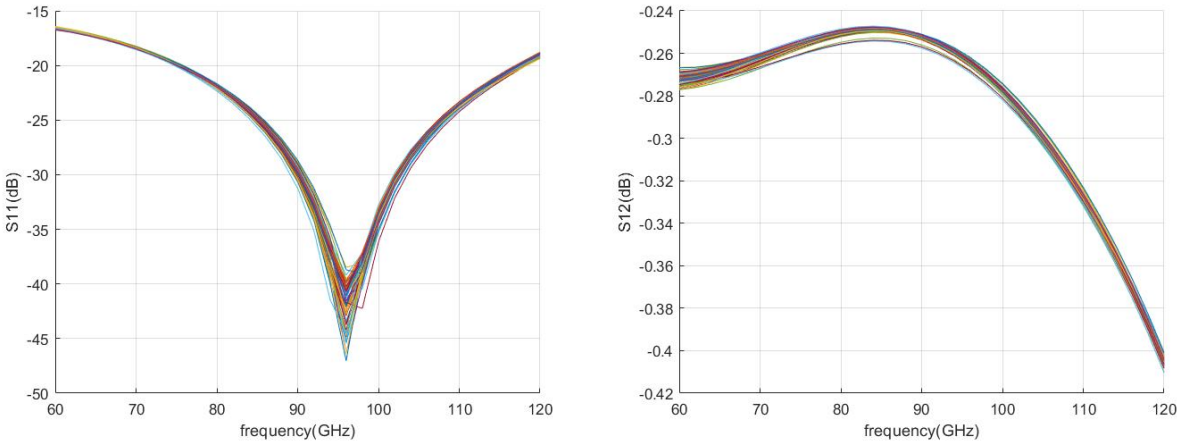


(a) S11 **(b)** S12

Figure 4.12: Sensitivity analysis on copper thickness

4.1.5 Layer Offset

86 sets of analysis has been performed on the models with different layer offset, S parameter can be seen in Figure 4.13. Both S11 and S12 did not show a significant change, so we don't consider the offset a key parameter in this case.



(a) S11 **(b)** S12

Figure 4.13: Sensitivity analysis results on layer offset

4.2 ROBUSTNESS ANALYSIS

Robustness analysis is a further step ahead of sensitivity analysis. Sensitivity analysis provides the information on how a specific parameter impacts the feeding performance, while robustness analysis provides the information on how multiple parameters can affect the performance when all of the parameters have fluctuations at the same time. This is a more realistic reproduction of the real manufacturing process.

All the variables applied in sensitivity analysis are also applied in the robustness analysis except for the layer offset, as it is shown in the last section that layer offset has a very minimum impact at a certain range.

4.2.1 Robustness Analysis Setup

Due to the lack of information about HDFO manufacturing accuracy, the purpose of the robustness analysis of this project is then not focused on the robustness of the package, instead, it is aimed to provide a manufacturing accuracy limitation reference. This chapter provides the package performance level when certain manufacturing accuracy is applied.

There are 3 sets of robustness analysis have been performed, respectively corresponding to 3 levels of manufacturing error rate: $10\%, 5\%, 2\%$. For each data set, 50 groups of random numbers for each variable generated in certain ranges are applied in the model and return loss and insertion loss are used to determine if the model still meets the requirements.

4.2.2 Robustness Analysis Results

For standardization purposes, the reflection coefficient of the system is used to define the performance of each robustness analysis. 4 levels of performance are divided according to the reflection coefficient. If the system has a reflection coefficient lower than -25dB at almost full frequency range, we define it as having very good matching, if the system has a reflection coefficient lower than -25dB at almost full frequency range, we define it as having very good matching, if the system has reflection coefficient lower than -20dB at almost full frequency range, we define it as having good matching, if the system has reflection coefficient lower than -10dB at almost full frequency range, we define it as having acceptable matching, if the system has reflection coefficient worse than -10dB at any frequency, we define it as a failure.

Figure 4.14 shows the model performance of all robustness analyses. Within the simulation sets listed below, the failure case is caused by material insertion at the coaxial outer conductor metal spread and inner conductor metal spread. From this table, we can conclude that if the manufacturing error can be restricted within 5% or lower, it can provide very stable and reliable performance.

Robustnes analysis dataset														
10%					5%					2%				
1	2	3	4	5	1	2	3	4	5	1	2	3	4	5
6	7	8	9	10	6	7	8	9	10	6	7	8	9	10
11	12	13	14	15	11	12	13	14	15	11	12	13	14	15
16	17	18	19	20	16	17	18	19	20	16	17	18	19	20
21	22	23	24	25	21	22	23	24	25	21	22	23	24	25
26	27	28	29	30	26	27	28	29	30	26	27	28	29	30
31	32	33	34	35	31	32	33	34	35	31	32	33	34	35
36	37	38	39	40	36	37	38	39	40	36	37	38	39	40
41	42	43	44	45	41	42	43	44	45	41	42	43	44	45
46	47	48	49	50	46	47	48	49	50	46	47	48	49	50
			very good matching <-25dB											
			good matching <-20dB											
			acceptable matching <-10dB											
			failure >-10dB											

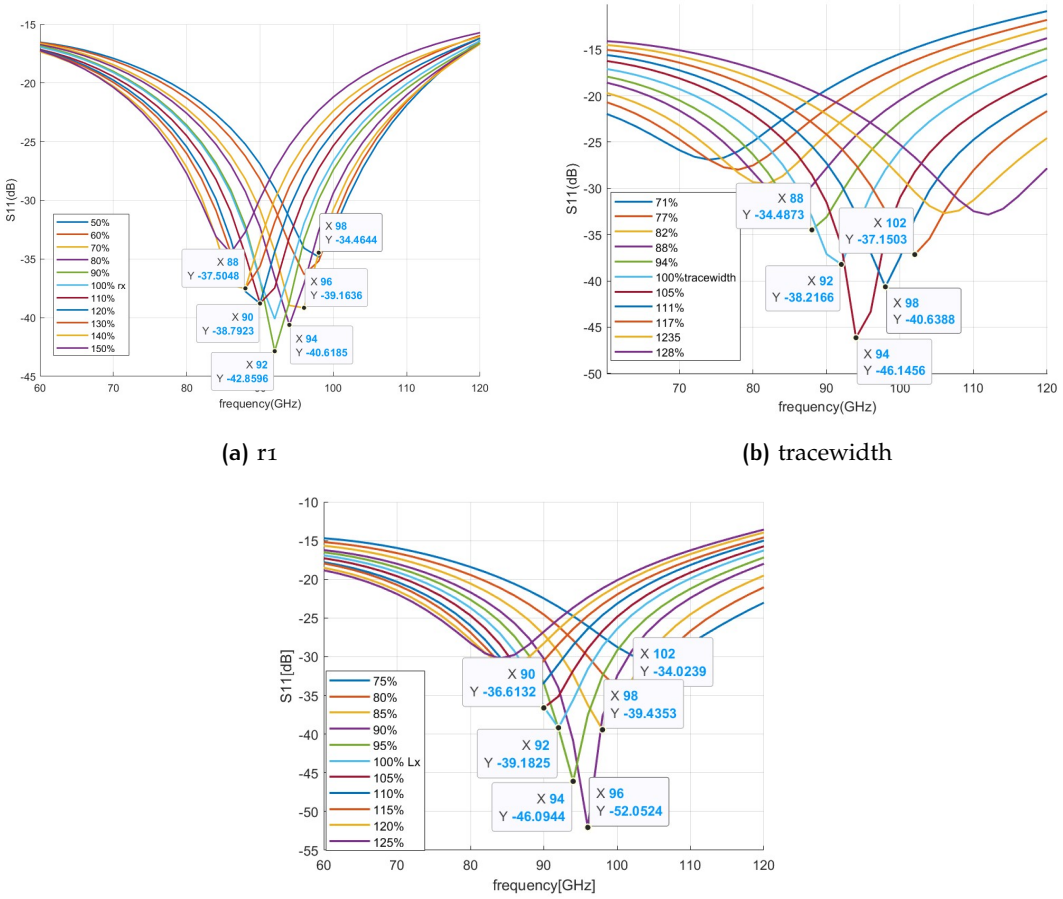
Figure 4.14: Robustness results

4.3 MODEL ADAPTATION FOR CHANGES IN FREQUENCY BAND

During the investigation of the manufacturing intolerance, it was found that some of the parameters have a more significant influence on the resonant frequency, these parameters thus are the key parameters when there is a need to shift the operating frequencies to adapt to different applications. This section is provided as an implementation of the design reference for this AiP feeding model.

From the sensitivity analysis introduced in the previous section, there are few parameters that have more significant influence on the resonant frequencies, the 1st layer coaxial inner conductor radius(rx, x=1)the microstrip line width(tracewidth), and the thickness of the layer on which the microstrip locates.

"r1" is directly related to the chip-feed transition impedance, whose value is also very sensitive. Thus its size plays an important role in the system resonant frequency. Figure 4.15a shows the relation between "r1" and resonant frequency. Similar to "r1", "tracewidth" is directly related to the impedance of another important transition. Figure 4.15b shows the relation between "tracewidth" and resonant frequency. the thickness of the layer on which the microstrip locates also has significant impact as shown in Figure 4.15c.



(a) r1 **(b)** tracewidth

(c) Lx

Figure 4.15: Key parameters for frequency shifting

4.4 SUMMARY

According to the sensitivity analysis, a few parameters have more significant impact on the model electrical performance. The reason is they have bigger impact of the impedance of the connected parts and the whole network. Among those parameter, some of them have more obvious impact on the matching frequency, which shows a potential of being utilized when frequency shifting is needed. The robustness analyses shows that if the manufacturing error can be restricted within 5% or lower, it can provide very stable and reliable performance.

5 CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

AiP technology is seen as the most promising solution to fulfill the high integration requirements for the 6G application. The current research on AiP fabrication technology is mainly focused on LTCC, HDI, and E-WLB technology. HDFO technology as a new raising technology provides the possibility of using coaxial structure as interconnection in AiP, which provides better isolation, lower insertion loss, and better impedance matching.

By investigating a dedicated AiP coaxial feeding model, this thesis aimed to provide a general insight into the practical value of HDFO technology for AiP applications, and the manufacturing intolerance impact on the final performance.

To define the AiP feeding model performance, the following work was performed:

- The feeding coaxial has been set to 50Ohms by calculation and simulation.
- The transition between the chip and coaxial feeding has been corrected to the deviated impedance by performing parametric analysis.
- The whole feeding structure is optimized accordingly by performing parametric analysis

To investigate the manufacturing intolerance impact, the following work was performed:

- Sensitivity analysis has been performed on all the key variables, in order to show how each key parameter affects the system performance.
- Robustness analysis has been performed on all the key variables, in order to show how manufacturing uncertainty affects the system performance.

As a result, a novel chip-to-antenna transition has been developed in HDFO technology. The HDFO design achieves 0.25dB insertion loss, 25dB return loss and 80dB isolation. It proves that coaxial interconnection built with HDFO technology is of great benefits regarding the matching, insertion loss, and channel isolation, compare to traditional vias or coax via design. Compared to the benchmark technology - the laminate PCB structure, the novel design in HDFO technology achieves a much larger operational bandwidth and, on average over the frequency band, has 0.2dB smaller insertion loss while keeping a similar return loss and has improved by 40dB channel isolation. Direct comparison between HDFO and traditional laminate design has been also done for the first time. Due to the flexibility of coaxial impedance tuning, it is much easier to realize better impedance matching in HDFO, even in the high-frequency application where the impedance discontinuity part can form a very different impedance.

A general vision of the impact on the package performance of manufacturing tolerance is provided as well. Some parameters like coaxial layer dimension, layer thickness of certain layers, and the microstrip dimension have a relatively bigger impact on the matching frequency, thus they can be particularly noted for applications in different frequencies. The Robustness analysis shows this feeding system has acceptable reliability if the manufacturing error can be restricted within 10%, and it has good reliability if the manufacturing error can be restricted within 5%. The manufacturers can also see this as a reference to manufacturing error requirements.

5.2 FUTURE WORK

For future work, there are a few aspects that are suggested to carry on,

- Integration with the antenna panel. The model discussed in this thesis work is only the feeding part, the antenna can be integrated into both the benchmark model and the HDFO feeding model to give a better scope of the performances. Furthermore, the antenna array panel can be integrated with the feeding model, to provide performance results more realistically.
- Measurements can be performed on the package sample, once the manufacturing is finished.
- A large set of parametric simulations are applied in this work, in order to optimize the coaxial feeding structure. To reduce the amount of the simulation and achieve the desired results with less time, machine learning method is an interesting and will be an effective way to increase time efficiency. Thus machine learning approach regarding the design optimization is worth investigating in the future.
- A research regarding the impedance deviation between CPW and coaxial transition under high frequency will be very useful. Such a common transition method will still be widely used in other 6G communication and other high-frequency applications. Instead of performing numerous parametric sweeps, it will save a lot of work whiling design the packaging if the mathematical relation between the dimension of coaxial and CPW, and the impedance is clear.

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