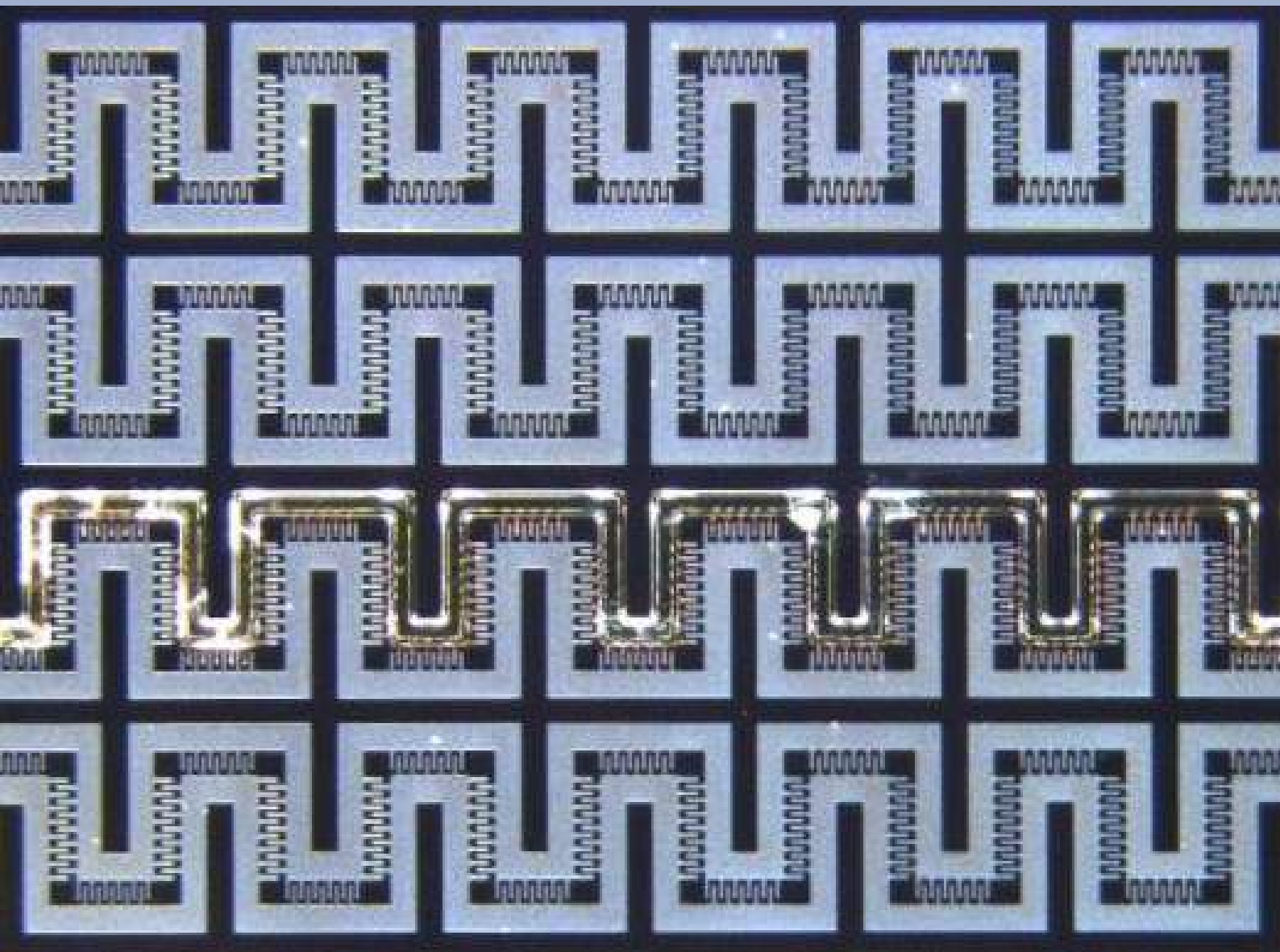
Polyimide Encapsulation for Implantable Medical Devices



Polyimide Encapsulation for Implantable Medical Devices

by

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Abstract

The application of implantable medical devices (IMDs) is increasing rapidly due to the many health benefits they provide in diagnosing and treating diseases. However, these devices have to be able to survive harsh body conditions to ensure their reliability and functionality. Bodily fluids initiate chemical degradation and corrosion in the devices especially in the metal interconnects. Therefore, the devices are encapsulated by various forms of hermetic and non-hermetic packaging.

The current standard hermetic packaging is not suitable for miniature microelectronics. As a result, conformal encapsulation is currently being developed. Multiple inorganic and organic layers of materials or a combination of different layers are used to achieve corrosion protection. Polyimide (PI) is a type of polymer that is used as encapsulation material in bioelectronic devices. Recently, there has been an increasing interest in using thin inorganic layers such as SiC and SiO_2 between the polyimide layers in order to improve the PI to PI adhesion.

In this thesis, first, the corrosion phenomenon in bioelectronics and the available packaging methods are explained. Next, test structures that contain polyimide encapsulation with and without the SiC and SiO_2 ceramic layers are microfabricated. In order to provide accelerated aging conditions to the samples, a lifetime measurement set-up is modeled and built. Finally, the test structures are tested in the lifetime set-up to evaluate their reliability performances in accelerated aging conditions.

The leakage currents of the test structures are measured as a function of the soaking time. Samples with SiC and SiO_2 thin layers exhibit a high leakage current value and fail relatively fast. In addition, samples are analyzed by electrochemical impedance spectroscopy (EIS) measurements and the samples without the ceramic layers demonstrate a capacitive behavior in lower frequencies.

Keywords: encapsulation, polyimide, corrosion, SiC thin layer, SiO_2 thin layer, ALTA, lifetime, reliability

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Sevda Malek Kani
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Introduction

In this chapter, the flexible implantable medical devices and the flex-to-rigid platform are introduced. Next, the thesis goals and approaches are summarized.

1.1. Implantable medical devices

Implantation of the first heart pacemaker in a patient was the beginning of a new era in our long-lasting fight against diseases and disorders. Since then, various implantable medical devices (IMDs) have been developed to increase the quality of our lives. The application of active IMDs is increasing due to their promising therapeutic and diagnostic benefits. Currently, neuroprosthetics such as cochlear implants, deep brain stimulation (DBS) devices, and retinal implants are widely researched and often commercialized [18]. Bladder stimulation, heartbeat monitoring, gastrointestinal motility sensing, and drug delivery systems are other examples of implantable bioelectronics [48].

One recent breakthrough in bioelectronics is the emergence of flexible implantable medical devices. Flexible and stretchable electronics fill the gap between human and machine interactions because it enables direct contact and real-time measurements. Rigid IMDs cause irritation and damage as they are not compatible with soft body tissues [48].

Despite the numerous benefits of IMDs, they must satisfy various criteria in order to be approved for clinical use. One important challenge for the devices is to be functional and to not cause harm to the body over the intended lifetime. The water, ions, and high temperature present in the body accelerate the degradation process. Corrosion of the wire bonds and the interconnects of the implants are among the most common failure reasons in microelectronics temperature, humid, and bias (THB) tests.

1.2. The Flex-to-Rigid platform

The flex-to-rigid (F2R) platform was developed for the fabrication of miniature flexible ICs and the integration of them with medical instruments [23]. In this platform, the silicon chips with the desired functionalities are connected by flexible polyimide foils

containing the interconnecting tracks. Figure 1.1 shows a functional silicon chip (in this example a capacitive micromachined ultrasonic transducer (CMUT)) and its bondpad chip connected by a flexible polyimide interconnect.

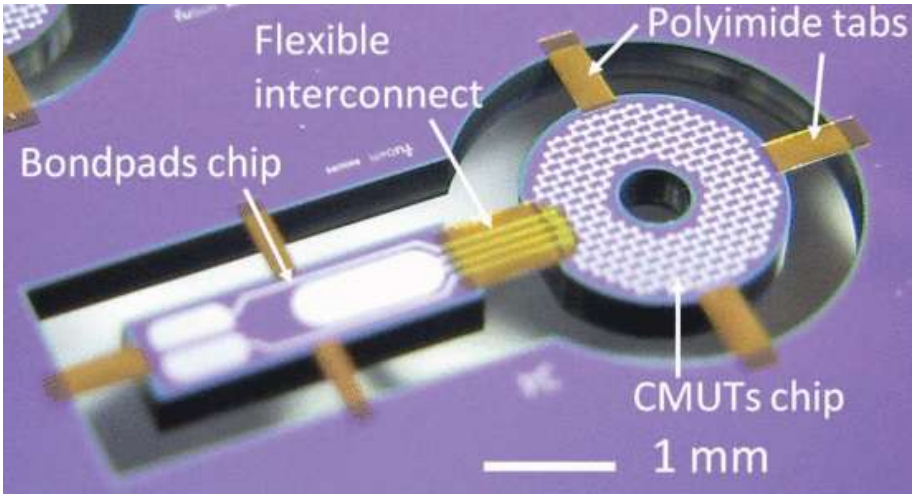

Figure 1.1: An illustration of a device manufactured by F2R platform, the functional chips are connected by a flexible polyimide interconnect [23]

The flex-to-rigid platform enables micro-scale device fabrication as the devices are manufactured by standard integrated circuit fabrication technologies. The flexible interconnections of the devices connect various functional silicon islands. The interconnections are aluminum-copper tracks sandwiched between two layers of polyimide. The flexibility of F2R devices enables their application in various geometries. Figure 1.2 illustrates an F2R device mounted on a catheter and wrapped around it.

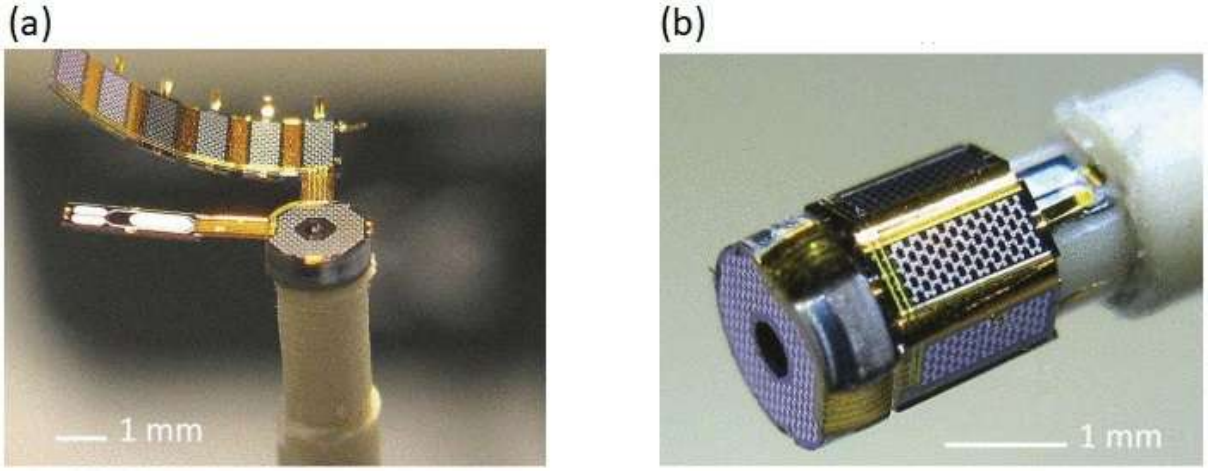

Figure 1.2: An illustration of a device manufactured by F2R platform (a) mounted on tip of a catheter (b) device wrapped around due to its flexibility [23]

1.2.1. Existing flexible interconnect test devices

The flexible foils in the F2R platform are fabricated and tested in previous projects to confirm their flexibility and ability to bend [20]. Figure 1.3 is a depiction of a previously fabricated flexible polyimide interconnect test structure and the corresponding chip of contact pads to enable electrical contact to the interconnects. In the fabrication process thin layers of SiC and SiO_2 were deposited between two polyimide layers to increase the adhesion between the layers.

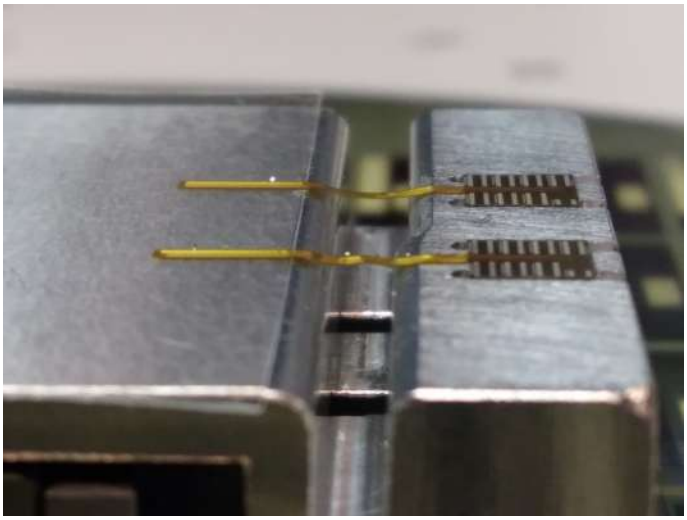

Figure 1.3: The flexible polyimide interconnects test structure and its contact pad chip

The test devices were examined for mechanical characterization under bending conditions. The promising results of these tests encourage a wider application of the flexible interconnects in the bioelectronics field. However, the lifetime and the reliability performance of the interconnects in the body environment has yet to be determined.

1.2.2. Initial lifetime evaluation of the existing test devices

The small size, flexibility, affinity with microfabrication processes, and biocompatibility of the flexible polyimide interconnects have led to an interest in utilizing them for IMDs. However, implantable bioelectronics faces several challenges. One important obstacle is the effect of body fluids on these devices. Various reactive components and water in the body can damage the electrical systems and particularly cause corrosion on the metal tracks.

Initially, the mentioned test devices were mounted on printed circuit boards (PCBs) and wire-bonded as shown in Fig. 1.4. The samples were soaked in Phosphate-buffered saline (PBS) solution and the electrical resistance of the tracks was measured. The purpose of this initial examination was to get an insight into the lifetime performance of these devices. For the available test devices, the tracks started to corrode within the first five hours of the experiments. The initial evaluation of the flexible interconnects revealed that a thorough and detailed lifetime examination was essential. More detailed pictures of the samples and the wire-bonding are available in Appendix A.

Figure 1.4: The flexible polyimide interconnects device with the contact pad chip mounted on a PCB that was fabricated in a previous project.

1.3. Project goals and approach

The goals of this project are to:

1. Fabricate samples with suitable structures for lifetime experiments;
2. Build an aging and life testing apparatus (ALTA) to perform lifetime tests;
3. Evaluate the lifetime of the flexible polyimide interconnects;
4. Investigate the effect of thin layers of SiC and SiO_2 on the corrosion protection of the metal (AlCu) tracks.

In order to realize these goals test samples are designed and fabricated in the clean-room of Philips Research. Half of the samples are fabricated with the SiC and SiO_2 adhesion layers and the other half don't contain these two layers. A lifetime testing set-up is designed and built to create aging conditions for the samples. Finally, the samples are tested and evaluated using the aging set-up.

2

Literature review

In this chapter, a literature study is performed in order to gain knowledge about corrosion in microelectronics and how to prevent it. In the first part of the chapter the corrosion phenomenon in microelectronics is explained and the factors influencing it are identified. Next, the packaging approaches for protecting the IMDs from corrosion are analyzed and summarized. Finally, a description of lifetime tests and measurement methods are provided.

2.1. Corrosion phenomenon in IMDs

Corroding metal lines in an electronic device can lead to open or short failures depending on the material of the tracks. If the corrosion products are insulating material such as the case in aluminum the process will eventually lead to an open circuit. However, in components in which the corrosion products remain as ions in the solution and plate out in the opposite electrode (cathode), shorting passages occur. Gold is an example of the latter type, it produces soluble ions with chloride which form a shorting passage between metal tracks [4].

Conventionally, impermeable ceramic or metal capsules were used to protect microelectronic devices from the harsh environment, and due to very low water intake inside these packages, they are assumed as hermetic packaging. However, by miniaturization of implants, the hermetic packaging is becoming insufficient. Conformal encapsulation is getting more attention as they promise good corrosion protection for the IMDs. Encapsulation performance of several inorganic and organic materials are investigated by researchers to achieve better corrosion protection.

The corrosion phenomenon in microelectronics follows the same mechanism studied in other fields, however, the extra small size of the features and cavities results in insufficient protection by the established methods. Aluminum and Aluminum-copper alloy are widely used in the electronics industry due to low price, good mechanical strength, and corrosion resistance. As a result, aluminum corrosion in microelectronics has been widely investigated in the literature and is presented in this report as an example of corrosion in microelectronics.

2.1.1. Corrosion of aluminum

Aluminum is believed to be resistant in contact with water, which is not true. In fact, the table of the reactivity series of material shows that aluminum easily oxidizes and it is widely used in fireworks and rocket fuel. However, aluminum is a valve metal and it forms a very stable oxide layer [22].

Aluminum oxidizes in less than a millisecond and forms an oxide layer immediately. This layer with a thickness of 2-4 nm, has a very strong adherence to the metal layer beneath. The oxide layer itself consists of two sub-layers, the inner layer covering the metal film is anhydrous and amorphous, on the other hand, the outer layer facing the environment is hydrated. Any condition affecting the oxide layer uniformity and stability highly impairs the corrosion protection of Al.

pH effect

One factor influencing oxide layer stability is the pH conditions. Pourbix's diagram [21] as shown in Fig. 2.1 depicts that in pH values between 4 and 9 this passivation layer is stable. However, the highly acidic (pH<4) and alkaline (pH>9) environments would dissolve the oxide layer and lead to corrosion.

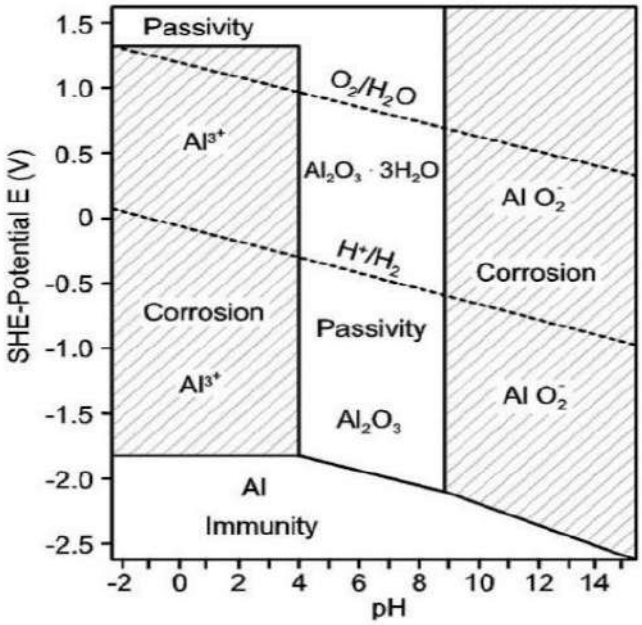

Figure 2.1: The Pourbix diagram of aluminum at 25 °C [21]

The electrochemical cell

The reactions in which one element loses electrons (oxidation) and the other element gains electrons (reduction) are called redox reactions. In an electrochemical cell the oxidation and reduction reactions happen in separate locations, however, they are connected through an external circuit and an electrolyte. Figure 2.2 depicts an electrochemical cell. The produced ions travel through the electrolyte (salt bridge) and the electrons are conducted in the external circuit from the anode to the cathode.

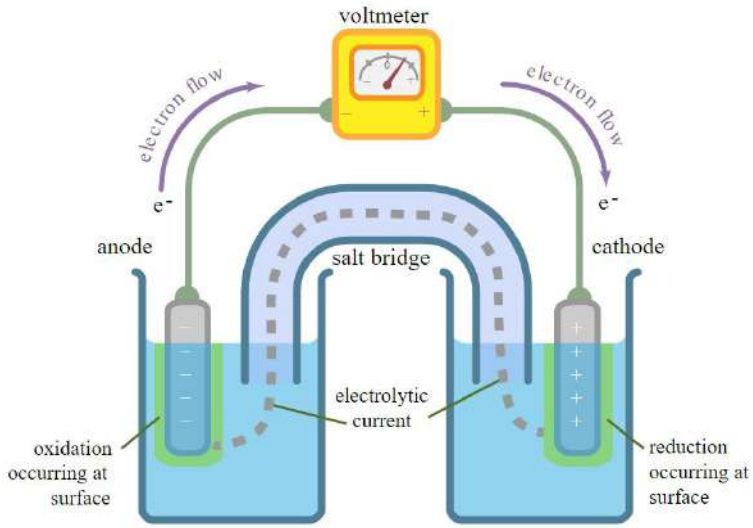

Figure 2.2: An electrochemical cell

2.1.2. Types of Aluminum corrosion

Various forms of corrosion exist including uniform, pitting, crevice, galvanic and intragranular corrosion. Factors such as, the nature of the material, geometry, and the protection method, determine the most dominant corrosion type in different conditions. Regardless of the mechanism, the aluminum oxidation reaction is depicted in Fig. 2.3 and described in Eqs. 2.1 to 2.3 [31].

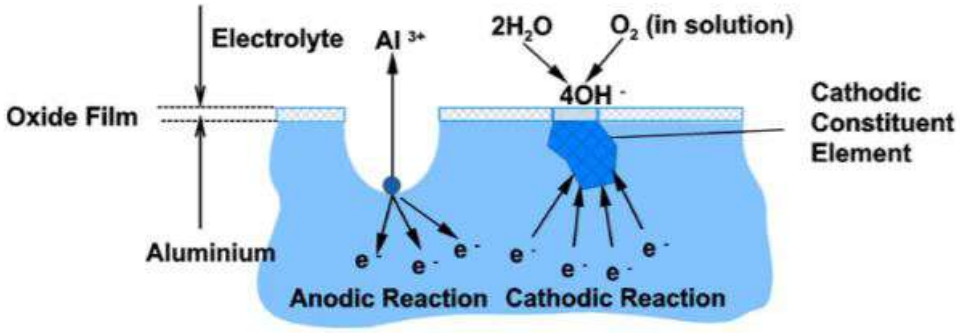

Figure 2.3: The electrochemical mechanism of aluminum corrosion

The aluminum corrosion reaction:

$$Al + 3H_2 \rightarrow Al(OH)_3 + 3/2H_2^{\uparrow} \tag{2.1}$$

At the anodic site, the aluminum oxidizes:

$$Al \rightarrow Al^{3+} + 3e^{-} \tag{2.2}$$

At the cathodic terminal, reduction reaction happens:

$$3H^{+} + 3e^{-} \rightarrow 3/2H_2^{\uparrow} \tag{2.3}$$

Pitting corrosion

Pitting corrosion is common in aluminum alloys and it happens locally where the passivation layer is impaired. It occurs in two general steps: 1-initiation 2- propagation. For pitting corrosion of aluminum, the presence of chloride and an oxidant is essential.

According to Reboul et al. [31] the following steps occur in the initiation stage of the pitting corrosion.

1. Absorption of chloride on the defects of the passivation layer
2. Oxygen reduction happens at the cathodic terminals
3. Oxide layer breaks down at local points
4. The aluminum beneath the defect starts to oxidize fast

However, the micro-scale defects are common on the oxide layer of aluminum. In fact, it is estimated that pure aluminum has ~ $10^4/cm^2$ and AlCu alloy has ~ $10^6/cm^2$ micro-pits. Considering the high amount of existing defects on the aluminum passivation layer, the initial pitting can't be the limiting step in the corrosion. The main determining factor for aluminum pitting is maintaining the pits active after formation. The following steps are suggested for the propagation of the pitting in aluminum.

1. The chloride ions start to accumulate in the pit
2. Chloride components result in a complex product ($AlCl_4^-$) that forms a layer, replacing the aluminum oxide layer
3. Aluminum ions hydrolyze and acidify the solvent in the pit
4. White alumina hydroxide precipitates and forms a cap
5. The cap hinders the exchange of the bulk electrolyte and the solution in the cavity
6. As the cavity gets isolated the solution gets more aggressive, a pH of 3 is reported for the pit solution and this leads to an auto-catalytic reaction

Finally, the hydrogen bubble build-up, limits the propagation, the chloride complex becomes unstable, and the pit re-passivates [31].

The presence of impurities such as Cu in the aluminum layer influences the corrosion behavior. Copper is added to the aluminum layer for better mechanical and electrical properties. However, additional elements form intermetallic compounds which intensify the corrosion of aluminum. There is an incorrect assumption that having nobler elements in the alloy would lead to less corrosion due to an increase in the pitting potential. In aluminum alloys, intermetallic compounds lead to higher numbers of defects on the passivation layer, thus increasing the corrosion rate. In addition, by having elements nobler than aluminum in the matrix the cathodic effect is accelerated resulting in less resistance against corrosion in the aluminum alloy.

Galvanic corrosion

The additional elements create the possibility of another type of corrosion known as galvanic corrosion. Three conditions are required for this type of corrosion [31]:

- Two metals of different kinds
- Having an electrical contact between two metals
- Immersion of the metals in the same electrolyte

The anodic metal is consumed in a galvanic reaction, which is usually aluminum, resulting in aluminum thinning. However, by avoiding contact of more cathodic metals with aluminum and plating the Al with more compatible material this type of corrosion is preventable.

Other forms of corrosion

Other forms of corrosion occur in aluminum alloys, including exfoliation and stress corrosion. Exfoliation corrosion happens on the parallel planes leading to layer separations by corrosion by-products. The stress corrosion cracking occurs in conditions in which the material is under mechanical and chemical stress. In this case, the corrosion starts at the tip of the stress positions [31].

2.1.3. A mathematical model of aluminum pitting corrosion

As mentioned before the corrosion phenomenon is an electrochemical reaction and it generates a current know as i_{corr} which consists of two currents i_{external} and i_{internal}. Because of the generated potential difference between metal tracks, the external current is measurable and it flows in an external circuitry. However, the internal current happens inside the cell and direct measurement is not possible. The i_{corr} is calculated as shown in the Eq. 2.4.

$$i_{\text{corr}} = i_{\text{external}} + i_{\text{internal}} \tag{2.4}$$

The general steps observed in corrosion phenomena are summarized below.

1. Formation of a thin film of moisture in contact with the metal layer from the condensation of water vapor molecules
2. Impurities such as Cl^- ions are transported to the water layer and are dissolved in it, creating an electrolyte solution
3. The passivation layer is disturbed by the reactive ions of electrolyte, exposing the aluminum layer to the electrolyte
4. The aluminum layer starts to oxidize (as described in the previous section) and the produced ions react with the anions available in the solution and form by-products

Carl E.Hoge [7] has suggested a mathematical framework for the corrosion of aluminum tracks. This model introduces various important factors that are influencing the corrosion rate and helps to evaluate the impact of each factor.

The kinetic of any reaction is determined by the slowest steps, especially if the remaining steps are many orders faster. Carl E.Hoge [7] suggests that the rate of aluminum

corrosion is determined by the diffusion of aluminum ions through the passivation layer which is the slowest step. This assumption is logical considering the fact that the oxidation of aluminum atoms and the transport of ions in the liquid are both much faster steps. However, any condition that affects the rate of each step can jeopardize the assumptions made here such as a change in the ion transport rate or the disturbance of the passivation layer, leading to different kinetics than explained in this report.

Ion diffusion

Nevertheless, assuming the ion diffusion as the rate-determining step leads to a direct correlation between the diffusion rate of aluminum ions and the corrosion current. The diffusion rate of aluminum ions is defined in the Eq. 2.5.

$$D_{Al^{3+}}(\text{ Chemical }) = D_o \left\{ \exp\left(-\Delta G^{o^+}_{\text{Chemical}} / RT \right) \right\} \tag{2.5}$$

Where

D_o	pre-exponential
$\Delta G^{o+}_{\text{Chemical}}$	chemical free energy
R	gas constant
T	absolute temperature

Gibbs free energy is the thermodynamic potential of a specie. It is defined to calculate the maximum work a system has to endure in a reaction depending on the temperature and pressure. For example, a negative difference in Gibbs free energy for a reaction means that the reaction is spontaneous and it will happen without any extra energy requirements. Equation 2.6 shows how the drift velocity of an ion in the presence of chemical potential is calculated. Where l, is the jump distance of the ion ($\approx 2 \times 10^{-8} cm$).

$$v_d(\text{ Chemical }) = D_{Al^{3+}}(\text{ Chemical }) / l = D_o \left[\exp\left(-\Delta G^{o+}_{\text{Chemical}} / RT \right) \right] / l \tag{2.6}$$

Electrical field effect

However, in the case of an electrical field presence, another term is included in the equation as shown in Eqs. 2.7 and 2.8.

$$v_d = D_{Al^{3+}}(\text{ Total }) / l \tag{2.7}$$

$$v_d = \left\{ D_o \left[\exp\left(-\Delta G^{o+}_{\text{Chemical}} / RT \right) \right] \cdot \left[\exp\left(-\Delta G^{o+}_{\text{Elect}} / RT \right) \right] \right\} / l \tag{2.8}$$

The terms D_o and $\Delta G^{o+}_{\text{Chemical}}$ are determined by the properties of the oxide layer on the aluminum which are related to the contamination concentration or the chosen deposition method. On the other hand, the $\Delta G^{o+}_{\text{Elect}}$ term represents the effect of an electrical field. The temperature influences the system exponentially, which is expected in a corroding system. The corrosion current is a function of drift velocity as shown in the Eq. 2.9:

$$i_{\text{corr}} = AzFcv_d \tag{2.9}$$

Where

A	a geometric factor
F	Faraday constant
c	concentration of the diffusing ion
Z	charge on the ion

Water height effect

Another important factor influencing the magnitude of the corrosion current is the geometric factor (A). The geometric factor is a representation of how the configuration of the water film above the metal lines would affect the corrosion rate. Since the ions need to travel through the bulk of the liquid film, the width times height (the path that the ions pass) of this layer plays an important role. It is widely suggested in the literature that three monolayers of water molecules (≈ 8 Angstroms thick) are enough to become electrically conductive. In addition, fewer layers of water lead to a higher concentration of ions due to the low volume of the solvent which creates a more conductive solution. The geometry used in this mathematical model is demonstrated in Fig. 2.4. Here t_{ox} is the thickness of the passivation layer.

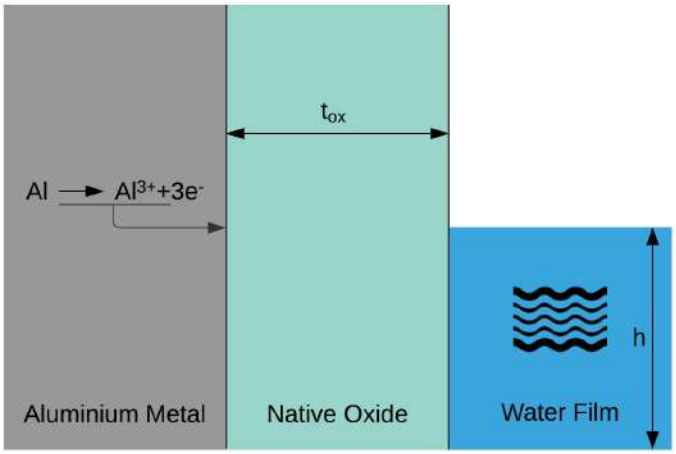

Figure 2.4: The geometry of the corrosion model [7]

In order to calculate the geometrical influence of the liquid film, the BET (Brunauer-Emmett-Teller) equation is commonly used. The amount of gas molecules absorbed on a solid surface at a specified partial pressure follows the BET Eq. 2.10. In this equation, the n and n_m are respectively the total amount of absorbed water and the monolayer coverage of the water. P_i is the partial pressure of the absorbed moisture. C relates to the difference between the latent heat of vaporization and the monolayer vaporization heat.

$$n/n_m = cP_i/\{(1-P_i)(1+(C-1)P_i)\} \tag{2.10}$$

The n/n_m is an estimation of the water layer height. It can be measured experimentally or by using the available plots as shown in Fig. 2.10. In any ambient condition, the value of C can be calculated and the value of n/n_m can be determined in any relative pressure.

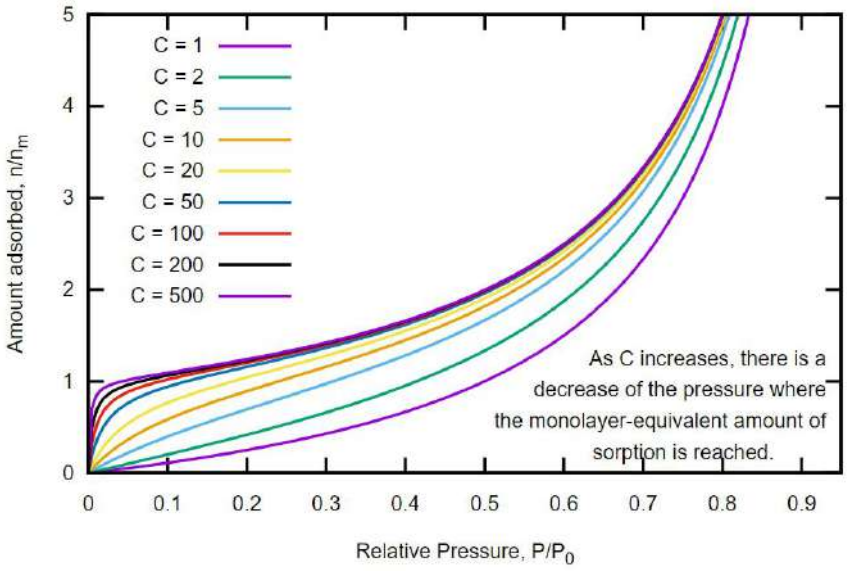

Figure 2.5: The monolayer coverage plot versus relative pressure [7]

Corrosion current

After the value of n/n_m is measured or calculated by using Eq. 2.10, an estimation of water height (h) can be calculated from Eq. 2.11. The A_{H20} is the cross-section area of a water molecule. After substituting the described equations in the corrosion current formula the final equation for the corrosion current is shown in Eq. 2.12.

$$\begin{aligned} h &= x\,(A_{H20})^{1/2} \\ x &= n/n_m \end{aligned} \tag{2.11}$$

$$\begin{aligned} i_{\text{corr}} &= zFcD_o \left\{ \exp\left(- \left[\Delta G^{o+}_{\text{Chemical}} + \Delta G^{o+}_{\text{Elect}} \right] / RT \right) \right. \\ &\left. \cdot \left[\left(CP_i\,(A_{H20})^{1/2} \right) / \{(1-P_i)\,(1+(C-1)P_i)\} \right] \right\} \end{aligned} \tag{2.12}$$

Corrosion current is analogous to the time of failure of an electronic circuit. It represents ion transport which results in aluminum corroding and becoming non-conductive. Equation 2.12 can be summarized as follows:

$$I_{\text{corr}} = \{(\text{ Constant }) \times (\text{ Film Height }) \times (\text{ Diffusivity })\} \tag{2.13}$$

The derived mathematical model help in understanding how the chemical deposition of the oxide layer, the presence of an electrical field, the amount of water absorption, and the temperature are influencing the corrosion rate. Among the influencing factors, the amount of water accumulated on the tracks is controllable by utilizing suitable packaging techniques. An isolating package assures that the device is protected from body fluids and corrosion. In addition, a suitable package protects the body tissues from the active parts and the sharp corners of the devices. The two types of packaging (hermetic and non-hermetic) are introduced in Section 2.2.

2.2. Packaging of IMDs

Protecting electronic devices from moisture ingress has always been a challenging task. Several methods have been developed for this purpose that can be categorized as hermetic and non-hermetic packaging options. Conventionally, IMDs are packaged in a hermetic way, which isolates them from bodily fluids and prevents corrosion. However, rapid developments in microfabrication have led to smaller and more delicate bioelectronic devices. As a result, hermetic packaging is becoming a limiting factor in the miniaturization of these devices. Therefore, different approaches are required for protecting microdevices from corrosion. One method is using polymeric encapsulation, especially for flexible microelectronics. Polymer encapsulation provides many advantages such as biocompatibility, affinity with existing microfabrication technology, and flexibility. On the other hand, polymers are permeable to water, as a result, further development is necessary to make this type of encapsulation suitable and safe for long-term implants [38].

2.2.1. Hermetic packaging

A hermetic package by definition means an airtight sealing. By using a water-impermeable material as a shell surrounding the components, hermetic sealing is achieved (Fig. 2.6). Several methods have been developed to reach an acceptable level of sealing. Metals, ceramics, and glass are used to fabricate the solid shell because of their impermeability to water.

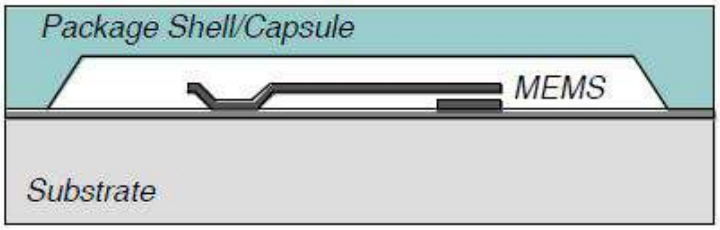

Figure 2.6: Hermetic packaging

Regardless of the method and the precision level, water can accumulate in this type of packaging during the packaging steps or by the feedthrough of the system and result in corrosion. However, if the water ingress level of a package is low enough so that no condensation will happen in the intended lifetime of the device, it is considered to be a hermetic package [36]. Helium leak tests are used to evaluate the reliability of hermetic packages. In order to perform the tests, the void of the package is filled with helium before sealing or the package is exposed to high-pressure helium to force it inside the package. Next with the use of a mass spectrometer, the leaking helium level is measured. According to a study done by Vanhoestenberghe et al. [44], the helium leakage rate (L_{He}) can be calculated by the following Eq. 2.14. It is assumed that the working temperature is 37 ° C and the gases are ideal gases.

$$L_{He} \leq \frac{V \times \ln\left(\frac{1}{1-RH_{\text{crit}}}\right)}{743 \times t_n} \tag{2.14}$$

The helium leakage detection depends on the sensitivity of the mass spectrometer. With currently available technology, leakages from volumes smaller than $\sim 1\text{mm}^3$ are

not in the detectable range. Thus, hermetic packaging reaches its limitation for miniature devices due to non-detectable leakage rates as well as fabrication constraints [44]. In addition, the reliability of hermetic packaging is further challenged by the assumption that three monolayers of water are required to initiate corrosion. By a decrease in packaging size, a smaller amount of water ingress can already result in three monolayers of coverage inside the capsule and promote degradation. In contrast to larger-scale packaging where a high water intake is required to form three layers of water on the interior of the device [5].

2.2.2. Non-hermetic packaging

Non-hermetic or conformal packaging is an alternative approach to protect electronic components by using a thin layer of material encapsulating the system. This thin layer is permeable to water molecules, thus, it is categorized as non-hermetic. However, advantages such as biocompatibility, low-cost, affinity with micro-fabrication processes, and the ability for it to be applied to miniaturized devices, make it attractive for application in bioelectronic devices. Both inorganic and polymeric materials are used separately or in combination for conformal encapsulation.

Inorganic thin-film layers

Inorganic materials provide low moisture and ion diffusion, thus making them suitable candidates for coating applications. Materials such as Al_2O_3, SiO_2, Si_3N_4, HfO_2, and SiC are used to passivate the surface of IC components.

Al_2O_3

Alumina has been used as a moisture barrier conventionally together with titanium hermetic sealings. It has been proven to be a moisture barrier and it is transparent to RF. Thin layers of alumina made by atomic layer deposition (ALD), pave the way for micro-scale conformal coverage by this material. However, alumina hydrolyzes and dissolves in water which results in insufficient protection for the IMD. In order to overcome this problem, researchers have used alumina in combination with polymeric coatings to reach a higher level of protection.

Minnikanti et al. [25] have tested interdigitated electrode (IDE) structures with 130 μm spacing and width. The electrodes of the samples were layered with Ti (100 nm)/Pt(150 nm)/Au(150 nm) combination. The samples were coated with 52 nm of ALD Al_2O_3 followed by 6 μm of Parylene C (deposited by Gorham process). Soaking tests were performed on the samples in 60 °C PBS solution.

By utilizing a potentiostat, EIS measurements were performed at a 0.01 Hz to 10 kHz frequency range and with a 50 mV_{rms} AC sinusoidal waveform. In addition, the leakage current (LC) of the comb structures was measured at 5V DC. Figure 2.7 shows LC measurements of a failed sample in this study. The results presented in this study suggest a mean time to failure (MTTF) of 36 months for the samples with alumina-Parylene C coating and 8 months for Parylene C samples. Delamination, blistering, and micro-pores are reported as the main causes of failure in this study.

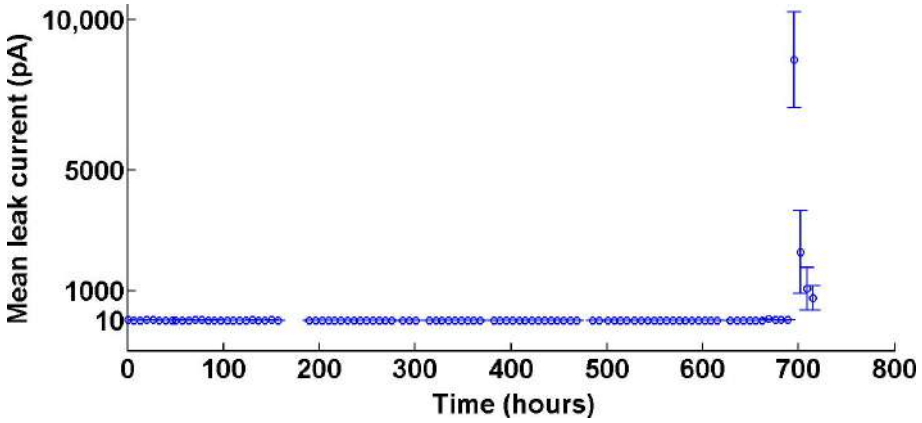

Figure 2.7: Leakage current at 5V DC over soaking time at 60 ° C for Alumina-Parylene C coated IDE sample [25]

SiO_2, Si_3N_4, and SiC

Plasma-enhanced chemical vapor deposition (PECVD) of silicon dioxide and/or silicon nitride as a passivation layer for electronic devices is common. This method of deposition results in strong chemical bonds due to the utilization of a plasma. In addition, PECVD enables low-temperature processes resulting in lower cost and wider material options.

Silicon dioxide has been used as an interlayer dielectric due to its high bulk resistivity. However, a high moisture permeation coefficient is reported for this material [26]. In silicon nitride, on the other hand, less ion and water permeation is observed. Thus, a combination of silicon oxide and silicon nitride components (SiO_xN_y) are also frequently used in passivation layers for electronic devices. Regardless of the many advantages that these layers provide, their dissolution in water still remains a challenge. Equations 2.15 to 2.17 depict the reactions of SiO_2 and Si_3N_4 in water (Si_3N_4 first oxidizes to SiO_2).

$$Si_3N_4 + 6H_2O \longrightarrow 3SiO_2 + 4NH_3 \tag{2.15}$$

$$SiO_2 + 2H_2O \longrightarrow Si(OH)_4 \tag{2.16}$$

$$Si(OH)_4 + OH^- \longrightarrow (OH)_3SiO^- + H_2O \tag{2.17}$$

In contrast to silicon oxide and silicon nitride, silicon carbide is proven to be robust against dissolution. SiC has low water diffusion and high flexibility and it is chemically inert. Additionally, studies have reported that SiC is highly biocompatible [35].

Lei et al. [15] have performed accelerated soaking tests at 87 °C on three types of silicon substrates coated by PECVD SiC, Si_3N_4, and thermal SiO_2. They report a high dissolution rate of 18.3 ± 0.3 nmd^{-1} for Si_3N_4 samples. They witness a color change, bubbling, and water ingress in this material in the course of 29 days. On the other hand, SiC samples didn't show dissolution in 16 weeks of the experiments. SiO_2 samples exhibit a dissolution rate of 0.104 ± 0.008 nmd^{-1} in this study. The thickness measurement results of these materials are plotted in Fig. 2.8.

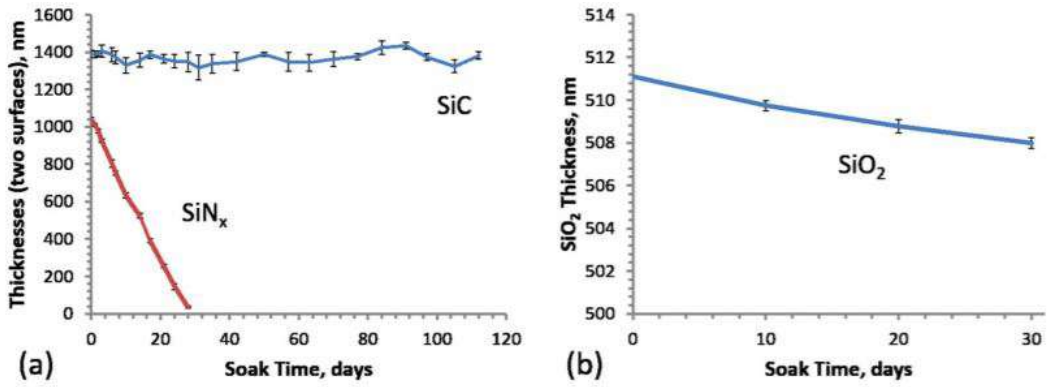

Figure 2.8: Dissolution rate in 87 °C (a) PECVD Si_3N_4 and SiC (b) thermal SiO_2 [15]

HfO_2

Thin films of HfO_2 are deposited by ALD technology. This material is optically transparent in the range of 300-10000 nm, thus, it is widely used as an optical coating [38]. Jeong et al [13] conformally coated on-silicon aluminum IDE structures with HfO_2 and a combination of HfO_2 and SiO_2 with the thicknesses as shown in Fig. 2.9.

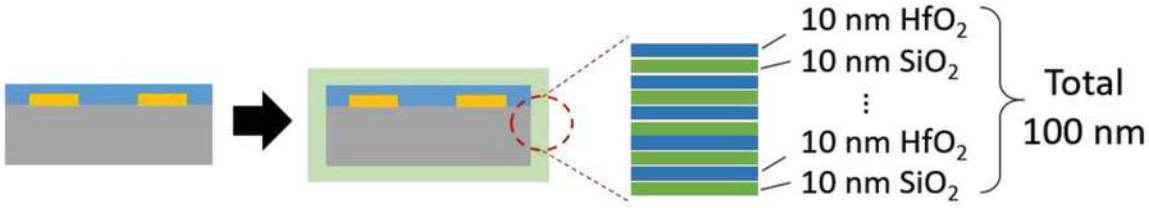

Figure 2.9: Stack-ups of the samples coated with HfO_2 and SiO_2 [13]

A soaking test at 87 °C in PBS solution is performed on the samples and the leakage current was measured. Following the immersion, a sudden increase of leakage current from a few pA to 10-100 pA is observed. The authors suggest that this increase can be due to the outgassing of the sealing at a higher temperature. A constant LC is seen after the initial increase until sudden jumps in the current (>1μA) happen and the devices fail. For samples with HfO_2 the failures happen at 126 days on average and for HfO_2/SiO_2 samples 170 days on average. In Fig. 2.10 the LC plots of the samples are depicted.

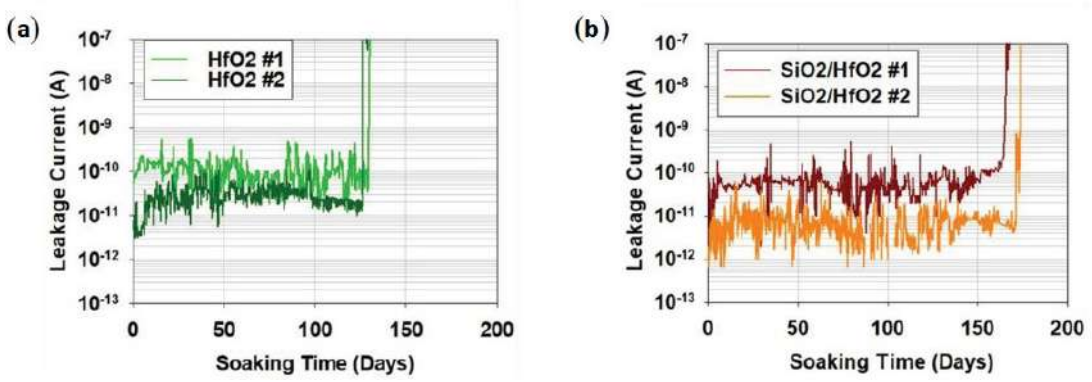

Figure 2.10: The leakage current plots of the samples with (a) HfO_2 (b) HfO_2/SiO_2 at 87 °C [13]

Organic packages

Although inorganic materials have high barrier properties, dissolution in an aqueous environment limits their application as conformal packaging. In contrast, polymers don't dissolve in water, they are flexible and stable. As a result, there is an increasing application of polymeric encapsulations for IMDs, especially for flexible electronic systems. Polymide, Parylene C, liquid crystal polymer (LCP), and Silicone elastomer are examples of polymers used for packaging purposes.

Polyimide

Polyimide is a polymer of imide monomers. Several types of these polymers exist depending on the composition of the monomer. However, BPDA/PPD is a common type used in medical devices. Studies have reported low cytotoxicity and high biocompatibility for polyimide [38]. The high chemical and mechanical stability of this material is promising for encapsulation applications. The high flexibility of polyimide makes it suitable for flexible electronics. In addition, polyimide is widely compatible with microfabrication processes and it can be applied by spinning the liquid form or using the film and tape forms.

Parylene-C

Parylene is a semi-crystalline polymer and the Parylene-N, Parylene-C, and Parylene-HT types are ISO 10993 certified. This polymer exhibits low moisture uptake (<0.1 %), especially for Parylene-C. Chemical vapor deposition (CVD) is used to create a pinhole-free and thin layer of this material on different topography configurations. However, on the downside, Parylene is not mechanically robust [38].

Liquid crystal polymer (LCP)

Liquid crystal polymer is a thermoplastic layer, and 3D structures can be created by thermal deformation of the LCP layers. Layers of LCP can be thermally pressed in order to bond them together or to a substrate. Low-temperature melting LCP is used as an adhesive layer between high-temperature melting LCP layers. The advantage this material provides is low water absorption (<0.04%) [38].

Silicone Elastomer

The most known silicone elastomer for microfabrication applications is polydimethylsiloxane (PDMS). This material is biocompatible and it is widely used for imprinting. PDMS is usually molded or cast and cured at an elevated temperature. Although it is widely used in flexible and stretchable devices, the high moisture absorption limits its usage as encapsulation material.

2.2.3. Organic encapsulation examples in literature

Table 2.1 summarizes some properties of the aforementioned polymers, and examples of lifetime tests performed on these materials are provided next.

Table 2.1: Properties of polymeric encapsulation material [38]

Properties of Materials	**Polyimide**	**Parylene C**	**LCP**	**Silicone Elastomer**
Encapsulation method	Spin coating	CVD	Thermal bond	Casting, spin coating
Tensile strength (MPa)	128	69	180-190	6.7
Elongation (%)	10	200	30-40	305
Moisture absorption (%)	2-3	0.06–0.6	0.04	-
Dielectric coefficient	3.3 (1 kHz)	3.1 (1 kHz)	3.3 (2.8 GHz)	2.68 (100 kHz)
Resistivity ($\Omega.cm$)	10^{16}	8.8 x10^{16}	2 x10^{16} – 3x10^{16}	2.9 x10^{14}
Refractive index	1.7	1.639	-	1.3997-1.4225

Lifetime evaluation of Polyimide, Parylene-C, and LCP

Woo Lee et al. [18] have evaluated the encapsulation performance of polyimide (PI2525), Parylene-C, and liquid crystal polymers (LCPs) on multi-interdigitated electrodes (MIDEs). The thickness of polyimide, Parylene-C, and LCP are 10, 10, and 25 μm respectively in this evaluation. IDE patterns of 300 μm width and 300 μm spacing are designed and fabricated by three different stacking layers as shown in Fig. 2.11. Soaking tests are performed on the samples in 37 °C and 75 °C with a 5V DC bias. The multi-channel IDEs structures and the schematic of the test set-up are shown in Fig. 2.12.

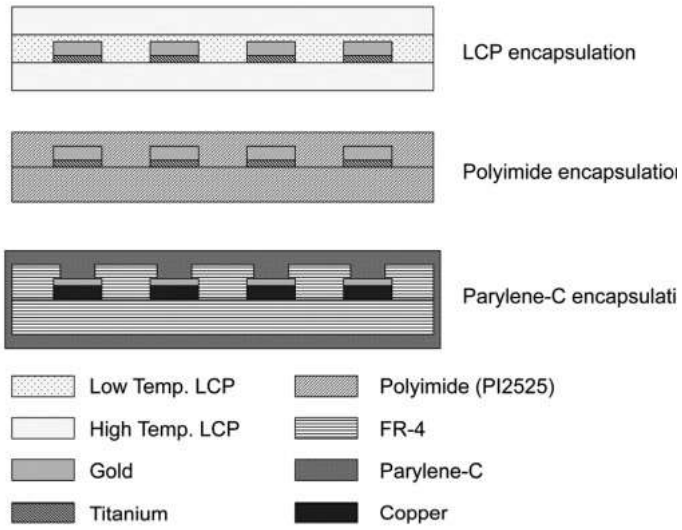

Figure 2.11: Cross-sectional view of the IDEs encapsulated by LCP, polyimide, and parylene-C.[18]

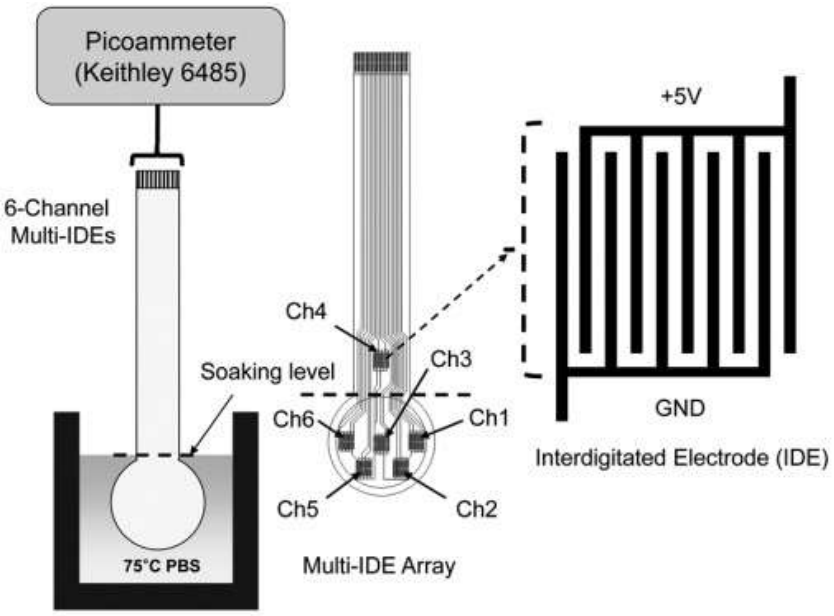

Figure 2.12: Schematic of the MIDEs and the measurement set-up[18]

The leakage current of the samples is used as an indication of the system's reliability performance. A threshold level of 1 μA is set for system failure. According to this study, the polyimide and Parylene-C packages fail at 66 and 117 days respectively. However, the LCP sealing is functional for more than 300 days. The detailed results for the polyimide soaking test are demonstrated in Fig. 2.13. Initially, leakage currents of 1 to 3.7 pA are reported for 5V DC bias. Within 48 days the current gradually increases to 16-152 nA. After this phase channels start to fail (current higher than 1 μA). However, it is reported that the channels located in the periphery (channels 1,2,5, and 6) fail earlier than the channel in the center (channel 3). Channel 4 is the unsoaked control unit in this experiment.

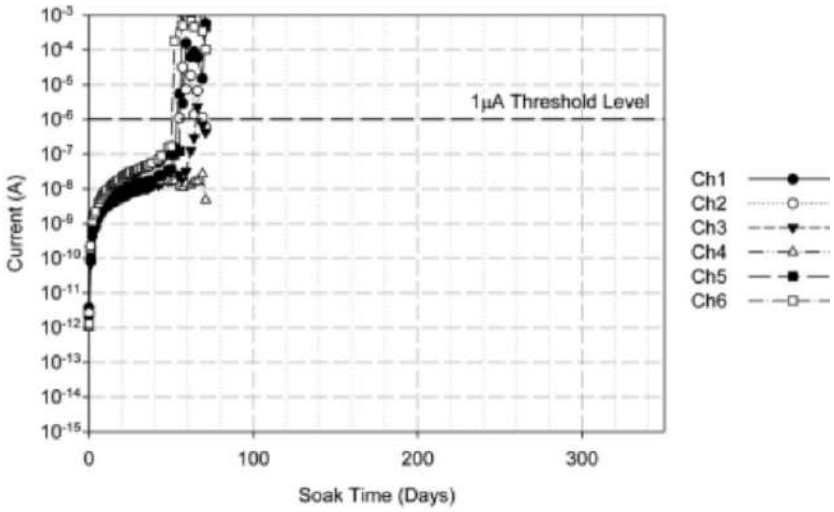

Figure 2.13: Polyimide leakage current measurement during in vitro accelerated soak tests using 75 °C PBS in log scale[18]

Lifetime evaluation of polyimide and LCP

In order to evaluate the long-term stability of neural interfaces, Woods et al. [46] tested samples of 61-channel micro-electrocorticographic (μECoG) electrodes, coated with polyimide and LCP encapsulations. The structures were made of pure gold, and the electrodes with a diameter of 200 μm and center to center distance of 400 μm were located in an 8x8 grid. The structures and their cross-section are shown in Fig. 2.14.

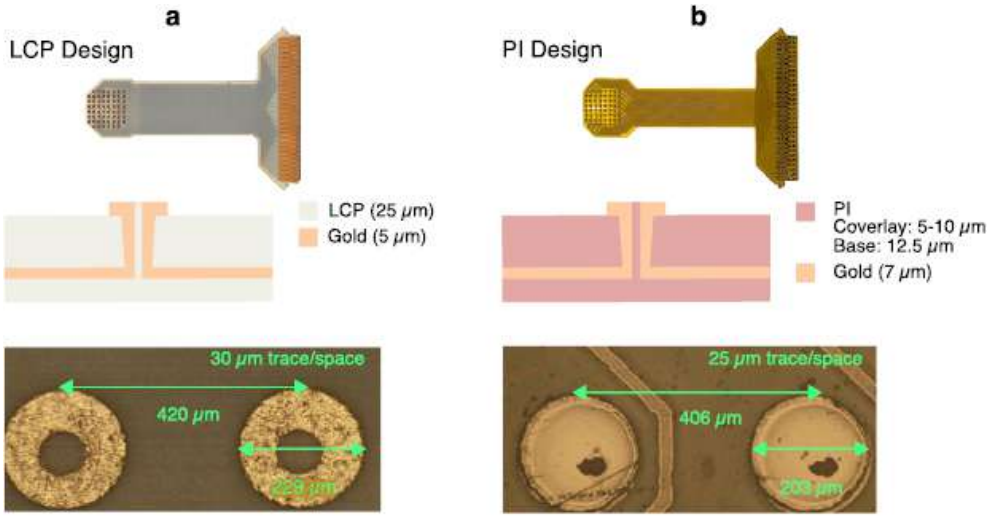

Figure 2.14: The μECoG design with gold interconnects and contacts with an encapsulation of (a) LCP (b) PI [46]

The samples were soaked in PBS solution at 60 °C and were tested by impedance measurements. In this study, an electrode yield (the ratio of working channels to the initial sites) less than 50% was considered to be the failure point. Lifetime estimations of 4-7 years had resulted from some of the polyimide samples. However, for other PI samples fabricated by the same method, delamination was observed. Figure 2.15 shows the delaminated polyimide samples in this study which unlike the samples without delamination, resulted in complete failure. The LCP encapsulation tests in this study didn't show any failure, however, due to a test chamber defect the data and samples were not useful anymore.

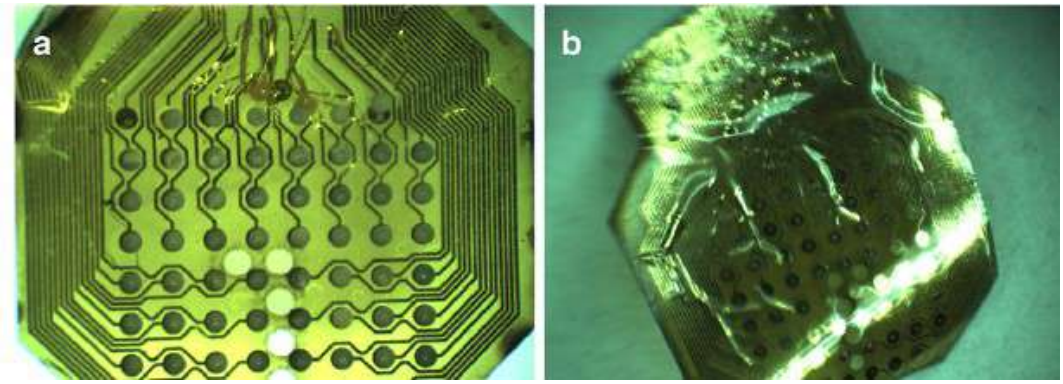

Figure 2.15: Pictures of the (a) PI delamination after 9 days of accelerated aging; (b) PI delamination after 191 days of accelerated aging [46]

2.2.4. Combination of inorganic and organic materials

It was mentioned earlier that inorganic materials, despite the fact that they have a low water absorption, tend to dissolve in water. In contrast, most organic material are permeable to water, but chemically and mechanically robust. These observations lead to a new approach in encapsulation that combines the properties of these materials. Examples of hybrid encapsulations are discussed in the following sections.

Polyimide and Hafnium dioxide

In a study done by Li et al. [19], four types of encapsulation including: (a) Al_2O_3 (b) $HfO_2/Al_2O_3/HfO_2$ (symbolized as ALD-3) (c) PI (d) PI/ ALD-3/ PI were applied to a copper film. A summary of the configurations and layer thicknesses is depicted in Fig. 2.16.

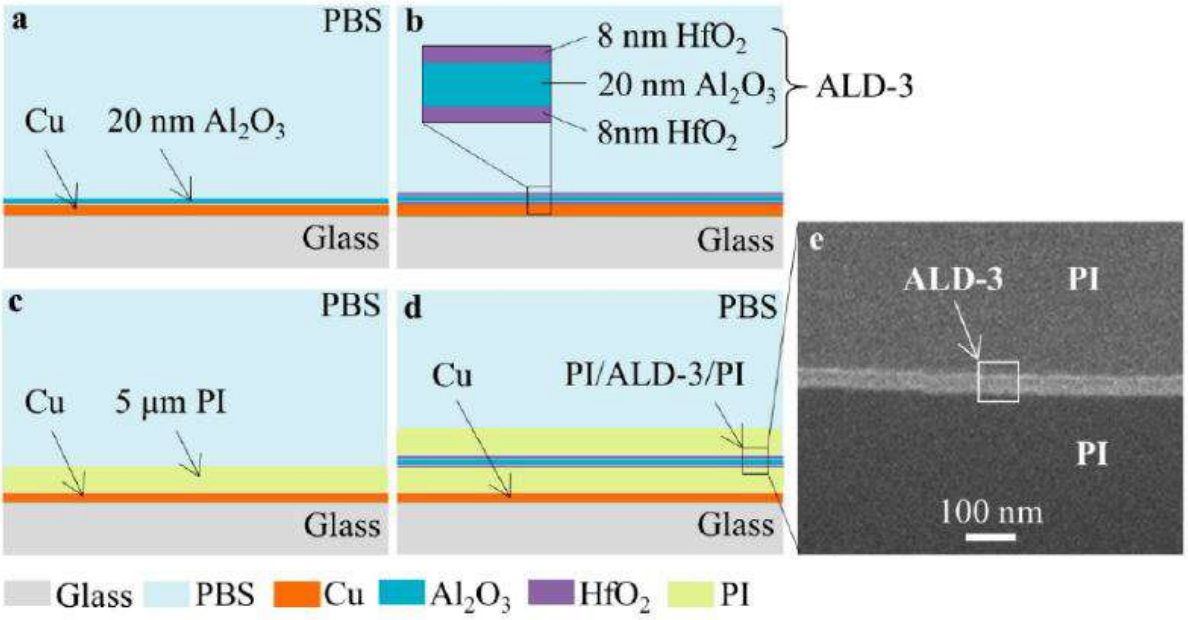

Figure 2.16: The stack-ups of four types of encapsulations on copper film (a) Al_2O_3 (b) $HfO_2/Al_2O_3/HfO_2$ (ALD-3) (c) PI (HD2611) (d) PI/ ALD-3/ PI (e) Cross-section FIB-SEM of the PI/ALD-3/PI [19]

The samples were soaked in PBS at 60 °C and characterized by EIS and water vapor transmission rate (WVTR). For the PI-only samples a WVTR of 4.3 $g \cdot m^{-2} \cdot day^{-1}$is reported while for the PI/ALD-3/PI samples this is less than 5×10^{-4} $g \cdot m^{-2} \cdot$ day $^{-1}$. Figure 2.17 shows the EIS measurements of these two samples.

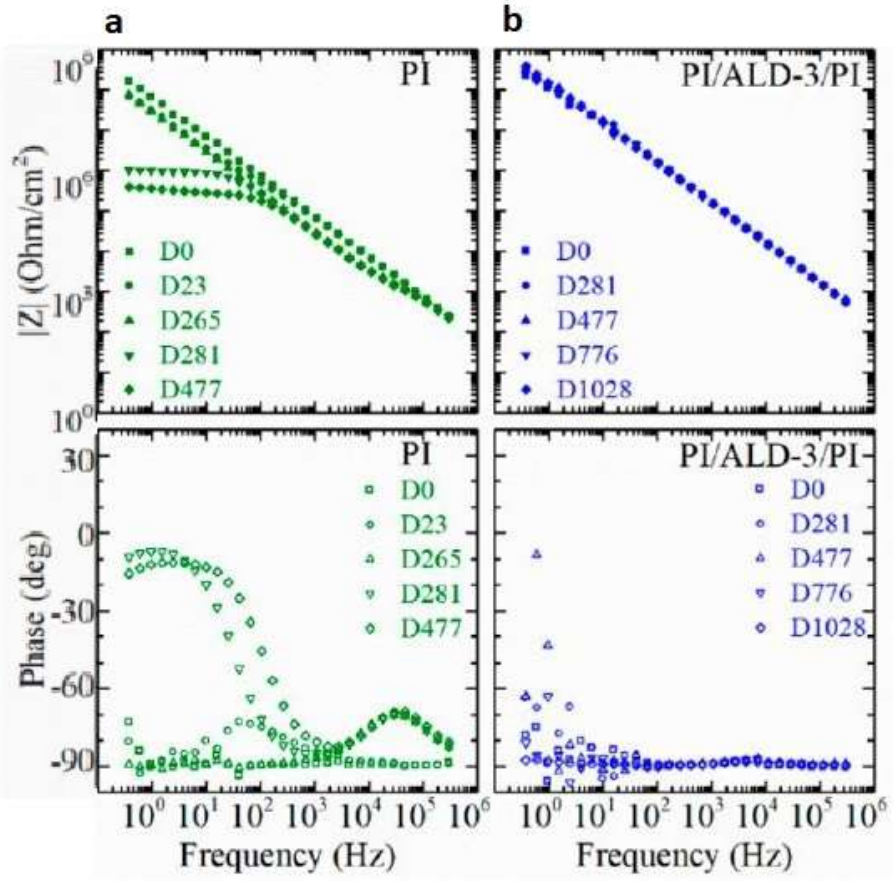

Figure 2.17: EIS results of (a) PI (b) PI/ALD-3/PI encapsulation with respect to days in PBS (D0,D29,...) [19]

In the early stage of soaking the PI-only samples showed a good barrier behavior with -90° phase at low frequencies. Following the soaking, polyimide (ε_r=2.9) absorbed water which has a higher dielectric constant (ε_r=78) resulting in a decreased impedance. Around day 281 the impedance at low frequency decreased rapidly, and the phase shifted from -90° to -10° which indicated the encapsulation failure. However, for samples with PI/ALD-3/PI, no failure was seen until day 1028, and a lifetime of 14.3 years was predicted in 37°C.

Polyimide and SiC/SiO_2

Ordonez et al. [28] have investigated the effect of thin ceramic layers of SiC and SiO_2 on the adhesion of PI (BPDA-PPD) to PDMS (MED-1000). A 5 μm thick layer of polyimide was covered by 50 nm SiC, 50 nm SiO_2, and 20 μm PDMS. The fabrication steps of the samples and the expected chemical bonds are shown in Fig. 2.18.

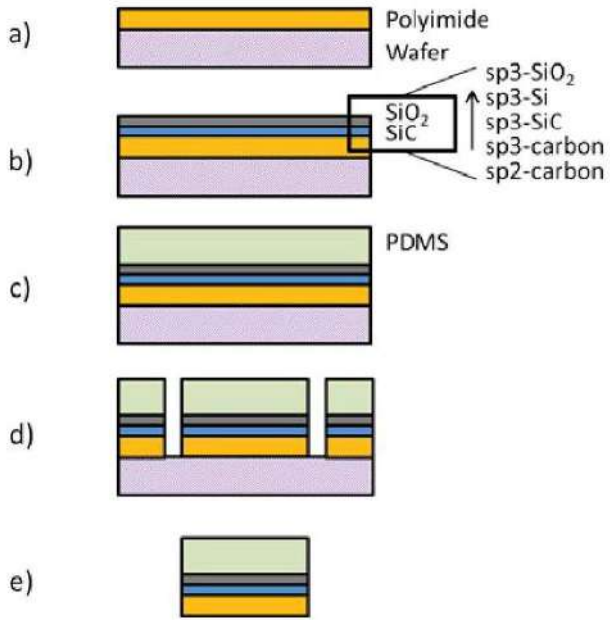

Figure 2.18: Process flow (a) deposition of PI (b) PECVD of ceramic layers and the chemical bonds formed between layers (c) PDMS coating (d) separation of samples (e) release from the wafer [28]

This experiment was based on using the interdiffusion principle. By utilizing the SiC and SiO_2 layers the two polymer surfaces are expected to form strong chemical bonds. The sp2-hybridized carbon in the aromatic structure of polyimide is believed to covalently bond to carbon in SiC (the sp3-hybridized carbon of SiC). Followed by a PECVD layer of SiO_2, Si-Si bonds are formed between the two ceramic layers. The SiO_2 if treated by the silanization process to make covalent -Si-O-Si- bonds, is a suitable surface to bond to PDMS.

Samples were placed in a pressure cooker (125 °C and 130 kPa) for 96 hrs. Samples without adhesion-promoting layers were easily delaminated by a scalpel blade. Units with adhesion-promoting layers were subjected to mechanical detachment tests. The mechanical force resulted in the rupturing of the polyimide, but not the separation of polymer layers. As a result, the PECVD stack of SiC and SiO_2 was suggested as a strong adhesion-promoting layer for polyimide and PDMS.

2.2.5. Summary of non-hermetic packaging studies

Various materials are used to protect bioelectronic devices from corrosion. Although an ideal method has not been found yet, several studies are conducted with different materials and methods to contribute to this important subject. In addition to the studies presented in this chapter, Tab. 2.2 and Tab. 2.3 present summaries of more lifetime estimations performed with various materials.

Table 2.2: Organic material used in literature as soft encapsulation [38]

Material	Deposition method	Thickness	Testing Temp. (°C)	Test Samples	Measured	Results	Lifetime years (37 °C)	Ref.
Polyimide	Spin	10 m	75	IDE	LC [1]	66 days	2.52	[18]
		10 m	60	Electrode array	EIS [2]	400	5	[46],[30]
Parylene C	CVD	10 m	75	IDE	LC	117 days	4.46	[18]
		40 m	85	Electrode array	Resistance	31 days	2.4	[2]
		6 m	60	IDE	LC, EIS	49 days	0.66	[24]
		6 m	57	IDE	LC	150 days	1.64	[47]
		6 m	67	t-type IDE	LC	110 days	2.4	[1]
PDMS	Spin	150 m	36.5	Electrode array	EIS	54% (209 days)	-	[12]
LCP	Thermal bonding	25 m	75	IDE	LC	379 days	14.5	[18],[11]
		25 m	87	IDE	LC	87 days	7.6	[6]

[1] Leakage Current
[2] Electrochemical impedance spectroscopy

Table 2.3: Inorganic material used in literature as soft encapsulation [38]

Material	Deposition method	Thickness	Testing Temp. (°C)	Test Samples	Measured	Results	Lifetime at 37 °C (years)	Ref.
SiO_2	Thermal	511 nm	87	Photodiode	DR[1]	0.104 nm/day	-	[15]
	LPCVD	520 nm	90	Films	DR	1 nm/h	No dissolution for 22 weeks	[3]
SiC	PECVD	694 nm	87	Photodiode	DR	No dissolution	-	[15]
		67 nm	90	Films	DR	0.1 nm/h	No dissolution for 40 weeks	[3]
		90 nm	90	IDE	EIS [2]	-	No dissolution >6 weeks	[8]
HfO_2	ALD	100 nm	87	IDE	LC [3]	126 days	11.1	[13]
HfO_2/SiO_2	ALD	100 nm	87	IDE	LC	170 days	14.9	[13]

[1] Dissolution Rate
[2] Electrochemical Impedance Spectroscopy
[3] Leakage Current

2.3. Accelerated lifetime tests for corrosion studies

To evaluate the functionality of a hermetic package, methods such as the helium leak rate is used. However, this method can't be used for non-hermetic encapsulations. To reach a reliable estimation of the lifetime of devices with a conformal encapsulation, accelerated life tests are performed. In an accelerated test, the stress factors are magnified in a controlled manner provided that irrelevant failure mechanisms are not introduced to the system. Stress factors vary depending on the system.

The corrosion processes are all chemical reactions and are directly influenced by the temperature, the humidity level, and the electrical field as discussed in previous sections. Implantable medical devices operate in a 100% humidity environment. To test the encapsulation, they are soaked in a Phosphate-Buffered Saline (PBS) solution at an elevated temperature under an electrical bias [29]. It is important to have an estimate of the influence of the stress factors to calculate an equivalent lifetime for the device under normal usage conditions.

2.3.1. Arrhenius relation for temperature effect

The Arrhenius Eq. 2.18 is used to estimate the temperature influence on the corrosion.

$$t = A \exp\left(\frac{E_a}{k_B T}\right) \tag{2.18}$$

Where

t	the time to failure
E_a	the activation energy of the reaction
A	pre-exponential constant
k_B	the Boltzmann constant
T	absolute temperature

By having the failure data of a device at multiple temperatures the E_a and A are calculated. Afterwards, the lifetime of the device is estimated by substituting the elevated temperature and the working temperature of the devices. However, an acceleration rate of $2^{\Delta T/10}$ is commonly accepted for lifetime tests. Meaning that every 10 °C increase in temperature, doubles the reaction rates [10].

2.3.2. Electrical characterization methods

For evaluating the packaging performance, various measurement methods exist such as dissolution rate, track resistance, Electrochemical Impedance Spectroscopy (EIS), and leakage current measurements. For the materials that dissolve in water, the dissolution rate is measurable by mass spectroscopy. The track resistance and leaking current between two isolated tracks are also good indications of the encapsulation failure. On the other hand, EIS is used to get a more detailed view of the mechanisms of the failure.

Four-point resistance measurement

Change in the electrical resistance of the interconnects in an electronic device is a sign of system failure. As previously mentioned, a corroded aluminum track results in an open circuit with very high resistance. In conventional two-terminal resistance sensing the contact resistance is negligible in comparison to the resistance of the intended circuit. However, two-terminal resistance sensing is not accurate for micro-scale interconnects due to the fact that the track resistance is small and the contact resistance is no more negligible.

To overcome this issue, a four-point measurement is used. Figure 2.19 is an illustration of the four-point resistance measurement system. In two-terminal sensing, the measured voltage drop is the result of voltage change over all of the connections, wires, and contact resistance. However, in a four-point system by one pair of the connections (force terminals), a known amount of current is applied to the track. Next, the voltage drop is measured by the other pair of connections (sense terminals) adjacent to the force terminals. Since the measurement devices have high resistance and don't allow current through, all the applied current will pass the unknown resistance. By knowing the measured voltage drop and the defined current value, the true resistance of the track is measured by Ohm's law (V=IR).

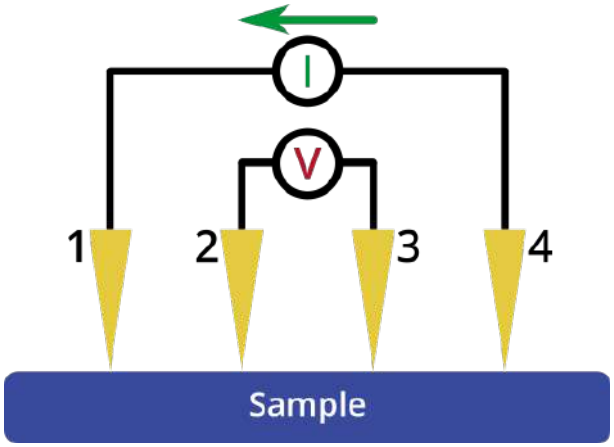

Figure 2.19: A schematic of the four-point resistance measurement system

Leakage current (LC) measurement

The leakage current in a component usually occurs due to imperfect insulators or moisture accumulation. In an ideal packaging situation, while biasing the electrodes no current should leak. However, no excellent encapsulation exists, as a result, an amount of current is measured. As the device encapsulation degrades, the leakage current increases. LC measurements are widely used for encapsulation evaluations [9]. A threshold current value is defined depending on the device structure, samples with higher LC are considered to have failed. LC values in the range of 1 nA and 1 μA are accepted as the failure threshold in various research projects [25] [13].

Electrochemical Impedance Spectroscopy

In an EIS measurement, by applying an AC signal, the dipoles of the system will orient in the direction of the electrical field. However, the frequency in which the dipoles turn has a delay compared to the electrical field frequency that is known as relaxation. The relaxation time is given by Eq. 2.19, R representing the resistance,

and C representing the capacitance of the system. For complex non-linear systems, the impedance is calculated by dividing the voltage U by the current I as a function of the angular frequency ω (Eq. 2.20). By a frequency sweep of the system, the resulting current is measured and the impedance can be calculated. In order to analyze the impedance spectrum, equivalent electrical circuit models are designed and the data is fitted on these models. Figure 2.20 is the equivalent circuit diagram representing a coated metal in an electrolyte solution. Figure 2.21 is the physical explanation of the elements in the electrical circuit model [45].

$$t = R \cdot C \tag{2.19}$$

$$Z(\omega) = \frac{U(\omega, t)}{I(\omega, t)} \tag{2.20}$$

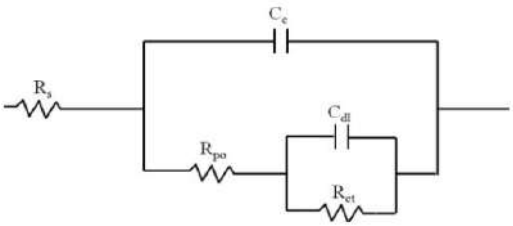

Figure 2.20: Equivalent circuit diagram representing a coated metal in an electrolyte solution [45]

Where

R_s	solution resistance
R_{ct}	charge transfer resistance
R_{po}	pore resistance
C_c	intact coating capacitance
C_{dl}	the double layer capacitance

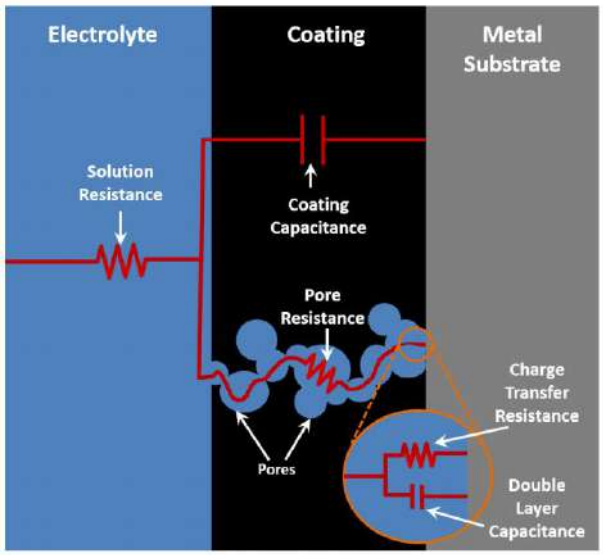

Figure 2.21: A schematic of the physical explanation of the equivalent circuit of a coated metal [45]

The impedance data is used to evaluate the elements of the equivalent circuit. A decreasing coating capacitance is an indication of coating degradation. In addition, water absorption over time decreases the pore resistance of the system. A functional coating should result in a full capacitance behavior with a -90° phase in the impedance measurements. For evaluating the coating properties lower frequencies are used as the surface properties are more visible in this range. At higher frequencies, the saline resistance and the comb impedance become more dominant.

3

Materials and methods

The materials and methods used in this thesis are explained in this chapter. The first section focuses on the sample structure and fabrication steps. Next, the testing set-up and the experimental methods are described.

3.1. Test devices

To evaluate the lifetime performance of polyimide encapsulated interconnects and the influence of SiC and SiO_2 layers on them, samples with and without SiC and SiO_2 layers are fabricated. Figure. 3.1 is a depiction of the cross-section of the samples (a) with the ceramic layers and (b) without the ceramic layers with the corresponding thicknesses.

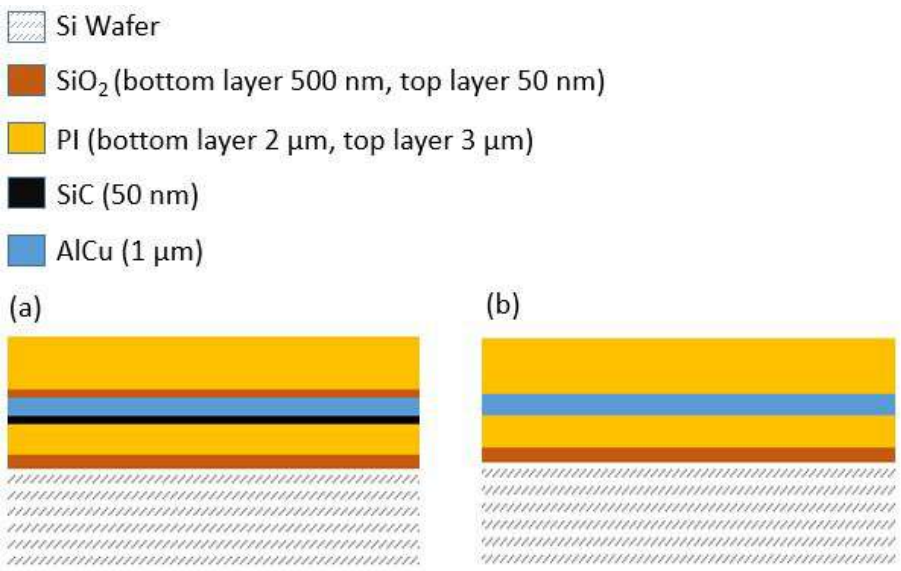

Figure 3.1: Stack-ups of samples (a) with thin ceramic layers of SiC and SiO_2 (b) without the ceramic layers

3.1.1. Materials

Polyimide (PI)

Polyimide-2610 (manufacturer: HD MicroSystems) is the polymer of choice for the flex-to-rigid platform. The thermal stability of this material enables high process temperatures and sterilization. The chemical stability, mechanical strength, and affinity with MEMS fabrication are among the reasons for this choice. The biocompatibility of this type of polyimide is widely investigated and no cytotoxicity is reported [33]. Polyimide is proved to have strong adhesion to metal oxide layers, which makes it a suitable candidate for encapsulation purposes [32].

Aluminum-copper alloy

Metal tracks of the devices are made of aluminum (Al) alloy with 1 wt% copper (Cu). Aluminum is widely used in IC fabrication processes and due to its oxide layer, it forms a strong adhesion to polyimide. The addition of copper to pure aluminum increases the maximum yield strength and stretchability of the material. Furthermore, copper atoms in the alloy improve the resistance against electromigration [42].

SiC

SiC is silicon (Si) and carbon (C) atoms covalently bonded together. These short strong bonds result in an inert and chemically and mechanically stable material. SiC is widely used in implantable devices such as bone prosthetics, dental implants, and coronary artery stents. The biocompatibility and hemocompatibility of this material are well documented [34]. Studies that test the adhesion between SiC and polyimide in accelerated conditions suggest that the adhesion stays intact and stable. The secure adhesion is achieved because of the strong covalent carbon to carbon bonds between polyimide and SiC [27].

SiO_2

SiO_2 layers are widely used in MEMS fabrication as protection layers. Due to covalent silicon-to-silicon bonds formed between SiC and SiO_2, strong adhesion between two materials is observed [28]. Due to numerous applications of SiO_2 in microfabrication, the adhesion of different materials to its surface is well studied and methods to improve this adhesion have been developed. One approach is using adhesion primers such as VMX651 (manufacturer HD MicroSystems) on the SiO_2 surface before applying organic materials. This aminosilane based primer initiates a process called silanization. Silanization is the process of adding organofunctional chloro or alkoxysilane molecules to the surface of an inorganic material. These functional groups create Si-O-Si bonds on the surface of SiO_2, creating an interface to form strong bonds with organic materials. As a result, primers such as VMX651 can be used to adhere SiO_2 to the polyimide.

3.1.2. The test structures

For lifetime tests, the devices under test (DUT) have to allow for electrical characterization such as measuring the line resistance or the line-to-line leakage current. Triple-Track [16] [43] and IDE [43] structures are commonly used for ageing tests (Fig. 3.2).

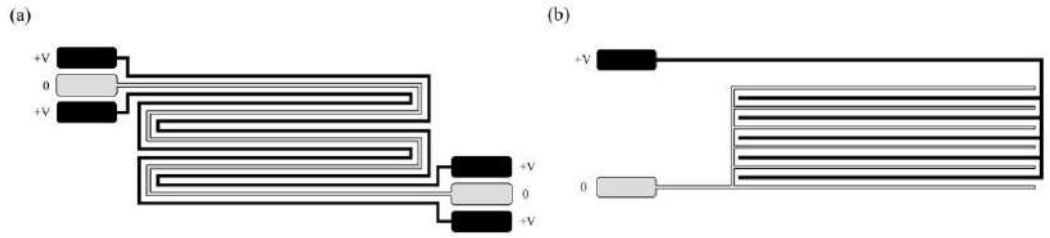

Figure 3.2: Schematics of aging test structures (a) triple-track (b) IDE [17]

Meandered IDE test samples

The samples are chips with 1×5 cm^2 dimensions that contain three aluminum-copper tracks of 150 μm width and spacing. The tracks are connected to large contact pads of 1×1 mm^2 for direct probing. In addition, smaller contact pads are incorporated in the design to allow for wire-bonding of the samples. The outermost track acts as a guard ring with 750 μm distance from the edge of the chip. Guard ring is suggested in literature in order to shield the tracks from external influences such as dicing and handling processes. Also, the guard track is connected to the ground of the system [14]. The two inner tracks form meanders in order to increase the total length of the interconnects. Interdigitated comb structures are implemented on the inner two tracks. Figures 3.3 and 3.4 illustrate the meandered IDE samples.

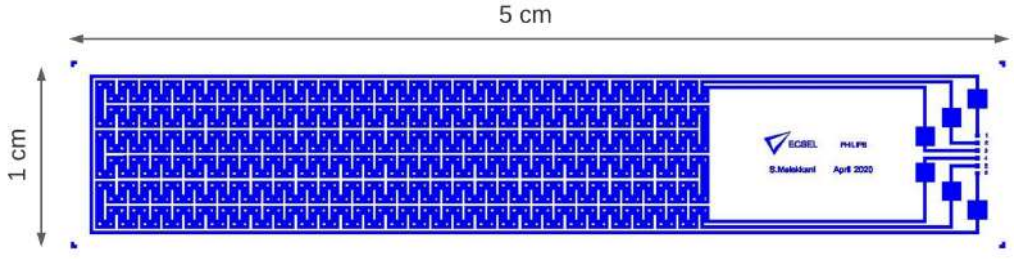

Figure 3.3: A schematic of a meandered IDE sample with 5 cm length and 1 cm width

The inner tracks are designed to have combs of 20×110 μm^2 and there is a spacing of 20 μm between the combs of the two tracks (Fig. 3.4).

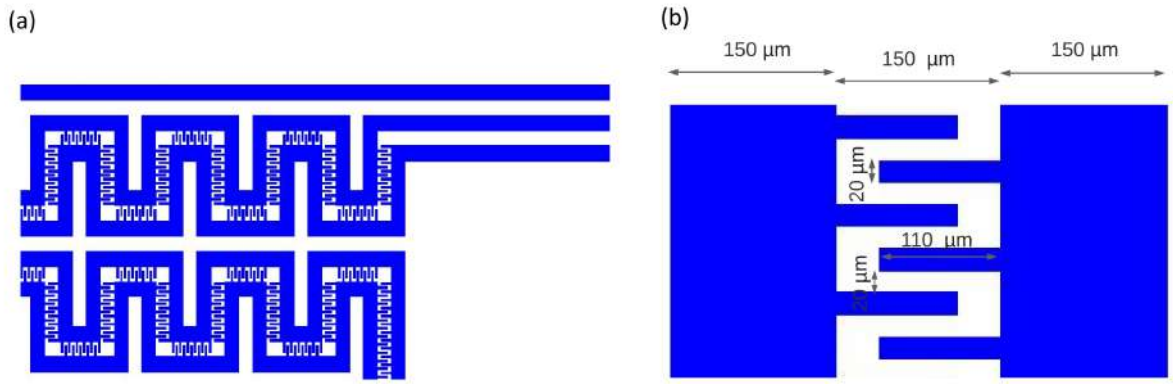

Figure 3.4: A schematic of a meandered IDE sample (a) the meander and tracks (b) a magnification of the combs with the spacing and width dimensions

Interface samples

In order to determine the water absorption path, samples with the structure as shown in Fig. 3.5 are designed. Three identical triple-track structures with 100 μm width and spacing are located on a 1×5 cm^2 chip (Fig. 3.5). The polyimide in the central part of each triple-track structure is etched down to the silicon dioxide layer. The resulting gap width of the triple-track structures varies from 460 μm for the upper structure to 300 μm for the middle structure and 100 μm for the lower triple-track as shown in Fig. 3.6. The gap width determines the distance of the gap to the tracks. As a result, for the upper triple-track structure the gap is 20 μm distance from the tracks and for the middle and bottom triple-tracks 100 μm and 200 μm respectively.

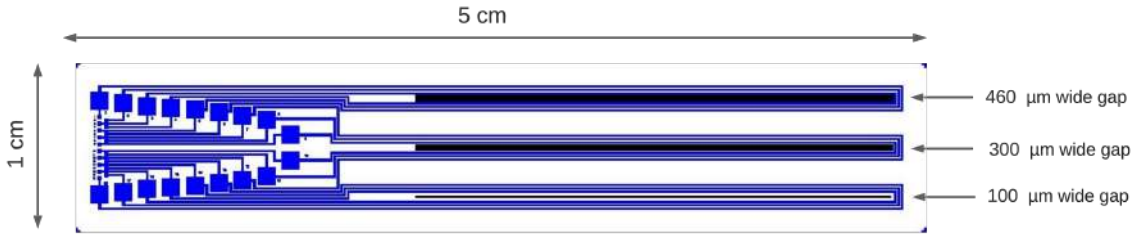

Figure 3.5: A schematic of an interface sample with three variations of gap size

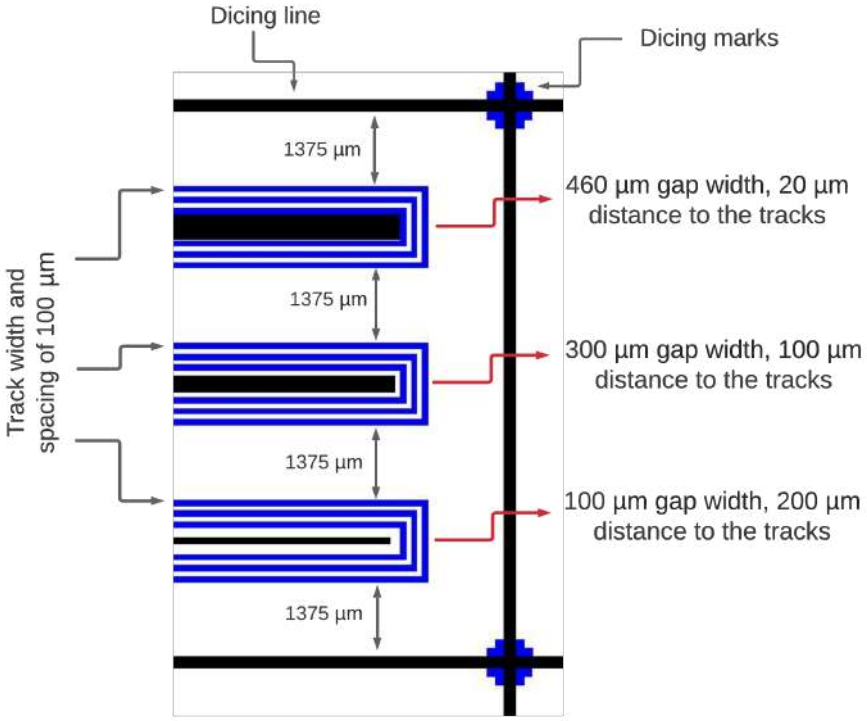

Figure 3.6: A schematic of an interface sample with higher magnification and the corresponding dimensions

Provided that the water intake happens through the interface of the layers, faster corrosion is expected in the upper tracks with a larger gap and less distance of tracks to the edge of the gap. However, if no significant difference is observed between the

three structures, water absorption from the bulk of the material (thorough the bulk of the polyimide in the vertical direction) would be a better representation of the water intake mechanism. The water intake paths are shown in Fig. 3.7.

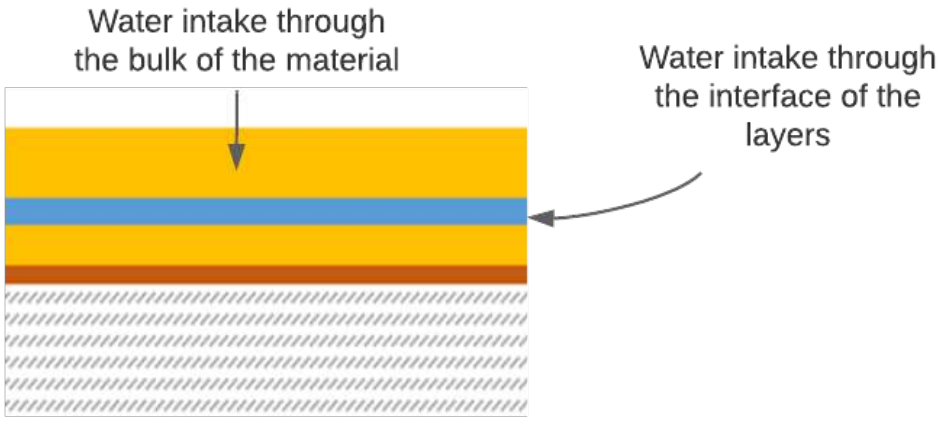

Figure 3.7: The water intake paths

3.1.3. Mask design

The photo-lithography and fabrication steps will be discussed in Section 3.1.4, however, the design of the lithography masks used in the project is presented in this section.

Photo-lithography masks of soda-lime (SL) glass are designed using the CleWin layout editor and ordered to create the test structures presented in the previous section. The dark areas on the masks are chromium which blocks the light. The aluminum-copper patterning mask contains the interconnect and contact pad structures as shown in Fig. 3.8. Provided that a positive photo-resist material is used, the white areas in the masks are etched away.

On the PI etch mask only the contact pads, dicing lines, and the gaps of the interface samples are not chromium. The PI etch mask is shown in Fig. 3.9. The dicing lines ($\approx$ 200 μm width) are not visible in this magnification of the design.

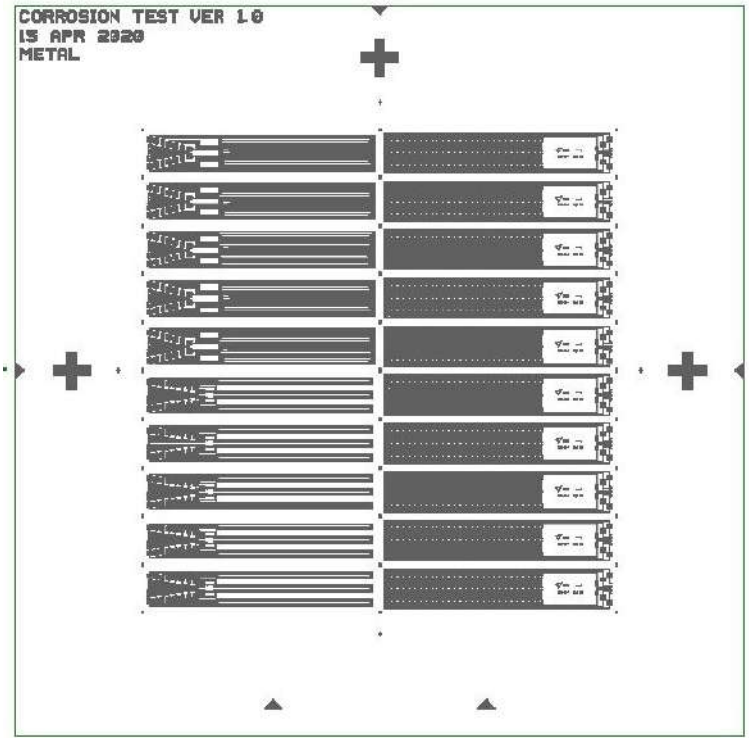

Figure 3.8: A schematic of the aluminum-copper patterning photo-mask

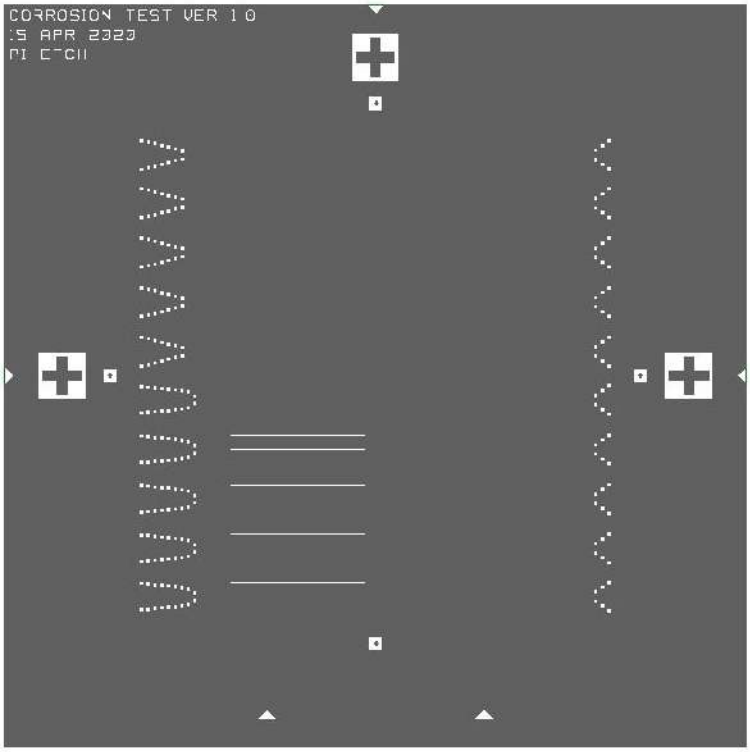

Figure 3.9: A schematic of the PI etching photo-mask

3.1.4. Cleanroom fabrication process

The samples are fabricated in the cleanroom of Philips Research in Eindhoven. The sample fabrication uses single-sided polished 6-inch silicon wafers (675 μm thickness). First, a 500 nm low-stress SiO_2 is deposited on the wafers in order to increase the polyimide adhesion. Figure 3.10 is a depiction of the fabrication process steps for the samples with the ceramic SiC and SiO_2 layers. For the samples without the ceramic layers, the SiC and SiO_2 deposition steps are skipped. In the next sections, each step is explained in detail. The complete cleanroom flowchart is provided in Appendix B.

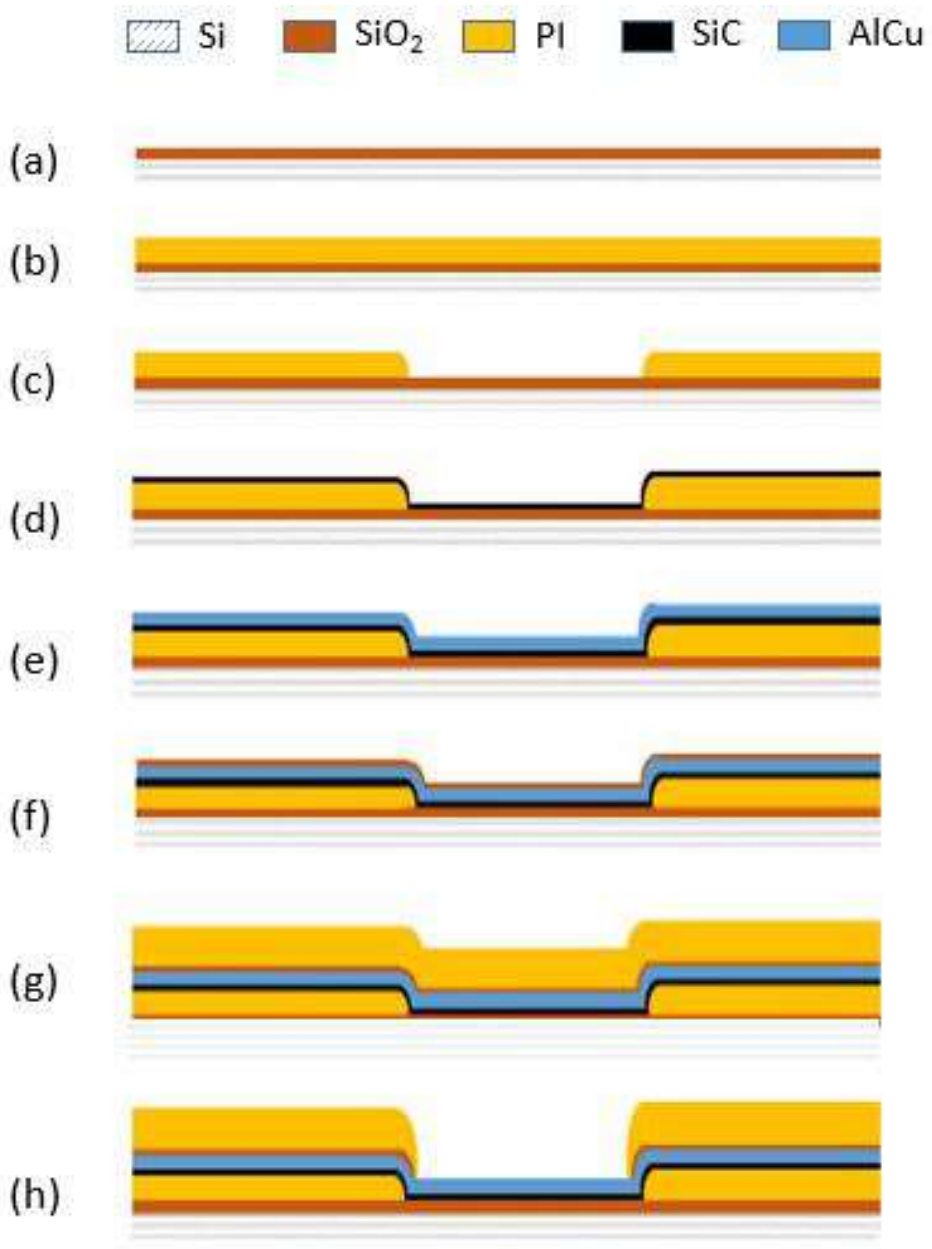

Figure 3.10: Fabrication process, (a) deposition of low-stress PECVD SiO_2 on Si wafer (b) spin coating the first layer of PI (c) PI etching to open the contact pad (d) depositing PECVD SiC (e) sputtering AlCu (f) depositing PECVD SiO_2 (g) spin coating the second layer of PI (h) PI etching to open the contact pad

Spin-coating of the first PI layer

An O_2 plasma at 90 °C is used for two minutes to clean the wafers and to make them hydrophilic, this process is referred to as the descum process. Prior to the PI coating, a thin layer of VMX651 primer (manufacturer HD MicroSystems) is applied to the wafers. VMX651 acts as an adhesion promoter between SiO_2 and PI layers. Polyimide is a viscous polymer, as a result, the n-methyl-2-pyrrolidone (NMP) solvent is added to the polymer to reduce its viscosity and to enable spin-coating. The polyimide is spin-coated by a predefined rotation rate to achieve ~ 3 μm thickness.

Directly after the spin-coating, the wafers are placed in a vacuum for 10 minutes in order to eliminate the air bubbles. Next, the polyimide is partially placed on a hotplate of 120°C for 10 minutes to increase its viscosity, however, to form the cross-links between the polyimide chains, the wafers are placed in a nitrogen oven of 275 °C for 3 hours (Fig. 3.10.(b)). The nitrogen ambient prevents oxidation of the polyimide and reduces the particles and moisture of the air.

PI patterning

In order to create a pattern on a layer in a microfabrication process, optical lithography is used. The wafer is covered with a photo-sensitive material known as photoresist and by exposing UV light through a photomask, an image of the desired pattern is transferred to the photoresist layer similar to photography. The resist material has two variants: positive and negative. In a positive resist, the exposed regions become soluble, as a result, in a process called resist developing the soluble parts are washed away from the wafer. The negative resist behaves in the opposite way, however, in this project positive resist is used.

Through the openings in the resist the layer underneath is etched either by liquid chemicals (wet etch) or by gaseous mixtures (dry etch), resulting in the engraving of the desired pattern in the layer of interest. In a wet etch process the wafers are immersed in the liquid mixture of chemicals. Wet etch usually is an isotropic process, as a result, the material is etched at the same rate in all directions. On the other hand, a dry etch process utilizes reactive ionized species and usually has a lower selectivity in comparison to the wet etch [37].

For polyimide patterning, 3900 nm of AZ4533 photoresist is applied on the cured PI layer and pattered in a photo-lithography step with the PI-etch mask (Fig. 3.8.(b)). An exposure energy of 120 mJ/cm^2 is chosen to pattern the resist layer. Next, the wafers are dry-etched in a pure O_2-plasma for 4 minutes and 40 seconds to open the dicing lines, contact pads, and the aforementioned gap areas for the interface samples. Figure 3.11 shows the contact pad openings in the first PI layer.

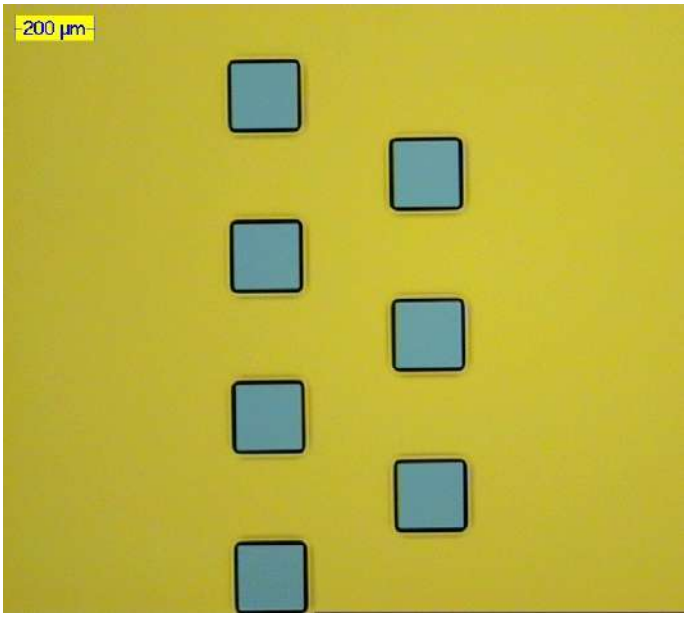

Figure 3.11: An example of contact pad openings on the first layer of PI

Following this step, inspection reveals that the PI layer thickness is decreased from 3 μm to 2 μm. Further investigation shows that the 3900 nm thickness for the photoresist is not enough and a 4900 thickness is more suitable. As a result, a roughness measurement on the surface of the polyimide is performed by a stylus surface profilometer (SSP). A surface roughness (p_a) less than 1 nm is observed for the over-etched wafers, which is in the range of a non-etched PI surface roughness (1.5 nm). As a result, it was decided to continue with the 2 μm thickness for the first layer of polyimide and to not repeat the PI deposition process.

SiC deposition

Prior to the SiC deposition, the wafer is placed in a convection oven of 125 °C for 30 minutes for dehydration. Next, the surface of the polyimide is activated by a descum process (O_2-plasma). The plasma treatment activates the carbon groups of the PI which forms strong bonds with carbon in the SiC. In addition, the O_2 plasma helps to slightly roughen the surface and increase the mechanical adhesion. Chemical vapor deposition (CVD), is used for creating thin layers of material in microfabrication. For this method, precursor materials are chemically bonded to the surface of the substrates by elevating the temperature. CVD usually requires a process temperature between 500 °C to 850 °C. Such high temperatures are not compatible with PI and aluminum, as a result, a glow-discharge plasma is used to reduce the process temperature to below 400°C which is commonly referred to as the Plasma-enhanced chemical vapor deposition (PECVD) [37]. PECVD at 250 °C is used to deposit 50 nm of SiC on the wafers as shown in Fig. 3.10.(d).

Metal deposition and patterning

Sputtering is a physical vapor deposition method (PVD), and it is commonly used for metal deposition. In this method, the target material is bombarded by accelerated argon ions. The atoms of the target material are sputtered in the vacuum space and once they reach the wafer surface, they form a thin layer. Before the metal deposition, the wafer surface is slightly etched in the sputtering chamber to increase the mechanical adhesion.

In this study, a metal layer of 1 μm thickness of AlCu 1 wt% is sputter deposited (Fig. 3.10.(e)). Next, the layer is covered by 1300 nm HPR504 photoresist and patterned using the aluminum layer photo mask (Fig. 3.8.(a)) with 40 mJ/cm^2 exposure energy. A wet etch process is used to engrave the patterns. First the wafers are immersed in Triton to improve the wetting and to avoid bubble formation in the etchant solution. After soaking the wafers in Triton they are placed in 30 °C PES solution, which is a mixture of nitric acid (HNO_3), phosphoric acid (H_3PO_4), acetic acid ($C_2H_4O_2$), and water. In approximately 10 minutes the aluminum layer is patterned and the interconnects are visible as shown in Fig. 3.12.

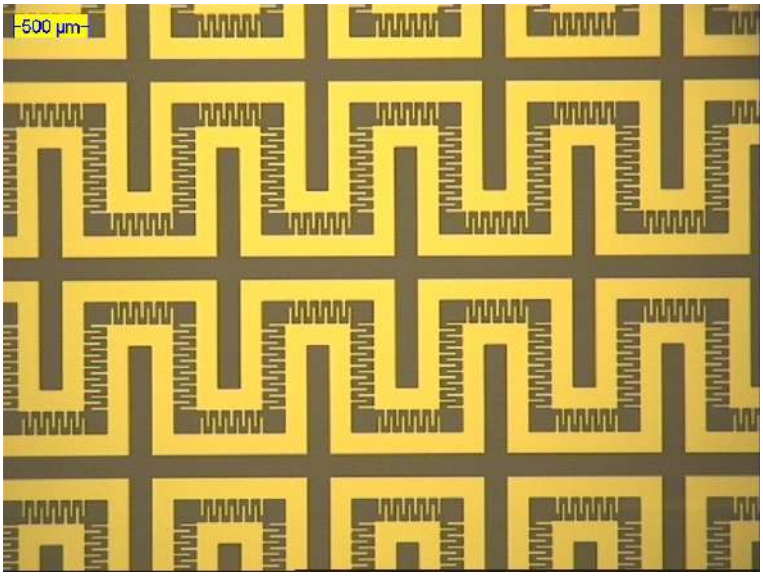

Figure 3.12: The aluminum interconnects after PES etching

SiO_2 deposition

Similar to the SiC deposition, 50 nm of SiO_2 is deposited by PECVD at 250°C (Fig. 3.10.(f)). The SiC and SiO_2 inorganic layers are expected to form strong Si-Si covalent bonds. Therefore, the aluminum interconnects are encapsulated between two thin layers of SiC and SiO_2.

Second layer of PI

The steps mentioned for the first layer of PI are applicable for the second layer of PI too. Similar to the first layer of PI, the VMX651 primer is used as an adhesion promoter because the surface of the wafers at this stage is SiO_2. After curing the second layer of PI (Fig. 3.10.(g)), AZ4533 photoresist is applied. This time the thickness is increased to 4900 nm to avoid the loss of all resistance during the PI etch. The PI layer is etched in a pure O_2-plasma for 4 minutes and 40 seconds and 3 μm thick PI layer is obtained.

The wafers are checked by a NanoSpec tool which is able to detect the SiO_2 layer by the means of reflectometry. Detection of SiO_2 layer on the dicing lines of the devices is an indication of successful PI etching. Therefore, it was confirmed that the polyimide is etched on the dicing lines, contact pads, and the gaps of interface samples. However, the contact pads in this stage are covered with a SiO_2 layer. In order to open the contact pads, a dry etch step of 30 seconds with sulfur hexafluoride (SF_6) and helium (He) plasma mixture is performed (Fig. 3.10 .(h)).

Following the fabrication process, the wafers are diced with a blade thickness smaller than the dicing line width (200 μm), and they are taken out of the cleanroom for testing.

3.2. Measurement methods

The samples are evaluated by scanning electron microscope (SEM) images, leakage current measurements, and electrochemical impedance spectroscopy (EIS) technique.

3.2.1. SEM sample preparation

The IDE samples are imaged with the JSM-7610FPlus system in the cleanroom of Philips Research in Eindhoven. Three samples (two dry samples and one corroded sample) are cleaved at relevant positions to obtain cross-sections for SEM imaging as shown in the Fig. 3.13

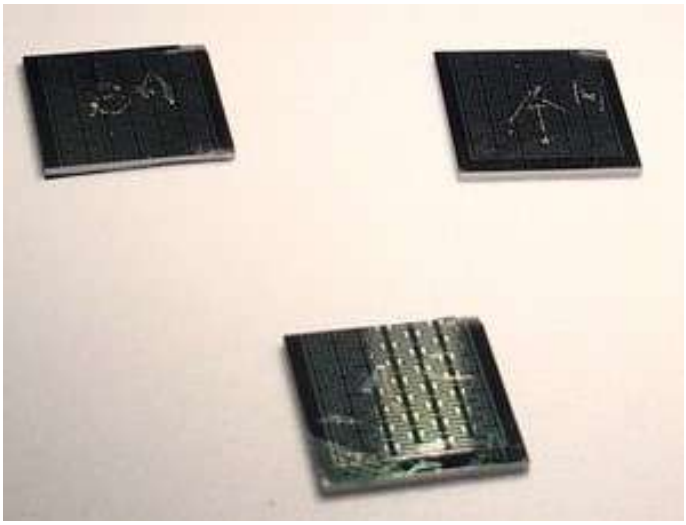

Figure 3.13: Samples prepared for SEM imaging of the cross-section

3.2.2. Leakage current and four-probe resistance measurements

In this section, the assembly of the samples, and the design of the aging and life testing apparatus (ALTA) for leakage current measurements are described. The test set-up overview is illustrated in Fig. 3.14.

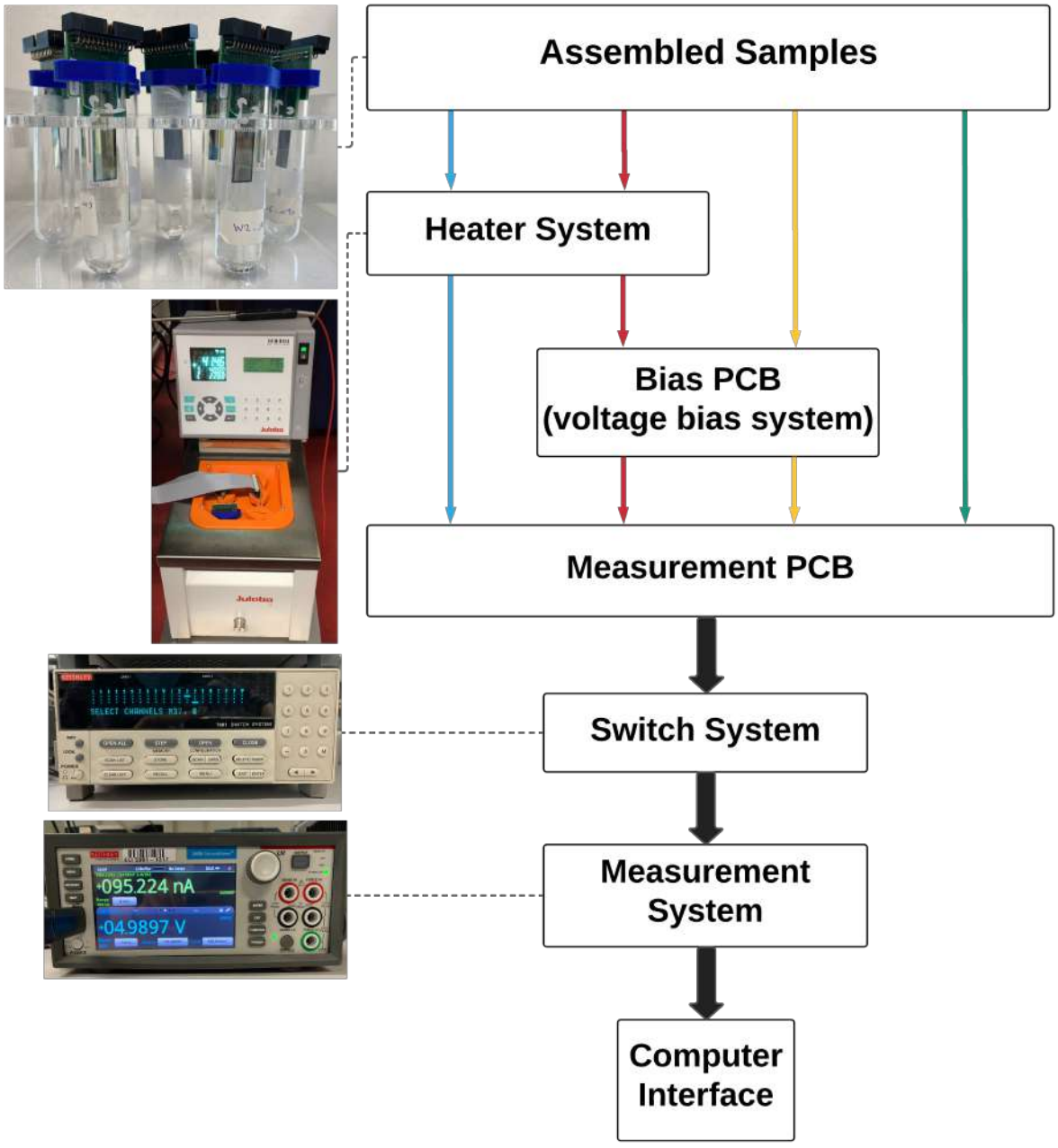

Figure 3.14: The leakage current test set-up overview

The experiment categories

Samples are soaked in phosphate-buffered saline (PBS) solution and tested in four categories as described below, each category is indicated with different arrow color in Fig. 3.14.

1. Samples soaked in PBS solution at room temperature (22 °C) (green arrow);
2. Samples soaked in PBS solution at 40 °C (blue arrow);
3. Samples soaked in PBS with 5 DC voltage bias at room temperature (22 °C) (yellow arrow);
4. Samples soaked in PBS with 5 DC voltage bias at 40 °C (red arrow).

Sterile-filtered 1X PBS solution manufactured by Alfa Aesar is used in this experiment. PBS solution (8 g/L of NaCl, 0.2 g/L KCl, 1.42 g/L Na_2HPO_4, and 0.24 g/L KH_2PO_4) with 7.4 pH is a good representation of bodily fluids and is widely used in biological research.

3.2.3. Sample assembly and integration

Following the dicing of the wafers, the samples are available to be tested. Next, the chips are inspected by an optical microscope, and the samples with the least handling damage and scratches are selected for testing. An interconnecting printed circuit board (PCB) is designed in order to hold the chip and to connect it to a connector. Figure 3.15 shows a sample mounted on an interconnecting PCB.

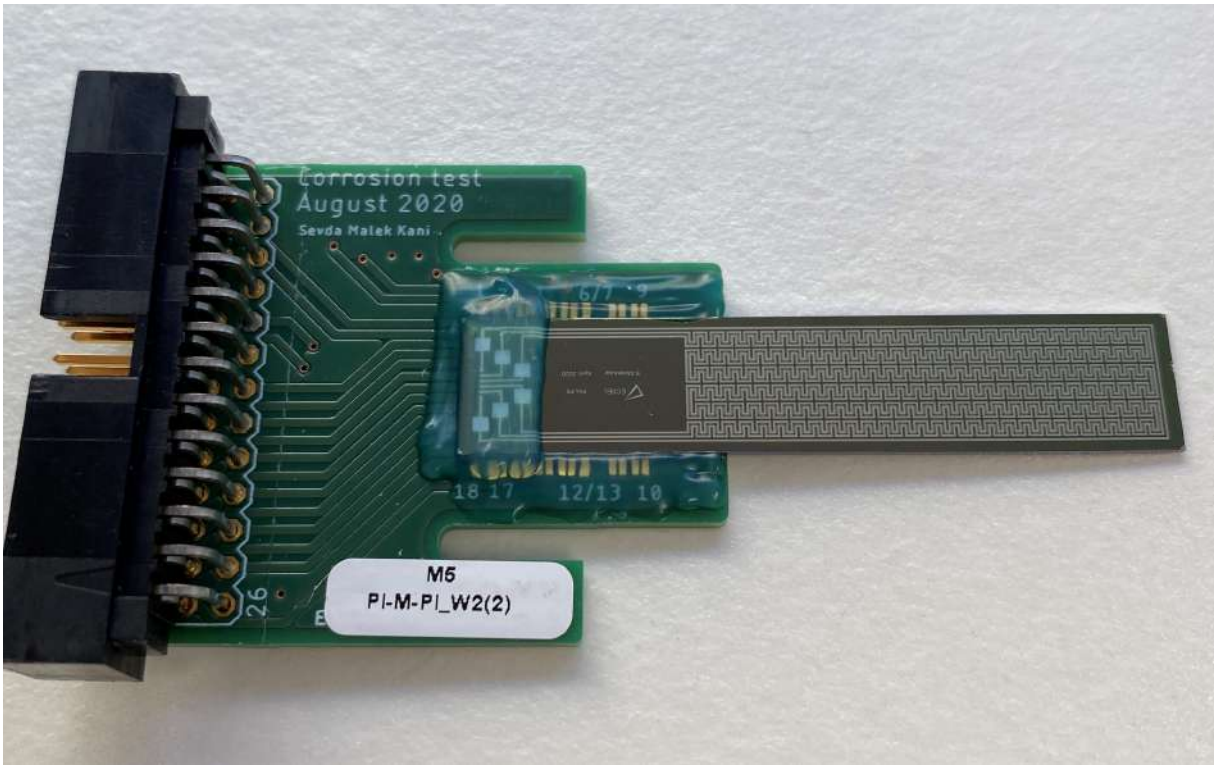

Figure 3.15: A picture of a meandered IDE sample mounted on the interconnecting PCB

The surface of the interconnecting PCB is covered with a thin layer of Parylene-C in order to make it waterproof. The chips are glued on the PCBs by EpoTek 301-1 and ultrasonically wire-bonded to the PCB contact pads. Following the wire-bonding, the contact pad areas are covered with Masterbond epoxy to secure them from moisture. The assembly is performed at the Green House micro-assembly center of Philips.

The ordered wire-bonding maps for meandered IDE and interface samples are shown in Figs. 3.16 and 3.17. To eliminate the contact resistance during the resistance measurements, a four-probe measurement is required. As a result, each contact pad on the chip has two connection points. In other words, two wires are bonded to each contact pad of the sample. Finally, as each track on the sample has two contact pads and each contact pad is connected to two pads on the PCB, four connections become available for a four-probe measurement of each metal track.

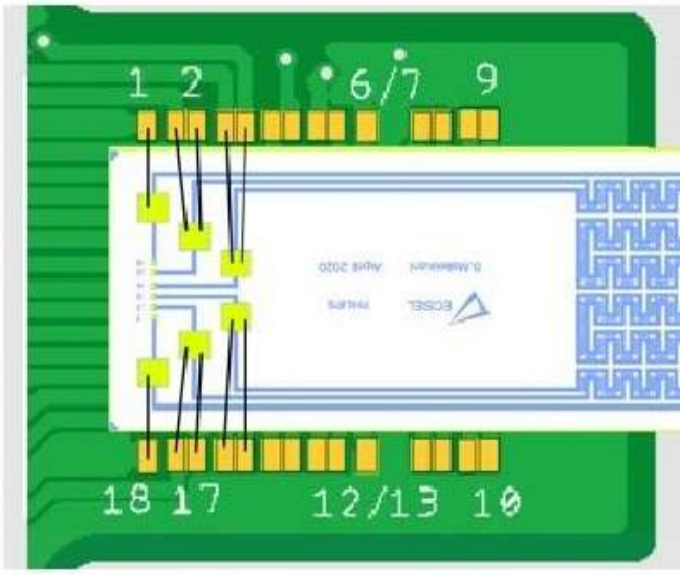

Figure 3.16: The wire-bonding map for the meandered IDE sample

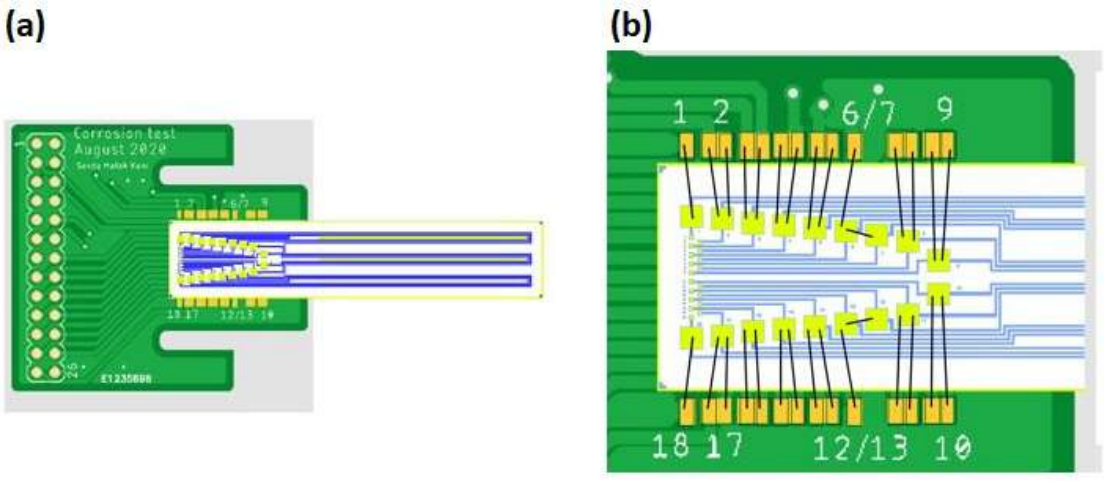

Figure 3.17: A schematic of (a) interface sample mounted on a PCB (b) the wire-bonding map for the interface sample

3.2.4. The ALTA

An overview of the aging and lifetime estimation set-up is shown in Fig. 3.18. Each part is individually explained in the following sections.

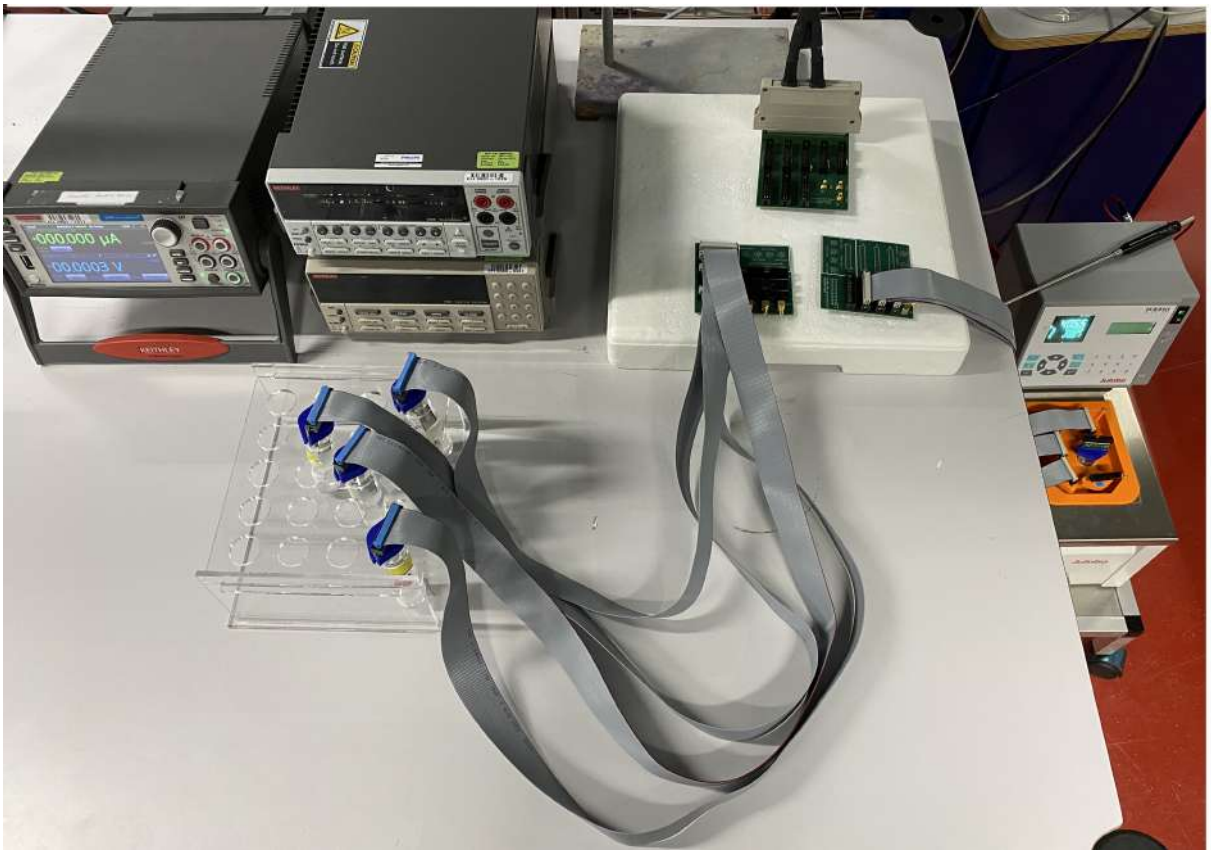

Figure 3.18: The overview of the ATLA set-up

Sample holders

Samples are placed in vials of 30 ml filled with phosphate-buffered saline (PBS). The shape of the interconnecting PCB supports the sample on the vial with the test structure immersed in the PBS solution and the contact pad area above the solution. A cap is designed and 3D printed (with a poly-lactic acid (PLA) material) to fix the PCB on the vial as shown in Figs. 3.19 and 3.20.

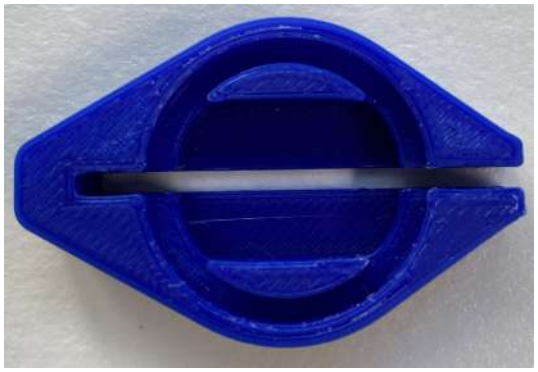

Figure 3.19: The 3D printed cap for supporting the interconnecting PCBs on the vials

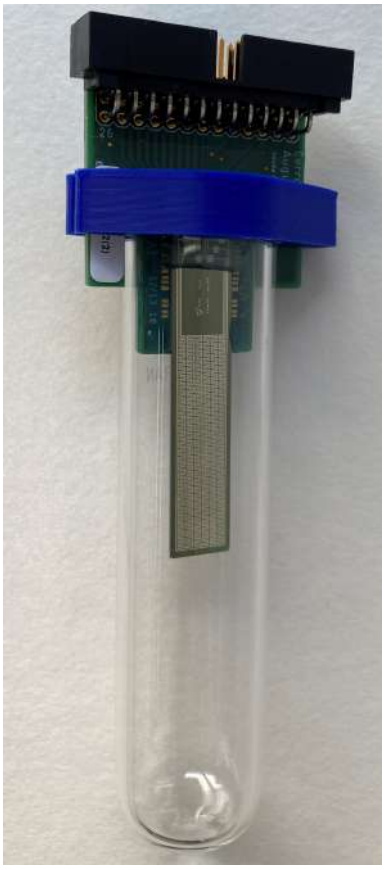

Figure 3.20: A sample mounted on the interconnecting PCB supported on the vial and fixed by the designed cap

Leakage current (LC) and four-point resistance measurements

In order to measure the leakage current (LC) of the samples, a source meter with femtoampere sensitivity (Keithley 2450) is chosen and programmed by a test script builder (TSB). Due to the large number of samples, a high-density switch system (Keithley 7001) is used to switch between the various samples by manual programming of the switch system. Both instruments are shown in Fig. 3.21. Additionally, the same instruments can be used to measure the electrical resistance of the tracks. The source meter is capable of four-terminal resistance measurement when provided with four contacts to the samples. With the aid of the switch system, the required four connections are established.

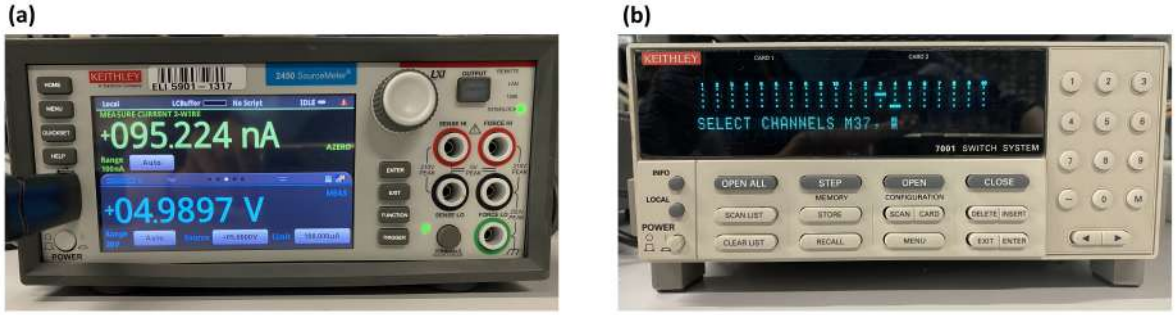

Figure 3.21: Pictures of (a) Keithley 2450 sourcemeter for leakage current measurement (b) Keithley 7001 multichannel switch system

The leakage current measurements are performed in two ways of continuous and daily measurements. When a detailed examination is required for a sample, such as during the starting phase of an experiment, continuous measurement is performed. In a continuous measurement, the device is constantly under 5V DC bias and at the same time, the leakage current data is recorded every 10 seconds.

Once the early stage of measurement is analyzed, the continuous measurement is switched to daily measurements. In the daily measurements, the samples are connected to 5V DC constantly, however, the leakage current data is not recorded. When a measurement is required (usually daily) the samples are disconnected from the bias to measure the leakage currents. In total, preparing the connections and the measurement process for all of the samples in combination takes approximately 45 minutes. The daily leakage current measurements are obtained by interrupting the constant bias or heating of the samples at specific times of the day to record their leakage current at 5V DC for 2 minutes. The daily recordings are performed to reduce unnecessary large data acquisition due to the fact that usually changes in the samples occur over a long time span. However, since access to the laboratory during weekends is not permitted, the data of Saturdays and Sundays are not available in the daily measurements.

Bias and measurement PCBs

The connection between the samples and the switch system is established by a custom-designed PCB as shown in Fig. 3.22.(a). The PCB used for biasing the samples is shown in Fig. 3.22.(b). The detailed schematic of the PCBs is given in Appendix. C.

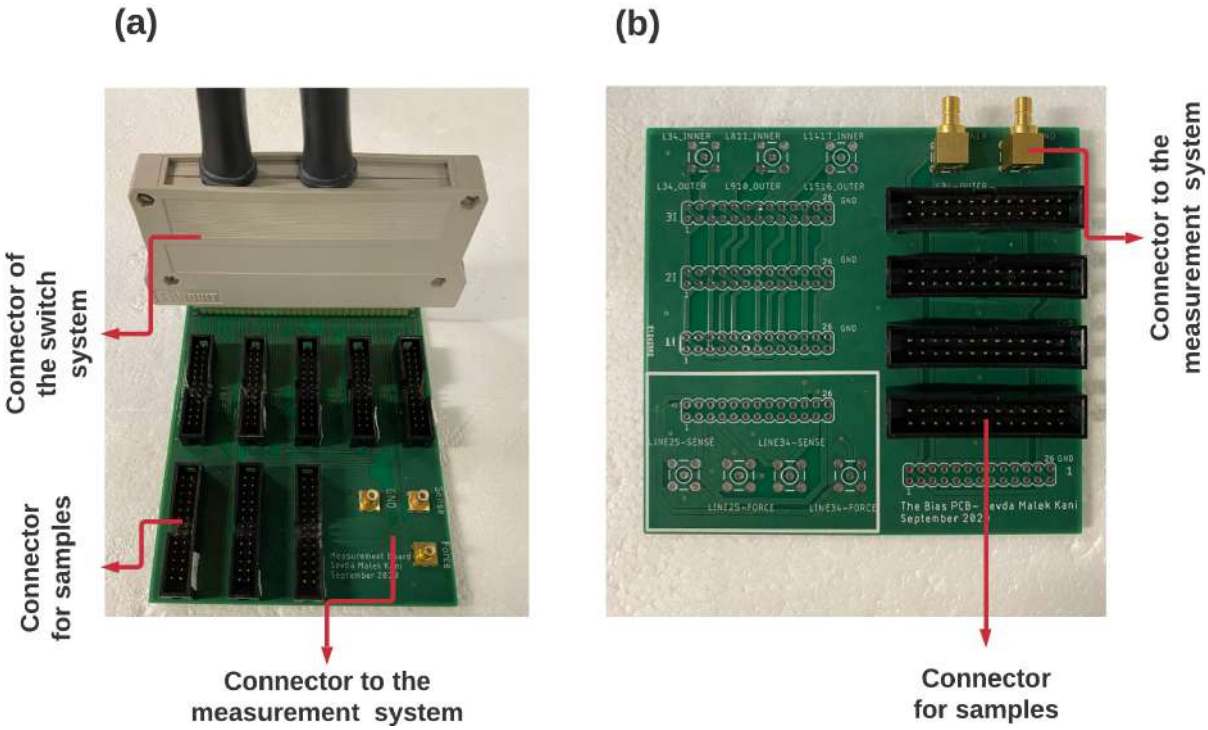

Figure 3.22: Pictures of (a) the PCB used for connecting to the switch system (b) the PCB used for biasing the samples

Elevated temperature system

The elevated temperature (40 °C) is achieved by utilizing a heating circulator (Julabo model HL). The original lid of the water bath is replaced by a 3D printed PLA lid. The 3D printed lid is specifically designed to hold the sample vials in an immersed position in the water bath. Figure 3.23 depicts the heater and the designed lid. The system is equipped with a temperature sensor to measure the temperature of the solution inside the vials. At the beginning of the experiments, the temperature of the PBS solution inside one control vial is checked to confirm that the temperature has reached 40 °C.

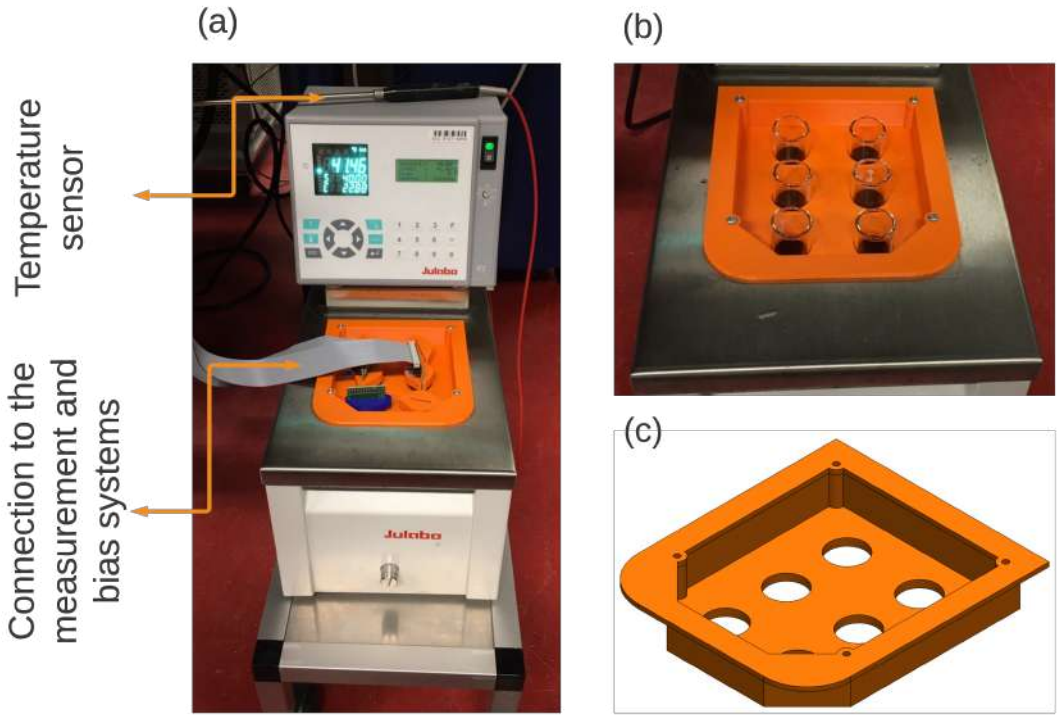

Figure 3.23: The elevated temperature set-up(a) the heating circulator containing samples connected to measurement and bias systems (b) the designed lid for holding the samples (c) 3D model of the lid

3.2.5. Electrochemical impedance spectroscopy (EIS) measurement

EIS is performed to evaluate the encapsulation performance more in-depth. The Solartron Analytical Modulab XM® system of Salvia BioElectronics, Eindhoven [1] is utilized in this study. The Solartron system was originally developed by University College London (UCL) for the evaluation of polymer encapsulated implants, and subsequently adapted by Salvia for the evaluation of their polymer encapsulated implant designed to treat migraine and cluster headache [17]. The Solartron system is capable of measuring impedances in the Giga-ohm range. In this experiment frequencies ranging from 10^{-1} to 10^{5} Hz are used. The whole set-up, including the water bath for testing at elevated temperatures, is enclosed in a Faraday cage to shield the set-up from noise. The outer and inner tracks of the meandered IDE samples are connected to the working electrode (WE) and the counter electrode (CE) respectively.

[1] https://www.salvianeuro.com/

4

Results

The results of the microfabrication process and the lifetime evaluation experiments are presented in this section.

4.1. Sample fabrication

A fabricated wafer before dicing is shown in Fig. 4.1.

Figure 4.1: An image of one wafer

Final checks to validate the wafers

By checking the resistance of the tracks with needle probes, the correct opening of the contact pads is confirmed. In addition, SSD (Surface step height) measurements are performed on the wafers to confirm that the final thicknesses of different structures match the expected values. Figure 4.2 illustrates the step height measurement for one wafer without ceramic layers, performed in the dicing line area. The x-axis shows the measured length on the wafer surface in mm, and the y-axis is the step height in nm. The measured height is ≈ 5 μm and it is calculated as the delta between the average of the red highlighted R-area (surface of the second PI layer) and green M-area (empty gap of dicing line). For this sample at the edge of the chip 5 μm thickness was expected as a combination of the 2 and 3 μm PI layers near the dicing line of the sample.

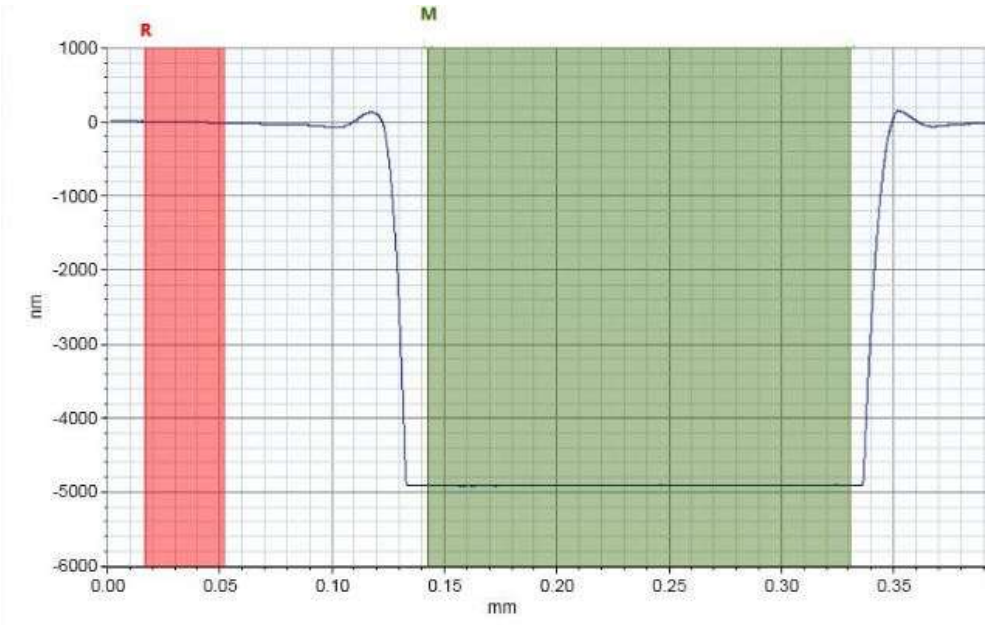

Figure 4.2: Step height measurement performed on the dicing line area. A step height of ≈ 5 μm is measured for this sample. The x-axis shows the measured length on the wafer surface and the y-axis the step height. The measured height is calculated as the delta between the average of the red highlighted R-area (surface of the wafer) and green M-area (empty gap of a dicing line)

4.1.1. SEM images

SEM cross-section images of the samples with ceramic layers and without ceramic layers prior to the experiments are shown in Figs. 4.3 and 4.4. Artifacts are seen in SEM images due to the charging of the polyimide since it is an organic material.

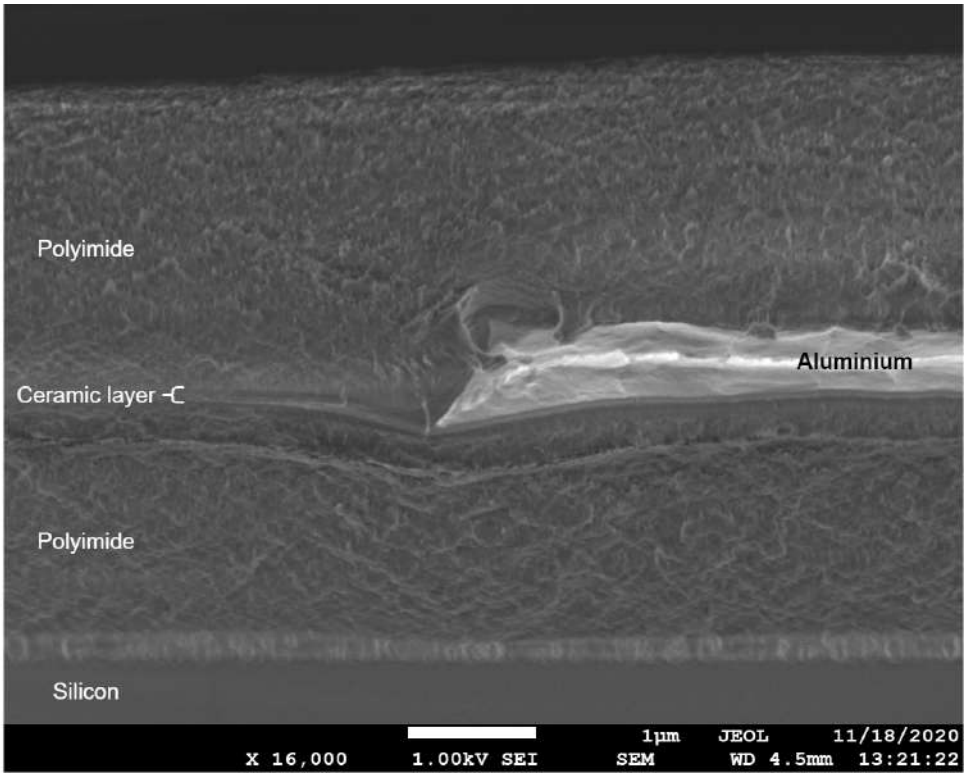

Figure 4.3: SEM cross-section image of a sample with ceramic layers

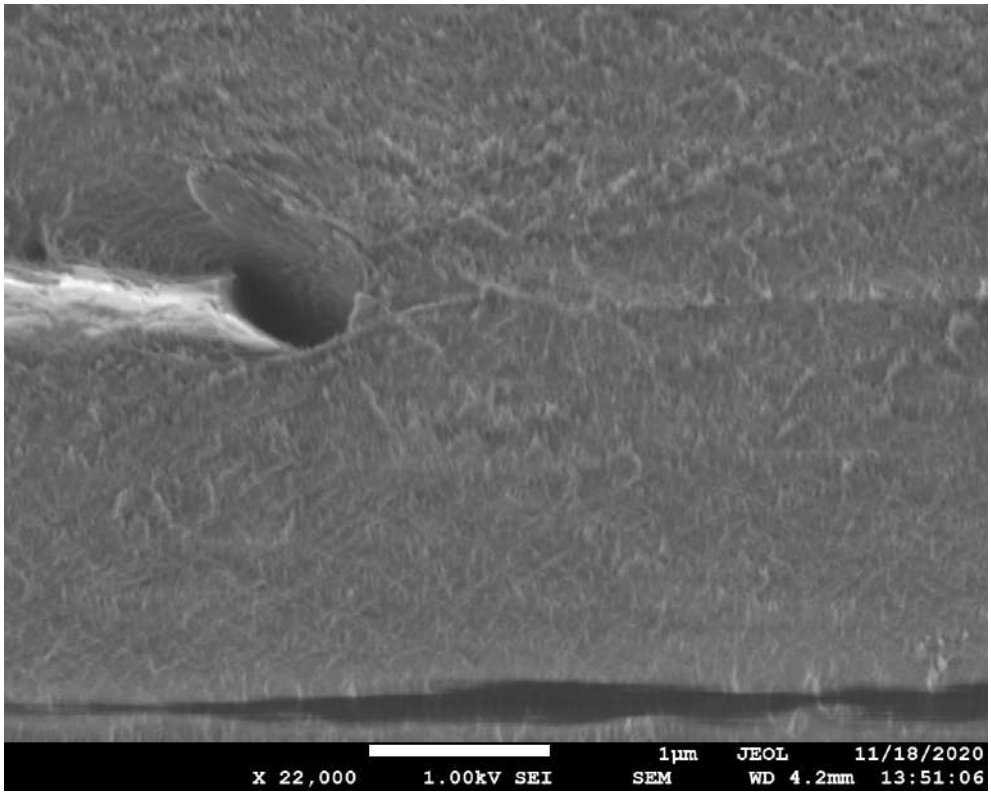

Figure 4.4: SEM cross-section image of a sample without ceramic layers, some artifacts are seen in the bottom layer of the sample due to the polyimide charging

4.1.2. Defective samples

After dicing, all the samples are inspected by an optical microscope to identify defects. Scratches, mouse bites, and disconnected combs are the most common forms of defects. Fig. 4.5 is a depiction of some defect examples on the samples. Test devices with the least amount of defects are separated and wire-bonded for the experiments.

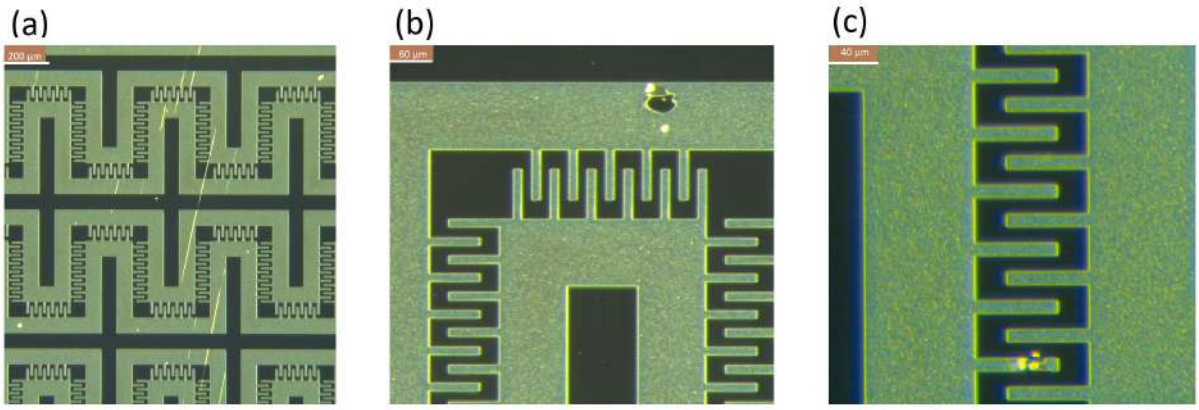

Figure 4.5: Examples of defects on the samples (a) scratches (b) mouse bite (c) deformed comb

4.2. Measurement results

The resistance of the metal tracks on the samples is measured with a four-point resistance. A value between 83 Ω and 85 Ω is observed for the meandered tracks of the samples, this measurement matches the sheet resistance calculated for the meandered tracks in the samples. The resistance measurement is used to validate the connectivity of the sample before leakage measurements. Problems such as disconnected wire-bonds and solder joints are identified through this connectivity check. In addition, as a corroded aluminum track becomes an open circuit, a high resistance in the order of MΩ is measured for corroded samples.

4.2.1. Leakage current results

The leakage current measurements of the IDE samples at 5V DC for the four aforementioned categories are presented in this section. Samples with SiC and SiO_2 layers are referred to as ceramic samples and the samples without the SiC and SiO_2 layers are referred to as non-ceramic samples. Although at the writing of this thesis the experiments are in progress, the data presented in this report represent the status until November 16, 2020. The plotted data points in the leakage current measurements are the average values over the time of the measurement (2 minutes).

The set-up used in this study (Fig. 4.6) including the instruments, PCBs, and the connectors, add an offset to the leakage current of the system. A fluctuation in the range of 0.01 nA is recorded when the system is disturbed by moving the wires or when different connectors are used. As a result, the accuracy of the measured values is limited to values higher than 0.01 nA.

Figure 4.6: The measurement set-up

A threshold of 0.1 μA (100 nA) is set to determine the failed devices. Samples with higher leakage current than the threshold are also examined by visual and optical inspection to confirm the existence of corrosion on the tracks.

Leakage current of the samples at dry condition

Prior to the soaking experiments, the leakage current of the samples is measured in the dry state. The measured LC ranges are 10 nA and 0.1nA for the ceramic and non-ceramic samples respectively. The ceramic samples show a higher leakage current than the non-ceramic samples in the dry state. This result indicates that due to an intrinsic reason the ceramic samples are more conductive.

Leakage current of the samples at room temperature without bias

Two ceramic samples and two non-ceramic samples are soaked in room temperature PBS solution. One pair of ceramic and non-ceramic samples is soaked for ~ 7 weeks and the other pair is soaked for ~ 5 weeks. In Fig. 4.7 the leakage current of all 4 samples over the soaking time is plotted. The LC values are shown on the y-axis on a logarithmic scale. It is important to emphasize the effect of the logarithmic scale on the lines in the plot. For the non-ceramic samples (blue lines) in Fig. 4.7 more fluctuations are observed, however, the fluctuations are magnified due to the logarithmic scale of the y-axis. In other words, the same fluctuations caused by the noise in the system are present for all samples, however, for ceramic samples (red lines) which are in the 10 nA range, the fluctuation is less apparent.

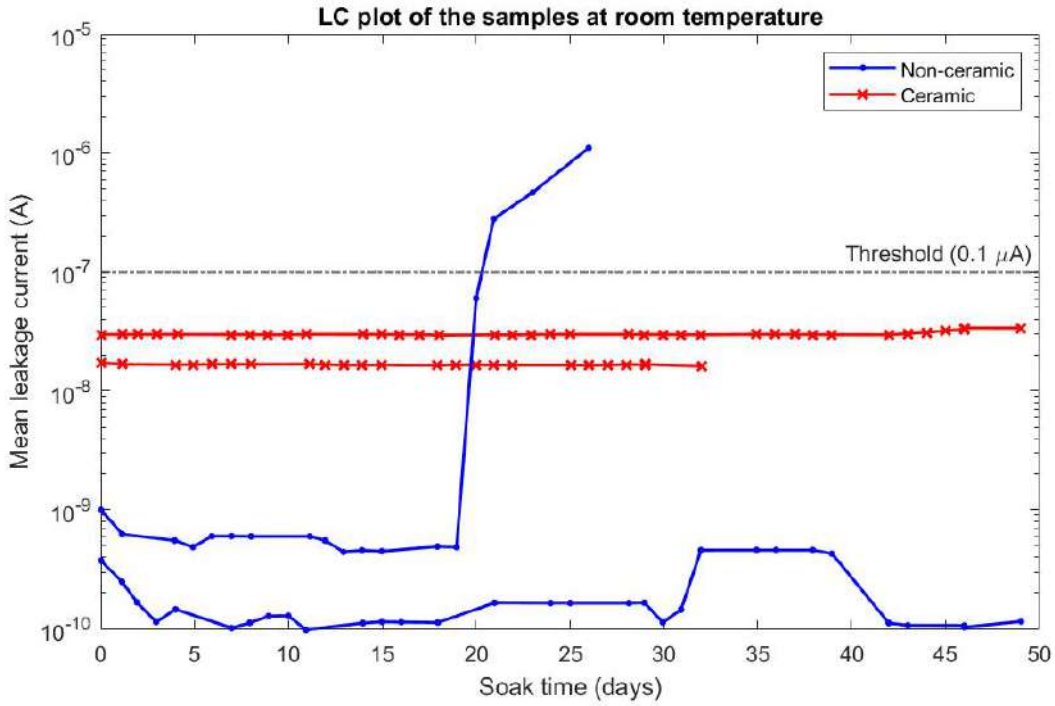

Figure 4.7: The LC plot for samples soaked at room temperature with a logarithmic scale for the current axis, the red lines representing ceramic samples and the blue lines representing the non-ceramic samples and the dashed line showing the threshold level

The non-ceramic samples (blue lines) demonstrate leakage currents lower than 1 nA. One non-ceramic sample fails on day 23 of the experiment with an LC higher than 100 nA. The corrosion of this sample is shown in Fig. 4.8.

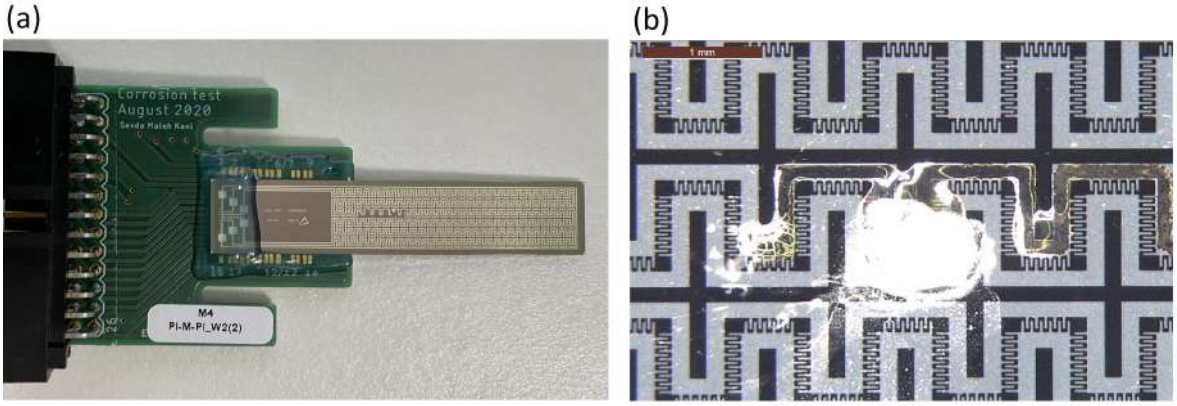

Figure 4.8: Pictures of (a) the corrosion in the non-ceramic soaked sample (b) higher magnification

In general lower LC values are measured for the non-ceramic samples during the experiments. However, the failure of one non-ceramic sample contradicts the lower leakage current values of this type. As a result, since no other failure is seen at the time of this report, it is not possible to identify the better performing samples in this experiment and more data is required.

Leakage current of the samples at 40 °C without bias

One pair of ceramic and non-ceramic samples is soaked in PBS and the vials are placed in the 40 °C water bath. The elevated temperature is expected to accelerate the corrosion exponentially (Arrhenius relation section 2.3.1). Figure 4.9 is an illustration of the leakage current plots of these samples. No failure is observed in 25 days, suggesting that the failure seen in the previous experiment is due to a defective sample. In this experiment, the LC of the ceramic sample is in the order of 80 nA and the non-ceramic sample shows a mean leakage of less than 1 nA.

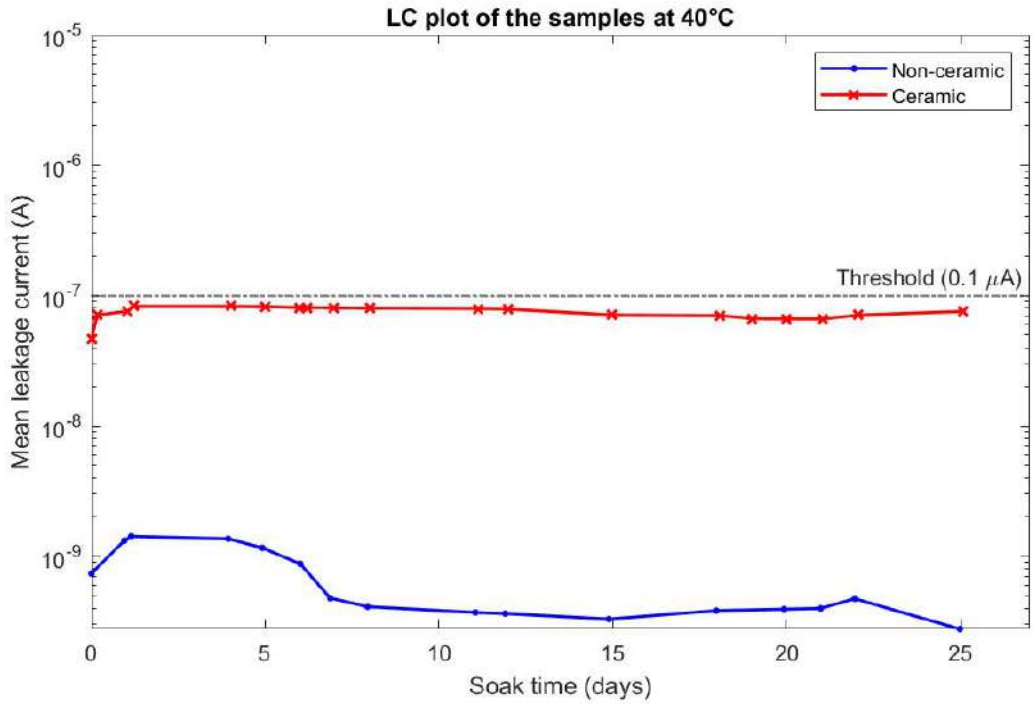

Figure 4.9: The leakage current plot for samples soaked at 40 °C with a logarithmic scale for the current axis, the red lines representing ceramic samples and the blue lines representing the non-ceramic samples and the dashed line showing the threshold level

Leakage current of the samples with 5V DC bias at room temperature

Six samples (3 ceramic and 3 non-ceramic) are connected to 5V DC and the LC plots are shown in Fig. 4.10. The experiment started with 2 samples and later increased to 4 and finally 6 samples. Thus, the samples have a varying soaking time. The non-ceramic samples demonstrate leakage currents less than 1 nA for all three samples throughout the soaking time. On the other hand, two of the ceramic samples failed on day 8 and day 9 of the soaking time.

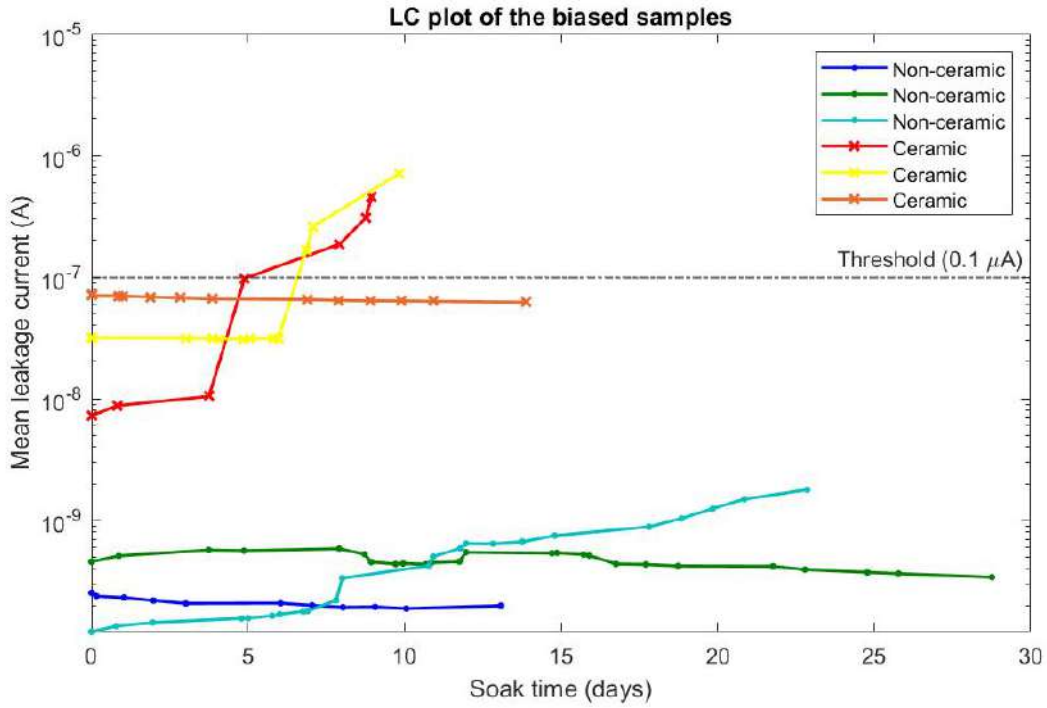

Figure 4.10: LC plot of biased samples (5V DC), with two ceramic samples passing the threshold

The failed two ceramic samples are shown in Fig. 4.11 and the corroded tracks are indicated by red circles. In addition, magnified images of corroded areas taken by microscope are shown in Fig. 4.12.

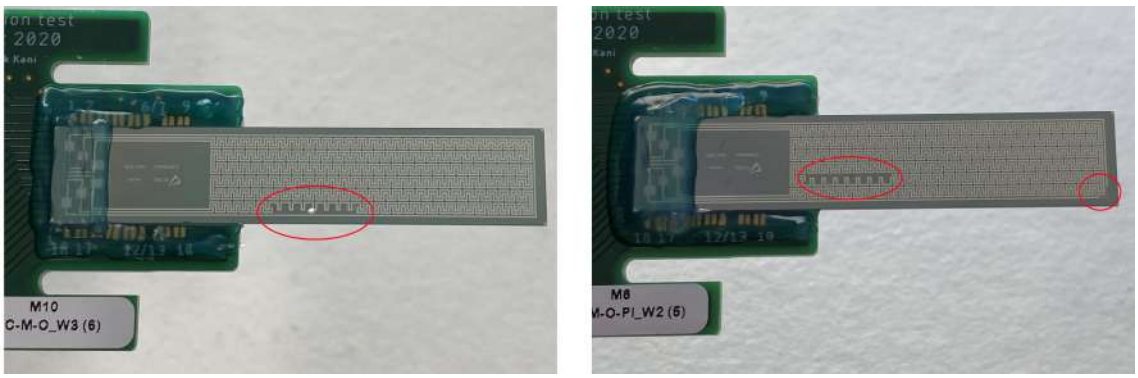

Figure 4.11: Two ceramic samples failed at day 8 and 9 under 5V DC bias, the corroded parts are indicated by red circles

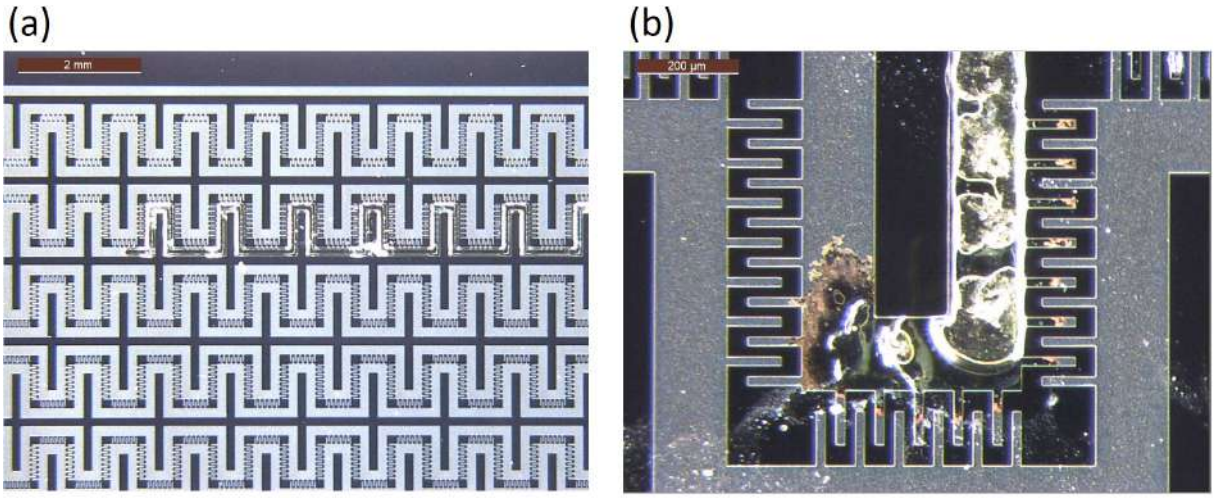

Figure 4.12: The failed bias sample (a) the corrosion area (b) higher magnification

Inspection of the corroded track shows that the corrosion propagated along the track in both directions starting from the initiation point (Figs. 4.13 and 4.14).

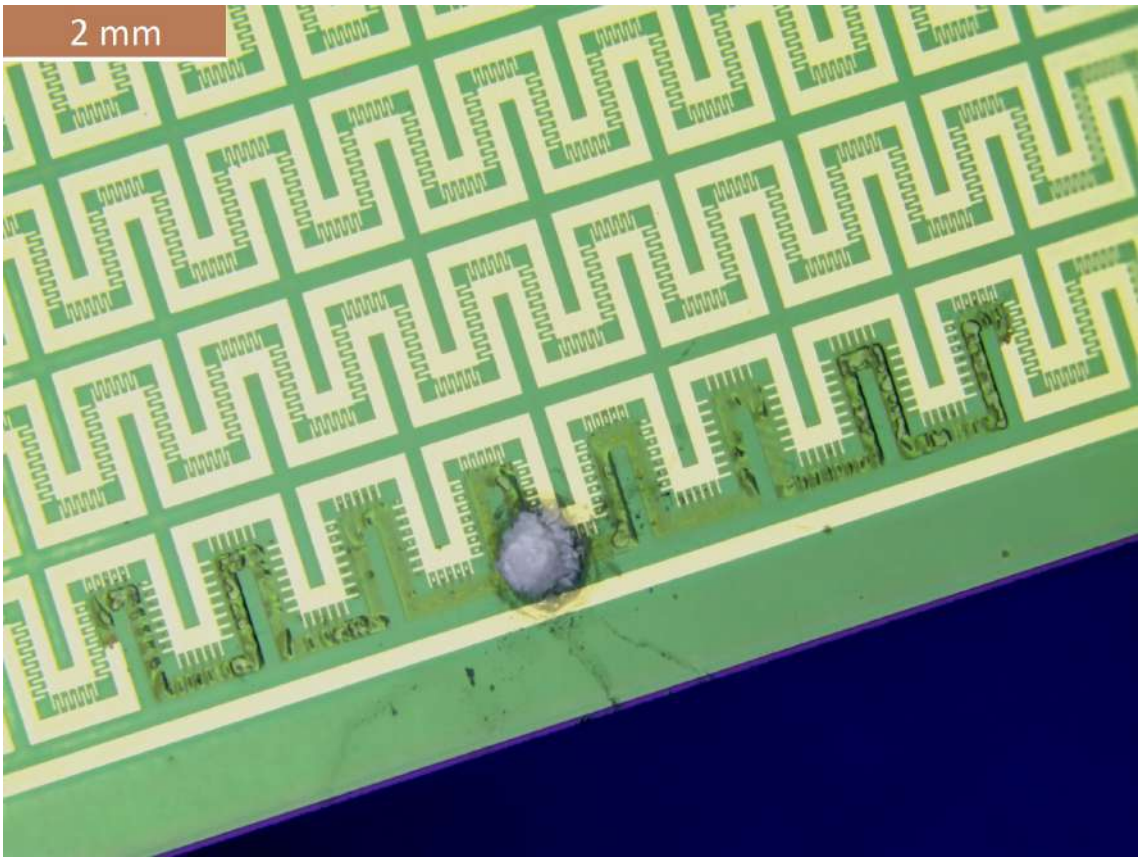

Figure 4.13: The failed bias sample with the the corrosion initiation area and the propagation along the track

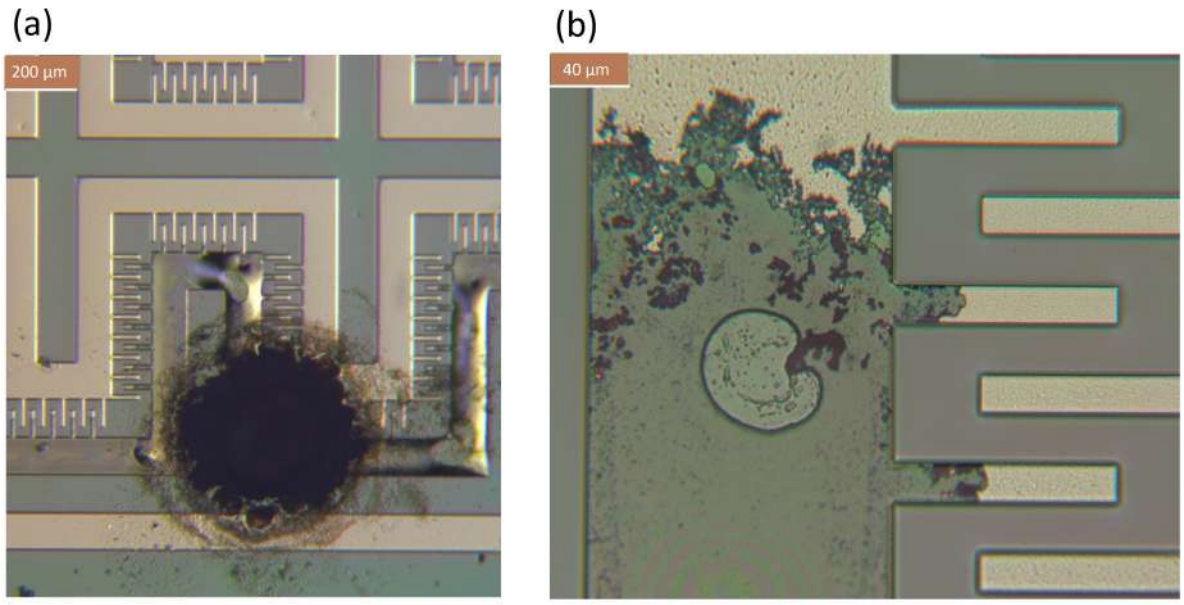

Figure 4.14: The failed bias sample (a) the corrosion initiation area (b) propagating corrosion

leakage current of the samples with 5V DC bias at 40 °C

Finally, 5 samples (3 ceramic and 2 non-ceramic) are placed in the 40 °C elevated temperature bath and connected to 5V bias simultaneously. The leakage current results are shown in Fig. 4.15. Similar to the previous experiments, two non-ceramic samples have leakage currents in the range of 1 nA. The ceramic samples have nearly 100 times larger LC values than the non-ceramic samples. Two of the ceramic samples fail on the fourth and the seventh hour of the soaking time. While the non-ceramic samples don't show degradation. However, one ceramic sample, as shown in the plot, has not corroded even after 19 days (orange line).

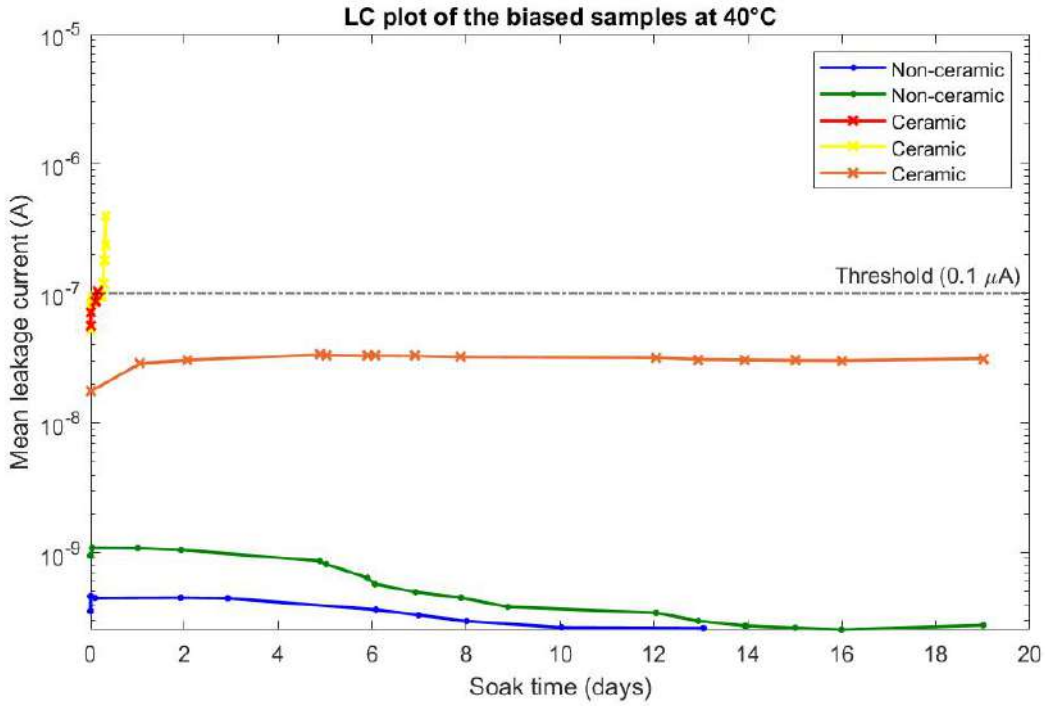

Figure 4.15: Leakage current plot of biased samples (5V DC) at 40 °C, two ceramic samples failed in the first hours of the experiment

Figure 4.16 shows the leakage current of the failed ceramic samples as a function of the soaking time in hours. For these samples, continuous measurement is performed and the mean value of the acquired data after every 30 minutes is plotted in Fig. 4.16. As shown in Fig. 4.17, multiple corroding areas are seen on these samples.

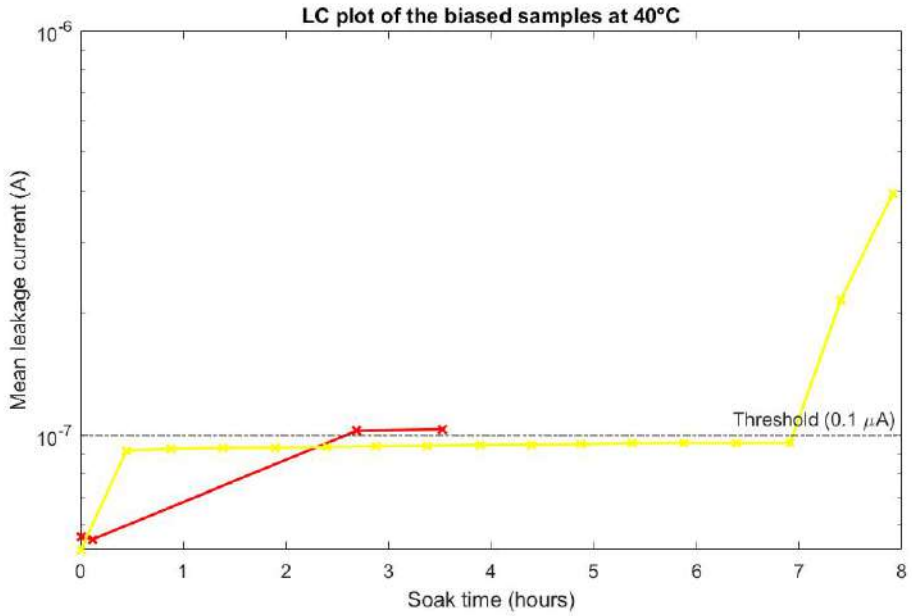

Figure 4.16: LC plot of biased samples (5V DC) at 40 °C, two ceramic samples failing in the first hours of the experiment

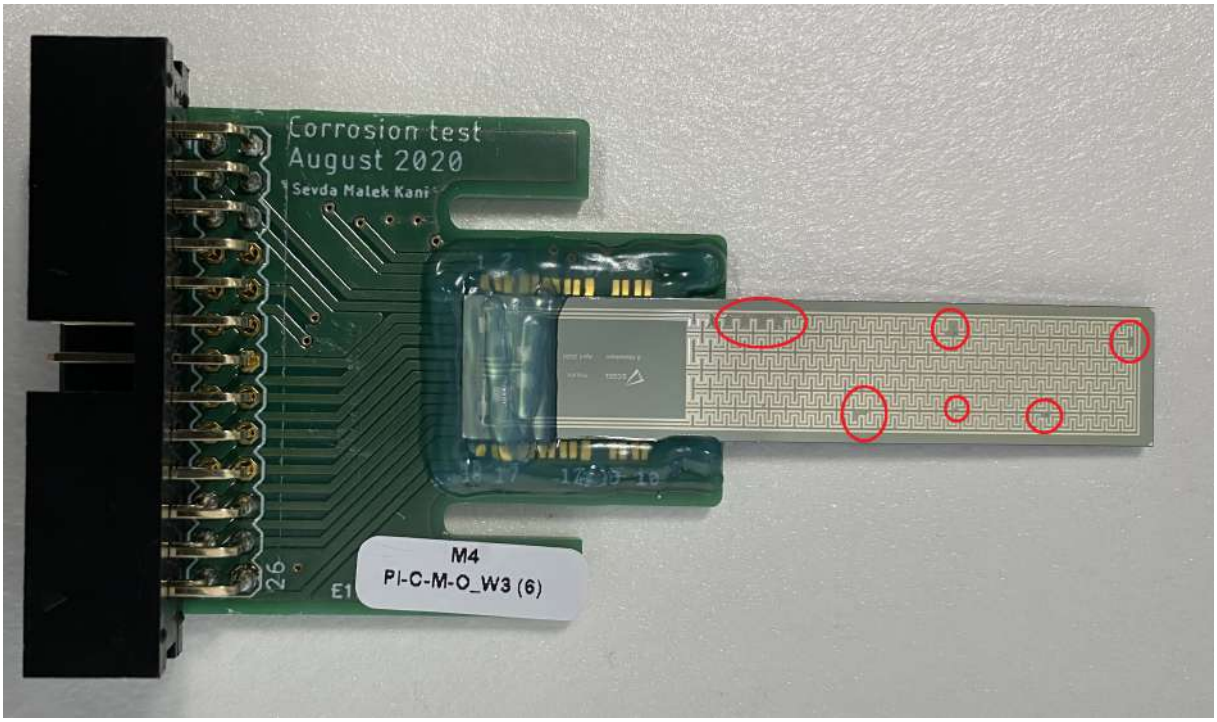

Figure 4.17: The failed biased sample (5V DC) at 40 °C, the corroded areas are indicated with red circles

The DC leakage current measurements indicate that in general, the ceramic samples have higher LC values. In addition, more ceramic samples have failed in comparison to the non-ceramic samples in different experiment categories. Two exceptions are seen in the experiments, one failed non-ceramic sample in the soaking experiment and one functional ceramic sample in the high temperature and bias conditions. Another important observation is that the ceramic samples demonstrate higher leakage currents prior to the soaking in the dry state in comparison to the non-ceramic samples. This observation indicates that the electrical properties of the ceramic layers are influencing the leakage current and the ceramic layers (especially SiC) are more conductive than anticipated.

4.2.2. SEM images of a corroded sample

Figures 4.18 and 4.19 show Cross-section of a metal track in a ceramic sample encapsulated by polyimide without corrosion and with corrosion respectively.

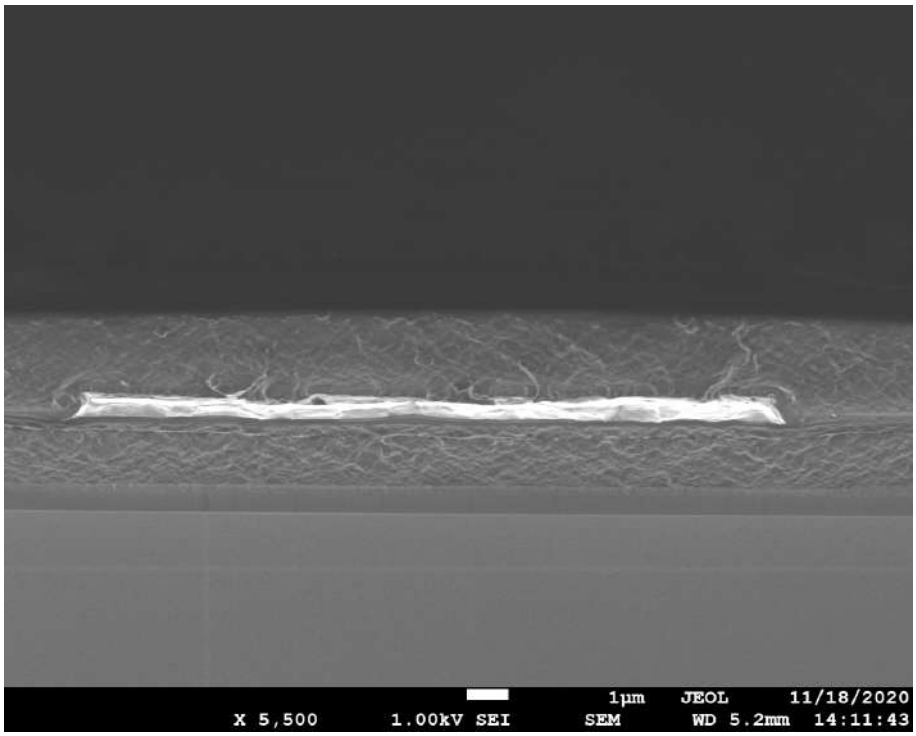

Figure 4.18: A metal track of a ceramic sample without corrosion

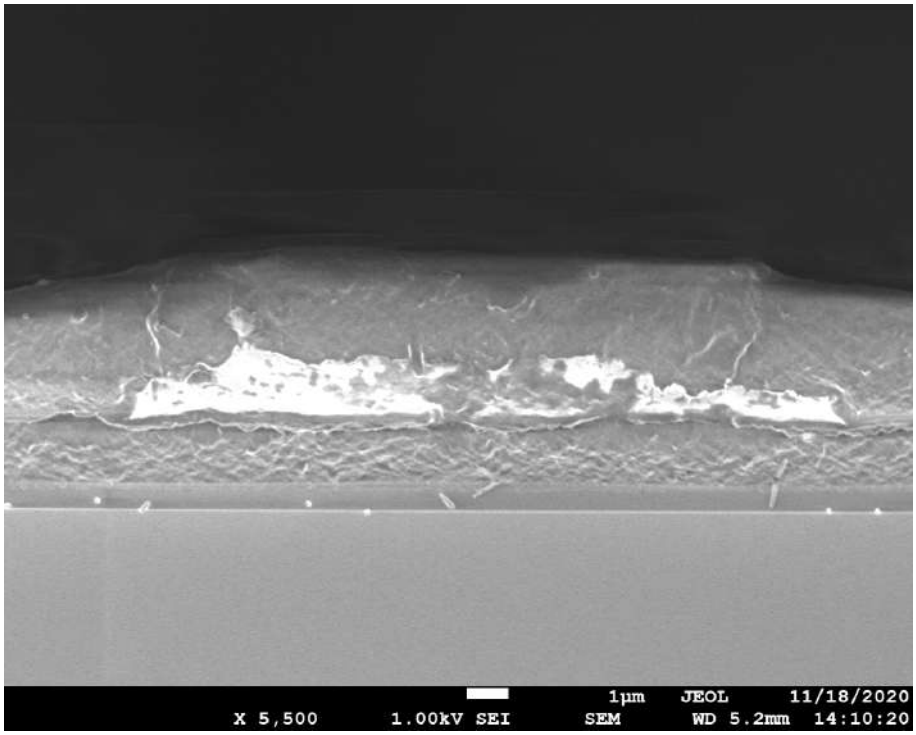

Figure 4.19: A metal track of a ceramic sample with corrosion

4.2.3. Electrochemical Impedance Spectroscopy (EIS) measurements

In this section, the same samples as tested in the LC measurements are examined by EIS, and the bode diagrams of IDE structures for the 10^{-1} to 10^{5} frequency range are shown and discussed for more in-depth analyses of the samples. In the first part, a comparison between the ceramic and non-ceramic samples in the dry, soaked, and heat-biased conditions is given. Next, a failed ceramic sample is compared to a non-failed ceramic sample that is exposed to similar conditions. A failed sample in this section is defined by having a corroded area within its structure. Additional bode diagrams from the experiments are available in Appendix. E.

Comparison between ceramic and non-ceramic samples

In Fig. 4.20 the EIS measurement of a ceramic and a non-ceramic sample in the dry state is shown. The resistance of the samples for lower frequencies matches the LC value for the DC measurements. The non-ceramic sample with -80 degrees phase at low frequencies shows a capacitive behavior. However, an irregular peak is seen for the non-ceramic sample at 100 Hz. This peak is unexpected and it is most probably due to a connection issue in the sample.

The ceramic sample shows a resistive behavior, suggesting that the SiC layer in the ceramic samples is not a complete insulator. This observation especially in the dry state highlights that the ceramic layer is more conductive than the non-ceramic sample. In addition, a constant impedance value is seen for the ceramic sample at low frequencies which is the resistance of the ceramic layer.

An EIS measurement of ceramic and non-ceramic samples soaked in PBS for 50 days is depicted in Fig. 4.21. The measurement for the samples soaked in PBS at 40 °C with 5V DC over 20 days is illustrated in Fig. 4.22. In both conditions, a behavior similar to the dry samples is observed.

Similar to the DC leakage measurements, lower impedance values (at low frequencies) are seen for the ceramic samples in the EIS measurements. Therefore, the ceramic samples are more conductive than the non-ceramic samples. However, these EIS results are not sufficient to achieve a conclusion about the adhesion and the encapsulation performances of the samples. In other words, a device can have layers with higher conductivity, but at the same time, exhibit reliable adhesion and corrosion protection.

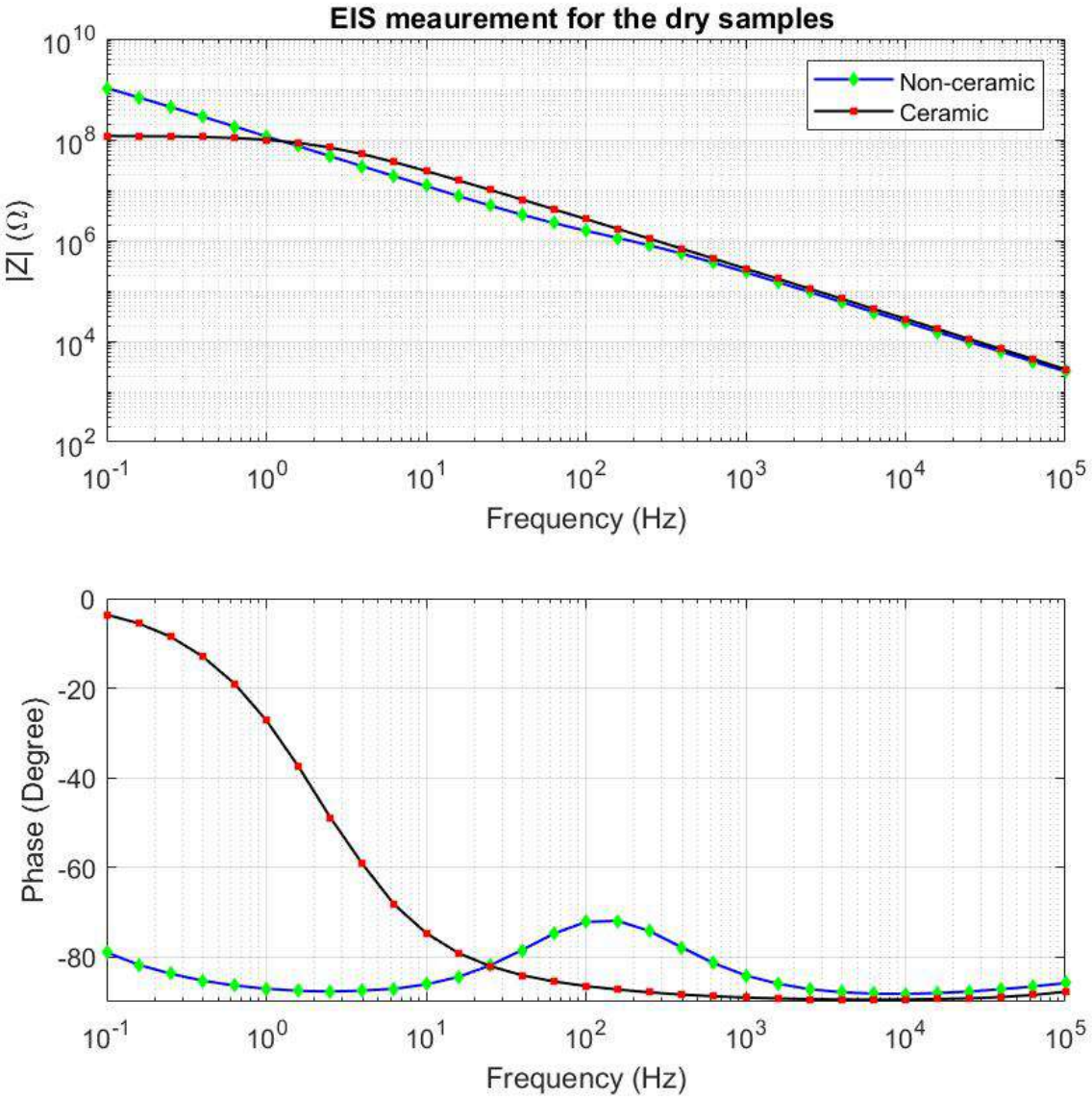

Figure 4.20: EIS measurement of a ceramic and a non-ceramic sample in the dry state

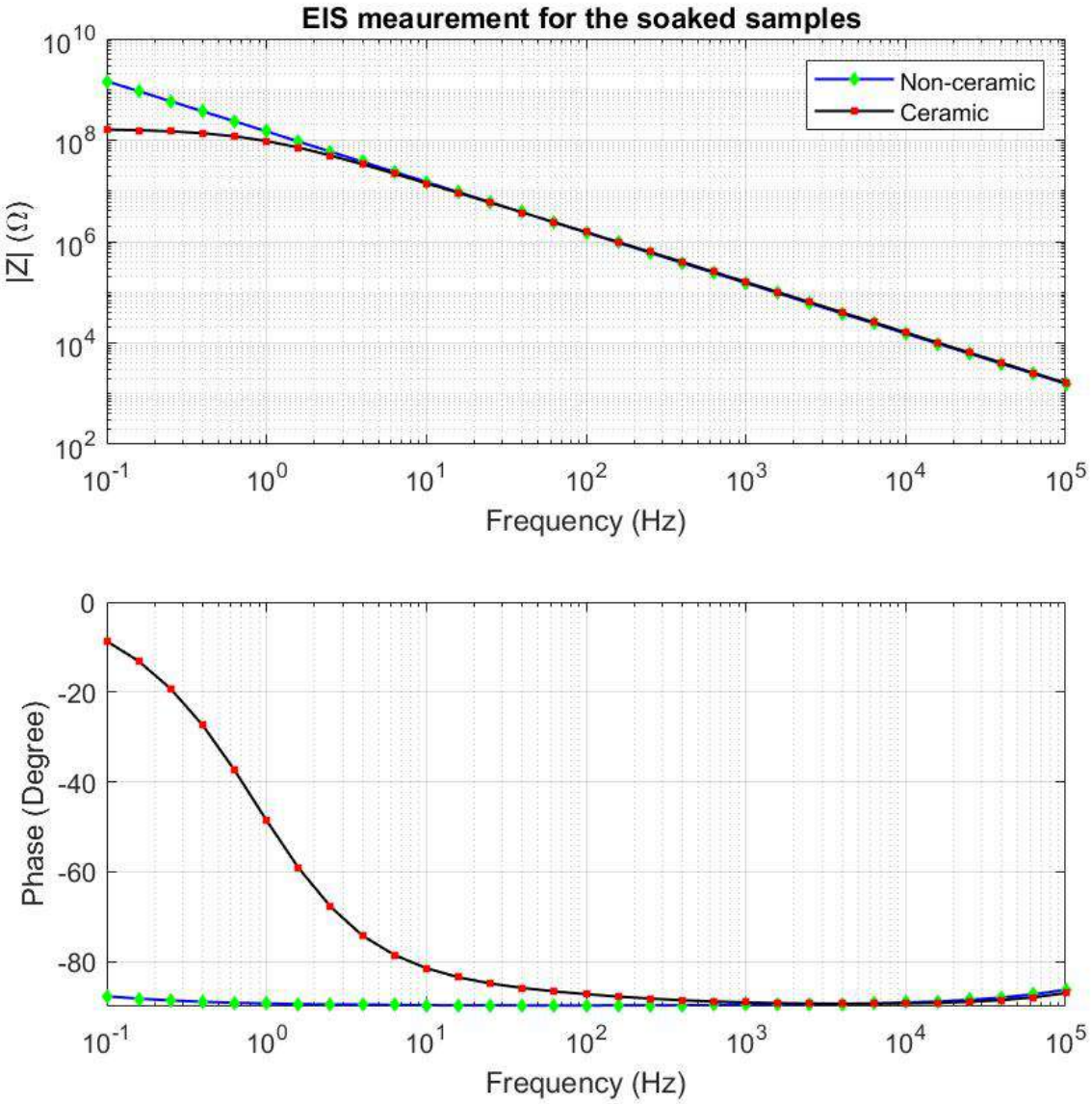

Figure 4.21: EIS measurement of a ceramic and a non-ceramic sample at 50 days soaking condition

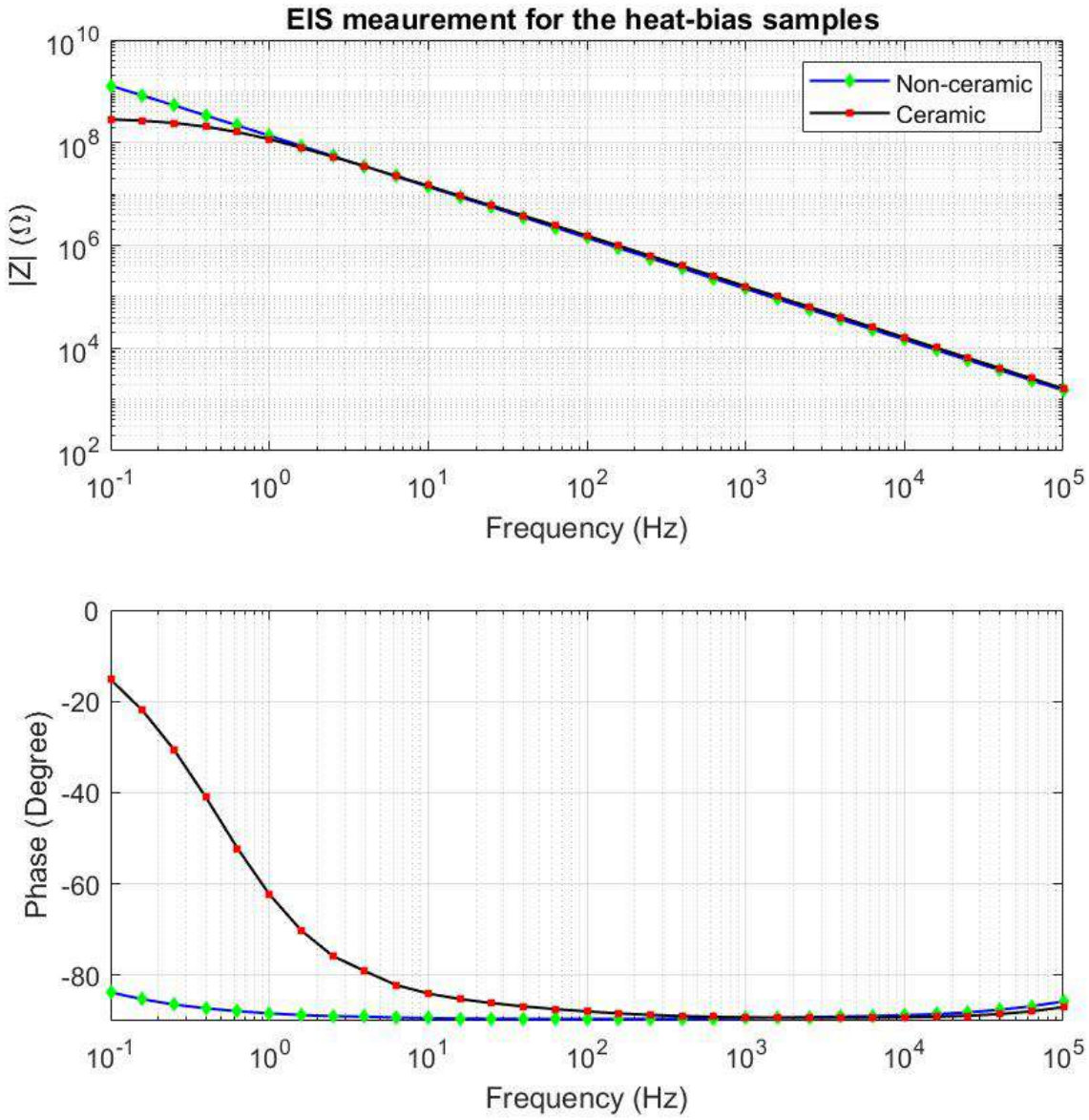

Figure 4.22: The EIS measurement for a ceramic and a non-ceramic sample soaked in 40 °C with 5V DC over 20 days

EIS measurement of a failed ceramic sample

The EIS measurement of a ceramic sample that failed during the heat-bias experiment in comparison to a non-failed ceramic sample under the same experimental conditions (40 °C and 5V DC) is depicted in Fig. 4.23. The failed sample shows a higher impedance for all frequencies as a result of the corroded metal layer. In other words, corrosion of the tracks leads to a lower capacitance and hence a higher impedance.

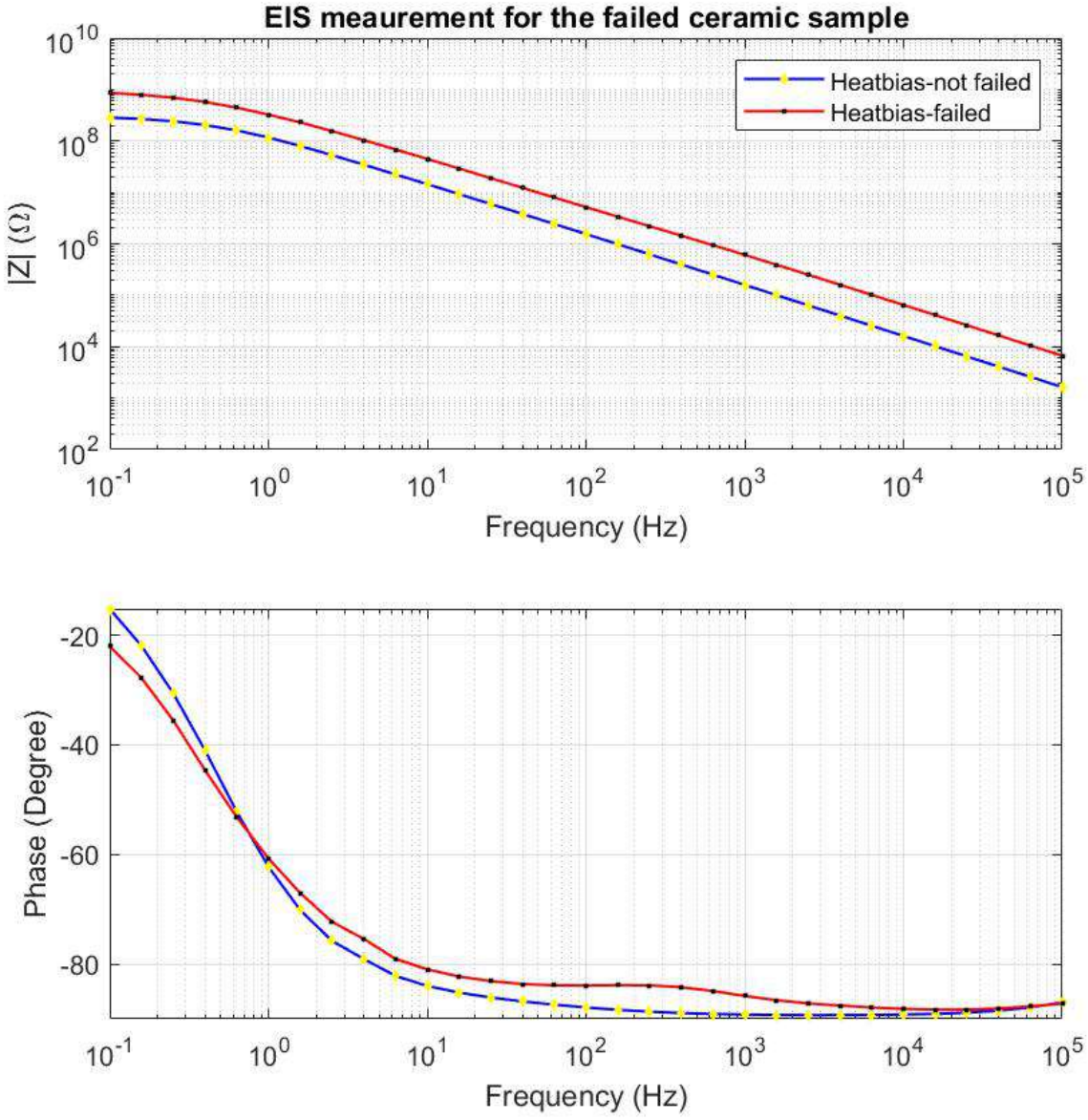

Figure 4.23

4.3. Interface samples

Interface samples as described previously are designed to determine the dominant water intake path. Three triple-track structures are present in every chip with an empty gap in the center of every structure. Provided that the tracks with less distance to the gap would corrode faster, the interface of the layers (polyimide to polyimide interface) would be the main water intake path. Figure 4.24 is a depiction of an interface sample.

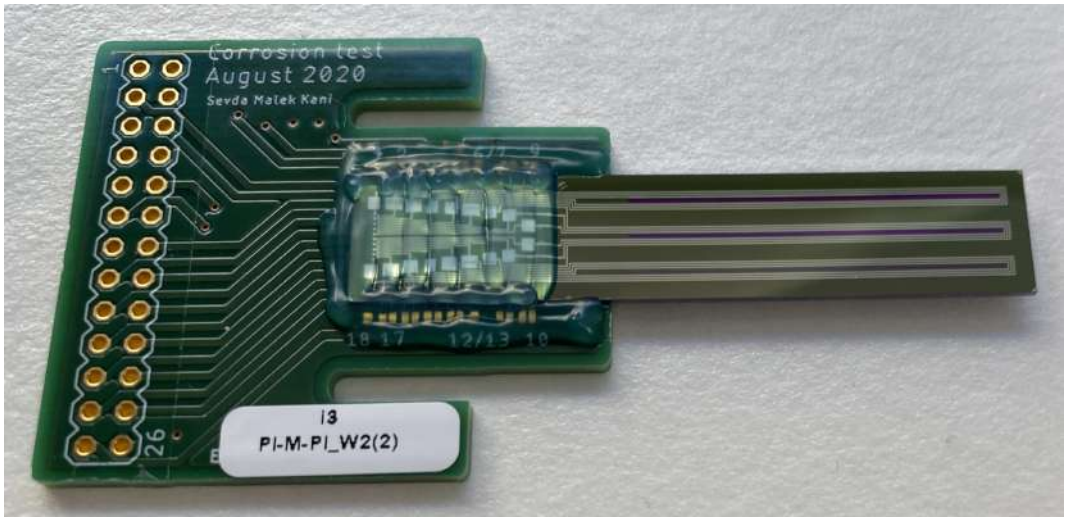

Figure 4.24: A picture of assembled interface sample

Three interface samples are tested for 46 days, one sample is soaked in PBS and 2 samples are in PBS with 5V bias. However, during the time of this study, no difference between the three triple-track's degradation has been observed. In addition, no failure of the tracks is detected visually and by resistance measurements. The interface samples don't have an interdigitated comb structure, as a result, the aging process is less effective on these samples (wider distance between tracks and weaker electric field).

The structure of the interface samples leads to slower degradation, as a result, a longer soaking time is required for these samples. Once the samples start to degrade depending on the sequence in which the triple-tracks corrode, conclusions can be made regarding the dominant water intake mechanism.

5

Discussion and future work

There are multiple explanations for corrosion types and mechanisms. However, for all corrosion incidents, the availability of condensed water in contact with the metal tracks is necessary. As a result, any approach hindering water accumulation on the interconnects has the potential to increase the lifetime of IMDs. Inorganic materials such as SiC have good barrier properties against moisture, however, they dissolve in water. On the other hand, organic materials are inert and stable in contact with water, although lacking barrier properties. As a result, combining inorganic and organic materials is a proposed approach to decrease water condensation and corrosion in microelectronics.

Inorganic thin layers are also utilized to increase the adhesion between the organic layers. Previously conducted projects and research suggest that thin layers of SiC and SiO_2 enhance the polyimide adhesion. These ceramic layers are used as adhesion promoters between PDMS and PI in a study conducted by Ordonez et al. [28]. The samples were tested by mechanical stress testing and it was concluded that the ceramic layers increased the adhesion of PI to PDMS. However, since no metal tracks were involved in the samples of this study no electrical characterization was performed. Therefore, although the influence of the ceramic layers on the adhesion has been investigated, there is not enough information regarding the electrical characterization and the corrosion protection of these layers. As a result, this thesis was defined to evaluate the influence of the ceramic layers on the leakage currents and the lifetime performances of the samples.

One important observation is that the leakage current of the ceramic samples is higher than non-ceramic samples prior to the soaking. This highlights the influence of the intrinsic variables such as material properties. SiC is a semiconductor that can be doped by impurities. In addition, an off-stoichiometric SiC with higher carbon concentration results in an increased electrical conductivity [41]. The ceramic layers in this study are deposited by the AKT®-PECVD system of Applied Material incorporate. It is required to investigate the composition of the SiC layer deposited in this study to confirm that the high leakage current values are due to the SiC layer conductivity.

One approach is performing X-ray photoelectron spectroscopy (XPS) on the samples. This technique is used to identify the elements present within a sample and additionally it recognizes the chemical bonds of the elements [39]. By examining the

composition of the SiC layer it is possible to explain the higher conductivity of this layer. In addition, the XPS method is useful to identify the chemical bonds within the ceramic samples and to confirm whether the expected covalent bonds with the polyimide are formed.

In addition to the higher LC results for ceramic samples, more failures and corroded tracks are observed in the ceramic samples as well. However, the corroded areas are localized in the samples. One possible explanation is that adding the thin ceramic layers introduces more voids and contamination to the devices. The presence of exceptions in the results highlights the effect of local irregularities in the devices. In other words, if adding thin layers of ceramic in the devices would result in an increase of local disturbances such as cracks, it would increase the number of voids available for the water condensation, thus, leading to local corrosion points.

In the fabrication process, a convection oven of 125 °C is used for 30 minutes before the ceramic layer depositions. The convection oven and the PECVD chamber are the machines used for ceramic samples and not for the non-ceramic samples which can be possible contamination sources. Contamination caused by a machine used for the ceramic samples could be a possible reason for the device failures. In addition, the AKT®-PECVD system is originally developed for flat display systems and it is not pinhole-free.

In this study, wafers with one layer of polyimide are fabricated alongside the two-layer samples. The one-layer samples contain aluminum-copper tracks encapsulated by polyimide with and without the ceramic layers as shown in Fig. 5.1. Due to the time restrictions, these devices are not tested. However, because the one layer samples have a simpler structure, their leakage currents could be used to evaluate the results obtained in this study. This can identify if the PI to PI interface is the main weak surface in the devices.

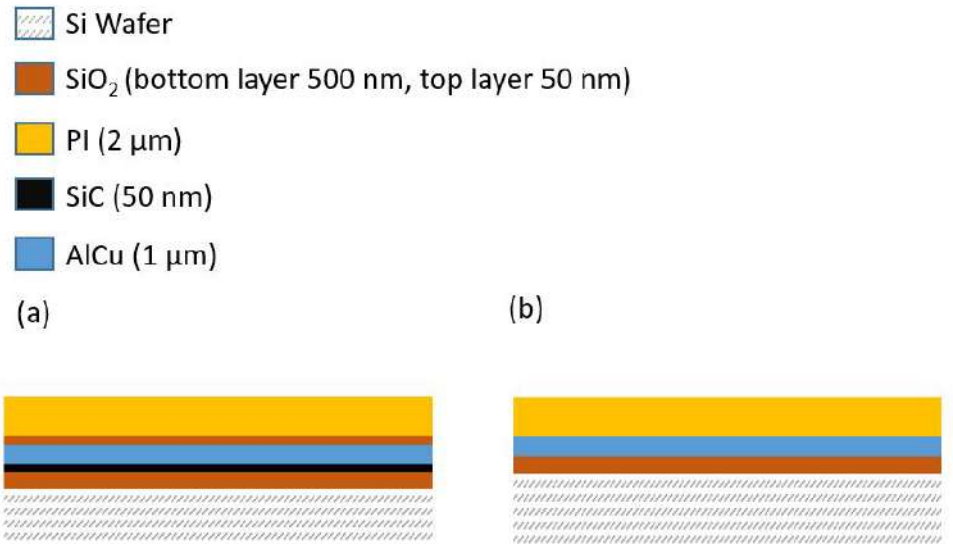

Figure 5.1: One layer samples, (a) with the ceramic layers (b) without the ceramic layers

The aging set-up designed in this study is suitable for evaluating samples at high temperatures and voltage bias. It provides real-time leakage current and resistance measurements for various types of samples in large numbers. However, the set-up can be boosted by some alterations. One necessary enhancement for the ATLA set-up is reducing the noise disturbance on the measured signals. Utilizing a Faraday cage and connectors that are fixed in a specific position will decrease the variations in the measurements in the sub-nano range. The elevated temperature of 40 °C is used in the set-up due to the glass transition temperature of the material used for the heater holder. The 3D printed holder is made of PLA with a glass transition temperature of 55–65 °C [40]. Therefore, by replacing the PLA holder with a heat-resistant material, a higher temperature can be reached. The higher temperature will accelerate the experiment results.

As the experiment of interface samples indicate, the lifetime experiments require long-term data acquisition. In addition, for gaining statistical reliability, a larger number of samples is required. Therefore, profound research and planning prior to the sample fabrication and testing are essential.

6

Conclusions

Corrosion has been a long-lasting challenge for IMDs, however, researchers have taken various steps forward in fighting this challenge and have achieved high reliability for bioelectronics. Polyimide is an example of the polymers used to isolate active electronics from harsh environments.

In this study, an aging and lifetime set-up is built in order to measure the leakage current and electrical resistance of the test samples in real-time. IDE structures of aluminum-copper with polyimide encapsulation and a variation of the samples with thin layers of SiC and SiO_2 in between the polyimide layers have been fabricated. The test devices are evaluated by their leakage current and EIS measurements.

It is concluded that the samples with SiC and SiO_2 layers show higher leakage current throughout the experiments and are more conductive. In addition, more failed (corroded) samples are observed for the ceramic variation. An in-depth study is required to understand the reason causing these unexpected observations, however, the off-stoichiometric composition of the SiC layer is suggested as the main possible reason. The results emphasize the importance of material choices for the fabrication of the devices. Any alternations in the design of the devices result in different electrical properties and it influences the lifetime reliability of the devices. Addition of any material influences the devices in multiple aspects which all require profound investigations.

In conclusion, the knowledge gained through this study not only targets corrosion protection but also contributes to our knowledge about the material characteristic and paves the way for a more in-depth understanding of the long-term performance of the IMDs.

A

F2R interconnect samples

The F2R samples fabricated by Corvin Messow [20] are shown in Fig. A.1. Some of the samples are previously used for the bending tests.

Figure A.1: Previously fabricated F2R interconnects, some samples are already taken out of the wafer for experiments

In the early stages of this thesis, the samples were wire-bonded as shown in Fig. A.2 and soaked in PBS solution. All samples corroded in the first hours of the experiments.

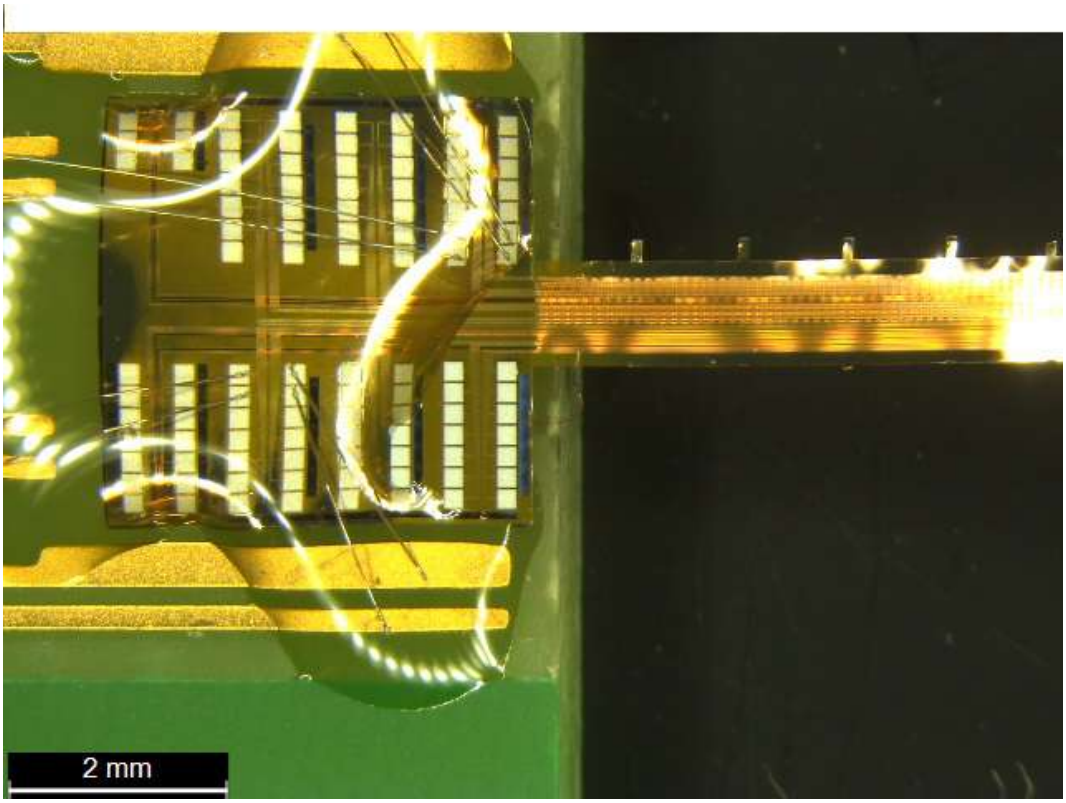

Figure A.2: Wire-bonded F2R interconnect samples

B

Microfabrication flowchart

Step ID	Process	Instruction
1	**Start of Technical Stage**	**First Oxide layer for PI adhesion**
2	Laser marking acc. WI	Batch owner will work together with operator to define wafer names.
3	FHZ4mHCl4m	4 minutes HF Ozone
4	Rinse / Dry	STD program
5	SiO2 400 700 Eng	500 nm thick low stress SiO2 deposition. Use recipe: SiO2 lowstress 400.
6		move test wafer to TS03 Metal deposition
7	**Start of Technical Stage**	**First PI coating & patterning**
8	Batch on hold	Please inform batch owner
9	Close couple	Within a day
10	DSCM 90C 2Min	descum 90C 2 minutes
11	Rinse / Dry	STD program
12	Spincoat VMX652	Manual Spinner 5s 500rpm + 25s 1000rpm
13	Bake VMX652 90s 125C	
14	Spincoat Polyimide PI2610 150mm	Bottle=PI2610 @RT, Pour 2cm drop at center of wafer, then start rotation Open 500rpm 8s, closed 1500rpm 45s, closed 3000rpm 2s

15	Vacuum Bake	t=10 min., T=room temperature
16	Bake on Hotplate	T=120°C, t=10 min
17	prog4 275gr 180min	O24, laad programma 4, 275grC, 180 min
18	Stop close couple	
19	Batch on hold	Please inform batch owner
20	HMDS_AZ4533_3900nm_SB110	
21	Batch on hold	Please inform batch owner
22	CorrosionTest_PI	50 m Prox, IFP 10006251 align to flat and triangles dose: 120 mJ/cm2
23	AZ4533_develop	
24	Batch on hold	Please inform batch owner
25	Reflow Bake	Resist Reflow 5min. at 125C
26	Poly-imide Metal	Tdesk 1m ECE0000 (ICP PAR02) on manual endpoint ~4min 40sec.
27	Microstrip 5010	Microstrip 5010 Bath 2 (Vuil) 15min
28	Microstrip 5010	Microstrip 5010 Bath 2 (Schoon) 5min -follow Microstrip by 5 min IPA rinse and then 5 min DI rinse.
29	Rinse / Dry	STD program
30	Batch on hold	Please inform batch owner
31	**Start of Technical Stage**	**SiC layer deposition**
32	Split batch	Start of Split
33	Close couple	From oven directly to trymax and to AKT
34	Postbake T=125°C t=var.	Bake in Convection Oven for >30min
35	DSCM 90C 2Min	descum 90C 2 minutes
36	sic 25 c xxx Cch	deposit recipe sic25c with the delivered thickness in 50 nm
37	Stop close couple	
38	Split batch	End of Split (Merge Batch)

39	Batch on hold	Please inform batch owner
40	Start of Technical Stage	Metal deposition & patterning
41	Close couple	From oven directly into load lock
42	Postbake T=125°C t=var.	Dehydration bake in convection oven t=30min @ T=125°C
43	ets 6nm Alcu1 1000nm 1kW	pm2 or pm5 ets 6nm AlCu1 1000nm 1kW
44	Stop close couple	
45	Batch on hold	Please inform batch owner
46	HMDS_HPR504_1300nm_SB110	Deposit PR; soft bake 110°C
47	CorrosionTest_AlCu	Hard Contact, IPF 10006249 align to flat, triangles and the cross structures dose: 40 mJ/cm2
48	Develop_HPR504	
49	Close couple	finalize within 1 days or place in vacuum environment
50	Reflow Bake 2min 125C	Post bake: 2min / 125 C
51	PES,30°C,6"	~10min PES etch, visual EP + 1 min OE Use Triton to improve wetting. - Follow etch by QDR: Process 3 (4 cycles)
52	Rinse / Dry	STD program
53	Stop close couple	
54	Microstrip 5010	Microstrip 5010 Bath 2 (Vuil) 15min
55	Microstrip 5010	Microstrip 5010 Bath 2 (Schoon) 5min -follow Microstrip by 5 min IPA rinse and then 5 min DI rinse.
56	Rinse / Dry	STD program
57	Batch on hold	Please inform batch owner
58	Start of Technical Stage	SiO2 layer deposition
59	Split batch	Start of Split
60	Close couple	From oven directly to trymax and to AKT
61	Postbake T=125°C t=var.	Bake in Convection Oven for >30min
62	DSCM 90C 2Min	descum 90C 2 minutes

63	sio 25 b xxx Cch	SiO25b50 the delivered thickness in 50 nm
64	Stop close couple	
65	Split batch	End of Split (Merge Batch)
66	Batch on hold	Please inform batch owner
67	**Start of Technical Stage**	**2nd PI coat & pattern**
68	Close couple	Within a day
69	DSCM 90C 2Min	descum 90C 2 minutes
70	Rinse / Dry	STD program
71	Spincoat VMX652	Manual Spinner 5s 500rpm + 25s 1000rpm
72	Bake VMX652 90s 125C	
73	Spincoat Polyimide PI2610 150mm	Bottle=PI2610 @RT, Pour 2cm drop at center of wafer, then start rotation Open 500rpm 8s, closed 1500rpm 45s, closed 3000rpm 2s
74	Bake on Hotplate	Hotplate 10 min @ 120°C, Use clean moitor wafer to place your wafer on
75	Bake PI 15min 150C	Put wafer horizontal in quartz rack
76	prog4 275gr 180min	O24, laad programma 4, 275grC, 180 min, In horizontal carrier
77	Stop close couple	
78	Batch on hold	Please inform batch owner
79	HMDS_AZ4533_3900nm_SB110	
80	CorrosionTest_PI	50m Prox, IFP 10006251 align to flat, triangles and cross structures dose: 120 mJ/cm2
81	AZ4533_develop	
82	Reflow Bake	Resist Reflow 5min. at 125C
83	Poly-imide Metal	Tdesk 1m ECE0000 (ICP PAR02) on manual endpoint ~4min 40sec.
84	Batch on hold	Please inform batch owner
85	Split batch	Start of Split

86	Experimental E28B	SiO2 50nm SiC 50nm TDesc 6 min PR Dummy ICP SiC01 3 min ICP SiC01 ~30sec (check on End Point) TDesc 30 sec between wafers
87	Split batch	End of Split (Merge Batch)
88	Microstrip 5010	Microstrip 5010 Bath 2 (Vuil) 15min
89	Microstrip 5010	Microstrip 5010 Bath 2 (Schoon) 5min -follow Microstrip by 5 min IPA rinse and then 5 min DI rinse.
90	Rinse / Dry	STD program
91	Batch on hold	Please inform batch owner
92	Outgoing Control	- Specify Outgoing Control. - Record number of total- and good substrates to be delivered.
93	Packing	Move wafers to labeled white container or single wafer boxes and double-pack.
94	Done	- Make sure flowchart is completely signed off. - Have product wafers delivered to customer. - Dispose or store testwafers (Remove from CR).

C

PCB design

The interconnecting PCB board map in the Eagle PCB design environment is shown in Fig. C.1 . All the routes are connected manually.

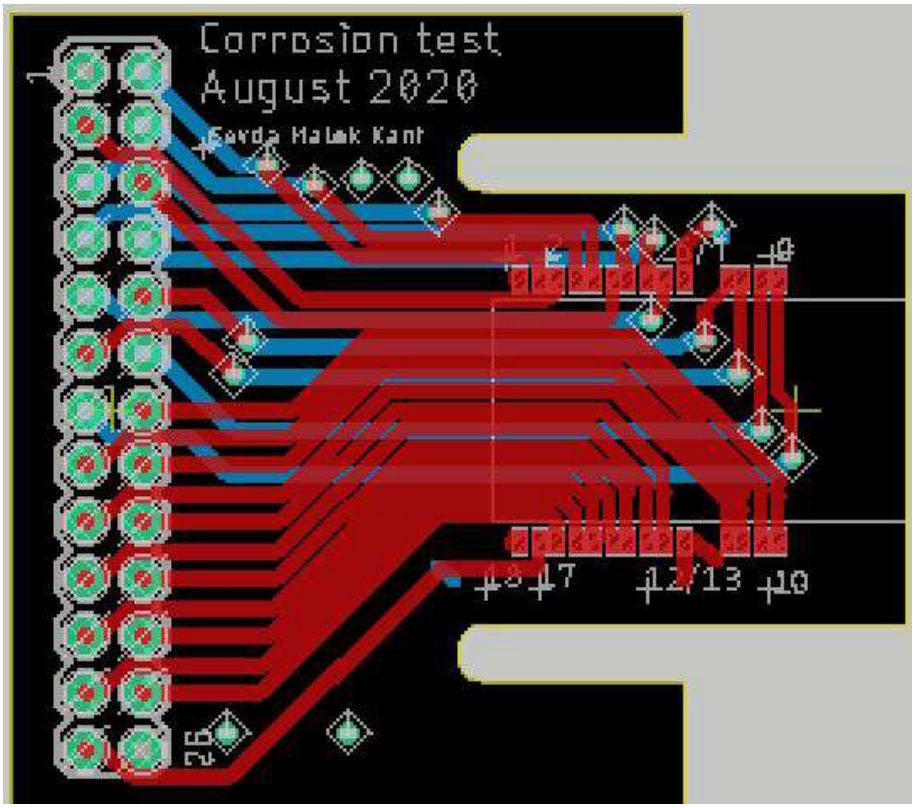

Figure C.1: Interconnecting PCB board design

The bias PCB board map is shown in Fig. C.2 . All the routes are connected manually.

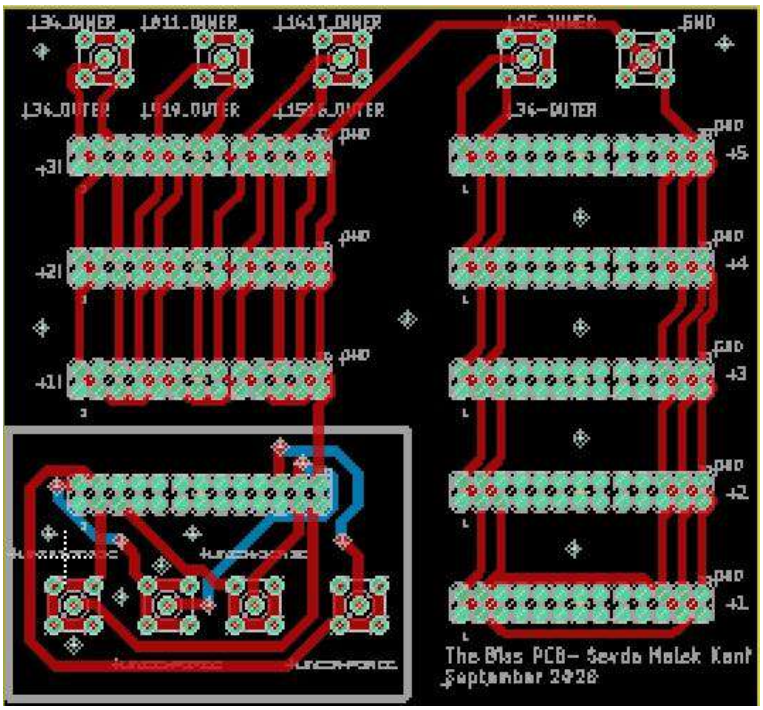

Figure C.2: Bias PCB board design

The measurement PCB board map is shown in Fig. C.3 . All the routes are connected manually.

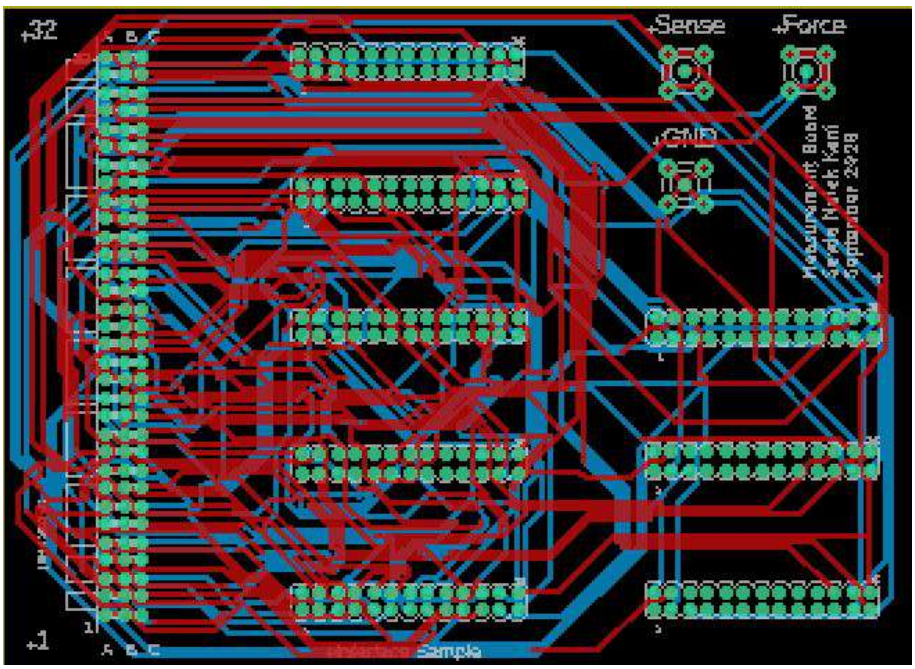

Figure C.3: Measurement PCB board design

D

Sample pictures

Prior to wire-bonding of the samples, initial trials with conductive glue was conducted on samples as shown in Fig. D.1

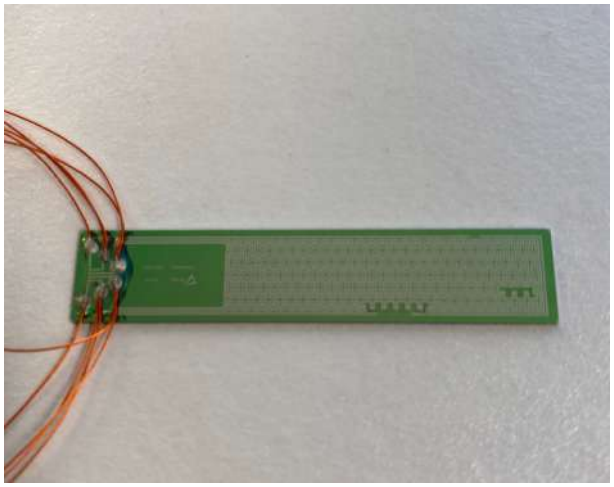

Figure D.1: A trial by a sample connected to wires with conductive glue

SEM images of the samples are presented as follows:

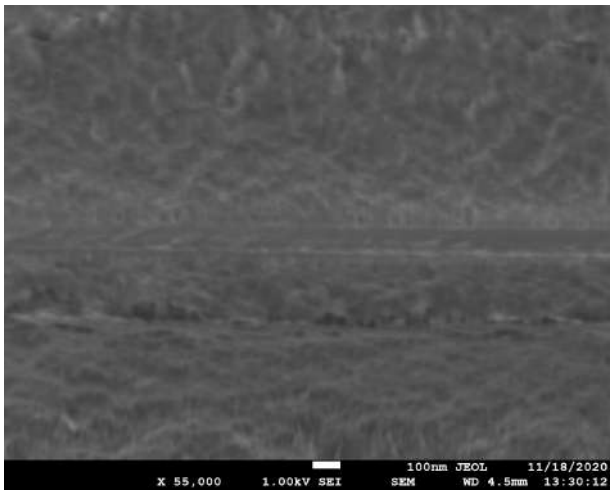

Figure D.2: SEM image of the ceramic interface of the samples

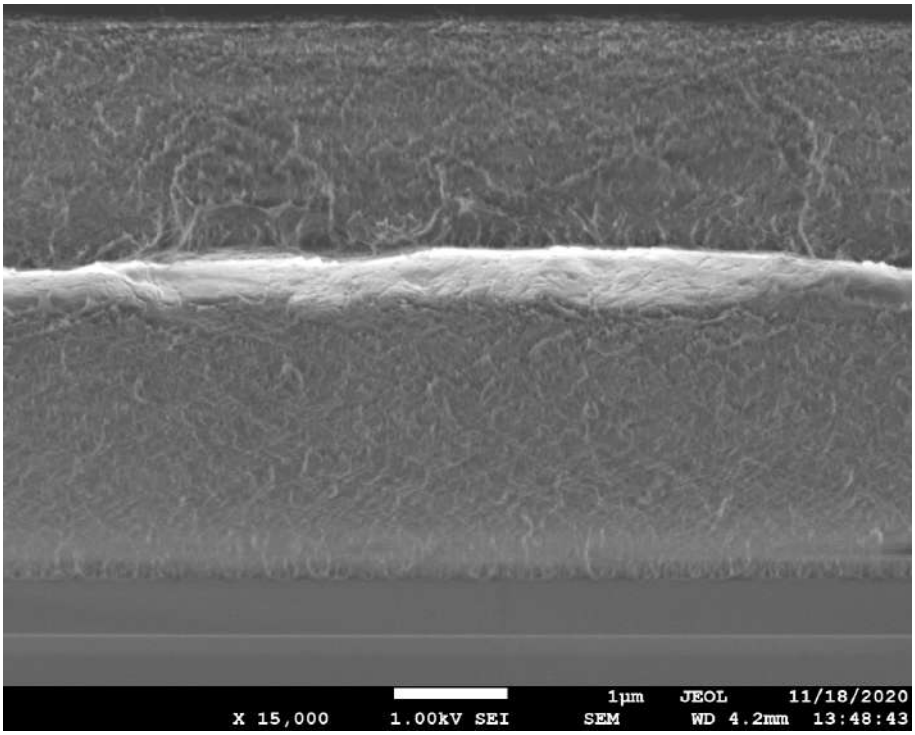

Figure D.3: SEM cross-section image of a non-ceramic sample

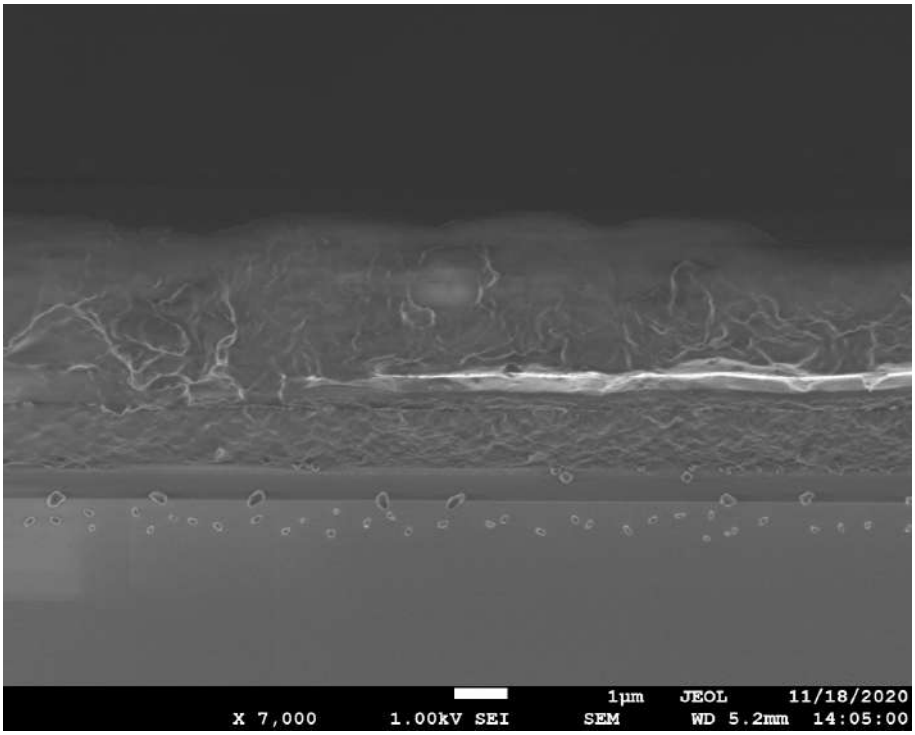

Figure D.4: SEM image of a degraded encapsulation for a ceramic sample

E

Additional EIS measurement results

Figure E.1 shows the EIS measurements of the non-ceramic samples in dry, soaked (50 days), and heat-biased conditions. The soaked sample shows more capacitive behavior than the other categories. It is expected for the soaked sample to be more capacitive than the heat-biased sample due to more degradation of the encapsulation in the accelerated conditions of the heat-bias experiment. However, a dry sample with a higher phase value is not expected and needs to be further investigated. The EIS measurements of the ceramic samples at different experimental conditions are shown in Fig. E.2. The samples demonstrate resistive behavior at low frequencies for all three conditions.

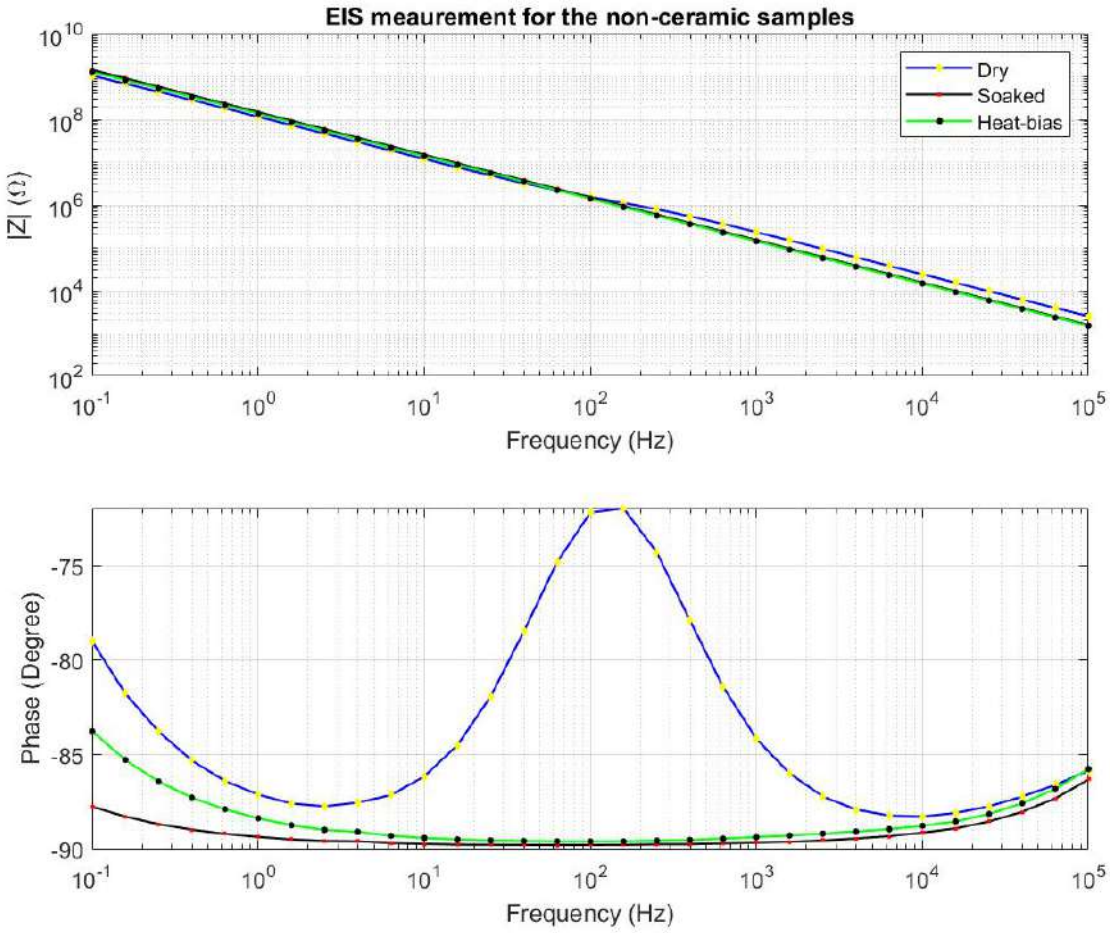

Figure E.1: EIS measurements of the non-ceramic samples with different conditions

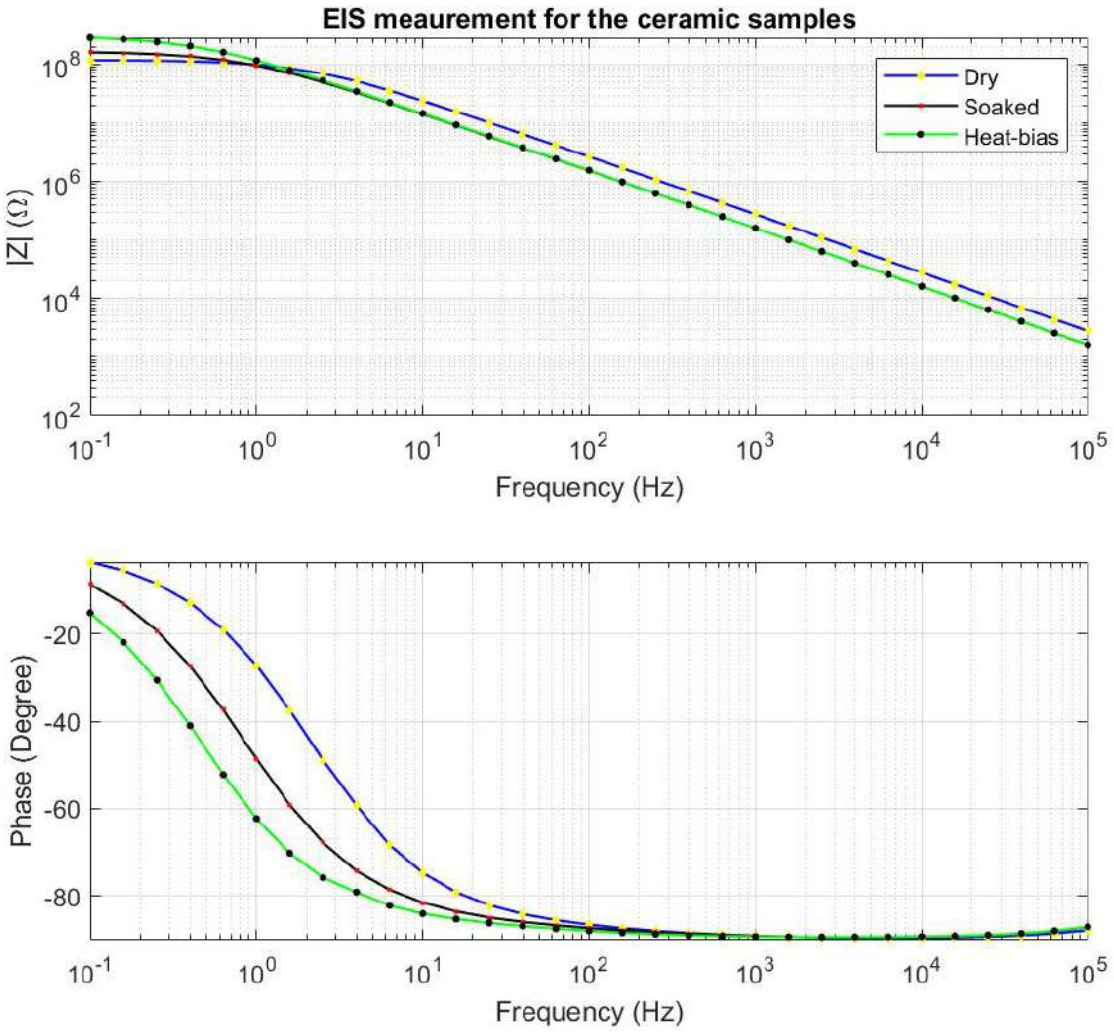

Figure E.2: EIS measurements of the ceramic samples with different conditions

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