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Hybrid Si/SiC Switch Modulation With Minimum SiC MOSFET Conduction in Grid Connected Voltage Source Converters

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***Abstract*— In this article, a hybrid Si/Si carbide (SiC) switch (HyS) modulation with minimum SiC MOSFET conduction (mcHyS) is experimentally characterized, so as to derive its conduction and switching performance. These are later used to derive a silicon (Si) area analytical model for the HyS configuration. The chip area model is used to benchmark the mcHyS modulation concepts against single-technology switches and typical HyS modulation when considering the implementation of a 100-kW two-level voltage-source converter (VSC) deployed for three industrial applications: photovoltaic inverter, electric vehicle fast-charging station, and battery storage systems for grid ancillary service. The two additional switching events of the SiC MOSFET, which differentiate the mcHyS modulation from the typical HyS one, are proven to happen in soft switching; therefore, the mcHyS switching performances are not penalized. Furthermore, the analysis presented shows how the studied mcHyS modulation performs against the single semiconductor technology and the typical HyS solution in terms of cost and power conversion efficiency. More specifically, it is shown that the HyS solutions are particularly competitive versus the full Si-based VSCs when the application at hand often operates at low partial loads. Finally, a 10-kW two-level VSC assembled with mcHyS is tested, so as to compare its efficiency versus single-technology switches.**

***Index Terms*— Double-pulse test (DPT), grid-connected voltage-source converter (VSC), hybrid silicon (Si)/Si carbide (SiC) switch, SiC MOSFET.**

I. Introduction

SILICON (Si) insulated-gate bipolar transistors (IGBTs) are currently the dominant power semiconductor technology for industrialized high-power grid-connected voltage-source converters (VSCs) due to their robustness, relatively low cost, and good conduction performance at high currents [1]. Nonetheless, Si IGBTs have unsatisfactory performance at low-current conditions, e.g., partial load efficiency, and especially in high-voltage class devices, the current tail observed during IGBTs turn-off results in high switching losses [2]. In this context, Si carbide (SiC) MOSFETs have gained popularity due to their excellent switching performance, the easy paralleling feature that can enable higher power handling, and, above all, the higher temperature capability of the SiC material, which can simplify the thermal management of the system [3]–[5]. The major drawback of the SiC MOSFET is the higher manufacturing cost and unproven reliability compared to the traditional Si IGBT [6]. The significantly higher cost of the SiC MOSFET calls for a compromised solution, e.g., a hybrid Si/SiC switch (HyS).

HySs are typically implemented by paralleling Si IGBTs and SiC MOSFETs, employing the excellent conduction and switching characteristics of the unipolar SiC devices to reduce the overall losses with respect to IGBTs [2], [7]–[9]. Various aspects of this HyS concept, such as current sharing and performance modeling [10], [11], switching strategy [12]–[14], fault tolerance [15], [16], and the influence of the parasitic inductance in the switching performances [12], have been investigated. Overall, HySs have demonstrated promising performances in several power electronics applications, including in aircraft's high-speed drives [17], wireless power transfer systems [18], and grid-connected inverters [19], while offering a compromised cost solution between full Si- and SiC-based switches.

An alternative HyS concept with minimum SiC MOSFET conduction (mcHyS) foresees the SiC MOSFETs acting only during the switching transitions and then being kept off during the main current conduction period. This HyS concept, shown together with its corresponding switching pattern in Fig. 1, may allow a further cost reduction since it allows the SiC device to have minimum conduction losses and, therefore, require a small chip area. In this HyS arrangement, the addition of an antiparallel diode is necessary, so as to conduct the reverse current, which, otherwise, would only be conducted by the body diode and the small chip area, i.e., MOSFET channel in the reverse direction, leading to unsatisfactory loss performance due to the high voltage drop. A comparison between the HyS with mcHyS and the typical HyS implementation (tHyS), which foresees SiC MOSFET to share the conducted

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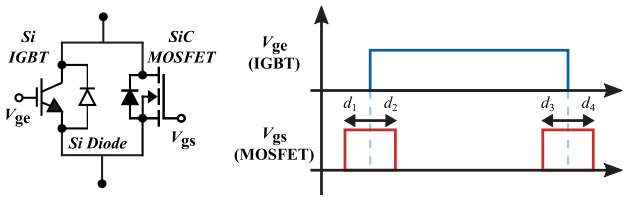

Fig. 1. Circuit schematic and switching pattern of the HyS with mcHyS, consisting of paralleling Si IGBT with SiC MOSFET, with the SiC MOSFET aiming solely the enhancement of switching performance. Note that the switching strategy can be optimized by the proper selection of the switching delays $d_1, \ldots, d_4$.

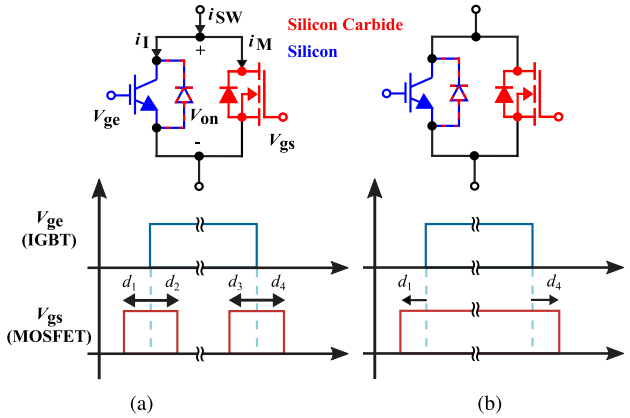

Fig. 2. Si/SiC HyS arrangements and switching patterns: (a) mcHyS where the SiC MOSFET is used for the switching transition only and (b) tHyS where the SiC MOSFET is used both for the switching transitions and sharing the current conducted by the switch with the Si IGBT.

current with the Si IGBT, has been described in [20] and [21]. However, these studies did not consider, in depth, its modeling, performance analysis, and chip area optimization, which are fundamental to properly gain insights on their performance and cost behavior compared to commercial Si- and SiC-based switches and so as to assess their suitability in industrial applications.

In this article, the mcHyS and the other switch arrangements, tHyS, SiC MOSFET, and Si IGBT, are experimentally characterized through double-pulse test (DPT) hardware platform, so as to derive their conduction and switching performance. Furthermore, a 10-kW two-level VSC (2L-VSC) assembled with mcHyS is tested, so as to compare its efficiency versus single-technology switches. Based on the DPT characterization, a Si area analytical model for the conceptualization of HyS switch configurations is derived. Then, the developed models are used to benchmark the mcHyS concept, against the tHyS implementation and the traditional full Si- and SiC-based switches. Herein, the device chip area is optimized deriving highly utilized solutions for cost competitiveness of the studied mcHyS operations. Furthermore, the mcHyS, with a 1200-V voltage class is compared when implemented in a 100-kW 2L-VSC deployed in various applications, such as photovoltaic (PV) inverter, electric vehicle (EV) fast-charging station (FCS), and battery energy storage systems (BESSs) providing grid ancillary service, therefore aiming at investigating its suitability on actual power electronics applications. These applications are selected due to their relevance in the modern electricity system and also because they require different operations of the 2L-VSC: in solar applications, the VSC acts primarily as an inverter; in EV FCSs, the converter acts as a rectifier, and in energy storage applications, the bidirectional operation is needed.

The contributions of this article are given as follows:

1) the analytical modeling, experimental characterization, and the digital control implementation in a 10-kW 2L-VSC of the mcHyS modulation shown in Fig. 1;
2) the generalized Si area analytical model for the conceptualization of HySs featuring minimum cost and high utilization of each switch technology for a cost–performance comparison of the HyS concepts;
3) the benchmarking of the mcHyS versus the other switch technologies in the grid-connected application of PV inverter, EV FCS, and BESS converter.

The remainder of this article is organized as follows. Section II describes the HyS arrangements and details the commutation process of the mcHyS. Section III provides the analytical models of 2L-VSCs based on the five-switch configurations (mcHyS, tHyS, Si IGBT, and SiC MOSFET), and Section IV details the HyS experimental characterization. The switch chip area and cost optimization procedure are described in Section V. Based on this, in Section VI, the different switches are compared when adopted in grid-connected applications, and the limitations of mcHyS are discussed. The concluding remarks are given in Section VII.

II. Hybrid Si/SiC Switches

The assembly of Si/SiC HySs is realized by paralleling a Si-based device with a SiC-based one. The possible structures and modulation patterns are shown in Fig. 2. The tHyS assembly and modulation are shown in Fig. 2(b). Here, a SiC MOSFET is paralleled to a Si IGBT, both to facilitate the switching transition and to share the conducting current. Such configuration, previously studied in literature [10]–[12], has shown to be well-performing from both the conduction and switching losses point of view, placing itself in between the pure Si IGBT and SiC MOSFET in the cost efficiency matrix. In the tHyS, the addition of a parallel diode is not strictly necessary. However, especially in grid-connected applications that require high reactive power operation and particularly during startup when all switches are kept OFF, it is useful to share the reverse conducting current with an antiparallel diode; otherwise, the SiC-MOSFET would have to be rated to withstand a high current, therefore losing its cost competitiveness.

The HyS with mcHyS, shown in Fig. 2(a), is an alternative configuration for an HyS. The key difference from the tHyS consists of the switching pattern. The detailed commutation process of the mcHyS is shown in Fig. 3, where it can be seen that switching losses occur only in the first and last MOSFET commutation, since the other switching events occur with the switch already on and so with ZVS soft switching because the parallel association is already conducting the impressed

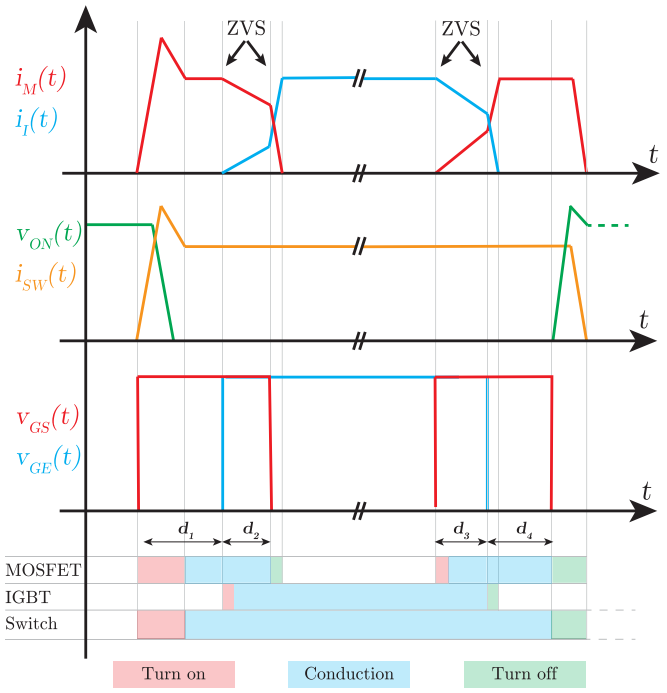

Fig. 3. Commutation process of the mcHyS. The switching transitions and conduction periods are highlighted with different colors, and the currents and voltages are referred to the schematic of Fig. 2(a).

ac current, and the voltage across the switch is very small. The delays $d_1, \ldots, d_4$ can be optimized, so as to enhance the switching and conduction performances of the mcHyS.

Furthermore, the additional diode for the mcHyS is a necessary component for the robust functioning of the switch, while, in the tHyS of Fig. 2(b), it is added for reducing the SiC MOSFET rating and/or to derisk body-diode degradation during startup [22]. This diode is required to conduct the reverse current since the SiC MOSFET is used only for the switching transitions, as possible to see from the switching pattern of Fig. 3. It has to be noted that this extra diode must be added; otherwise, the current would forcefully flow through the SiC MOSFET body diode, which is not sized to withstand the high current, and using the MOSFET channel in reverse conduction would not be economical because the chip area would need to increase. Both Si or SiC diodes are suitable for this purpose; in this article, the mcHyS is assembled with Si diode since there are commercially available devices already packaged together Si IGBT/Si diode. TO247 devices are used in the experimental characterization. In this way, the commutation inductance loops are minimized, and the two devices are properly designed and selected to be complementary. As just mentioned, the advantage of such configuration is that the SiC MOSFET can have a low-current rating and so low cost, while the switching losses of the switch are greatly reduced with respect to a pure Si IGBT. Such cost–performance analysis for this mcHyS is missing from the literature; therefore, the potential advantages and disadvantages and practical implementation issues of such HyS are not yet clear. These are discussed in this article in the following.

III. Hybrid Switch Analytical Modeling

A. Conduction Losses

Conduction losses in power semiconductors can be modeled as

$$P_c = v \cdot I_{\text{avg}} + r \cdot I_{\text{rms}}^2 \tag{1}$$

where v stands for the p-n junction barrier voltage, which is present in IGBTs and diodes, r stands for the ON-state resistance of the device, and I_{avg} and I_{rms} are the average and rms current flowing through the switch, respectively. The ON-state parameters of semiconductors can be extracted by the I–V curves presented in datasheets or experimentally derived. Furthermore, they are influenced by the junction temperature, T_j, following [23]

$$r(T_j) = r_{25^\circ\text{C}} + \text{tc}_r(T_j - 25) \tag{2}$$

$$v(T_j) = v_{25^\circ\text{C}} + \text{tc}_v(T_j - 25) \tag{3}$$

where v and r are the semiconductor p-n junction barrier voltage and the ON-state resistance, and tc_v and tc_r their respective temperature coefficients. These can be derived from the datasheet of the semiconductor, for example, the thermal coefficient of the ON-state resistance

$$\text{tc}_r = \frac{r_{T\text{j,max}} - r_{T\text{j,min}}}{T_{\text{j,max}} - T_{\text{j,min}}} \tag{4}$$

where Tj, max and Tj, min indicate the maximum and minimum junction temperatures. The ON-state resistance of a device increases with the temperature, and so tc_r is positive, while v decreases with temperature; therefore, tc_v takes negative values.

Typically, for the estimation of the conduction losses through (1), the ON-state characteristics are taken at the maximum allowed operating temperature, in the range of 125–150 °C, depending on the semiconductor and packaging technologies [23]–[26]. Following this approach, the losses can be accurately estimated at full power when, with a properly designed cooling system, it is expected that the junction temperature reaches its maximum level. At lower power, however, the power losses will be slightly overestimated.

In a grid-connected 2L-VSC, the analytical expression of I_{avg} and I_{rms} can be found averaging the line current during a switching period according to the switch duty cycle. In the case of sinusoidal PWM with one quarter zero-sequence voltage injection [27], the duty cycle of the upper $[D_u(\omega)]$ and bottom $[D_b(\omega)]$ switch can be expressed, respectively, as

$$\begin{aligned} D_u(\omega) &= \frac{1}{2} + \frac{m}{2}\sin(\omega) + \frac{m}{8}\sin(3\omega) \\ D_b(\omega) &= 1 - D_u(\omega) \end{aligned} \tag{5}$$

where m is the modulation index and ω is the phase angle. This modulation strategy leads to an improved harmonic performance with respect to simple sinusoidal PWM and space vector modulation [27].

Considering a pure sinusoidal phase current

$$I(\omega) = \hat{I}\sin(\omega + \varphi) \tag{6}$$

where φ is the phase shift between the fundamental line voltage and current, $\hat{I}$ is the peak ac line current, and the active

switch average and rms current can be calculated solving the following equations:

$$I_{\text{avg}} = \frac{1}{2\pi}\int_a^b I_c(\omega)D(\omega)d\omega \tag{7}$$

$$I_{\text{rms}} = \sqrt{\frac{1}{2\pi}\int_a^b I_c^2(\omega)D(\omega)d\omega} \tag{8}$$

while substituting the expression of the conducted current to I_c, the angular position of the beginning and end of the conduction period to a and b, and the switch duty cycle expression to $D(\omega)$. This approach provides accurate results if the converter switching frequency f_s is much greater than the grid frequency f_g, the bridge-leg dead time is negligible with respect to the switching period, and the maximum current ripple within a switching period is much smaller than $\hat{I}$. Such assumptions hold in grid-connected VSCs since f_s is in the order of kHz, and an L or LCL filter, which is typically designed to strongly limit the current ripple flowing in the converter, has to be placed between the VSC and the grid, so as to respect the grid connection standards. The semiconductors' current stress in single switch technology-based 2L-VSC can be calculated as [28]. HyS-based VSCs, instead, require different approaches.

1) mcHyS-Based 2L-VSC: The mcHyS, as shown in Fig. 1, foresees the MOSFET only for switching, i.e., for chip area minimization, and the full current conduction through the Si-based devices. Therefore, the conduction losses in this HyS arrangement can be calculated as the ones of a Si IGBT-based 2L-VSC. Nonetheless, as shown Fig. 1, the switching strategy can be optimized by the proper selection of the switching delays $d_1, \ldots, d_4$. Therefore, if the MOSFET is turned on before the IGBT and turned off after the IGBT, in this time period, it will conduct the full current. These extra conduction (ec) losses depend on the total time in which the SiC MOSFETs conduct the full current, d_{tot}, and they can be evaluated as

$$P_{\text{exC-M,mcHyS}} = d_{\text{tot}} f_s r_{\text{ds,on}} \hat{I}^2 \frac{8m\cos\varphi + 3\pi}{24\pi} \tag{9}$$

where $r_{\text{ds,on}}$ is the MOSFET ON-state resistance.

2) tHyS-Based 2L-VSC: The tHyS intends both IGBT and MOSFET for current conduction, as presented in [10]. This hybrid switch is typically implemented paralleling Si IGBTs and SiC MOSFETs; however, in this article, a Si diode is added also in this configuration, so as to reduce the current stress on the SiC MOSFET in rectifier operation, which, otherwise, leads to a large MOSFET area; therefore, the tHyS would lose its cost competitiveness. Furthermore, it is considered that the SiC MOSFET body diode does not conduct due to its high forward voltage drop. Such an assumption is confirmed by the third quadrant operation I–V curves provided by the device manufacturer [25].

The Si devices will not conduct until the voltage across the switch, V_{on}, overcomes its p-n junction barrier potential v_{pn}, that is, $v_{\text{ce},0}$ in the case of the IGBT and $v_{f,0}$ in the case of the diode. Therefore, the current values over which the bipolar devices start conducting and their angular position are defined as

$$I^* = \frac{v_{\text{pn}}}{r_{\text{ds,on}}} \tag{10}$$

$$\delta^* = \arcsin\left(\frac{v_{\text{pn}}}{r_{\text{ds,on}}\cdot\hat{I}}\right). \tag{11}$$

The Si IGBT conducts in the angular interval $\omega \in [\delta - \varphi; \pi - \delta - \varphi]$ and the diode during the interval $\omega \in [\pi + \delta_r - \varphi; 2\pi - \delta_r - \varphi]$, where δ and δ_r are found substituting, respectively, the IGBT and diode ON-state parameters in (11).

For line current values, $I(\omega)$, larger than I_f^* and lower than I_r^* the current sharing between Si devices and MOSFET can be derived according to the devices' ON-state characteristics as

$$I_{\text{M,f}}(\omega) = \frac{I(\omega)r_{\text{ce}} + v_{\text{ce},0}}{r_{\text{ds,on}} + r_{\text{ce}}} \tag{12}$$

$$I_I(\omega) = \frac{I(\omega)r_{\text{ds,on}} - v_{\text{ce},0}}{r_{\text{ds,on}} + r_{\text{ce}}} \tag{13}$$

$$I_{\text{M,r}}(\omega) = \frac{I(\omega)r_f + v_f}{r_{\text{ds,on}} + r_f} \tag{14}$$

$$I_d(\omega) = \frac{I(\omega)r_{\text{ds,on}} - v_f}{r_{\text{ds,on}} + r_f} \tag{15}$$

where r_{ce} and r_f are the ON-state resistances of the Si IGBT and Si diode, respectively. Equations (12) and (13) are referred to the forward conduction stage of the switch, while (14) and (15) are referred to the reverse conduction stage. Overall, the tHyS ON-state characteristics can be expressed as

$$V_{\text{on,tHyS}}(I) = \begin{cases} r_{\text{ds,on}}\cdot I_{\text{M,r}}, & \text{if } I <= I_r^* \\ r_{\text{ds,on}}\cdot I, & \text{if } I_r^* < I < I_f^* \\ r_{\text{ds,on}}\cdot I_M, & \text{if } I >= I_f^*. \end{cases} \tag{16}$$

The average and rms current flowing through the IGBT can then be calculated substituting $I_I(\omega)$ in (7) and (8) and integrating during its conduction interval

$$I_{\text{avg,I}} = \frac{1}{2\pi}\int_{\delta-\varphi}^{\pi-\delta-\varphi} I_I(\omega)D_u(\omega)d\omega \tag{17}$$

$$I_{\text{rms,I}} = \sqrt{\frac{1}{2\pi}\int_{\delta-\varphi}^{\pi-\delta-\varphi} I_I^2(\omega)D_u(\omega)d\omega}. \tag{18}$$

Similarly, the diode current stress can be found as

$$I_{\text{avg,d}} = \frac{1}{2\pi}\int_{\pi+\delta_r-\varphi}^{2\pi-\delta_r-\varphi} I_d(\omega)D_u(\omega)d\omega \tag{19}$$

$$I_{\text{rms,d}} = \sqrt{\frac{1}{2\pi}\int_{\pi+\delta_r-\varphi}^{2\pi-\delta_r-\varphi} I_d^2(\omega)D_u(\omega)d\omega}. \tag{20}$$

It has to be noted that, for peak ac current lower than the minimum current necessary for the IGBT to conduct, the value of δ becomes equal to $\pi/2$, and therefore, the integration interval in (17)–(20) becomes null. The conduction losses are then fully flowing across the SiC MOSFET.

As previously mentioned, the MOSFET conducts during the full period; however, when the bipolar devices are conducting, the MOSFET sees only a fraction of the total current. The rms current flowing through it is then found according to, (21), as shown at the bottom of the next page.

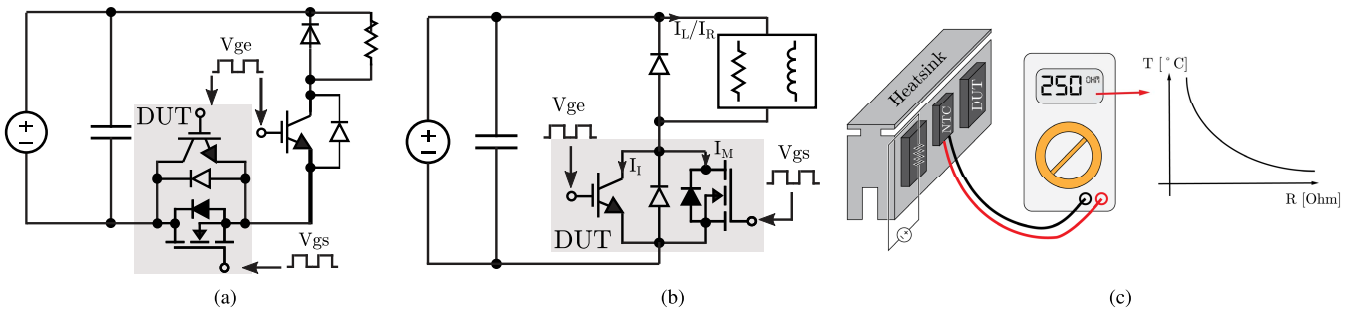

Fig. 4. Electrical circuit schematics for the experimental derivation of (a) reverse conduction characteristics of various switches, (b) forward conduction and switching characteristics, and (c) thermal circuit for the control and monitoring of the semiconductor case temperature.

In addition, the ec losses in the MOSFET due to the turn-on and turn-off delays would then only happen for current levels higher than I^* since, for lower current, the MOSFET would conduct the full current anyway. These can then be estimated by

$$P_{\text{exC-M,tHyS}} = \frac{r_{\text{ds,on}} d_{\text{tot}} f_s \hat{I}^2}{24\pi} \times \left[6(2m + \sin\delta)\cos\delta - 4m\cos^3\delta + 3(\pi - 2\delta)\right]. \tag{22}$$

3) Current Stress Equations Verification Through Circuit Simulator: The accuracy of the proposed equations is verified with the circuit simulation software PLECS.

A simulation model of a 2L-VSC assembled with different switch technologies has been built, so as to calculate the average and rms current flowing through the different components of the HySs at different operating points. The simulation parameters considered are $f_s = 10$ kHz, $V_{\text{dc}} = 900$ V, $V_{\text{ac,ll}} = 400$ V, $P_n = 100$ kW, and $\varphi = 0$.

The 2L-VSC is interfaced with the grid through a filter inductance with a value of 1 mH, thus resulting in a low-current ripple, below 1% the peak ac current. For the verification of the HySs arrangements, $v_{\text{ce},0}$ and $v_{f,0}$ are set to 0.9 and 1 V, respectively. The ON-state resistances considered are $r_{\text{ce}} = 20$ mΩ, $r_{\text{ds,on}} = 40$ mΩ, and $r_f = 15$ mΩ. These values are compatible with the I–V characteristics of the devices considered in experimental testing in Section IV. The simulations are run with a variable step solver, DOPRI (nonstiff), with maximum step size and relative tolerance of 1 μs. Table I displays the average and rms current values flowing through a single switch of a 2L-VSC operated as a full-power factor inverter calculated through the analytical method presented in this section and the PLECS model. It can be noted that the analytical expressions provide excellent accuracy with respect to the circuit simulations.

TABLE I
VALIDATION OF THE EQUATIONS PROPOSED IN SECTION III-A THROUGH THE CIRCUIT SIMULATOR PLECS

		Analytical calculation	Simulation	Error %
mcHyS	$I_{\text{avg,T}}$	51.01	49.78	+2.41
	$I_{\text{avg,D}}$	13.97	14.09	-0.85
	$I_{\text{rms,T}}$	90.87	89.14	+1.90
	$I_{\text{rms,D}}$	46.48	46.08	+0.86
tHyS	$I_{\text{rms,M}}$	42.94	42.50	+1.02
	$I_{\text{avg,T}}$	28.51	28.23	+0.98
	$I_{\text{rms,T}}$	52.27	51.40	+1.66
	$I_{\text{avg,D}}$	8.06	8.11	-0.62
	$I_{\text{rms,D}}$	28.50	28.27	+0.81

B. Switching Losses

The switching losses of a 2L-VSC can be analytically calculated through the following general equation:

$$P_s = \frac{f_s}{2\pi}\int_0^{2\pi} E_{\text{sw}}\big(V_{\text{dc,sw}}, I(\omega)\big)d\omega \tag{23}$$

where E_{sw} represents the device switching energy as function of the switched voltage $V_{\text{dc,sw}}$ and current I. The voltage dependence can be considered linear, while the current dependence can be approximated by quadratic functions. This approach is valid for 2L-VSCs, regardless of the switch configuration. E_{sw}, instead, is characteristic of each device, and for HySs, it is also influenced by the switching delays $d_1, \ldots, d_4$, as it is discussed in Section IV.

IV. EXPERIMENTAL CHARACTERIZATION

The conduction and switching performances are characterized through a single-pulse test (SPT) and a DPT whose circuit schematics are illustrated in Fig. 4(a) and (b), together with the thermal conditioning circuit in Fig. 4(c). The tests have been carried out with four devices in parallel with a common

$$I_{\text{ms,M}} = \sqrt{\frac{1}{2\pi}\left(\int_{\delta-\varphi}^{\pi-\delta-\varphi} I_M^2(\omega)D_u(\omega)d\omega + \int_{\pi-\delta-\varphi}^{\pi+\delta_r-\varphi} I^2(\omega)D_u(\omega)d\omega + \int_{\pi+\delta_r-\varphi}^{2\pi-\delta_r-\varphi} I_{\text{M,r}}^2(\omega)D_u(\omega)d\omega + \int_{2\pi-\delta_r-\varphi}^{2\pi+\delta-\varphi} I^2(\omega)D_u(\omega)d\omega\right)} \tag{21}$$

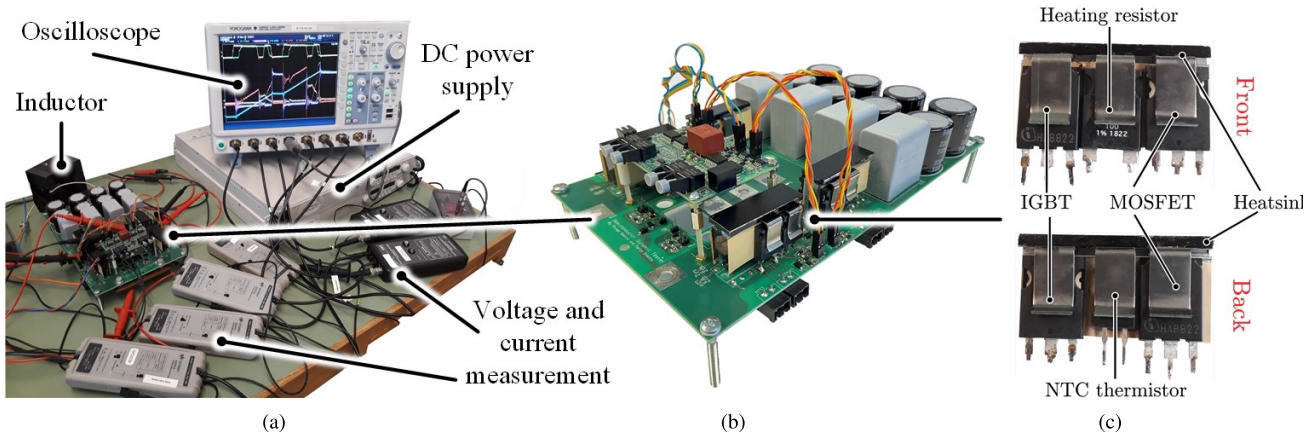

Fig. 5. (a) Test setup, (b) DPT board with gate driver on top, and (c) semiconductors and thermal management devices for the characterization of the semiconductors devices.

external gate resistor, R_g of 4 Ω, and gate driver voltages, V_{gs}, V_{ge} for MOSFET and IGBT, respectively, of +17/−4 V. In order to control the temperature of the device under test, a heating resistor MP9100-100 and an NTC thermistor TO-103J2F are attached to the semiconductors' heatsink. The thermal circuit for the control and monitoring of the semiconductor case temperature is shown in Fig. 4(c). In addition, during the tests, an FLIR thermal camera is used to ensure that the temperature is within the test range. The semiconductors under tests are the 1200-V class SCT3040KL SiC MOSFET manufactured by Rohm Semiconductor [25] and the IKQ40N120CT2 Si IGBT/diode manufactured by Infineon [24], both rated for 40 A. The choice of discrete TO-247 semiconductors for the HyS testing is driven by the necessity of minimizing the commutation loops between the switches that are detrimental to the switching performances. In this context, the paralleling of modules would require significantly larger connections between the individual components due to their larger size compared to discrete TO-247 devices. Ideally, commercial HyS could be assembled with both Si and SiC devices inside the same power module to further reduce stray inductances and ensure optimal performances.

The tests are carried out with four devices in parallel to constitute a single switch, resulting in a 160-A switch; therefore, the HySs are assembled with the hard-paralleling of two SiC MOSFETs and two Si IGBTs. The PCB layout aims at minimizing the parasitic inductances between the switches, placing them close to each other, so that they would properly share the dynamic current. A perfect current sharing during the switching transitions between the parallel devices can be ensured only by employing a properly tuned separate gate driver for each device. This solution increases the complexity and cost of the system. Alternatively, one gate driver for each switch technology can be used, resulting in a good tradeoff between optimal current sharing and system complexity. In this way, the switching transitions are properly coordinated between the SiC-MOSFETs and the Si-IGBTs. Nonetheless, it is not guaranteed that the two SiC-MOSFETs exactly share the current during the switching transitions.

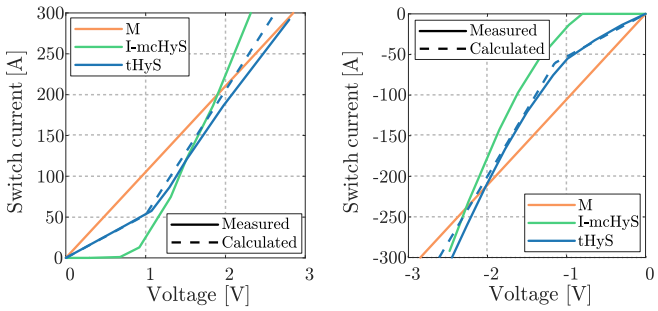

Fig. 6. (a) Forward and (b) reverse ON-state characteristics of four parallel SiC MOSFET, four parallel Si IGBT, and two Si IGBT plus two SiC MOSFET in parallel, derived for $T_j = 25$ °C, V_{gs} and $V_{ge} = +17/-4$ V, and $R_g = 4$ Ω, and analytically calculated according to (16).

In this context, the PCB layout and minimization of parasitic inductances are crucial to ensure the best performances.

The experimental implementation of the double-pulse tester is shown in Fig. 5(a), together with the semiconductor board and its gate driver [see Fig. 5(b)], and the thermal management devices and their arrangement together with the semiconductors [see Fig. 5(c)].

1) Conduction Losses: The forward conduction losses are evaluated through a resistive SPT where a resistive load is connected in parallel to a diode and a short pulse is sent to the bottom switch [see Fig. 4(b)]. The pulsewidth is selected to be 15 μs to limit self-heating, but long enough to compensate for the parasitic circuit voltage drops. For the reverse conduction characteristics, the circuit is slightly modified, and the device under tests is connected between a switch and the dc capacitors with the emitter/source connected with the emitter of the switch [see Fig. 4(a)]. A low dc voltage, in the range of 5–20 V, is impressed across the half-bridge so that low voltage probes can be used for measuring the voltage drop over the switch, guaranteeing higher accuracy, since the voltage across the switch under test is in the order of few volts.

The forward and reverse ON-state characteristics of the single-technology switches are shown in Fig. 6(a) and (b)

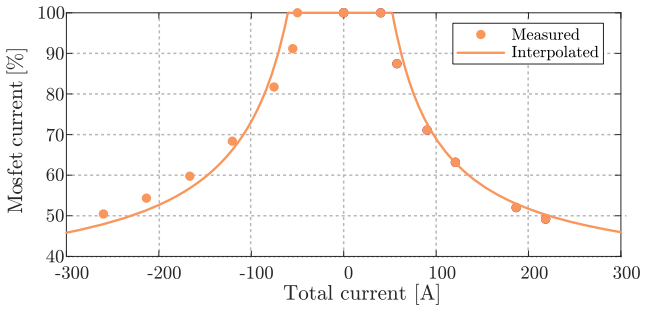

Fig. 7. Percentage of the total conducted current by the tHyS flowing through the MOSFET channel; derived for $T_j = 25$ °C, V_{gs} and $V_{ge} = +17/-4$ V, and $R_g = 4\ \Omega$, and analytically calculated according to (12) and (14).

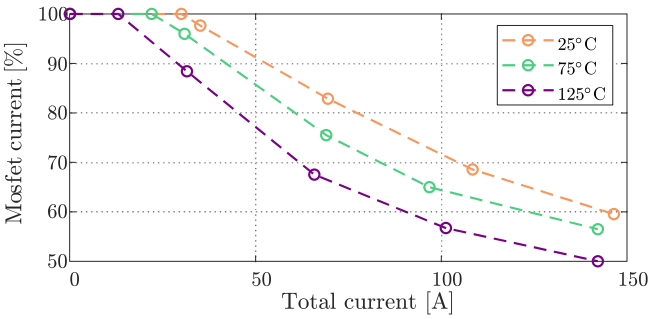

Fig. 8. Measured current flowing through the MOSFET in a HyS at different junction temperatures, derived for V_{gs} and $V_{ge} = +17/-4$ V, and $R_g = 4\ \Omega$.

together with one of the HySs. Comparing the tHyS's conduction I–V curves with the IGBT and MOSFET ones [see Fig. 6(a) and (b)], it can be seen that, for low-current levels, such as below 50 A, the tHyS would perform significantly better than the IGBT and mcHyS solution, very close to the MOSFET curve. In this context, the tHyS becomes attractive for applications that require frequent operation at low partial loads. Furthermore, at a high current level (>250 A), this hybrid solution starts having better conduction performances than the MOSFETs but worse than the IGBT and mcHyS. It has to be noted that the mcHyS follows the Si IGBT-diode I–V curve since the SiC MOSFET is activated only during the switching transitions. Therefore, only the tHyS shows an improved conduction characteristic with respect to the IGBT solution.

Together with the HyS I–V curve, the current sharing between IGBT/diode and MOSFET is crucial information for the design and optimization of the HyS and its components. The current sharing at different total switch current with $T_j = 25$ °C, $V_{gs} = 17/-4$ V, and $V_{ge} = 17/-4$ V is shown in Fig. 7. As described in Section III, the junction temperature influences the ON-state parameters of the switches and, therefore, the current sharing in the hybrid switch [29]. The resistance of the MOSFET channel increases with the rise in temperature; on the other hand, the p-n junction barrier voltage of the IGBT decreases. In consequence, the starting value for the conduction of the IGBT is lower at a higher temperature, and overall, the MOSFET will conduct a lower percentage of the total current due to the higher ON-state resistance. This trend is shown in Fig. 8 where the percentage

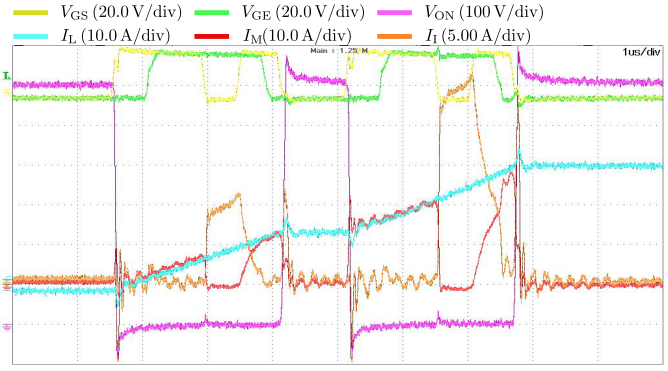

Fig. 9. Double-pulse test waveforms of mcHyS obtained through the test setup of Fig. 5 and referred to the circuit schematic of Fig. 4(a).

of current flowing through the MOSFETs of the tHyS is measured at various junction temperatures, between 25 °C and 125 °C, which is the temperature range in which power semiconductor typically operates. The difference in current sharing is significant for a high-temperature swing, as shown in Fig. 8. During the switching transition and the 50-Hz cycles, instead, the temperature rise is smaller due to the lower time constants, and so the current sharing is not significantly influenced by such fast temperature swings [30], [31].

The HyS I–V curves and the IGBT/MOSFET current sharing can be analytically derived, as presented in Section III, from the single component's ON-state characteristic and (12)–(15). The analytically calculated and the experimentally measured I–V curves and current sharing are compared in Figs. 6 and 7, where it can be seen that the analytical equations provide a fair accuracy.

2) Switching Losses: The switching performances are characterized by inductive DPT, as illustrated in Fig. 4(a). Various tests have been performed, investigating the effect of temperature, turn-on and turn-off delays, and the losses sharing between IGBTs and MOSFETs in the HySs. The dc voltage V_{dc} is kept to 600 V, while different current points are achieved varying the inductance value and the pulsewidth. An example of the DPT waveform for the alternative HyS is shown in Fig. 9. After the deskew of the measurement probes, the switching losses can then be calculated by multiplying the voltage and current waveforms during the switching event, as detailed in the datasheets of the components [24], [25].

The turn-on and turn-off delays, d_1 and d_4, have been proved in the previous literature to strongly influence the switching performances of HySs. At the turn on, a small or even null delay between MOSFET and IGBT leads to minimized overall turn-on losses since both devices offer a path for the reverse recovery current and, therefore, shorten the turn-on time and reduce losses. This trend is also confirmed in the performed experiments, as possible to see in Fig. 10(a). Regarding the turn off, instead, a longer delay, in the range of 1–2 μs, is found to be the most suitable to reduce the turn off losses, as shown in Fig. 10(b). This comes from the fact that a long delay allows the IGBT to be switched OFF with ZVS. However, after switching OFF the IGBT, the MOSFET conducts the full current, creating additional conduction losses. Therefore, long

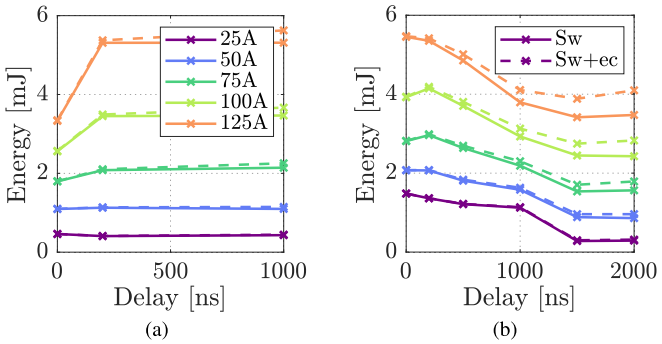

Fig. 10. HySs (a) turn-on and (b) turn-off switching energies (sw) and extra conducton (ec) losses varying the switched current and the MOSFET-IGBT delays d_1 and d_4.

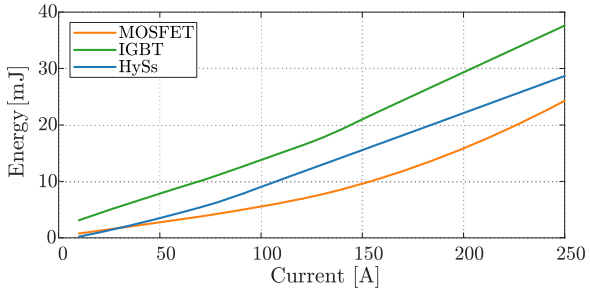

Fig. 11. Switching characteristics of HySs and Si IGBTs and SiC MOSFETs derived through DPT at $T_j = 25$ °C, $V_{\text{dc}} = 600$ V, and $R_g = 4\ \Omega$.

turn-off delays are penalized from these additional conduction losses, and so the optimal turn-off delay, for the considered components, has been found to be equal to 1.5 μs, a value compatible with the one reported in other studies [32]. In these conditions, simultaneous turn on and 1.5 μs delay for turn off, the switching losses are concentrated in the MOSFETs with the IGBT operated in soft-switching. After all, HySs position themselves very well compared with single-technology Si and SiC switches, as indicated in Fig. 11. Both HySs can significantly reduce switching losses with respect to Si IGBTs; however, full SiC MOSFETs still exhibit the best switching performances.

3) Parasitic Inductance Effect in the mcHyS: The mcHyS concept, presented in Fig. 1, requires two additional switching events, defined by d_2 and d_3. These have been tested to be lossless since they happen when the switch is already conducting, and therefore, the voltage across the switch is in the order of few volts, as it can be seen in Fig. 9. This soft-switching condition is maintained when the parasitic inductance between MOSFET and IGBT is very low so that the current commutation between the two switches occurs smoothly, as can be seen in Fig. 12(a), where the commutation inductance of the testing setup, indicated by the red area in Fig. 13, is estimated to be 50 nH. However, if the commutation inductance is increased, the voltage across this can force the conduction of the upper diode and the rise of the voltage across the switch, as possible to see in Fig. 12(b), where the commutation inductance of the setup, indicated by the blue area in Fig. 13, is increased to 140 nH. This voltage spike introduces additional switching losses. Therefore, a low-inductive commutation path between

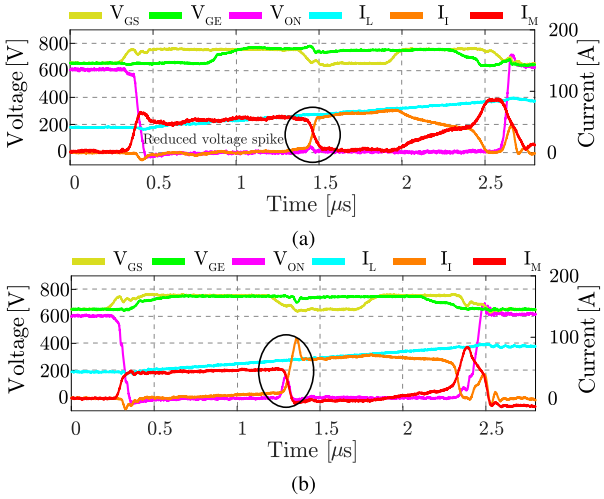

Fig. 12. Experimental verification of the influence of parasitic inductance on switching behavior of hybrid switches: (a) low-inductive commutation path, estimated to 50 nH, and (b) high-inductive commutation path, estimated to 140 nH.

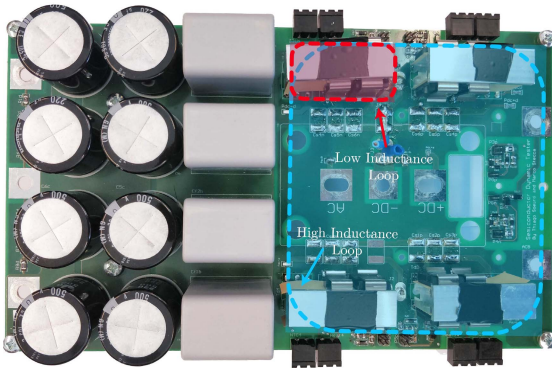

Fig. 13. Large (blue) and low (red) inductance commutation loops between parallel switches in the experimental prototype.

the SiC MOSFET and Si IGBT is fundamental in HySs. Furthermore, no influence of d_2 on the switch turn-on losses, dependent instead on d_1, has been found. Hence, d_2 and d_3 can be set very small so as to avoid ec losses in the MOSFETs.

4) Common-Mode EMI: The conductive EMI of a grid-connected converter is related to the switched terminal voltages' amplitude and to switching transitions where dv/dt is particularly relevant for common-mode EMI. The switch terminal voltage amplitude is defined by V_{dc} and the selected circuit topology. Therefore, the main switching transitions and the amplitude of the terminal voltages will be defined by the circuit topology. Regarding dv/dt of the terminal voltages, as shown in Figs. 9 and 12, only the first and last switching events of the SiC MOSFET in a mcHyS have an influence on the voltage across the switch and the equivalent terminal voltage since the other switching transitions within the pulse period are functional switching events, so as to shift the current conduction from the SiC MOSFET to the Si IGBT, and vice versa. Therefore, the voltage across the switch is driven by the first turn on and the last turn off of the SiC MOSFET, and so the dv/dt at the mcHyS output terminals is

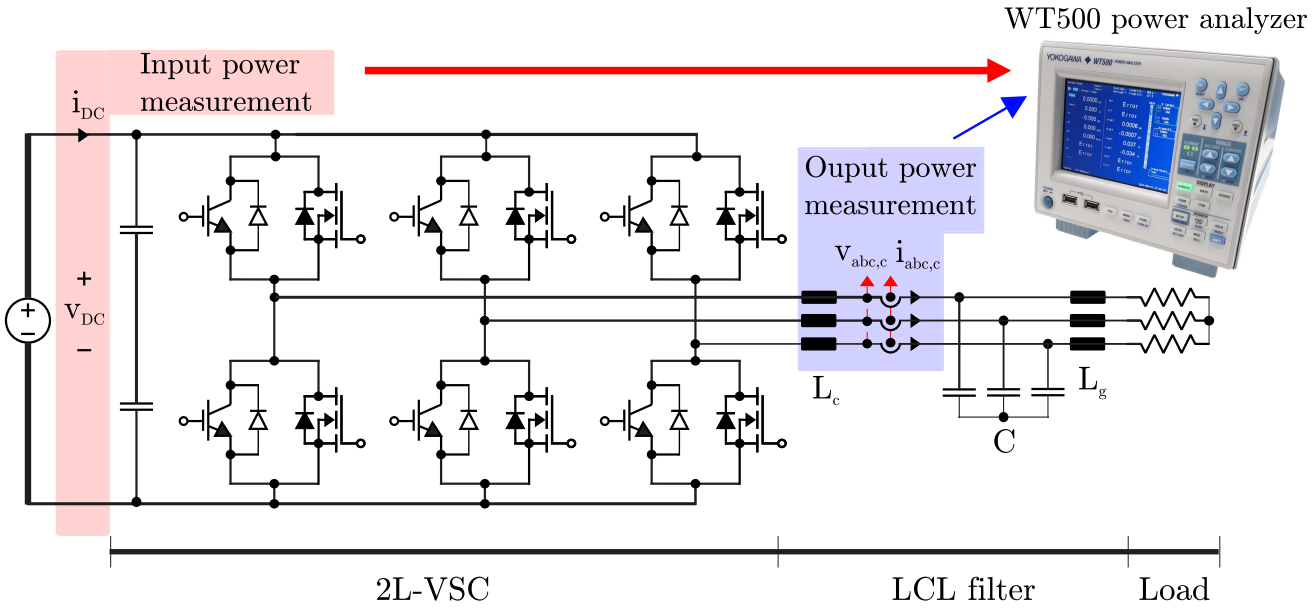

Fig. 14. Circuit schematic of a 2L-VSC operating as inverter supplying a resistive load. The connection points for the efficiency measurements through the WT500 power analyzer are highlighted.

Fig. 15. Prototype of the 10-kW 2L-VSC used for the efficiency testing of the mcHyS with an LCL filter in the bottom.

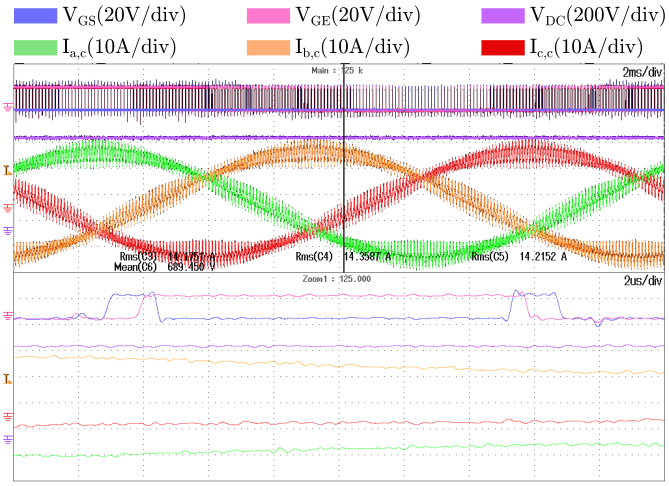

Fig. 16. Waveforms of a mcHyS-based 2L-VSC supplying a resistive load. The switching pattern of the mcHyS can be distinguished in the zoomed bottom area of the figure; the gate signals of the SiC-MOSFET and the Si-IGBT are shown with the blue and pink waveforms, respectively.

driven by the switching speed of its SiC MOSFET. Hence, the mcHyS shows similar performances to the pure SiC MOSFET solution. Overall, the pure Si IGBT solution is the one with lower high-frequency common-mode noise due to the slower switching transitions [33].

5) Efficiency Testing of a 10-kW 2L-VSC: After the experimental characterization of the mcHyS, its efficiency has been benchmarked versus pure technology switches when implemented in a 10-kW three-phase 2L-VSC operating as an inverter supplying a resistive load. The circuit schematic of the 2L-VSC is illustrated in Fig. 14. The 10-kW 2L-VSC prototype is shown in Fig. 15, with, at the bottom, the output LCL filter used to interface the VSC with the resistive load. This 10-kW VSC could be used as a power electronic building block (PEBB) for a 100-kW unit; however, here, the VSC is optimized only for verifying the advantage of the system in the 2L-VSC inverter application. Nonetheless, the performances should be similar in terms of efficiency.

The mcHyS switching waveform during the inverter operation at 10 kW is shown in Fig. 16, where the VSC three-phase converter side output currents are indicated with the green, orange, and red waveforms, and the gate signals of the mcHyS MOSFET and IGBT with the blue and pink signals. The modulation pattern of Fig. 1 can be recognized in the zoomed-in lower part of Fig. 16. Furthermore, the dc voltage waveform is displayed in purple.

TABLE II

SWITCH COST AND MEASURED EFFICIENCY OF A 10-kW 2L-VSC ASSEMBLED WITH VARIOUS SWITCH TECHNOLOGIES [34]

Parameter	Si-IGBT	mcHyS	SiC-MOSFET
Single switch cost [€]	5.53	16.48	21.90
Cost ratio to Si-IGBT [p.u.]	1	2.98	3.96
2L-VSC efficiency at 10kW [%]	98.19	98.56	99.00
Loss reduction to Si-IGBT [%]	-	-37.45	-83.23

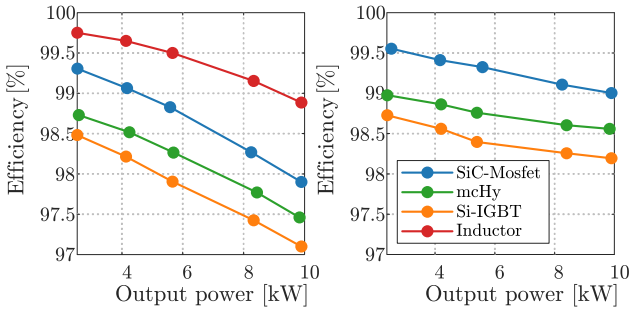

Fig. 17. (a) Measured efficiency of a 10-kW 2L-VSC and of the converter side inductor, assembled with different switch technologies, and calculated efficiency of the inductor at various power, and (b) derived VSC efficiency.

Three different switch configurations have been benchmarked: two pure switch technologies, the Si-IGBT and SiC-MOSFET, and the mcHyS. The switches are selected to have comparable rated continuous collector/drain current at 100 °C. The IKQ40N120CH3 Si-IGBT, rated for 40 A, from Infineon has been selected. Two SCT3105KL SiC MOSFETs, rated 17 A, from Rohm Semiconductors have been paralleled to assemble the SiC-based switch. Finally, the mcHyS has been set up paralleling an IKQ40N120CH3 Si-IGBT, rated for 40 A, and one SCT3105KL SiC MOSFETs, rated for 17 A. Considering the cost figures from components distributors, the costs of a single switch are compared in Table II [34]. It can be seen that the pure SiC-MOSFET solution is nearly four times more expensive than the pure Si-IGBT, while the mcHyS provides a tradeoff solution with triple the IGBT price.

The efficiency tests have been performed with an input dc voltage of 685 V, an output ac rms voltage of 230 V, a modulation index of 0.95, and a 10-kHz switching frequency. An LCL filter is placed between the VSC and the load resistors to filter the current harmonics, as required by the grid connection standards. The LCL filter is assembled with the commercially available 750343810 inductors from Wurth Electronics rated 340 mH both in the converter and the grid side, L_c and L_g, and 9.9-μF capacitance, C. The efficiency, evaluated through the Yokogawa WT500 Power Analyzer, has been measured between the dc side of the VSC and the converter side inductance of the LCL filter, L_c. In this way, both the losses of the 2L-VSC and L_c are measured. The power analyzer connection after L_c has been selected to ensure that the efficiency measurement has high accuracy since the switched voltage at the output of the VSC has very high dv/dt and cannot be properly measured by the power analyzer, while, after L_c, the voltage has a more sinusoidal shape with much lower dv/dt than that the WT500 power analyzer can accurately measure. In Fig. 17(a), the measured efficiency of the three-switch configuration in five operating points is shown. In addition, the losses in the converter side inductors are calculated by evaluating the ac winding losses, proximity effect losses, and core losses through the methods described in [35]. The ac and dc resistances have been measured through the Agilent 4294a Impedance Analyzer, while the Steinmetz parameters are derived from the datasheet of the inductor's core material. The calculated inductor efficiency for different power flowing through it is also shown in Fig. 17(a).

Finally, given the measured efficiency of the setup of Fig. 14, VSC $+L_c$, and the calculated losses of L_c, it is possible to provide a close estimate of the semiconductors' efficiency, as plotted in Fig. 17. The pure SiC MOSFET switch, as expected, provides the most efficient solution. Furthermore, the efficiency gain of mcHyS with respect to the pure Si-IGBT is remarkable, positioning itself as a good tradeoff between Si-IGBT and SiC-MOSFET. As summarized in Table II, the mcHyS allows a 37.45% reduction of power losses with respect to the IGBT at 10 kW.

V. CHIP AREA AND COST OPTIMIZATION

In HySs, the current ratio between the SiC MOSFET and Si IGBT defines not only the current sharing behavior and, thus, the performance of the switch but also its cost. A low-current ratio, in fact, would result in a small SiC chip area and, therefore, lower switch costs since the SiC devices are by far more expensive than their Si-based equivalents. However, a small chip area leads to worse conduction and thermal performances. On the other hand, a too high current ratio could result in over dimensioning the SiC area and, thus, loses cost-competitiveness versus the full Si IGBT-based switches. In this context, optimizing the Si and SiC chip area ensures that both technologies are properly utilized, and the switch cost is optimized [12]. The chip area optimization consists of finding the minimum necessary Si and SiC chip areas of each switch so that the semiconductors' thermal limitations are not exceeded, which means a maximum junction temperature of 150 °C.

Therefore, in this section, the semiconductor chip area optimization of a grid-connected 100-kW 2L-VSC is presented. A low line-to-line ac voltage, $V_{\mathrm{ac,ll}}$, of 400 V, a dc-link voltage, V_{dc}, of 900 V, and a switching frequency, f_s, of 10 kHz are considered. The analysis here presented is based on the analytical equations provided in Section III, on the experimentally derived switching energies, as illustrated in Section IV, on datasheet values from semiconductor manufacturers [24]–[26], and on the cost figures from components distributors [34].

Power semiconductors ON-state resistance r_{on} and junction to case thermal resistance $R_{\mathrm{th,jc}}$ are generally modeled following an inverse correlation with the chip area A_c, as [36], [37]

$$r_{\mathrm{on}} = \frac{x}{A_c} \tag{24}$$

$$R_{\mathrm{th,jc}} = M \cdot A_c^{-l}. \tag{25}$$

The p-n junction barrier voltage of IGBTs and diodes instead depends on its manufacturing technology, not on the device chip area.

TABLE III

PARAMETERS FOR THE CHIP AREA ANALYSIS FROM DATASHEETS [24]–[26] AND EXPERIMENTAL MEASUREMENT

	Parameter		Si IGBT	Si diode	SiC MOSFET
Chip area	A_i	mm^2	20-70	10-60	2-20
Conduction	x_i	$^{m\Omega}/_{mm^2}$	723	233	357.3
	V_{ce}	V	0.9	1.05	-
Turn on/[1]	$m_{s,i}$	mJ/mm^2	-0.134	0.0814	-0.058
Reverse Rec	$q_{s,i}$	mJ	11.29	1.7456	1.945
Turn off [1]	$m_{s,i}$	mJ/mm^2	0.018	-	-0.033
	$q_{s,i}$	mJ	2.977	-	0.882
Thermal	M_i	-	6.558	3.022	1.585
	l_i	-	0.826	0.491	0.705
Cost [2]	$m_{c,i}$	€/mm^2	0.2	0.15	4.256
	$q_{c,i}$	€	2.846	0.827	-5.264

[1] at 50A/600V.
[2] for Si IGBT and Si diode referred to bare dies, while for SiC MOSFET to TO-247 packaged, subtracting the packaging cost (cf. [38]), due to the unavailability of bare die cost information.

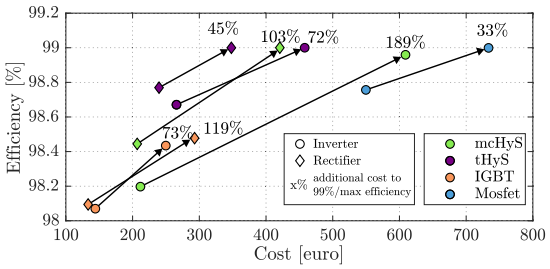

Fig. 18. Semiconductor chip costs and efficiency design space for different switch configurations that satisfy the thermal limits during operation at full power in a 2L-VSC working as inverter and rectifier. The percentage shown is related to the incremental cost needed to bring the minimum cost designs to efficiency of 99% or the maximum efficiency.

The switching losses and chip area can be correlated with piecewise linear functions as a function of the switched current. However, to provide a fair chip area analysis, it has to be considered that generally larger chips are switched faster through smaller gate resistances [24], [37], [39], [40]. Therefore, the switching losses are first to be scaled to have a fixed value of gate resistance per mm^2 of semiconductor area, according to the suggested values from the manufacturers, and then interpolated. The switching losses' relation with chip area can then be modeled as

$$E_{sw}(A_c, I, V) = m_s(I, V) \cdot A_c + q_s(I, V). \tag{26}$$

In addition to the performance indicators, the semiconductor cost can be expressed proportionally to its chip area and linearized in the form of

$$C = m_c \cdot A_c + q_c. \tag{27}$$

The fitting coefficients of (24)–(27), as listed in Table III, have been derived consulting the manufacturer's datasheet, the components distributors prices, and the experimentally derived results presented in Section IV.

The minimum cost chip area configurations are then calculated for a 2L-VSC, IGBT-based, MOSFET-based, and HyS-based, designed to operate as an inverter or a rectifier. The operation mode influences the conduction losses, e.g., the

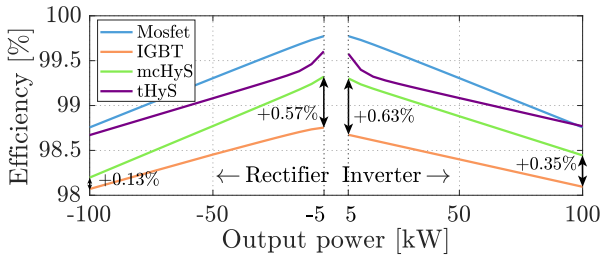

Fig. 19. Semiconductor efficiency of the switch configurations of Fig. 19 varying the output power operating as inverter and rectifier 2L-VSCs. The selected designs are shown in Fig. 18 and represent the chip area optimized for minimal cost.

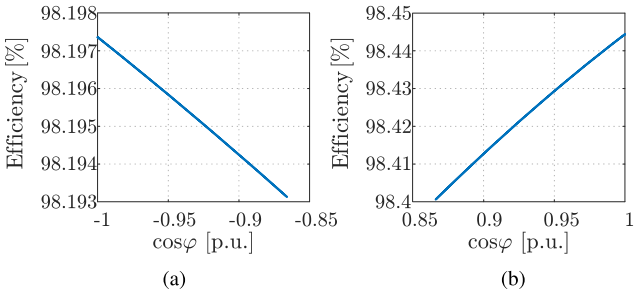

Fig. 20. Semiconductor efficiency of a mcHyS-based 2L-VSC designed as (a) rectifier and (b) inverter operating at rated apparent power and varying the power factor.

rectifier mode leads to a higher reverse conduction current in the switches. These are plotted versus their efficiency in Fig. 18, where it can be noted that the IGBT-based switch, as expected, provides the cheapest solution in both operating modes. In the same figure, the designs that reach 99% semiconductor efficiency or, in the case of the IGBT, the maximum efficiency designs are also plotted, so as to show the required cost increase to reach such efficiency value. The mcHyS minimum cost solution shows relatively low costs compared to its full SiC MOSFETs equivalent. The tHyS still provides a cheaper solution than the pure SiC MOSFET one; however, since the SiC MOSFET is also used for conduction, it requires a larger area than the mcHyS and, thus, becomes more expensive. For high-efficiency designs, $\eta \geq 99\%$, the tHyS shows low costs, lower than mcHyS, and full SiC MOSFETs. Furthermore, in Fig. 19, the minimum cost configurations' efficiency is plotted for various power outputs. Overall, at low power, the efficiency gain of HySs and MOSFETs versus the IGBT-based solution is remarkable with an efficiency gain of the mcHyS of up to 0.6% with respect to the IGBT. Grid connection standards typically require VSC to support the grid voltage with reactive power; therefore, it is important to consider the standard required power factor, typically 0.9, in the VSC design [41]–[43]. In Fig. 20, the efficiencies of mcHyS-based 2L-VSCs designed as an inverter and a rectifier are shown to varying the power factor when operating at rated apparent power. It can be seen that the efficiency drops slightly when more reactive power is generated; nonetheless, it remains satisfactory.

In this section, the semiconductor costs of various switch technologies have been considered. Nevertheless, the semiconductor die is not the only cost factor. Other elements are, for

example, the packaging, gate driving and protection circuit, and digital controller cost.

A fixed cost disadvantage of HySs versus the pure technologies is found on the gate-driving circuits. Such switch assembly, in fact, requires two separate gate-driving circuits per single switch since the Si-IGBT and SiC-MOSFET are controlled separately, as detailed in Fig. 1. Nonetheless, commercial dual-channel digital isolators can be purchased with similar costs to their single-channel counterparts, i.e., the ADUM1100 and ADUM1200 series. Therefore the extra costs in the dual-channel gate driver of the mcHyS consist of the two buffers required instead of one, which are a relatively cheap component, i.e., the ZXMC4559DN8. Regarding all the remaining previously mentioned elements, the HySs do not require higher fixed costs or significantly higher complexity. Packaging costs can be assumed to be constant between the switch technologies. The current implementation of HySs is based on paralleling separate discrete Si- and SiC-based devices [17], [19]; therefore, there are no added packaging costs for HySs with respect to single-technology switches. Furthermore, also, if packaged in a power module, there would not be significantly different packaging costs since multidevice packaging technology is already mature, as most high-power semiconductors' modules are assembled with multiple dies in parallel [23]. This is particularly true in the case where the die attachment and bond-wiring technologies can be the same for both Si and SiC, e.g., similar die sizes.

The protection of the switch can be ensured through several ways, depending on the switch short-circuit withstanding time. Si-IGBT generally can withstand short circuits for a longer time, up to 8–10 μs; therefore, the desaturation method, implemented in the gate driver, is the most commonly used protection systems [44]. SiC-MOSFETs, instead, require a faster clearing time, in the order of 1-2 μs, which is quite challenging to achieve through the desaturation method. Therefore, other protection systems have been studied, such as di/dt measurement through Rogowski coils or direct switch current measurement [44], [45]. In this context, HySs have the same requirements as the pure SiC counterparts.

The digital controller, which is typically used for generating the PWM signals of the converter with a single switch, can be used also for the control of HySs-based converters. The gate signals, in fact, are typically generated through a counter compare technique, i.e., by comparing a value, which defines the switch duty cycle and varies each switching period, with a triangular carrier. In the same way, the gate signals strategies of a HyS can be generated, using an additional counter compare, shifted from the first counter compare accordingly to the delays between the IGBT and MOSFETs switching transitions. The implementation of the mcHyS PWM pattern in a TI μcontroller is shown in Fig. 21, where it can be seen how using two counters compares the modulation signal of the mcHyS can be generated in the high-resolution PWM module.

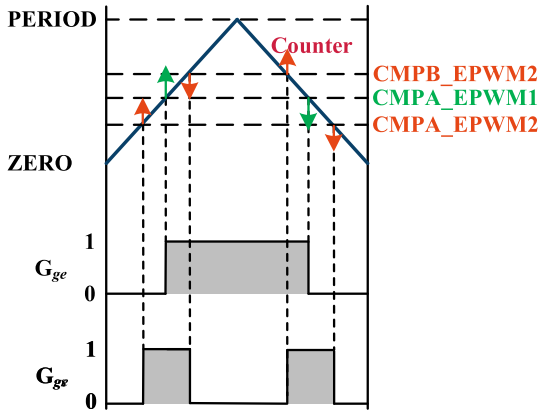

Fig. 21. Implementation of the mcHyS PWM in a digital controlled.

VI. Applications in VSCs

The particular characteristics of HySs make them valuable candidates for the utilization of power electronics converters for multiple applications. As shown in Sections IV and V, both HyS concepts exhibit excellent switching performances and lower cost than pure SiC MOSFETs; furthermore, tHySs have also low conduction losses at low partial load, both in forward and reverse conductions. This occurs due to the fact that only the SiC MOSFET will be conducting, since to the junction barrier voltage of the Si IGBT, during forward conduction, and the Si diode, during reverse conduction, will force the current to flow only through the MOSFET channel, as detailed in Section III. Nonetheless, the SiC MOSFET exhibits the lowest conduction losses at low partial load. In this section, the performances of HySs are compared with the pure Si and SiC switches when implemented in 2L-VSC performing a specific load profile that reflects different applications of the converter. The minimum cost designs illustrated in Fig. 18 are considered for the following study, as reflecting the goal of competitive business. The selected applications consist of a PV inverter, an EV FCS converter, and a BESS converter, all rated with the specifications previously used for the chip area analysis. These applications are deployed in The Netherlands.

A. PV Central Inverter

PV energy is a mature and consolidated application of power electronics converters. In such systems, 2L-VSCs are widely applied as central inverters [46], interfacing the strings' MPPTs with the ac grid. A solar inverter's load profile is inherently affected by the PV plant's location since the solar irradiation on the ground is strongly influenced by the geographical location.

B. EV Fast Charging Station

Fast charging of EVs is a rising application of power electronics converters. In this application, a high-power 2L-VSC is a well-suited circuit topology for interfacing the ac grid with multiple isolated dc–dc battery chargers connected at the dc side. The profile used for the study, provided by experts from a Dutch DSO, consists of the aggregation of the measured profiles of two 50-kW chargers during one year.

C. BESS Providing Primary Frequency Regulation

Primary frequency regulation (PFR) using grid-connected BESS is another growing area for power electronics

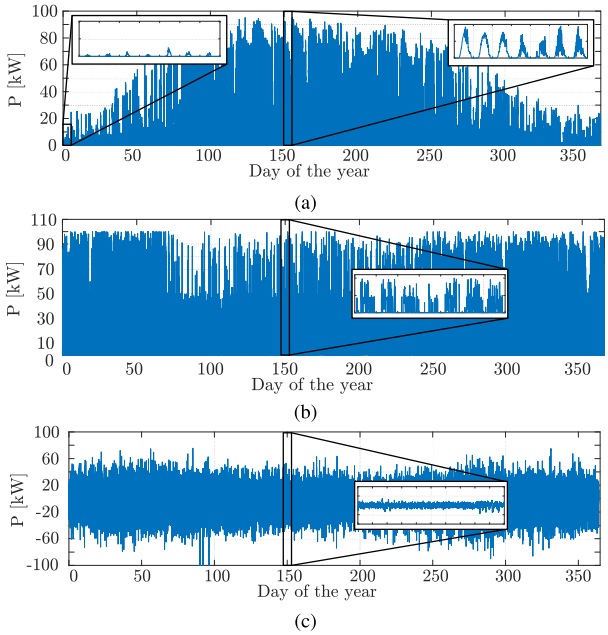

Fig. 22. Yearly mission profiles of a 100-kW 2L-VSC used as (a) PV central inverter, with zoomed-in view two weeks of low and high solar irradiation, (b) FCS grid-connected converter, with zoomed-in view one week, and (c) grid interface for a BESS providing frequency regulation, with zoomed-in view of one day.

converter [31], [47]. PFR consists of responding to the frequency variations of the grid with a droop logic, where the maximum power has to be delivered for deviations higher than ±200 mHz, following the guidelines provided by the Dutch TSO [48]. A typical load profile of a BESS providing PFR would mostly consist of operation at very low partial loads, where HySs perform very well, due to the high inertia and regulating power of the Central European Transmission Grid that effectively limits the frequency variations [49].

D. Switch Comparison

The yearly mission profiles described are shown in Fig. 22. As it is possible to see, the EV charging station has the profile that leads to the highest power utilization, followed by the PV, and the PFR application. On the other hand, the latter has a very high utilization rate, having the BESS working 98% of the considered time. The comparison of the switches for various applications is presented in Fig. 23, where cost and losses of an mcHyS based 2L-VSC is compared with an tHyS-based 2L-VSC when performing different mission profiles. From the figure, it can be noticed that the mcHyS provides a cheaper solution than the typical HyS; however, it also shows slightly worse performances. Overall, HyS provides a substantial cost saving with respect to SiC MOSFETs. On the performance side, the smaller SiC MOSFET of the mcHyS leads to slightly higher losses than the tHyS. Nonetheless, the improvement with respect to the IGBT solution is substantial, almost halving the losses over the yearly profile.

E. Limitation of the mcHyS

To summarize, the analysis presented in this section suggests that HySs are a valid cost–performance tradeoff

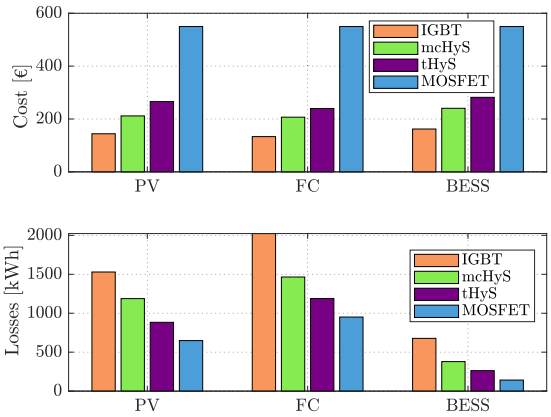

Fig. 23. Semiconductor cost and losses of 2L-VSCs assembled with various switch technologies performing the mission profiles shown in Fig. 22.

alternative to the common Si IGBT and SiC MOSFETs when applied in industrial power electronics applications. HySs can offer various degrees of loss saving and power density increase versus single-technology IGBT-based 2L-VSC. However, HySs, due to the fact that they are assembled through the paralleling of two active devices, presents also some drawbacks with respect to single-technology switches. The main drawback consists of the fact that HyS requires two independent gate-driving circuits per single switch, adding an extra cost versus single-technology switches. However, in high-power applications, the costs of the extra gate driver are generally much lower than the power modules. An additional factor to consider for the mcHyS implementation is the commutation inductance between its elements. As shown in Section IV, a large inductance between the HyS components can be detrimental to its performances. In this context, it is of fundamental importance to consider a minimum distance between IGBTs and MOSFETs in PCB layout when discrete devices are used for mcHyS realization. This issue could be solved by packaging the Si-IGBT and SiC-MOSFET together in a custom power module; however, to the best of our knowledge, such a module is not a commercial product yet.

VII. Conclusion

In this article, the conduction and switching performances of the mcHyS are experimentally characterized and compared with the one of SiC MOSFETs, Si IGBTs, and the tHyS concept. The experimental results proved that the analytical equations given for modeling HySs provided excellent accuracy and showed how HySs position themselves between the pure Si IGBTs and SiC MOSFETs in terms of performances and costs. In addition, a 10-kW 2L-VSC prototype has been assembled to test and benchmarked the efficiency of a mcHyS-based VSC versus a single-technology VSC. Furthermore, it was shown that the two additional switching events of the mcHyS happen in soft switching as long as the commutation inductance is minimized. Afterward, the switches have been compared in terms of chip area and, thus, in costs, upholding that the mcHyS provides a cheaper alternative to SiC MOSFETs and the commonly studied, in the literature, tHyS. HySs have also

been shown valuable candidates for 2L-VSC switches applied in three power electronics industrial applications: PV inverter, EV FCS, and battery storage systems for grid ancillary service.

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