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Silicon Dioxide Photonic MEMS

Chip-to-chip Alignment with Positionable Waveguides

SILICON DIOXIDE PHOTONIC MEMS

CHIP-TO-CHIP ALIGNMENT WITH POSITIONABLE WAVEGUIDES

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus, prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates,
to be defended publicly on
Wednesday, March 6, 2019 at 10:00 o'clock

by

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born in Balk, the Netherlands

This dissertation has been approved by the promotor and the copromotor.

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Front: Photograph of a photonic interposer chip with positionable waveguide array (WGA) mounted and wirebonded to a custom printed circuit board. Photograph by Hans de Lijser.

Back: Scanning electron microscope images of the positionable WGA within a photonic interposer chip. Top: overview image of the positionable WGA. This particular type consists of four suspended waveguide beams, adjacent to which two sets of four actuator beams are located. For more details, see Page 41, Figure 4.7. Middle: detail of the free end of a set of actuator beams. Bottom: detail of the base of a set of actuator beams.

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CONTENTS

1

INTRODUCTION

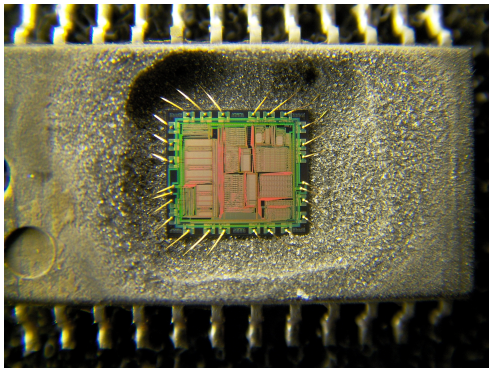
This chapter provides an introduction into the research presented in this thesis. Section 1.1 provides a short introduction into photonic integrated circuits. Although the field of photonic integrated circuits is showing progress, a gap exists between research and commercialization, which is explained in Section 1.1.1. Section 1.1.2 discusses the challenges of photonic alignment, which is the main contributor to packaging costs of photonic devices. Aiming to reduce the costs of photonic alignment, a novel alignment concept is introduced in Section 1.1.3. Section 1.2 provides the objective of the research and the structure of this thesis.

1

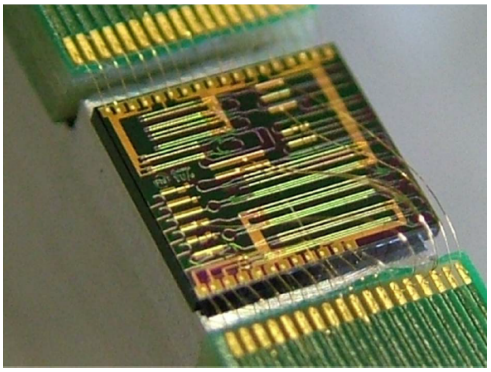
1.1. PHOTONIC INTEGRATED CIRCUITS

ELECTRONIC integrated circuits (ICs) have been around for more than 55 years and due to their enormous impact on our lives, it is hard to imagine today's world without them. ICs are used in nearly all modern electronic devices, such as computers, cars, television sets, and smartphones. Furthermore, the IC is the key element behind valuable inventions such as the internet.

ICs are miniaturized complex electronic circuits, utilizing and controlling the flow of electrons to achieve various functionalities. Nowadays, a vast variety of electronic ICs is available, based on only a small set of basic elements (e.g., transistors, resistors, and capacitors). Electronic ICs are manufactured in highly specialized facilities that are called fabs or foundries, using microfabrication processes. Figure 1.1a shows a photograph of a decapsulated electronic IC.



(a) An electronic audio chip (Yamaha YMF262) that was used in PC soundcards including Sound Blaster 16. The package is decapsulated in order to make the chip visible.



(b) A photonic integrated circuit: prototype of a widely tunable laser. Photograph by S. Latkowski, the Photonic Integration group at TU Eindhoven, used with permission.

Figure 1.1: Examples of (a) an electronic IC and (b) a photonic IC.

Photonic integrated circuits (PICs) were invented over thirty years ago, and they will bring technological advances that are comparable to those of electronic ICs. PICs manipulate an optical signal (photons) instead of an electrical signal (electrons). Optical signals can be transmitted with a higher transfer rate than electrical signals; because optical signals with different wavelengths can be transmitted simultaneously through a single waveguide, optical fibers and waveguides provide a larger bandwidth. Moreover, photonic devices result in reduced propagation losses and produce less heat. Figure 1.1b shows a photograph of a photonic IC.

Similar microfabrication technologies that are used for creating electronic ICs are utilized for the manufacturing of PICs. As a result, large numbers of PICs can be produced simultaneously on wafer-level. Moreover, the scaling laws for PICs are similar to those for electronic ICs, so with increased wafer size and throughput, the square millimetre price will strongly decrease. A significant difference between microelectronics and microphotonics is in the availability of basic building blocks [1]. Most microphotonic integration

technologies are application-specific, which makes transferring designs from one application to another difficult.

1.1.1. GAP BETWEEN RESEARCH AND MARKET

Currently, the number of commercially available PICs as well as devices based on PICs are limited. Large financial investments have been made and research efforts have led to more advanced and more complex PICs. In the field of telecom, indium phosphide (InP) PICs did become a commercial success. For example, Kish [2] demonstrated devices which "are driving the successful commercial scaling of highly integrated InP-based PICs". Apart from the telecom field, the majority of the complex PICs is stuck in a research environment and cannot easily make the transition to a commercial product.

This gap between research and commercialization of PICs results from the high cost of the final photonic device. Currently, three technology platforms are available for photonic applications, for example in multi-project wafer (MPW) runs: InP, silicon (Si), and TriPleX™(proprietary to LioniX International B.V., the Netherlands). Depending on the required functionality, a specific material platform can be more beneficial than the others. For example, optical amplifiers are available in InP, while they are much more difficult to realize in Si or TriPleX. Unfortunately, the different technology platforms are not compatible with each other. As a consequence, for some applications it is currently more beneficial to have a hybrid integration [3] than it is to use a single material platform. In hybrid integration, components from different material platforms are combined to realize the final device.

Different circumstances cause photonic devices based on PICs to be expensive. To start with, the number of PICs being manufactured is simply too low to reach reduced square millimetre costs. Secondly, the field of PICs has developed in such a way that almost every application has its own specific technology. Having a single, standardized technology that can be used for a wide variety of applications would be much more cost effective[1] [1]. Finally, *packaging*, which is the integration of all components in a housing, has become a large contributor to fabrication costs. Therefore, improvement in optical packaging and optical interconnect technology is required to get PICs out of the lab and into the world.

1.1.2. PHOTONIC ALIGNMENT

The packaging process of photonic devices involves the assembly of the components and the realization of the electrical and optical connections. Making the electrical connections is relatively easy, due to the vast experience offered by the established field of microelectronics. The optical connection is less straightforward to accomplish.

The requirements of the optical coupling depend on the components that need to be coupled. The most simple optical coupling case is a fiber-to-chip alignment, for example that of a single mode fiber with a laser diode. In this case, the mode field diameter is relatively large (~10 μm), resulting in a large misalignment tolerance.

When one photonic chip is optically coupled with another photonic chip, it is called chip-to-chip alignment. An example of chip-to-chip alignment can be found in *hybrid*

[1] Initiatives already emerged to transform from separate technologies to a generic technology model, e.g., the European FP7 project Paradigm [4].

packages, resulting from the aforementioned hybrid integration. Hybrid packages combine different types of photonic chips (based on different photonic platforms and material systems) in a single package. The strong mode confinement of the optical channels of photonic chips results in smaller spot sizes and reduced misalignment tolerances compared to the fiber-to-chip alignment case. More details on optical coupling are provided in Section 2.1.2.

Moreover, the complexity of the optical coupling grows with the increasing number of optical ports within photonic devices. Coupling a single channel is less demanding in terms of optical coupling complexity than coupling an array of 32 channels. To put this in perspective, a large amount of photonic devices requires only a single optical port, but multi-channel PICs with up to 48 optical ports are reported in literature [5].

Photonic alignment is traditionally achieved with one of two different principles: passive or active alignment. The distinction between the two is the use of a feedback loop, enabling the monitoring and optimization of the optical coupling. Active alignment relies on such a feedback loop, while passive alignment achieves optical coupling with alignment features, e.g. pedestals, v-grooves or alignment marks. Generally, active alignment is more accurate while passive alignment requires less time. A few alignment approaches use a combination of passive and active alignment to get the best of both worlds. Section 2.1 includes a more detailed review of photonic alignment.

Current alignment approaches for chip-to-chip alignment are not as cost effective as they need to be. Commonly, photonic alignment is achieved with specialized equipment, requiring complex and time consuming manual or semi-manual operations. Increasing the level of automation will make the photonic alignment process more scalable and reliable, similar to what has been achieved in large volume electronics manufacturing.

1.1.3. FLEX-O-GUIDES ALIGNMENT CONCEPT

Flex-O-Guides is an STW funded project that aims to develop technologies for the alignment of multichannel photonic chips to fiber arrays. The project proposes improvements in channel count, alignment precision and automation while radically changing the cost for packaging and alignment. The essence of the technology is an alignment concept which optimally combines passive and active alignment. Also, by implementing the alignment functions within the package using microfabrication technologies, the solution aims for low cost and a high level of automation.

A product case will be used to demonstrate and prove the alignment concept. This case consists of three photonic components: a glass fiber array, a TriPleX interposer chip and an InP PIC. A schematic representation of the photonic alignment assembly is presented in Figure 1.2. The InP PIC is the chip that needs to be optically coupled. The waveguide side of this InP PIC interfaces with the side of the interposer chip that incorporates integrated alignment functionality. The other side of the interposer chip couples to the fiber array, providing an external optical connection.

1.2. OBJECTIVE AND STRUCTURE OF THE THESIS

This thesis work aims to develop a technology for high precision (sub-micrometer), highly automated alignment of multi-channel photonic systems, as part of a generic photonic in-

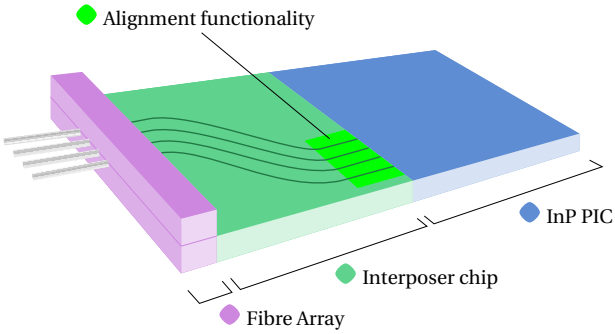


Figure 1.2: Schematic representation of the photonic alignment assembly which is used to demonstrate the proposed alignment concept.

tegration technology platform. The work in this thesis focuses on the integrated alignment functionality of the Flex-O-Guides alignment concept. The pre-alignment of the chips and the final fixing of the waveguides are part of a European follow-up project, PHASTFlex [6].

This thesis is organized as follows. A review of photonic waveguiding, optical coupling, and photonic alignment is provided in Chapter 2. Also, the proposed alignment approach and its main elements – the interposer chip, the InP PIC, and the fiber array – are specified in the same chapter. Chapter 3 explains the fabrication process of mechanically flexible SiO_2 waveguide structures without integrated actuator functionality. By implementing a reinforcing layer during the release stage, the risk of fracturing of the waveguide structures is reduced. Suspended SiO_2 structures are created and are mechanically characterized. In Chapter 4, suspended SiO_2 structures are equipped with integrated actuators to enable out-of-plane positioning. A microfabrication process is developed which includes the special reinforcement method from Chapter 3. The fabricated devices are characterized by measuring the post-release deformation (i.e., without actuation), as well as the deflection resulting from quasi-static and dynamic actuation. The results from Chapter 3 and Chapter 4 are used in Chapter 5 for the design and characterization of a positionable waveguide array. A finite-element model is developed to provide insight in the way the design of the system affects the performance. The finite-element analysis gives guidelines for the design parameters of an optimal positionable photonic waveguide array. Chapter 5 includes experiments to determine the stability over time of the positioning system and mode field profile measurements of partly suspended waveguide beams. The alignment concept is demonstrated by actively aligning three adjacent waveguide beams within a positionable waveguide array with the channels of another photonic chip. Finally, Chapter 6 summarizes the advantages of the realized alignment approach and gives recommendations for future research.

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E. Bitincka, V. Moskalenko, J. Zhao, R. Santos, G. Gilardi, W. Yao, K. Williams, P. Stabile, P. Kuindersma, J. Pello, S. Bhat, Y. Jiao, D. Heiss, G. Roelkens, M. Wale, P. Firth, F. Soares, N. Grote, M. Schell, H. Debregeas, M. Achouche, J.-L. Gentner, A. Bakker, T. Korthorst, D. Gallagher, A. Dabbs, A. Melloni, F. Morichetti, D. Melati, A. Wonfor, R. Penty, R. Broeke, B. Musk, and D. Robbins, *An introduction to InP-based generic integration technology,* Semiconductor Science and Technology **29**, 083001 (2014).

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2

STATE OF THE ART AND CASE DESCRIPTION

The previous chapter introduced the objective of this research and stated the focus of this thesis: the development of a photonic alignment approach. This chapter provides background information regarding photonic alignment and describes the current state of the art. Furthermore, this chapter introduces the configuration of the alignment case that serves as product case for the investigation.

The different types of alignment approaches are reviewed in Section 2.1, and the relevant principles of optical waveguiding and optical coupling are described. Section 2.2 explains the alignment concept proposed in this thesis by means of a product case in which a PIC is aligned with another photonic chip.

Based on
T.-J. Peters, M. Tichem, U. Staufer, *Suspended photonic waveguide arrays for submicrometer alignment*, Proc. SPIE 9133, Silicon Photonics and Photonic Integrated Circuits IV, 913317 (1 May 2014)
(with addition of Sections 2.1.1 and 2.1.2)

2.1. PHOTONIC ALIGNMENT

WITHIN the packaging process, alignment of photonic components is a crucial step. Two categories of alignment approaches can be distinguished: active and passive alignment. Active alignment uses the measured light coupled through the optical path as a feedback signal in order to attain the position with lowest coupling loss. In passive alignment the final position is obtained without monitoring the coupling of light. Usually passive alignment uses alignment structures or alignment marks. Once successfully aligned, whether by active or passive alignment, another challenge is fixing the position of the photonic components without disturbing the alignment. For fixation mostly epoxy attachment, solder attachment or mechanical clamping is implemented. Depending on the attachment method, the alignment might be affected by a post-bonding shift.

Different implementations of alignment approaches have been demonstrated in literature, based on either active alignment, passive alignment or a hybrid form. For example, active alignment and clamping of an optical fiber is achieved using microelectromechanical actuators [1]. Passive alignment with submicrometer accuracy is reported using two photonic chips on a silicon optical bench [2]. Furthermore, alignment of multi-channel configurations is studied utilizing a micromechanical connector [3], a grating coupler array [4], laser adjustment [5] and spot size converters (SSCs) [6]. Current technology for precise photonic assembly employs the use of micromanipulators [7].

Passive photonic alignment is usually a much preferred method over active photonic alignment, because the latter can be time-consuming and costly [8, 9].

2.1.1. OPTICAL WAVEGUIDE

An optical waveguide is used to direct light by guiding it in a specific propagation direction. Optical waveguides rely on a difference in refractive index to provide total internal reflection of optical waves. In the example of an optical fiber, a waveguide core is embedded in a waveguide cladding, the core having a higher index of refraction. Figure 2.1 shows the concept of total internal reflection inside an optical waveguide. Total internal reflection in a waveguide occurs if $n_1 > n_2$ and the angle θ is larger than the critical angle θ_c, which depends on the refractive indices n_1 and n_2.

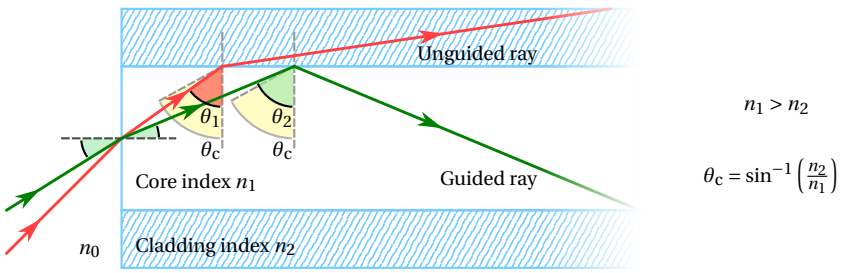


Figure 2.1: Schematic representation of total internal reflection. A ray of light is either unguided or guided in the waveguide, depending on the angle θ.

The model of the reflected ray is only valid if the waveguide diameter is several times larger than the wavelength of the light. For systems with a waveguide diameter in the order of the wavelength, the wave nature of light needs to be taken into account. For specific combinations of waveguide diameter and wavelength, the light is so confined that it travels through the waveguide without reflecting. Waveguides that only allow such a fundamental mode to propagate are called single mode waveguides. The spatial distribution of the optical energy of a light wave guided by a single mode waveguide is given by the Gaussian beam function, as shown in Figure 2.2. A measure for the size of the guided light is the mode field diameter (MFD), which is defined as the width that contains 86.5 % (or $1 - 1/e^2$) of the optical power. Also shown in this figure is w, the half-width of the Gaussian beam. Figure 2.2 shows that the distribution overlaps with the cladding on both sides, which means that a small part of the light travels through the cladding. As a consequence, the MFD is larger than the core diameter. The mode shape as shown in Figure 2.2 is typical for single mode fibers as well as single mode waveguides on PICs.

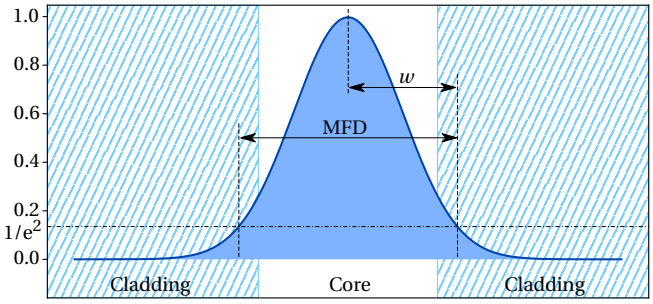


Figure 2.2: The spatial distribution of the optical energy of a light wave in a single mode waveguide.

2.1.2. OPTICAL COUPLING

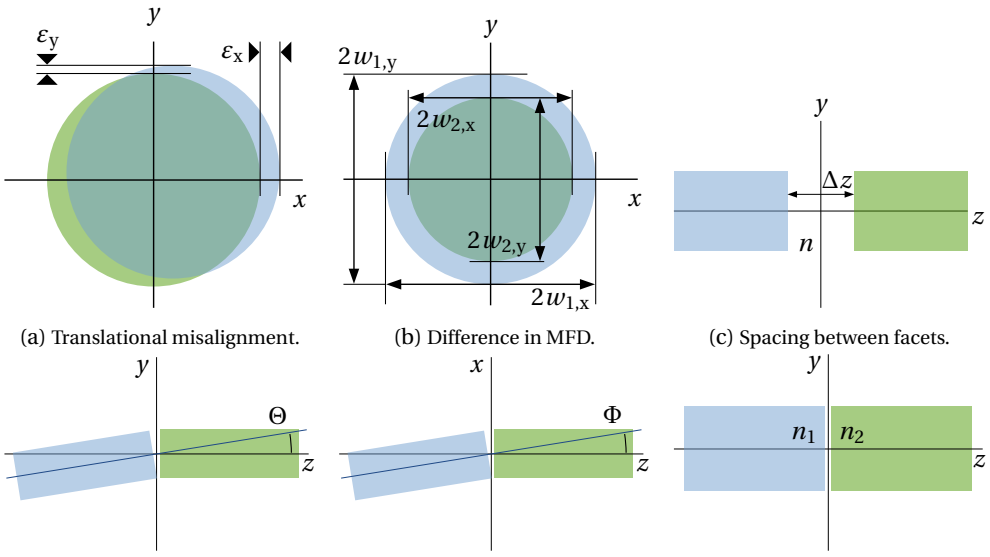
An important, quantifiable factor in optical coupling is the coupling loss, which is preferably as small as possible. For example, in case a specific waveguide is coupled with a larger one, the difference in cross section causes coupling loss. To optimally transfer the optical energy, the overlap of the two mode fields should be maximized. The alignment of Gaussian beams and the corresponding coupling efficiencies have been thoroughly investigated, and analytical expressions are available in literature [10]. Table 2.1, adopted from [11], provides an overview of the most important factors influencing photonic coupling. Figure 2.3 provides visualizations of the different types of misalignment and mismatch.

2.2. ALIGNMENT CONCEPT AND ALIGNMENT CASE

The proposed alignment concept offers high precision alignment of two PICs by using internal alignment functionality and mechanically flexible waveguides, both integrated in one of the PICs. In relation to comparable alignment approaches the proposed alignment concept aims to reach higher accuracy and precision and is designed for increased automation capability to ensure low cost and short assembly times. The proposed concept offers alignment of waveguide arrays making it suitable for multiport PICs. The increase in fabri-

Table 2.1: Factors influencing the coupling efficiency between Gaussian beams

Type	Impact of mode size on coupling efficiency	Measure of coupling efficiency
Translational misalignment	Larger for waveguides with smaller mode sizes	$\eta_\varepsilon = \mathrm{e}^{-\left(\frac{\varepsilon_\mathrm{x}^2}{\left(\frac{1}{2}\sqrt{2}\sqrt{w_{1,\mathrm{x}}^2+w_{2,\mathrm{x}}^2}\right)^2}+\frac{\varepsilon_\mathrm{y}^2}{\left(\frac{1}{2}\sqrt{2}\sqrt{w_{1,\mathrm{y}}^2+w_{2,\mathrm{y}}^2}\right)^2}\right)}$
Angular misalignment	Larger for waveguides with larger mode sizes	$\eta_\mathrm{ang} = \mathrm{e}^{-\frac{1}{4}\left((n_\mathrm{gap}k_0\sin\Phi)^2 w_x^2+(n_\mathrm{gap}k_0\sin\Theta)^2 w_y^2\right)}$
Spacing between facets	Larger for waveguides with smaller mode sizes	Compute width w of diffracted beam and curve radius R of wave front $w(\Delta z) = w_0\sqrt{1+\left(\frac{2\Delta z}{k w_0^2}\right)^2}$ with $k = \frac{2\pi}{n\lambda}$ $R(\Delta z) = \Delta z\left(1+\left(\frac{k w_0^2}{2\Delta z}\right)^2\right)$
Difference in MFD	Proportional to mode size	$\eta_\mathrm{mfd} = \frac{4w_{1,\mathrm{x}}w_{2,\mathrm{x}}w_{1,\mathrm{y}}w_{2,\mathrm{y}}}{(w_{1,\mathrm{x}}^2+w_{2,\mathrm{x}}^2)(w_{1,\mathrm{y}}^2+w_{2,\mathrm{y}}^2)}$
Difference in refractive index	Independent on mode size	$\eta_n = 1-\left(\frac{n_1-n_2}{n_1+n_2}\right)^2$



(a) Translational misalignment.

(b) Difference in MFD.

(c) Spacing between facets.

(d) Angular misalignment in the yz-plane.

(e) Angular misalignment in the xz-plane.

(f) Difference in refractive index.

Figure 2.3: Optical coupling factors influencing the coupling efficiency between two Gaussian beams.

cation costs is limited because most of the functionality is realized on the interposer chip through post-processing, for the most part using existing chip area that otherwise remains

unused. Moreover, standard microfabrication processes suffice for the realization of these functions in the post-processing step.

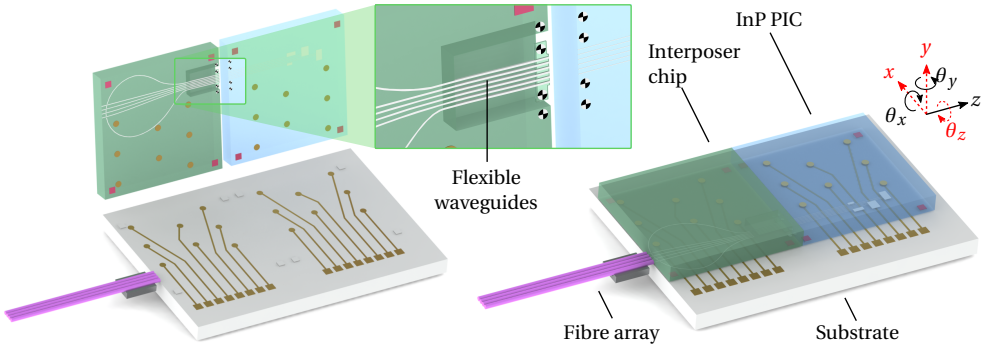


Figure 2.4: Schematic representation of pre-alignment of the assembly. Left: before pre-alignment. The inset shows a close-up view of the partly suspended and flexible waveguide array. Right: the interposer chip and PIC are flip-chip mounted on the substrate. The DOFs aligned within pre-alignment are indicated in black (solid) and the DOFs to be aligned in fine-alignment are indicated in red (dashed).

Indium phosphide (InP) based technology is a leading candidate for complex (multi-port) photonic circuits [12]. If a fiber array is butt coupled to a multiport InP chip, the difference in MFD of the InP waveguides and the fibers causes significant loss of the optical signal. In theory, this problem can be solved by implementing SSCs, but at this moment it is technically very challenging to realize SSCs in InP technology which enable butt coupling to a fiber array with acceptable coupling efficiency. Moreover, matching the pitch of a fiber array will require a significant increase in InP chip area, making the device more expensive. Our alignment approach combines InP-based technology with TriPleX platform technology [13] to have a small InP footprint as well as sufficiently low coupling loss of the optical signal. The TriPleX platform technology offers buried dielectric silicon nitride (Si_3N_4) waveguide structures in a silicon dioxide (SiO_2) cladding with low propagation loss through the full wavelength range from visible to infrared [14, 15]. An advantage of this technology is the ability to design and realize SSCs which convert in-plane as well as out-of-plane.

Three benefits result from positioning an interposer chip based on TriPleX technology between a fiber array and an InP chip. Firstly, the coupling losses are reduced by minimizing the difference in MFD at both interfaces of the interposer chip. Secondly, when a fan-out of the waveguides is implemented on the interposer chip, the pitch of the InP waveguides can be smaller than the fiber pitch, reducing required chip-area and thereby lowering costs. Finally, combining different material technologies in a hybrid package allows implementing additional functionality, and rethinking functional partitioning between the PICs, in order to benefit most from each material platform's characteristics.

While the optical waveguides on the interposer chip are passive so have no need for electrical connections, the microactuators and possibly the fixing mechanism do require electronic control. In our alignment approach, solder bump technique is envisioned to get the interposer chip both electrically and mechanically connected to the substrate. The InP

chip is attached in the same way, mechanically fixing it and creating an electrical connection to power the light transmitter and receiver during the active fine-alignment step.

Submicrometer alignment is achieved in two steps. First, the InP chip and interposer chip are coarsely pre-aligned and then attached to a common substrate (see Figure 2.4). At this stage an alignment precision around 5 µm is sufficient. Flip-chip bonding technology is used to align and mount the chips on the substrate, which is a fast and cost-effective technique offering the pre-alignment accuracy necessary for the subsequent fine-alignment. Second, microactuators fine-adjust the position of the flexible waveguide array to obtain maximum light-coupling and finally the waveguide array is fixed in its final position. The goal is a final misalignment in the submicron region, as will be calculated below. To illustrate the principle of fine adjustment, alignment in the x-direction only is presented in Figure 2.5.

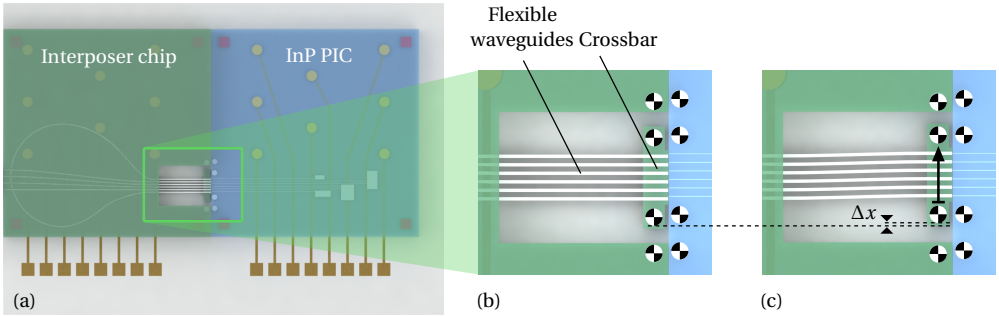


Figure 2.5: Schematic representation (top view) of in-plane fine alignment and fixation of the waveguides. (a) Top view of the interposer chip and PIC after coarse pre-alignment. (b) Close-up view of the flexible part of the waveguides before fine alignment. A small misalignment of the waveguides and alignment marks is visible. (c) Close-up view of the flexible part of the waveguides after fine-alignment. Fine-alignment is achieved by translating the crossbar over a distance Δx in the direction of the arrow (no microactuator is included in this schematic representation).

Since the pitch of the interposer waveguides is defined by photolithography, it can be very accurately realized to be similar to that of the InP waveguides. In order to retain this well defined pitch, the design includes a crossbar located at the free end of the interposer waveguide array. Furthermore, the number of required actuators is significantly reduced by employing a waveguide array with a crossbar. For accurate displacement of this crossbar in the fine-alignment step, microactuators are integrated in the interposer chip.

The alignment configuration of the InP PIC and TriPleX interposer chip will now be evaluated in terms of coupling efficiency. With typical values for the photonic platforms and the equations from Table 2.1, a quantification of the alignment tolerances can be obtained. The refractive indices of the two photonic platforms is different: InP has $n_{\text{eff}} \approx 3.2$ while TriPleX has $n_{\text{eff}} \approx 1.5$. Even if the alignment is perfect, the coupling loss due to this difference in n_{eff} is 0.6 dB in case of direct coupling, and 1.5 dB in case the chips are separated by air. It must be noted that anti-reflective coating can significantly reduce this loss.

To see how sensitive the configuration is to translational misalignments, we calculate what the tolerances must be for a specific coupling loss. The definition of the coordinate

system used here and elsewhere in this thesis is shown in Figure 2.4. We assume an ideal case with the MFD of the TriPleX waveguides matching the MFD of the InP chip. MFD_x = 2.1 µm and MFD_y = 0.96 µm for InP. With such strongly confined modes, the tolerance in x-direction is ±300 nm and the tolerance in y-direction is ±185 nm to obtain 1 dB. In case the application is less demanding and a coupling loss of 2 dB is allowed, tolerances are ±280 nm and ±300 nm for alignment in x and y-direction, respectively. Table 2.2 summarizes these values.

Table 2.2: The calculated tolerances required to achieve 1 dB and 2 dB coupling loss. Three situations are considered: misalignment in x only, in y only, and in x and y simultaneously.

Misalignment (nm)		Coupling loss (dB)
x	y	
504	0	1
0	230	1
300	185	1
714	0	2
0	326	2
280	300	2

Small modeshapes are less sensitive to angular misalignment. Assuming θ_x (or Φ) and θ_y (or Θ) are 1°, the coupling loss due to this combined misalignment is only 0.03 dB. With such low loss, these two degrees of freedom are not critical to obtain good coupling efficiency. However, in (the not very realistic) case of a large number of waveguides and a large waveguide pitch, a misalignment in θ_y will give a strong varying separation distance between the waveguides of the two chips. In principal, rotational misalignment θ_z only influences polarization. But in case of a waveguide array, manipulation of θ_z is required to get all the waveguides in line with the opposite waveguides.

The concept requires z, θ_x and θ_y to be sufficiently aligned during the pre-alignment. As discussed above, θ_x and θ_y are not critical, and are expected to be controlled with sufficient accuracy by the flip-chip bonding technology. Achieving the required z alignment is an important requirement for this technology. Several hundreds of nanometers difference in separation distance can give an extra 1 dB of loss.

Finally, for the fine-alignment, the microactuators must be capable of displacement in x-direction, y-direction and rotation around the z-axis. The goal for adjacent waveguides is a final misalignment smaller than 300 nm, resulting in a maximum coupling loss of 2 dB. The resolution that can be achieved with microactuators is sufficiently high to achieve this desired tolerance. An obvious but important requirement is for the microactuator strokes to be larger than the pre-alignment error in the corresponding DOF.

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3

SUSPENDED SILICON DIOXIDE BEAM STRUCTURES

This chapter focuses on the realization of flexible waveguides in the interposer chip. The interposer chip, based on the TriPleX photonic platform, consists of a ~15 μm thick material stack atop a silicon wafer. This material stack serves as the waveguide material, and consists of Si_3N_4 cores embedded in a SiO_2 cladding. Waveguide beams are locally released from the substrate by removing surrounding material (i.e., material located alongside and underneath the waveguide beam). Due to the fabrication process, in which the SiO_2 is grown on silicon at a high temperature, and the difference in coefficient of thermal expansion, the SiO_2 is subject to compressive stress at room temperature. As a result, during the release of the waveguide from the substrate, the material expands which can lead to fracturing. This chapter describes a reliable method to fabricate >10 μm thick suspended SiO_2 structures. These suspended structures are not only an essential element of the proposed alignment concept, but also important for the development of SiO_2-based MEMS technology in general.

The enabling technology and microfabrication process are explained in Section 3.2. A supporting layer of Si functions as a reinforcing layer during etching and release of the SiO_2 structures, thereby preventing fracturing of the beams. Section 3.3 presents and discusses the results of the proposed Si reinforcement method. In order to demonstrate the method, suspended SiO_2 structures with and without Si support are fabricated. Furthermore, the feasibility of positioning the suspended SiO_2 structures with microactuators is evaluated by estimating the beam spring constants and the beam curvature. Section 3.4 presents the conclusions.

Based on
T.-J. Peters, M. Tichem, *Fabrication and characterization of suspended beam structures for SiO_2 photonic MEMS*, Journal of Micromechanics and Microengineering 25, 105003 (2015)

3.1. INTRODUCTION

SILICON (Si) has been extensively studied and used as a construction material for microelectromechanical systems (MEMS), because of its favorable mechanical and electrical properties. Si is a mechanically strong and elastic material, contributing to reliable micromechanical devices. Moreover, Si is stable up to high temperatures and has a tunable electrical conductivity.

However, Si is not necessarily the material of choice for microsystems with optical functionality. Other material systems deliver better photonic performance. An example is a stoichiometric silicon nitride (Si_3N_4) waveguide core encapsulated in a silicon dioxide (SiO_2) cladding [1], showing a propagation loss which is lower than that of a Si waveguide. A similar $Si_3N_4-SiO_2$ waveguide configuration is applied in the TriPleX technology [2]. The means are available to realize functionally complex photonic integrated circuits (PICs) based on these and other material systems.

The waveguides in PICs are mostly buried in or created atop a solid layer. If suspended and mechanically flexible waveguide beams can be created, this will open up entirely new possibilities, combining the advantages of MEMS with the preferred optical performance of photonic material systems. Chapter 2 introduced the concept for the alignment of the waveguides of two PICs, based on suspended TriPleX waveguides and integrated MEMS actuators. This alignment concept and comparable SiO_2 photonic MEMS applications require the development of fabrication processes for realizing mechanical structures in SiO_2. This chapter addresses the challenges in creating such structures and proposes a method for their high-yield fabrication.

The fabrication of structures for SiO_2 photonic MEMS is challenging because of the thickness of the layer. The use of SiO_2 as a construction material which at the same time has good optical properties requires thick SiO_2 cladding layers. A total thickness of approximately 15 µm is required for a $Si_3N_4-SiO_2$ photonic waveguide with acceptable propagation loss. This thickness differs from the thickness required for other uses of SiO_2. For example, when used as a dielectric material or as a (local) doping/etching mask, a thin (< 1 µm) layer of SiO_2 suffices.

The principle of suspended photonic waveguides has already been demonstrated in literature. Suspended waveguides have been fabricated using various materials, e.g., polymer [3], InP [4], and Si [5]. While some research groups have described the release of SiO_2 structures, the obtained structures have different properties than we aim for. Carpenter et al. [6] reported on the fabrication of suspended SiO_2 cantilevers, but the structures were produced by flame hydrolysis deposition instead of thermal oxidation. Ollier [7] described the fabrication of suspended SiO_2 structures made of PECVD SiO_2 instead of thermal SiO_2. The SiO_2 cantilevers fabricated by Chen et al. [8] are in the thickness range from 4 µm to 6 µm and therefore do not meet our thickness requirements. It is important to mention that both Ollier [7] and Chen et al. [8] included additional lateral beams in their design in order to reduce stress-induced out-of-plane bending of the structure. Wang [9] successfully released 2 µm thick thermal SiO_2 with no additional lateral beams. The suspended SiO_2 structures were instead supported by a 28 µm to 38 µm thick layer of Si. Reports on suspended structures realized out of SiO_2 with a thickness around 15 µm were not found in literature.

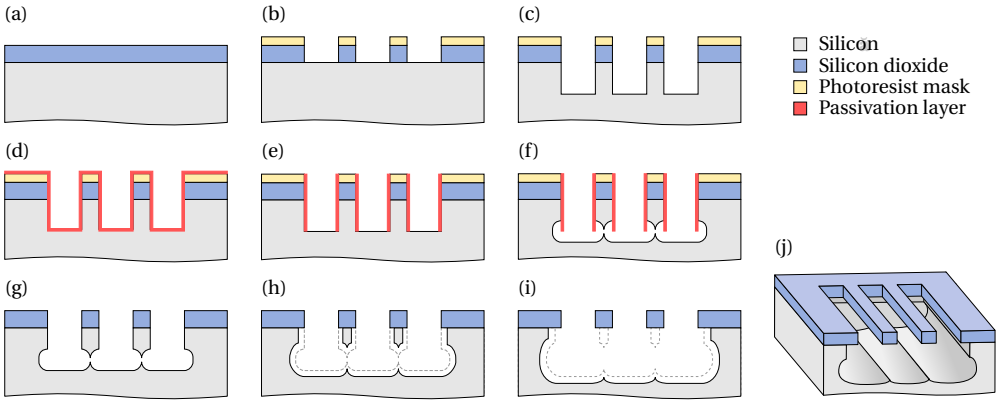


Figure 3.1: Fabrication steps for the release of reinforced structures. (a) Starting material: Si wafer with thermal SiO_2. (b) Photoresist patterning and plasma etching through SiO_2. (c) DRIE of Si. (d) Deposition of passivation layer. (e) Removal of the passivation layer from the trench bottom. (f) Isotropic plasma etching of Si. (g) Removal of the passivation layer and photoresist mask results in released SiO_2 beam structures with Si support. Optionally, the supporting Si can be removed by additional steps: (h) Isotropic plasma etching of Si. (i) Continued isotropic plasma ething of Si. (j) 3D representation of the end result: suspended SiO_2 structures.

3.2. TECHNOLOGY

3.2.1. FABRICATION PROCESS

The realization of suspended SiO_2 – Si (henceforth referred to as bilayer) beam structures is accomplished by plasma etching both the SiO_2 and the Si. Plasma etching is preferred over wet etching for releasing a suspended structure, to prevent stiction due to surface tension driven adhesion.

In this chapter, we describe the release of thermal SiO_2 structures. The results of releasing suspended TripleX structures are expected to be comparable to those obtained with thermal SiO_2 structures, since the dominant factor leading to beam fracturing is the mean residual stress. Thermal SiO_2 has a compressive mean residual stress resembling that of the TriPleX stack.

Figure 3.1 presents the steps of the single mask fabrication process. The starting material is a Si wafer with a thickness of ~525 µm and a 14.8 µm thick thermal SiO_2 layer. A 6 µm-thick spray-coated layer of *AZ9260* photoresist was applied on top of the SiO_2 and patterned. The design of the photolithography mask allows control over in-plane dimensional parameters like the width and the length of the waveguide beams. The SiO_2 was etched using a *Drytek Triode 384T* with C_2F_6 - CHF_3 chemistry (Figure 3.1b). After etching through the SiO_2 layer, the photoresist mask was not removed but was used once more to etch trenches in the Si (Figure 3.1c). From this fabrication step on, an *SPTS Omega i2L Rapier* deep silicon etcher was used, unless stated otherwise. A trench depth of ~70 µm was realized by deep reactive ion etching (DRIE) and the trench width varied from 30 µm to 100 µm.

After etching the trench in the Si, a ~1 µm thick passivation layer was deposited (Figure 3.1d), which was then locally removed from the trench bottom by directional ion bom-

bardment (Figure 3.1e). The CF_X passivation layer was deposited using C_4F_8 gas. SF_6 gas and 75 W platen RF power were applied during the trench bottom removal. With the Si sidewalls protected, the Si underneath the beams was then removed by isotropic plasma etching (Figure 3.1f). During this etch, SF_6 was used without applying any platen RF power. Removal of the passivation layer and photoresist mask by an O_2 plasma in a *Tepla 300* plasma system resulted in suspended bilayer structures (Figure 3.1g). As long as bilayer structures are required, no further processing is needed. In this study, the supporting Si was completely removed by performing additional fabrication steps. Another isotropic plasma etching step with SF_6 gas was performed for 60 s, reducing the Si reinforcement (Figure 3.1h). All the supporting Si was then removed by a final isotropic plasma etch of 210 s using SF_6 (Figure 3.1i). These two separate isotropic Si etch steps were performed to enable intermediary measurements.

The advantage of Si reinforcement can be demonstrated by comparing the release of a beam structure with and without Si reinforcement. Figure 3.2 illustrates the state at a certain moment during the underetching of a SiO_2 beam structure without Si reinforcement. In this figure, the beam structure is almost entirely suspended. Only at the beam crossings, the SiO_2 is attached to the Si wafer. Due to the geometry of the beam structure, the release of the beams occurs before the beam crossings are released. The three beams, being suspended but also clamped at both ends (at their base and at the beam crossings), are actually doubly-clamped beams. These SiO_2 bridges, no longer supported by any Si, will expand and buckle, leading to stress concentrations and possibly beam failure.

Figure 3.3 illustrates the state at the same moment during the underetching of a SiO_2 beam structure using Si reinforcement. Again, the beam structure is suspended everywhere except at the beam crossings. However, the created bridges are bilayer structures instead of SiO_2 bridges. The supporting Si limits the expansion of the SiO_2, which results in lower stress concentrations, reducing the chance of beam failure during fabrication.

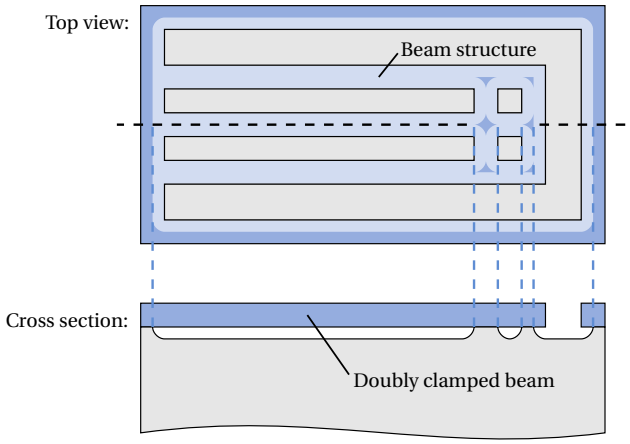


Figure 3.2: Schematic representation of a SiO_2 beam structure during the underetching process without Si reinforcement.

The Si support is only required at a specific stage during the fabrication process, i.e., until the bilayer structure is released. Once the bilayer structure is fully suspended (i.e., when the beam crossings are also suspended), the supporting Si is no longer necessary. Any compressive stress remaining in the SiO_2 will not lead to fracturing when the supporting Si is removed since restrictions of longitudinal strain no longer exist.

In addition to the delayed release of beam crossings, another beam failure mechanism can be identified. Although isotropic etching is by definition a process with similar etch rates in all directions, the 'isotropic' plasma etch that was used in this study appeared to not be perfectly isotropic. For example, the etching of a rectangular window revealed a lower underetch rate in the corners compared to the underetch rate at the middle of the straight sections. This etch anisotropy caused doubly-clamped beam situations during the underetching of cantilever beams. Si reinforcement reduces the risk of cantilever beam fracturing caused by local etch rate differences. Similar to the situation depicted in Figure 3.3, any doubly-clamped beams formed during underetching will be reinforced by the supporting Si.

3.2.2. DESIGN

In order to test the effect of Si reinforcement on structures with and without beam crossings, the design included individual waveguide beams and waveguide beams connected at their free ends by a crossbar. The individual beams were designed in sets of one, two, and four parallel beams; the connected structures consisted of two and four parallel beams. All the beam structures were designed with a variety of lengths (250 μm, 500 μm, 750 μm and 1000 μm) and widths (18 μm, 26 μm and 34 μm). These dimensions are a trade-off between having a sufficient cladding thickness (for low propagation loss of future photonic waveguide beams) and obtaining a low bending stiffness (in order to position the beams using microactuators). Furthermore, test cantilevers were included with a designed width

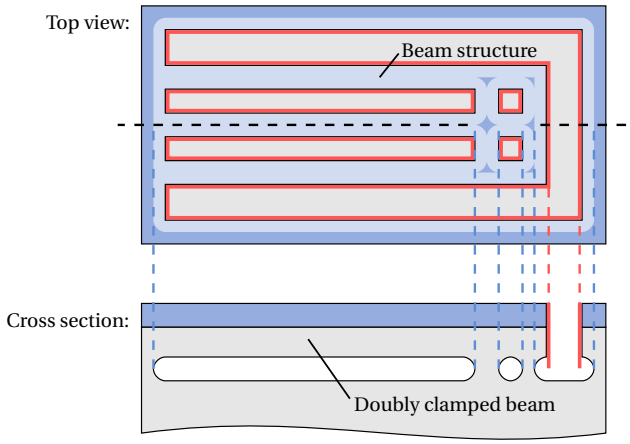


Figure 3.3: Schematic representation of a SiO_2 beam structure during the Si-reinforced underetching process.

of 15 µm and a varying designed length. A single wafer contained 72 identical arrays of 60 cantilevers of which the length ranged from 10 µm to 1000 µm with a step size of 16.5 µm.

3.3. RESULTS AND DISCUSSION

3.3.1. RELEASED STRUCTURES

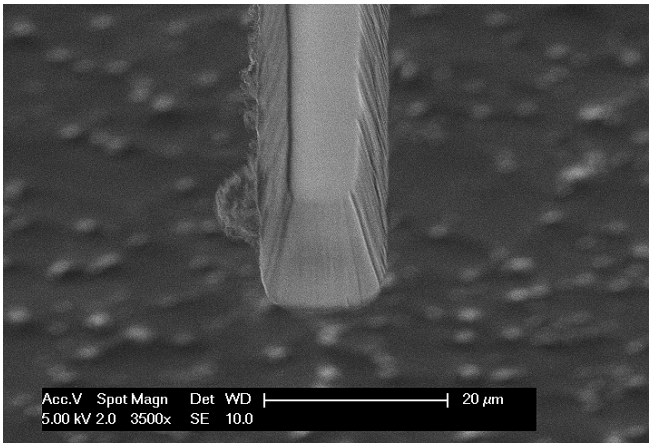
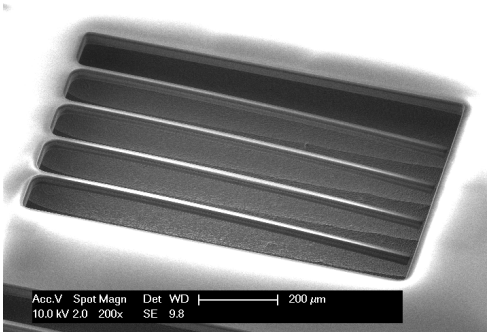


Figure 3.4: Scanning Electron Microscope (SEM) image of a suspended SiO_2 beam, with the end facet of the beam in the center of the image. This image was acquired with a tilted stage.

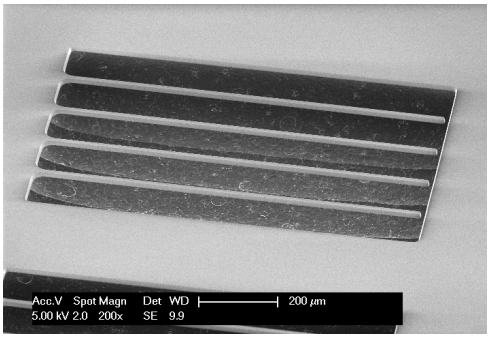
The realized structures were measured to be approximately 5 µm less wide than designed, resulting in 13 µm, 21 µm and 29 µm wide beams and 10 µm wide test cantilevers. The etch profile had a positive taper between 9° and 10°, resulting in a trapezoidal cross section of the SiO_2 beams. Figure 3.4 shows an angled view of one of the fabricated SiO_2 beams. The beam widths mentioned above are the mean values of the narrow top and the wider bottom of this trapezoid. The exact cause of the difference between the designed and the obtained width is under investigation. All the final structures had a measured thickness of 14 µm, roughly 0.8 µm less than the SiO_2 thickness at the start of the fabrication. This means that approximately 0.8 µm of SiO_2 was etched from the top surface after removal of the photoresist mask.

Figure 3.5a and Figure 3.5b show four parallel suspended beams with and without supporting Si, respectively. The SiO_2 beams in both figures are 1000 µm in length and 13 µm in width. Furthermore, suspended structures consisting of parallel waveguide beams, connected by a crossbar, were fabricated. Figure 3.5c shows a suspended SiO_2 structure consisting of 4 connected waveguide beams, each 1000 µm long and 13 µm wide.

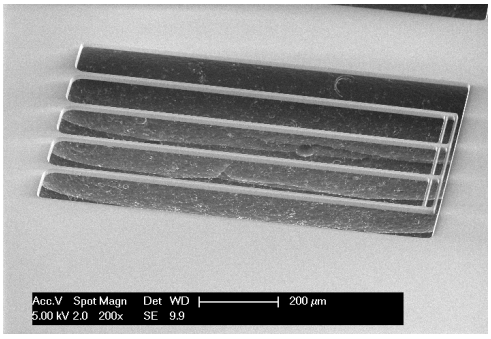
The fabrication yield of single cantilevers was determined by counting the number of truncated test cantilevers. Based on a single wafer with 4320 cantilevers in total, an overall yield of 97.8 % was observed. Up to a length of 750 µm, all cantilevers were intact. Above this length, the number of truncated cantilevers increased with the cantilever length. The most affected cantilevers were the longest ones, resulting in a yield of 83 % for the 1000 µm long cantilevers.



(a) SEM image of suspended bilayer beams.



(b) SEM image of suspended SiO_2 beams.



(c) SEM image of suspended SiO_2 structure consisting of four beams, connected at their free ends.

Figure 3.5: SEM images of different types of suspended structures.

As opposed to the test cantilevers, the beam structures only showed incidental beam failure. This can be explained by the fact that they consist of beams that are wider than the test cantilevers, making them less fragile. Because of the large variation in beam length and beam width of the structures, the number of implementations of one version was limited. As a consequence, the number of realized beam structures of a specific size was too low to estimate the corresponding yield with any degree of confidence.

3.3.2. BEAM DEFLECTION

This section discusses the initial out-of-plane bending of the suspended beams, which was caused by residual stress originating from the thermal oxidation. The profiles of cantilever beams were measured at room temperature using white light interferometric profilometry. A *Bruker Contour GT-K 3D* optical profilometer was used. Measurements were performed at three different moments during the fabrication process. The first measurement was performed after the release of the bilayer beam, the second after partly etching the supporting Si (i.e., 60 s of ething), and the third after fully etching the supporting Si (i.e., another 210 s

of ething). These three states correspond to steps (g), (h), and (i) in Figure 3.1 and will be referred to as 'Released', 'Si-etch1', and 'Si-etch2', respectively. Figure 3.6 schematically illustrates the cross sections at the three measured moments during fabrication.

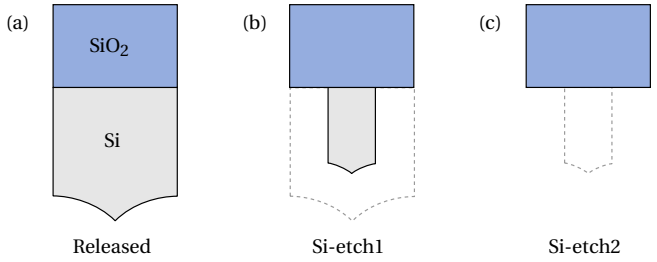


Figure 3.6: Schematic cross sections of a waveguide beam at the three measurement moments during the release process: (a) after the initial release; (b) after 60 s of etching the supporting Si; (c) after an additional 210 s of etching the supporting Si layer.

The transverse deflection measurements (of which one example is presented in Figure 3.7) show that the profile of the beam is different at the three fabrication states. The maximum deflection of the free end occurred after Si-etch1, and was almost 100 µm for this measured cantilever. The beam curvatures were retrieved by curve-fitting the measured profiles with a circle. Only the relevant part of every measurement was used for the curve fitting, indicated by the dashed vertical lines in Figure 3.7. From the measured beam profiles two deformation effects can be distinguished.

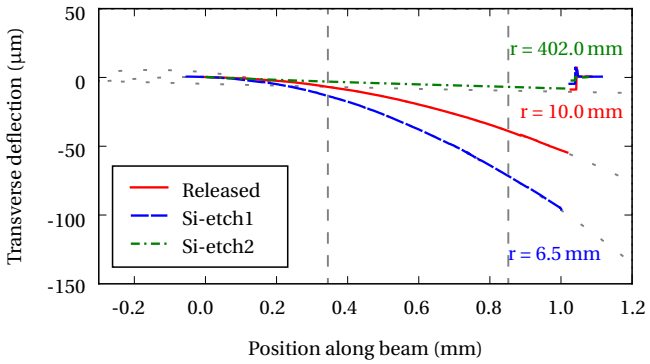


Figure 3.7: Measured deflections of a single cantilever at the three states during fabrication. The cantilever was 1000 µm long, 21 µm wide and 14 µm thin. The segment of the profiles between the dashed vertical lines was curve-fitted with a circle, and the corresponding radii of curvature are included in the plot. The top surfaces on both sides of the beam correspond with a transverse deflection value of 0 µm. The profile measured after Si-etch2 has a negative slope at the base and a curvature in the direction opposite to the curvatures measured at the other states (not visible at the scale of the plot).

BEAM CURVATURE

The first effect is an out-of-plane deflection with a constant radius of curvature, which was dependent on the amount of supporting Si. The curvature of the bilayer beams corresponded to a concave downward (∩) profile for both the released and Si-etch1 state. However, the SiO_2 beams revealed a small curvature in the opposite direction (concave upward, ∪).

The curvature at the different states during the release process depends on the configuration of and the residual stress in the bilayer beam. Residual stresses originate from the high temperature oxidation and the subsequent cooling down to room temperature in combination with the different thermal expansion coefficients of SiO_2 and Si. As a consequence, the bilayer beam will show a curvature.

The amount of curvature is a non-linear function of the Si layer thickness. At the Released state (see Figure 3.7), there will be a certain concave downward curvature, caused by the prevailing Si and SiO_2 thickness. Etching of the Si reduces its thickness. In addition, the Si is also etched from the sides, reducing its width and resulting in an irregular cross-sectional shape, defined by the progressing etch fronts. These effects reduce the area moment of inertia of the Si layer and, as a consequence, the concave downward curvature increases during etching (Si-etch1 in Figure 3.7). At small dimensions of the Si layer, the SiO_2 layer becomes dominant in the mechanics of the beam, and the curvature decreases with etching of Si. When all the Si is etched, the SiO_2 beam shows a small concave upward curvature (Si-etch2 in Figure 3.7), which is caused by the intrinsic gradient stress present in thermal SiO_2 [10, 11].

SLOPE AT THE BASE OF THE BEAM

The second effect is a negative slope at the base of the cantilever. At this location the Si under the cantilever is removed, leaving a Si sidewall beneath the cantilever base. The compressive and gradient stress in the SiO_2 lead to deformation of the SiO_2 near this Si sidewall. If a pure SiO_2 cantilever is considered, the SiO_2 layer is free to expand at its top, but is constrained by the stiff Si, which causes the initial negative slope. For the SiO_2 beams, a negative slope of approximately 0.5° was observed. The initial slope of bilayer beams was smaller with increasing thickness of supporting Si.

MEAN BEAM CURVATURES

The mean curvatures as a function of Si reinforcement of measured beam arrays (consisting of either four separate or connected beams) with a length of 250 μm, 500 μm, 750 μm and 1000 μm are presented in two separate figures. Figure 3.8 shows the mean curvatures of beams underetched with a narrow trench (~30 μm), while Figure 3.9 includes the mean curvatures resulting from a wide etch trench (~100 μm). In both figures, a positive curvature corresponds to a concave downward profile. It is observed that the narrower trench resulted in a lower underetch rate, causing an increased degree of Si reinforcement after the same etch duration.

The curvature of the bilayer beams does not depend on the length. It does depend on the beam width, as can be seen in both figures. This can be explained by the differences in Si support. Different beam widths result in different cross sections of the Si part, affecting the curvature.

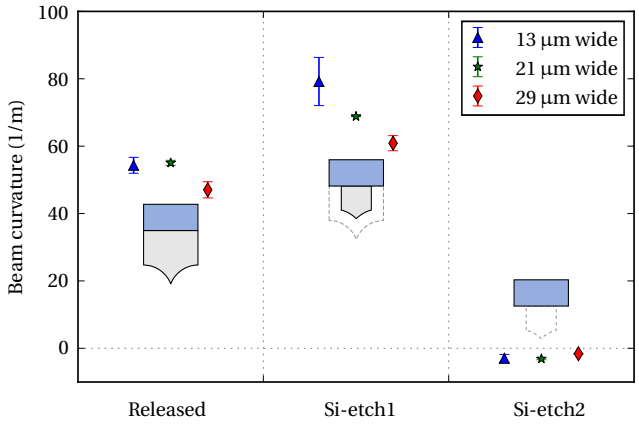


Figure 3.8: Beam curvatures measured at the different states during the release process. The error bars indicate the standard deviation from the mean value. This plot only includes the cantilevers with a narrow etch trench (~30 µm).

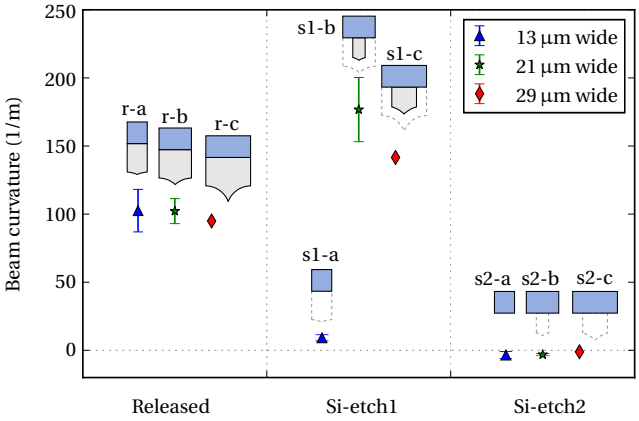


Figure 3.9: Beam curvatures measured at the different states during the release process. The error bars indicate the standard deviation from the mean value. This plot only includes the cantilevers with a wide etch trench (~100 µm).

An unexpected observation is that the curvatures of the 13 µm wide beams after Si-etch1 (s1-a in Figure 3.9) are much smaller than those of the wider beams (s1-b and s1-c in Figure 3.9). Moreover, the beams with a similar width, but released using a narrow trench, do not show this decrease in curvature (see Figure 3.8). The reason for this inconsistency is that a wider etch trench causes a higher etch rate. The 13 µm wide beams no longer have any Si reinforcement after Si-etch1, if they are released using a wide trench. However, the wider beams (s1-b and s1-c) are still supported by Si after Si-etch1, as well as the beams of similar width that are released using a narrow trench.

3.3.3. BEAM BENDING STIFFNESS

This section describes the bending stiffness of the SiO_2 beams. In the application of photonic alignment, integrated MEMS actuators will be implemented to position the array of waveguide beams. Because the available force of MEMS actuators is limited, the waveguide array should have a low bending stiffness. In order to obtain a rough estimate of the desired stiffness, one can imagine a microactuator capable of delivering 1 mN. The out-of-plane positioning of a waveguide array over a range of 5 µm requires a maximum array stiffness of 200 N/m. In case the waveguide array comprises ten parallel beams, this corresponds to an out-of-plane bending stiffness of individual beams of approximately 20 N/m.

The bending stiffness can be determined using the relation

$$k = m_{\text{eff}}(2\pi f)^2, \tag{3.1}$$

where k is the bending stiffness, m_{eff} is the effective mass, and f is the natural resonance frequency. The out-of-plane natural resonance frequency was measured with laser Doppler vibrometry at ambient conditions. The effective mass was based on dimensions which were estimated from scanning electron microscope (SEM) images.

The determined out-of-plane bending stiffness values of SiO_2 cantilevers (not Si-reinforced) are presented in Table 3.1 and depicted in Figure 3.10. The values for a length of 250 µm are included in the table, but are not shown in the graph, since they are not compatible with the photonic alignment concept. The determined bending stiffness values corresponding to a cantilever of 250 µm in length are greater than 50 N/m. As seen in the rough calculation above, those stiffness values are outside our range of interest. All cantilevers with a length of 500 µm or more have a derived bending stiffness smaller than 20 N/m and therefore satisfy our stiffness requirement.

Table 3.1: Determined out-of-plane bending stiffness values (mean and standard deviation) of SiO_2 cantilevers.

Length (µm)	Width (µm)	Stiffness (N/m)	
		mean	s
250	13	53.7	1.6
	21	73.1	1.7
	29	93.6	0.8
500	13	6.9	0.1
	21	9.5	0.1
	29	12.2	<0.1
750	13	2.1	<0.1
	21	2.9	<0.1
	29	3.8	<0.1
1000	13	0.8	n/a
	21	1.2	<0.1
	29	1.6	<0.1

Figure 3.10 shows the decrease in stiffness with increasing cantilever length. The stiffness and length are related by the equation

$$k = \frac{3EI}{L^3}, \tag{3.2}$$

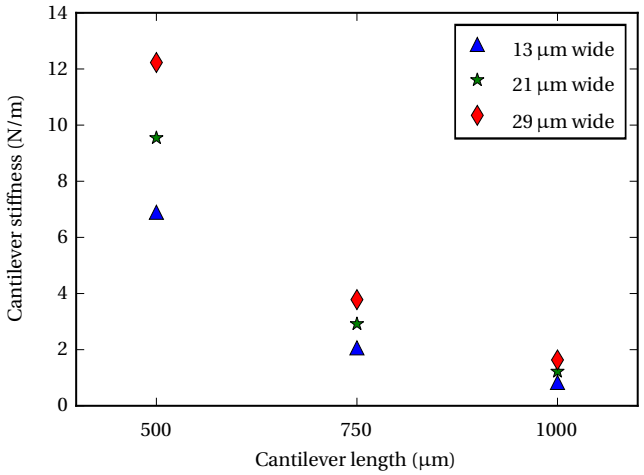


Figure 3.10: Determined out-of-plane beam bending stiffness of SiO_2 cantilevers (not Si-reinforced) as a function of beam length, plotted for different cantilever widths.

where k is the bending stiffness, E is the Young's modulus, I is the area moment of inertia, and L is the length of the cantilever. The data points in Figure 3.10 corresponding to a specific width show a third power relationship, which is in accordance with Equation (3.2).

For a specific cantilever length, the bending stiffness is expected to scale linearly with the cantilever width, because the area moment of inertia is proportional to the width. For a rectangular beam, the area moment of inertia is

$$I = \frac{1}{12} b h^3, \tag{3.3}$$

with I, b, and h the area moment of inertia, the beam width and the beam height, respectively. The determined data show a deviation from this linear relation of up to 15 %. Especially the determined stiffness of the narrow beams is larger than expected. The trapezoidal shape of the cross-sections of the beams only accounts for up to 1.2 % of the difference between expected and calculated value. The cause of this length-dependent deviation is not known.

As described in this chapter, suspended structures of thick SiO_2 were realized. Their compatibility with microactuators in terms of stiffness proved to be mostly dependent on the cantilever length. Follow-up experiments will include the integration of microactuators with functional suspended waveguide beams and will involve optical characterization. We expect that the optical properties of suspended waveguide beams will be affected by the SiO_2 etch. Properties like the sidewall surface roughness and the etch taper will influence the performance at the waveguide end facet (e.g., scattering and propagation direction of the guided light).

3.4. CONCLUSION

This chapter has presented a robust microfabrication process for the release of SiO_2 structures. This novel process reinforces the SiO_2 with Si, thereby reducing the risk of beam fracturing. Moreover, the fabrication process allows for a configurable thickness of the final Si support. The advantages of the Si reinforcement are control over the beam stiffness and a greatly enhanced design freedom for suspended SiO_2 structures. The fabrication yield was 97.8 % for cantilever beams with a thickness of 14 µm, a width of 10 µm and a length ranging from 10 µm to 1000 µm. In addition to cantilever beams, more complex structures were successfully realized, consisting of parallel beams, connected by a crossbar at their free end.

The bilayer beams were measured to have a concave downward profile with a constant radius of curvature, which was observed to change as a function of Si support. SiO_2 beams without supporting Si were found to have a concave upward profile and a much smaller curvature. A 1000 µm long bilayer beam of 21 µm width was observed to have a radius of curvature of 10 mm after its release. Partly etching the supporting Si resulted in a smaller curvature, corresponding to a radius of curvature of 6.5 mm. After complete removal of the supporting silicon, the cantilever showed a concave upward profile with a radius of curvature of 402 mm.

The measured out-of-plane bending stiffness of the SiO_2 beams ranged from roughly 1 N/m to 100 N/m. The long beams (i.e., 500 µm and longer) are compliant enough to be positioned by microactuators. The short beams, however, are probably too stiff to be positioned by microactuators within the required motion range.

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4

INTEGRATED ACTUATORS

The previous chapter introduced a method to reliably fabricate suspended structures in thick SiO_2, despite the tendency of SiO_2 beams to fracture upon release. In this chapter, micro-actuators will be integrated with suspended SiO_2 structures, making them positionable.

This chapter first discusses the design of the structures and the actuators (Section 4.2), followed by an overview of the fabrication process steps, as an extension of the method presented in the previous chapter (Section 4.3). Section 4.4 includes the characterization of fabricated devices. Measurements of the post-release deformation (i.e., without actuation), as well as the deflection resulting from quasi-static and dynamic actuation are performed. Finally, the actuator performance is discussed in the light of the photonic alignment solution in Section 4.5.

Based on
T.-J. Peters, M. Tichem, *Electrothermal Actuators for SiO_2 Photonic MEMS*, Micromachines 7 (11), 200 (2016) (with modifications to Section 4.3)

4.1. INTRODUCTION

COMBINING suspended photonic waveguides and microactuators enables positionable waveguides, resulting in the photonic switch [1–3] and numerous other MOEMS applications [4–6]. However, the majority of research on positionable waveguides is limited to silicon photonic devices. The positionable waveguides presented in this chapter are based on silicon nitride (Si_3N_4) waveguide cores within a thick (~16 µm) SiO_2 cladding. We propose the name 'SiO_2 photonic MEMS' for this platform, due to the mechanically dominant material being oxide.

We have explored the use of suspended SiO_2 waveguides with integrated actuators as part of a novel chip-to-chip alignment concept for photonic integrated circuits (PICs). This concept is based on a two-step assembly process, in which two PICs are first coarsely aligned and locked in position, after which the waveguides of the PICs are fine-aligned and locked in position. The strength of the alignment approach lies in a positionable waveguide array that is locally realized in one of the PICs and which is equipped with on-chip MEMS actuators to achieve sub-micrometer precise alignment with the waveguides of the other PIC. Figure 4.1 shows an illustrative case in which a fiber array is coupled to an Indium Phosphide (InP) PIC through an interposer chip with a positionable waveguide array. We emphasize that this is only one of many possible applications using positionable waveguides, and in this chapter we focus on the characteristics of the bimorph actuators in general.

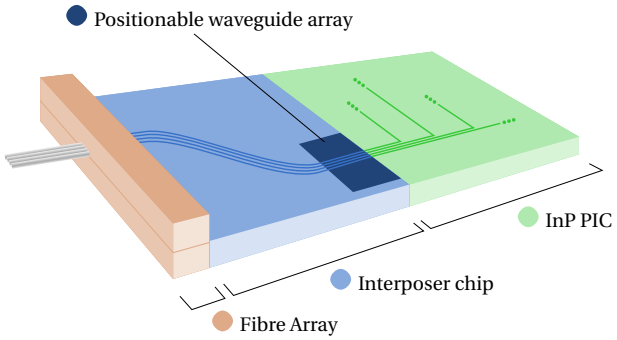


Figure 4.1: Alignment assembly with fiber array, interposer chip, and InP PIC. The location of the positionable waveguide array on the interposer chip is indicated.

The interposer chip, on which the positionable waveguide array is realized, is based on the TriPleX photonic platform, comprising ~200 nm thin silicon nitride (Si_3N_4) cores embedded in a ~16 µm thick SiO_2 cladding. This photonic material stack, which is realized on top of a silicon substrate, poses challenges when used as a separate mechanical material.

The release of thick (> 10 µm) SiO_2 structures from their silicon substrate is afflicted by buckling of the structures, due to compressive stress in the SiO_2. The buckled structures generate stress concentrations, which can lead to fracturing. Reports on suspended SiO_2 structures with a thickness around 15 µm (the total thickness required for the TriPleX platform), a width of ~18 µm, and a length of roughly 1000 µm are not abundant in literature. Ollier [2] reported on the realization of suspended structures of 25 µm thick PECVD SiO_2

using isotropic reactive ion etching (RIE). The problem of mechanical structures breaking is mentioned, as well as a solution: anti-buckling structures in combination with a specific Si etching process. Cooper et al. [7] demonstrated suspended silica waveguides with a cross section of 100 μm×40 μm. Their waveguide material is thermal SiO_2 in combination with silica created by flame hydrolysis deposition (FHD), and the suspended waveguides are realized by a combination of dicing and wet etching.

This chapter presents the design, fabrication, and characterization of suspended TriPleX structures that are positionable by integrated out-of-plane actuators. Chapter 3 included the initial fabrication results of thermal SiO_2 suspended structures without photonic waveguide cores. The same silicon reinforcement method is used in this chapter to create suspended positionable waveguide structures. The thermal actuators are realized by depositing poly-Si on top of SiO_2 beams, creating bimorph structures. The poly-Si is not only used as structural material, but also as heater material, obviating the need for additional metal heaters.

4.2. DESIGN

The requirements imposed on the positionable waveguide arrays follow from the misalignment after the first assembly step. Flip chip bonding, one of the available pre-alignment methods for the first step, aims to place the top surfaces of the interposer chip and the PIC in the same horizontal plane. The tolerance that can be achieved with flip chip bonding is in the order of one or two micrometers in out-of-plane alignment and several micrometers in in-plane alignment.

4.2.1. OUT-OF-PLANE ACTUATORS

For out-of-plane translation and rotation around the propagation direction of the light, a set of bimorph actuator beams is placed on either side of the waveguide beams, see Figure 4.2. A crossbar is included in the design to connect the photonic waveguide beams and bimorph actuator beams at their free ends. In this way, all waveguide beams can be positioned by controlling only two actuators. One of the advantages of this approach is that the waveguide pitch, which is well-defined by lithography, is preserved. Moreover, a very small pitch can be realized, as no space is occupied by individual actuators between waveguide beams.

The waveguide beams are SiO_2 beams that contain a waveguide core. The actuator beams are SiO_2 beams with a patterned layer of poly-Si on top, as illustrated in Figure 4.2. Because the coefficient of thermal expansion (CTE) of poly-Si is larger than that of SiO_2, the crossbar moves towards the silicon substrate when the actuator beams on both sides are operated simultaneously. In the presented designs, the poly-Si covers the full length of the actuator beams. In other work [8] we reported on bimorph beams that are partially covered by poly-Si, having the opportunity to, based on the design, control the postrelease deformation, as is explained later.

The poly-Si material is both a structural part of the bimorph actuator and a heating element, by means of resistive heating. The doping level controls the resistivity of the poly-Si, and the resistivity, together with the shape of the poly-Si heater (length and cross section), determine its resistance. The actuators merge into electrical leads that terminate in bond-

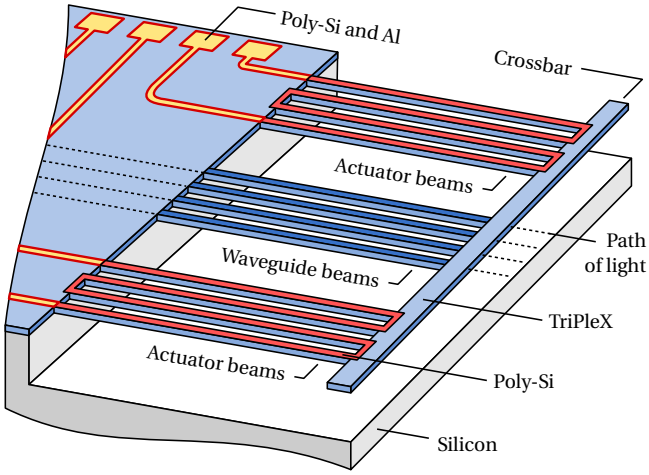


Figure 4.2: Schematic representation of a suspended beam array with waveguide beams in the center and out-of-plane actuator beams on both sides.

pads. The electrical leads and bondpads consist of poly-Si with a layer of aluminum (Al) on top.

4.2.2. DIMENSIONS

The configuration and dimensions of the positionable waveguide arrays follow from photonic as well as mechanical requirements. An overview of the most important parameters, values, and their rationale is given in Table 4.1. The number of waveguide beams is dependent on the number of channels of the photonic application. The cross section of the waveguide beam is preferably as small as possible to ensure a low bending stiffness. The values for the waveguide thickness and width follow from the minimum required cladding thickness that ensures low propagation loss. The waveguide beam length is based on the required deflection and the force that thermal actuators can provide. The 127 µm pitch matches the pitch of commercially available fiber array units (FAUs). This pitch was chosen for convenience, and a smaller pitch (e.g. 50 µm) is feasible. A total of eight bimorph beams is included in the design (four on either side), placed at a pitch of 50 µm. The width of the crossbar is larger than the beam width to increase the crossbar stiffness. The crossbar is provided with etch holes to facilitate the release process. Two poly-Si thicknesses are selected, predominantly based on the resulting actuator stroke, as will be discussed below. The waveguide core width together with the core thickness (which is not a parameter in the mask design, but defined by the Si_3N_4 thickness) determine the mode field diameter (MFD). At a wavelength of 1550 nm, 1 µm wide and 200 nm thin cores are single-mode.

The waveguides in the bulk of the chip are designed to have an *S-shape* (visible on the surface of the interposer chip in Figure 4.1), to ensure that only the light that is coupled into the waveguide cores is guided to the positionable array.

Table 4.1: Overview of the most important parameters and values used in the suspended beam arrays. The rationale column indicates whether the value is defined by photonic (p) or mechanical (m) requirements.

Parameter	Value	Rationale
Number of WG beams	4	p
WG beam thickness (μm)	16	p + m
WG beam width (μm)	18	p + m
WG beam length (μm)	800	m
WG pitch (μm)	127	p
Number of bimorph beams	8	m
Bimorph beam pitch (μm)	50	m
Crossbar width (μm)	118	m
Poly-Si thickness (μm)	3 or 5	m
WG core width (μm)	1	p
WG core thickness (nm)	200	p

The actuator stroke of a single bimorph beam can be estimated using an analytical model. Based on the analytical multilayer beam model as described by Scott et al.[9], the curvature of a trilayer cantilever is

$$\kappa = \frac{(2\mathbf{R}\mathbf{A}^{-1}\mathbf{S})}{2+\mathbf{R}\mathbf{A}^{-1}\mathbf{B}},$$

with

$$\mathbf{R} = \begin{bmatrix} \frac{t_1}{2} \\ t_1 + \frac{t_2}{2} \\ t_1 + t_2 + \frac{t_3}{2} \end{bmatrix} \frac{-1}{E_1 I_1 + E_2 I_2 + E_3 I_3},$$

$$\mathbf{A} = \begin{bmatrix} (E_1 A_1)^{-1} & -(E_2 A_2)^{-1} & 0 \\ 0 & (E_2 A_2)^{-1} & -(E_3 A_3^{-1}) \\ 1 & 1 & 1 \end{bmatrix},$$

$$\mathbf{S} = \begin{bmatrix} \epsilon_2 - \epsilon_1 \\ \epsilon_3 - \epsilon_2 \\ 0 \end{bmatrix},$$

$$\mathbf{B} = \begin{bmatrix} t_1 + t_2 \\ t_2 + t_3 \\ 0 \end{bmatrix},$$

$$I_i = \frac{b_i t_i^3}{12},$$

$$A_i = b_i t_i,$$

$$\epsilon_i = \alpha_i \Delta T,$$

and where b_i, t_i, E_i, α_i are the width, thickness, modulus of elasticity, and the CTE of layer i respectively. ΔT is the applied temperature difference. This model considers thermal stress only.

The free end deflection δ of a beam with curvature κ can be approximated by

$$\delta = \frac{(1-\cos\kappa L)}{\kappa},$$

where L is the length of the beam (800 µm in our case). For a given length and thickness of the three layers, the deflection of the free end is found to be a linear function of the actuator temperature change. The values used to obtain Figure 4.4 are summarized in Table 4.2. The bottom layer of the actuator beams consists of TriPleX material, but without the Si_3N_4 core.

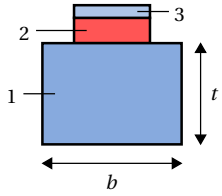


Figure 4.3: The cross-sectional dimensions of the three layers representing a bimorph beam.

Table 4.2: The values of the trilayer materials.

	Layer 1	Layer 2	Layer 3
Material	TriPleX	Poly-Si	SiO_2
b (µm)	18	12	12
t (µm)	16	3 or 5	2
E (GPa)	70	160	75
α (10^{-6}/°C)	0.5	3.44	2.5

Figure 4.4 shows the free end deflection of an example bimorph beam as a function of the poly-Si thickness, for a given TriPleX thickness, at three different actuator temperatures. The free end moves in a downward direction upon actuation, and the maximum deflection is obtained with a poly-Si thickness that is slightly larger than 5 µm.

The postrelease deformation is affected by the poly-Si thickness in a similar way. After the deposition of poly-Si at 1050 °C, the temperature decreases to room temperature, introducing thermal stress. Inevitably, the bimorph effect causes a concave upward curvature of the actuator beams at room temperature. The maximum postrelease curvature coincides with the maximum actuator stroke, at a poly-Si thickness just above 5 µm.

This chapter aims to provide basic characteristics of SiO_2/poly-Si bimorph actuators for universal use, rather than for a specific application only. To obtain a large deflection, two poly-Si thicknesses are selected, based on the curves in Figure 4.4: 3 µm and 5 µm. Furthermore, the bimorph actuators are designed to be fully covered by poly-Si, so that their

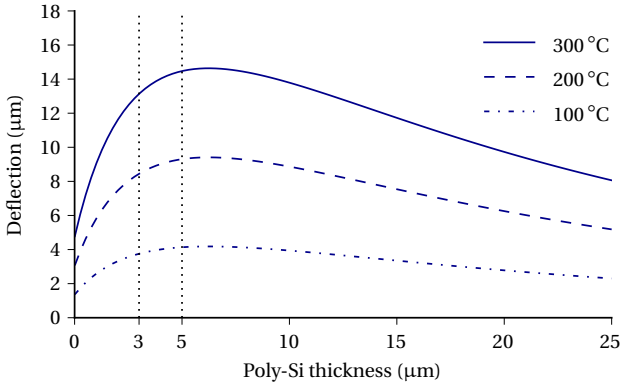


Figure 4.4: The deflection of the free end of an 800 μm long, 18 μm wide single bimorph beam as a function of the poly-Si thickness for a given SiO_2 thickness of 16 μm. The three curves represent different actuator temperatures.

performance is easily comparable with bimorph actuators based on different material configurations. These design choices are expected to result in a significant postrelease deformation. Should the application require it, the postrelease deformation can be reduced by means of alternative designs, e.g. partially covering bimorph beams with poly-Si [8].

4.3. MICROFABRICATION

The suspended waveguide beams are released using a special reinforcement method, reducing the risk of beam fracturing. Without reinforcement, the compressive residual stress in the TriPleX layer causes the beams to buckle and fracture. Temporarily reinforcing the TriPleX beams with silicon (Si) reduces the expansion and buckling of suspended structures and prevents fracturing.

The fabrication process of positionable waveguide arrays comprises two consecutive fabrication sequences, which are schematically illustrated in Figure 4.5. First, waveguiding functionality is added to a silicon wafer by depositing a TriPleX [10] layer stack. This TriPleX stack predominantly consists of the following four different materials, from bottom to top: (1) ~8 μm thick thermally grown SiO_2 bottom cladding layer; (2) 200 nm × ~1 μm (thickness × width) silicon nitride (Si_3N_4) waveguide cores, grown by low pressure chemical vapor deposition (LPCVD); (3) ~3 μm thick LPCVD SiO_2; and (4) ~5 μm thick SiO_2 grown by plasma enhanced chemical vapor deposition (PECVD). Materials (3) and (4) together form the top cladding layer, and are annealed at 1150 °C to bring their mechanical and optical properties close to those of thermally grown SiO_2. The Si_3N_4 layer includes alignment marks for the alignment of photolithography masks with the waveguide pattern.

After the waveguiding layer is formed, the SiO_2 MEMS fabrication is performed, requiring a total of six lithography masks. The starting point of the MEMS fabrication is a 100 mm TriPleX wafer, resulting from the photonic waveguide fabrication as is illustrated in Figure 4.5. The steps of the MEMS fabrication are as follows, and are graphically presented in Figure 4.6.

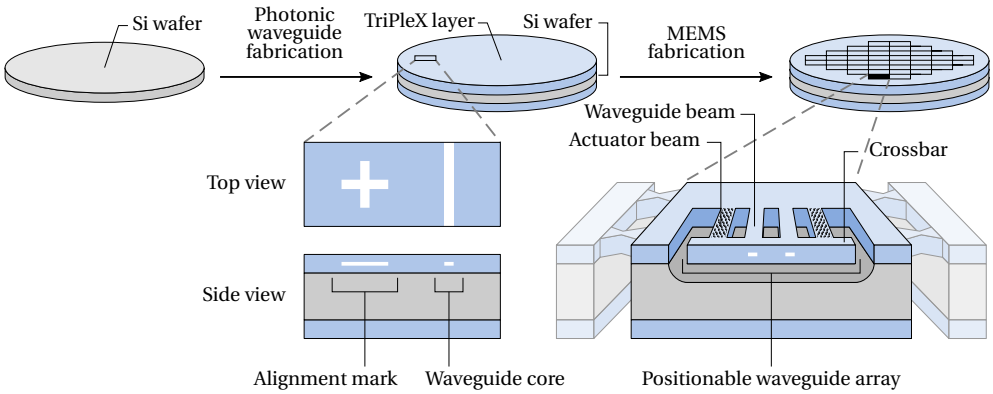


Figure 4.5: The two consecutive sequences for the fabrication of positionable waveguide arrays. First, photonic waveguide functionality is created. After that, MEMS functionality is realized.

A 130 nm thin seed layer of LPCVD poly-Si is deposited on the TriPleX wafer. To prevent poly-Si accumulation on the backside in the consecutive epitaxial growth step, the poly-Si is removed from the backside of the wafer. This etching step is completed without a mask in a Trikon Omega 201 plasma system. The etch recipe consists of a SiO_2 breakthrough followed by a Si etch, both performed using an ICP power of 500 W at a temperature of 20 °C. The SiO_2 breakthrough uses 20 sccm of O_2 and 40 sccm of CF_4, a pressure of 5 mTorr, and a bias RF power of 60 W. The Si etch uses 80 sccm of Cl_2 and 40 sccm of HBr, a pressure of 60 mTorr, and a bias RF power of 20 W.

Immediately before the epitaxial growth, native oxide is removed by wet etching in a solution of water with 0.55 % hydrogen fluoride (HF) for 4 min. During the epitaxial growth, the thickness of the poly-Si seedlayer is increased. The final thickness is controlled by the duration of the epitaxial growth process, taking into account the growth rate (i.e. approximately 1 µm/min). The epitaxial growth process is performed at a temperature of 1050 °C, a pressure of 60 Torr, and with a flow of diborane (B_2H_6) diluted with hydrogen gas (H_2) to control the p-type doping level of the poly-Si layer. A source/inject/diluent ratio of 110 sccm/65 sccm/20 SLM was applied, aiming for a doping concentration equal to 2×10^{16} B /cm^3 in crystalline Si. The resulting cross section is depicted in Figure 4.6a.

Locally, rectangular openings are plasma etched in the poly-Si layer to regain visual access to the alignment marks. SPR3012 positive resist with a thickness of 1.4 µm is used as etch mask. A Bosch process is employed by means of an SPTS Omega i2L Rapier deep silicon etcher. This process continually cycles through the deposition of a passivation layer and two etch steps. The deposition step has a duration of 1.2 s and uses C_4F_8 gas without platen RF power at a chamber pressure of 40 mTorr. The first etch step lasts 1.2 s, using O_2 gas and 75 W platen RF power. The second etch step is 2.5 s long and uses SF_6 gas with 24 W platen RF power. Both etch steps use 30 mTorr chamber pressure. The deposition as well as the etch steps are performed with 2500 W primary source power and 500 W secondary source power.

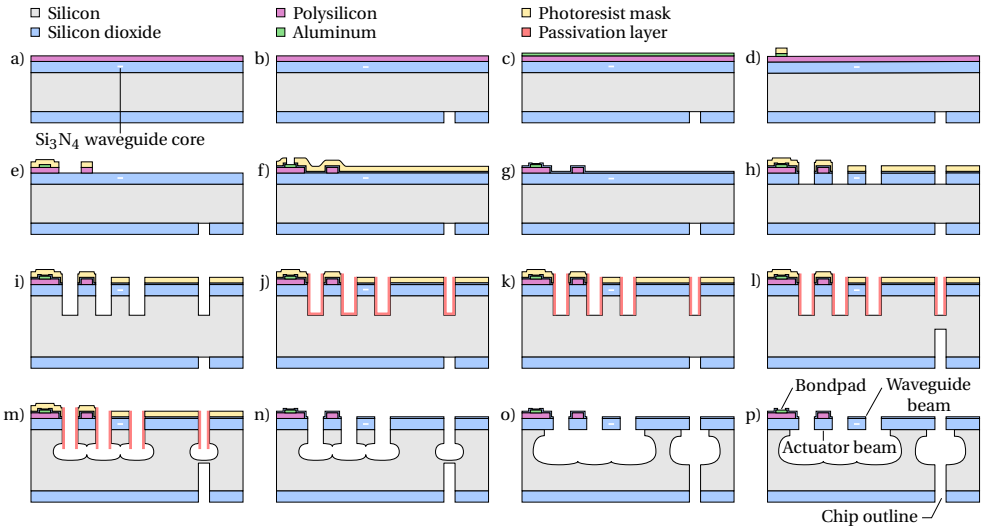


Figure 4.6: Fabrication steps for positionable suspended waveguide beam structures. a) Deposition of poly-Si. b) Plasma etching of SiO_2 on backside. c) Deposition of aluminum. d) Plasma etching of the aluminum. e) Plasma etching of the poly-Si. f) Deposition of PECVD SiO_2 and local removal by plasma etching. g) Deposition of PECVD SiO_2. h) Plasma etching of SiO_2 on frontside. i) Anisotropic plasma etching of Si. j) Deposition of passivation layer. k) Local removal of passivation layer. l) Anisotropic plasma etching of Si on backside. m) Isotropic plasma etching of Si. n) Removal of photoresist and passivation layer. o) More isotropic etching of Si. p) Plasma etching of PECVD SiO_2, to expose the bondpads.

Next, the desired singulation pattern is etched into the SiO_2 layer on the backside of the wafer, see Figure 4.6b. This backside processing step is performed at this stage of the fabrication process in order to prevent possible damage to the future structures at the frontside. The etching is performed with a 6 µm thick etching mask (positive AZ9260 resist) and a Drytek Triode T384 system using C_2F_6 and CHF_3 gasses. The gas flows are 36 sccm and 144 sccm, respectively, and an RF power of 300 W is used at 180 mTorr chamber pressure. After removing the photoresist using an oxygen plasma, the processing continues on the frontside.

On top of the poly-Si layer, a 675 nm thin layer of Al with 1 % of Si (Al-1%Si) is deposited by sputter deposition (Figure 4.6c). Al-1%Si is used instead of pure Al to prevent Al spikes in the Si due to Si–Al interaction at elevated temperatures. The deposition is performed with a Trikon Sigma 204 sputter coater, at 350 °C, using a base pressure of 1×10^7 Torr and 10 kW target power. Locally, rectangular openings are plasma etched in the Al-1%Si layer to regain visual access to the alignment marks. The Trikon Omega 201 plasma system is used for this etching step, applying 30 sccm of chlorine gas (Cl_2), 40 sccm of hydrogen bromide gas (HBr), 5 mTorr proces pressure, 40 W platen RF power, and 500 W ICP RF power.

With the alignment marks visible, a 1.4 µm thick SPR3012 positive resist layer is spin coated, and its pattern is used as mask during the etching of the Al-1%Si, forming the electrical leads and the bondpads, which is illustrated in Figure 4.6d. The etching of Al-1%Si is done in the Trikon Omega 201 plasma system, employing a plasma etch process with HBr

(40 sccm) and Cl_2 (30 sccm) at a process pressure of 5 mTorr. The etching is performed in two steps, first applying 50 W platen RF power and 500 W ICP RF power for 25 s and subsequently 40 W platen RF power and 500 W ICP RF power for 40 s.

A 4 µm thick layer of SPR3017M photoresist is then spin coated, covering the >0.675 µm topography of the Al-1%Si and poly-Si. The pattern in this mask includes the electrical leads and bondpads but also defines the poly-Si heating structures as follows. The combination of poly-Si and Al-1%Si is used for electrical conductance whereas poly-Si without Al-1%Si serves as a heater. For the etching of the poly-Si, the same recipe was used on the SPTS Omega i2L Rapier deep silicon etcher as in the step in which the openings were etched in the poly-Si. The resulting cross section is presented in Figure 4.6e.

A 2 µm thick layer of SiO_2 is deposited by plasma enhanced chemical vapor deposition (PECVD). This layer is applied to prevent the poly-Si from being etched during the upcoming Si etch steps. The PECVD SiO_2 is deposited with a Novellus Concept One system, using a temperature of 400 °C, a pressure of 2.2 Torr, and a RF power of 1000 W. Gas flows of 205 sccm for SiH_4, 6000 sccm for N_2O, and 3150 sccm for N_2 are used. After spincoating and patterning a 4 µm layer of Shipley SPR3027 photoresist, the PECVD SiO_2 is locally etched where bondpads will be realized (shown in Figure 4.6f). For the SiO_2 etching, the Drytek Triode T384 system is used again, with similar settings.

Although finally the Al bondpads are required to be accessible for making electrical connections, they must be protected from being etched during the intermediate process steps. For that reason, another layer of PECVD SiO_2 – this time 0.3 µm in thickness – is deposited, as depicted in Figure 4.6g. The Novellus Concept One system is used with similar temperature, pressure, gas flows, and power, but shorter deposition time.

Photoresist (AZ9260) is spin coated with a thickness of 12 µm and patterned into a photoresist mask. A thickness of 12 µm is used for two reasons. Firstly, the topography that has to be covered is significant, with height variations up to 7 µm. Secondly, this mask is used during multiple etching steps, one of which is a relatively long etch through ~18 µm of SiO_2. The frontside SiO_2 is etched using the Drytek Triode T384 system with the same parameters as used for the etching of the singulation pattern on the backside. Figure 4.6h shows the cross section resulting from this etch. This etching step not only defines the beam structures that will be suspended, but also the chip outline on the frontside, including supports on the corners of every chip (as indicated in Figure 4.5).

After that, the SPTS Omega i2L Rapier deep silicon etcher is used to perform consecutive steps, applying SF_6 for etching and C_4F_8 for passivation layer deposition. (1) Without removing the photoresist mask, the same pattern is anisotropically plasma etched in the Si (Figure 4.6i). (2) A CF_X passivation layer with approximately 1 µm thickness is deposited (Figure 4.6j) and then (3) locally removed from the trench bottom (Figure 4.6k). (4) From the backside, Si is etched using the SiO_2 as a mask (Figure 4.6l). (5) The unprotected Si is now isotropically plasma etched, until the complete structure of Si-reinforced SiO_2 is suspended (Figure 4.6m). After (6) complete removal of the photoresist and passivation layer (Figure 4.6n) in an O_2 plasma (Tepla 300 plasma system), (7) more isotropic etching of Si leads to suspended SiO_2 structures without Si reinforcement (Figure 4.6o).

In the final step, ~0.3 µm of PECVD SiO_2 is etched with an Alcatel GIR300 Fluorine etcher, enabling electrical access to the Al bondpads, see Figure 4.6p. Gas flows of 50 sccm

for CF_4, 25 sccm for CHF_3, and 40 sccm for He are used at a pressure of 0.05 mbar and with 60 W power.

A realized positionable suspended waveguide array with 3 µm poly-Si thickness is presented in Figure 4.7. After singulating the PIC, it is mounted on a dedicated PCB and wire-bonded, as shown in Figure 4.8. Besides the 3 µm thickness variant, a positionable waveguide array with 5 µm thick poly-Si is realized.

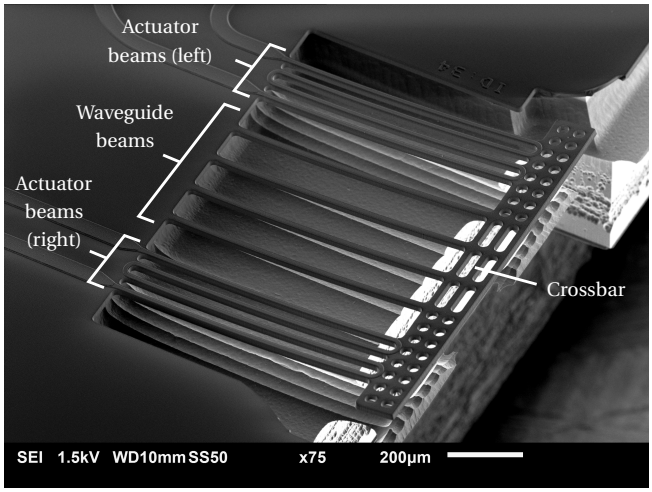


Figure 4.7: SEM image of a realized positionable waveguide array with a poly-Si thickness of 3 µm.

4.4. EXPERIMENTAL RESULTS

This section describes the characterization of realized suspended structures. The safe actuator voltage of 3 µm and 5 µm thick poly-Si bimorph actuator beams is first determined. Furthermore, the postrelease deformation, the deflection upon quasi-static actuation, the frequency response, the actuator force, and the transient response of bimorph structures are measured. For all these measurements, a comparison of the bimorph structures with 3 µm and 5 µm poly-Si thickness is presented.

4.4.1. ACTUATOR OPERATING RANGE

A known issue with doped (poly-)Si actuators is the thermal runaway effect [11]. This effect can occur when a semiconductor heater is voltage-controlled. At a specific voltage regime, the resistive heating of the actuator causes the resistance of the poly-Si material to decrease. As a result, more current will flow through the actuator, heating it even more. If no limitation is set on the current, it will rapidly increase, resulting in the actuator to burn out. Lee et al. mention a typical thermal runaway temperature between 500 °C and 600 °C [12].

In order to identify the thermal runaway point and the breakdown point, the response of a sacrificial 3 µm poly-Si actuator to a current sweep was obtained using a *Keithley 2611 system sourcemeter*. Figure 4.9 shows the measured resistance as well as voltage of the sac-

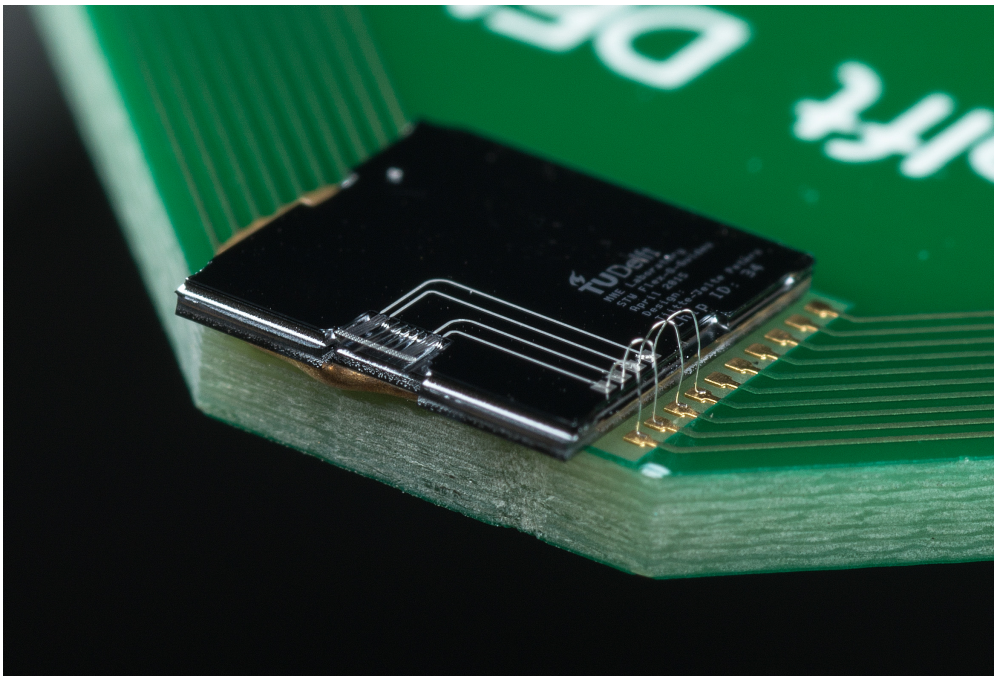


Figure 4.8: Photograph of a realized PIC with positionable waveguide array, mounted on a PCB and electrically connected by wirebonds. Photograph by Hans de Lijser.

rificial actuator as a function of the applied current. Three regimes can be distinguished in this graph, indicated with the vertical dotted lines. Between 0 mA and 0.7 mA the resistance slightly decreases with increasing current. When the actuator current is between 0.7 mA and 1.6 mA the resistance increases with the current. This phenomenon is known from other highly doped poly-Si devices [13]. For 1.6 mA and higher, the resistance decreases as the actuator current increases. When voltage-controlled, this is the regime where the thermal runaway would occur.

The measured voltage over the actuator increased from 0 V to 75.5 V, after which it decreased. Up to 7.2 mA could be applied to the actuator before it burnt out, corresponding to almost 400 mW of dissipated power. At an applied current of 3.7 mA (~250 mW) and higher, the actuator emitted visible light.

To determine the safe operating range of the 3 µm and 5 µm thick poly-Si actuators that will be analysed below, comparable current sweep measurements are performed, with a maximum current just above the thermal runaway point. Figure 4.10 presents the measured change in resistance of the actuators on the left and right side of the two variants as a function of the measured voltage. The thermal runaway point is located around 70 V (~130 mW) for the 3 µm variant and around 40 V (~125 mW) for the 5 µm variant. Around the thermal runaway point, electrical resistances of approximately 38 kΩ and 13 kΩ were measured for the 3 µm and 5 µm variant, respectively. While there is a difference in voltage,

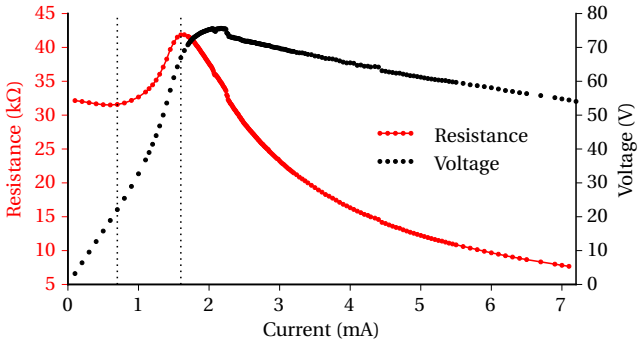


Figure 4.9: The measured resistance of and voltage over a sacrificial actuator (3 µm poly-Si thickness) as a function of the actuator current.

caused by the difference in actuator resistance, the actuators show a comparable amount of power being dissipated around the thermal runaway points. The plot also shows that at low voltages, the resistance of the left actuators is slightly lower than that of the right actuators. We expect that this is due to the length difference of the poly-Si/Al electrical leads.

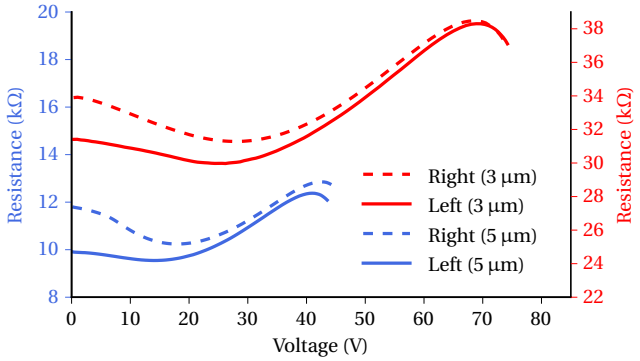


Figure 4.10: The results of current sweep measurements, showing the measured resistance of the actuators as a function of the measured voltage over the actuator.

4.4.2. POSTRELEASE DEFORMATION

The surface contours of suspended structures are obtained by means of white light interferometry (Bruker Contour GT-K 3D optical profilometer). The profiles measured over the length of one waveguide beam and two actuator beams are presented in Figure 4.11 for both variants (3 µm and 5 µm poly-Si thickness). For convenience, the vertical position of the base of the beams is aligned with the zero point of the vertical axis.

The beams have a postrelease (i.e., without actuation) out-of-plane deflection. As a result, the free ends of the beams are located approximately 60 µm and 80 µm above the

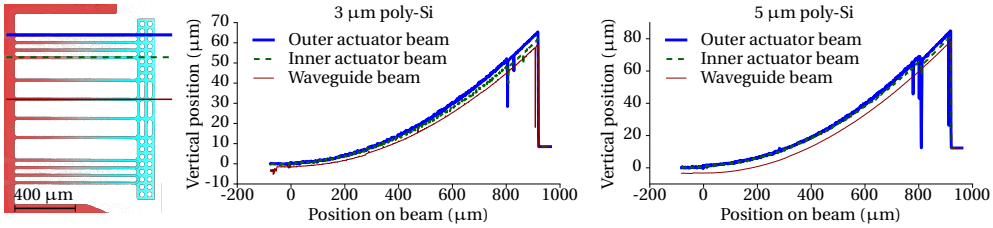


Figure 4.11: Left: top view of the measured suspended structures, indicating the locations of the three profiles. Left and right plot: the postrelease deflection (without actuation) measured over the length of three beams.

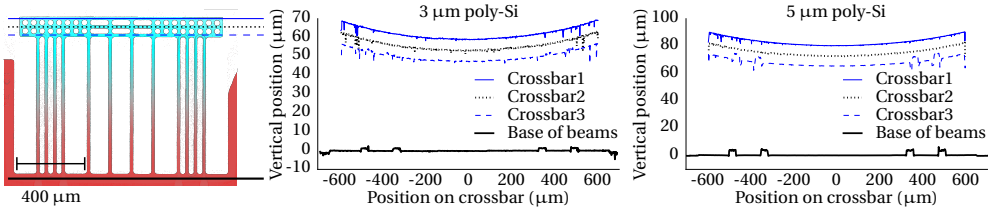


Figure 4.12: Left: top view of the measured suspended structures, indicating the locations of the four profiles. Left and right plot: the postrelease deflection (without actuation) measured over the length of the crossbar.

surface of the PIC, for the 3 µm and 5 µm poly-Si thickness, respectively. The curvatures of the three measured beams range from 126/m to 142/m for the 3 µm poly-Si structure and from 180/m to 204/m for the 5 µm poly-Si structure.

Figure 4.12 presents the profiles as measured on three locations on the crossbars and at the base of the beams. The profiles at the base of the beams reveal elevated regions, corresponding to the poly-Si/Al pattern. Furthermore, these profiles indicate that the PIC surfaces are flat. For convenience, the vertical position of the surface of the PICs is aligned with the zero point of the vertical axis. The profiles measured over the length of the crossbars reveal that the crossbars have a concave upward curvature, corresponding to approximately 20/m. There are two effects that influence the curvature of the crossbar. Firstly, the curvature of the bimorph beams is larger than that of the waveguide beams. Secondly, the crossbar itself has a post-release curvature due to residual stress in the various oxide layers. In previously fabricated suspended SiO_2 structures without actuators, this curvature was measured to be ~87/m.

4.4.3. ACTUATION: BIMORPH ACTUATORS

The actuators are characterized by operating them with a *Keithley 2611 system sourcemeter*, while measuring their deflection with the white light interferometric profilometer. The bimorph actuators on both sides of the waveguide beams are electrically connected in parallel, and the out-of-plane deflection of the crossbar is measured at different voltage levels. To prevent the thermal runaway effect, a very safe power limit of 60 mW per actuator was imposed.

In order to obtain high quality deflection data of the narrow beams, the profilometer was operated using a 20× magnification. As a consequence, covering the full crossbar surface required multiple images to be recorded and stitched. A full crossbar measurement takes roughly 90 s, during which the voltage over the actuators is kept constant. Over this time span, the deflection can be assumed to be constant. This is confirmed by a stability experiment of a positionable waveguide array with a smaller pitch (50 µm), revealing a 0.16 µm drift in 5 min with approximately 50 mW actuation power [14].

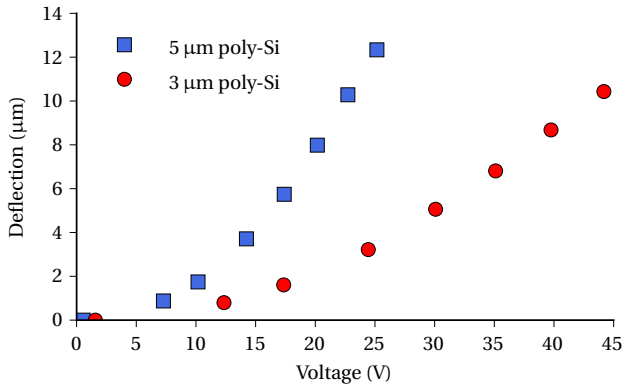


Figure 4.13: The vertical deflection of the center of the crossbar as a function of the actuator voltage.

Figure 4.13 presents the out-of-plane deflection of the center of the crossbars as a function of actuator voltage. The 3 µm actuator achieves a 10.4 µm vertical deflection (towards the chip substrate) when 44.2 V is applied. The 5 µm variant delivers 12.3 µm out-of-plane motion with an actuator voltage of 25.2 V. This difference in voltage is caused by the difference in actuator resistance. When the leftside and rightside are connected in parallel, the actuators have a mean resistance of ~15.4 kΩ and ~5.2 kΩ, for the 3 µm and 5 µm actuators respectively.

Figure 4.14 shows the out-of-plane deflection of the crossbars as a function of the total power applied to the two actuators. It can be seen that the deflection of the 5 µm version is larger than that of the 3 µm version for a given amount of dissipated power. With 120 mW power applied for example, the 5 µm thick poly-Si achieves a ~1.9 µm (or ~18 %) larger deflection than the 3 µm variant.

For an estimation of the mean actuator temperature, the change in deflection of single actuator beams due to a temperature difference is determined using the analytical model in Section 4.2.2. The analytical model shows that the deflection of the free end of a trilayer beam changes linearly with the temperature: 47 nm/°C and 52 nm/°C for the 3 µm and 5 µm poly-Si thickness, respectively. Using this linear relationship, the deflection can be plotted as a function of the estimated actuator temperature, as is presented in Figure 4.15.

The data points in Figure 4.15 correspond well with their linear fits, which is in agreement with the linear temperature dependence of the deflection following from the analytical model. Comparing the deflection values at 100 °C, 200 °C and 300 °C with the analytical results presented in Figure 4.4, they match quite well. The temperature of the

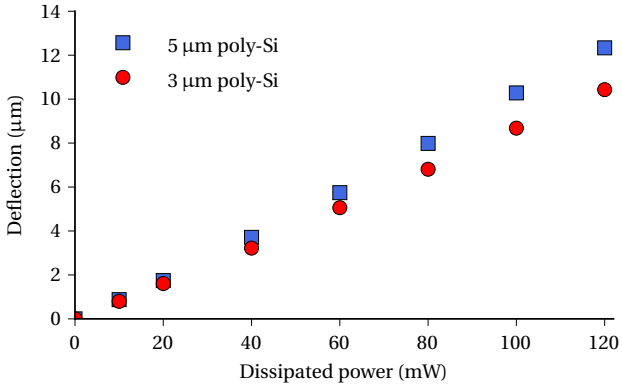


Figure 4.14: The vertical deflection of the center of the crossbar as a function of the power dissipated in the two actuators.

integrated actuators will be slightly higher than the estimated temperature, because deflecting a positionable array (consisting of both actuator beams and waveguide beams) requires more force than deflecting a single actuator beam. Nevertheless, the analytical single beam model is a good estimator for the vertical deflection of this positionable waveguide array. Additionally, based on this temperature estimate, it is safe to assume that the actuator temperature stays well below the recrystallization temperature of poly-Si, which is around 600 °C [15].

4.4.4. FREQUENCY RESPONSE

The frequency response of the positionable waveguide arrays is measured using a *Polytec MSA-400 scanning vibrometer*. From 0 kHz to 25 kHz only one resonance peak was observed for both systems. A resonance peak at 13.8 kHz was measured for the 3 µm poly-Si variant, while the 5 µm poly-Si system has a peak at 16.2 kHz, both corresponding with the first vertical resonance mode. The 5 µm poly-Si array, having a larger thickness than the 3 µm variant, has a higher out-of-plane stiffness. As a result, although the length and width are the same, the resonance frequency of the 5 µm system is higher than that of the 3 µm system.

4.4.5. BENDING STIFFNESS AND ACTUATOR FORCE

The out-of-plane bending stiffness of the array can be approximated using the measured resonance frequency. The first mode frequency f_0 and the out-of-plane stiffness k are linked by the relation

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m_{\text{crossbar}} + \frac{33}{140}m_{\text{beams}}}}, \tag{4.1}$$

where m_{crossbar} is the mass of the crossbar and m_{beams} is the mass of the waveguide and actuator beams [16]. The measured waveguide arrays consist of four waveguide beams (SiO_2 only) and eight actuator beams (SiO_2 with poly-Si).

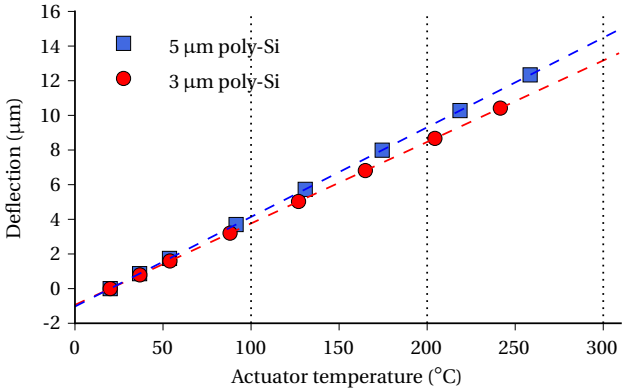


Figure 4.15: The vertical deflection as a function of the estimated actuator temperature. The dashed lines represent linear functions fitted to the data points. As a visual guide, 100 °C, 200 °C and 300 °C are indicated by dotted lines.

DETERMINING THE MASS

The out-of-plane bending stiffness of the complete system is calculated using Equation (4.1), which requires the mass of the beams and the crossbar. Figure 4.1 presents the layout of the positionable waveguide array. The total system comprises eight actuator beams, four waveguide beams, and a crossbar. The mass of the beams is approximated as follows, using the values from Table 4.2.

Waveguide beams A single waveguide beam consists of two layers. The bottom layer has a width of 18 µm, a thickness of 16 µm, and a density of 2200 kg/m^3. The top layer has a width of 18 µm, a thickness of 2 µm, and a density of 2300 kg/m^3. Furthermore, the beam length is 800 µm. The mass of a single waveguide beam $m_{\text{wg-beam}}$ is

$$\begin{aligned} m_{\text{wg-beam}} &= \rho_1 V_1 + \rho_3 V_3 \\ &= \rho_1 L b_1 t_1 + \rho_3 L b_3 t_3 \\ &= 2200\,\text{kg/m}^3 \times 800\,\mu\text{m} \times 18\,\mu\text{m} \times 16\,\mu\text{m} + \\ &\quad 2300\,\text{kg/m}^3 \times 800\,\mu\text{m} \times 18\,\mu\text{m} \times 2\,\mu\text{m} \\ &\approx 5.73 \times 10^{-7}\,\text{kg} \end{aligned}$$

Actuator beams The mass of the actuator beams depends on the poly-Si thickness. A single actuator beam consists of the same two layers comprising a waveguide beam, with an extra layer of poly-Si. The poly-Si layer has a width of 12 µm, a thickness of 3 µm, and a density of 2320 kg/m^3. Again, a beam length of 800 µm is used. The mass of a single 3 µm

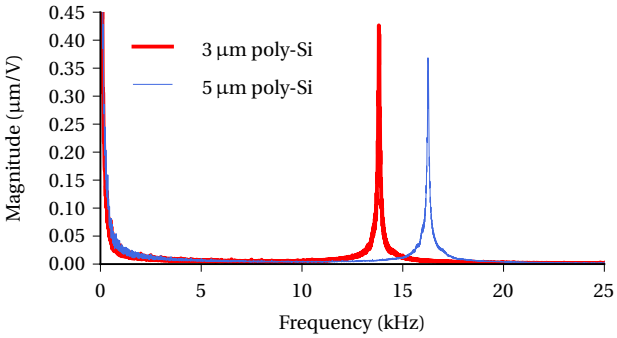


Figure 4.16: The frequency response from 0 kHz to 25 kHz. The measured resonance peaks are at 13.8 kHz and 16.2 kHz.

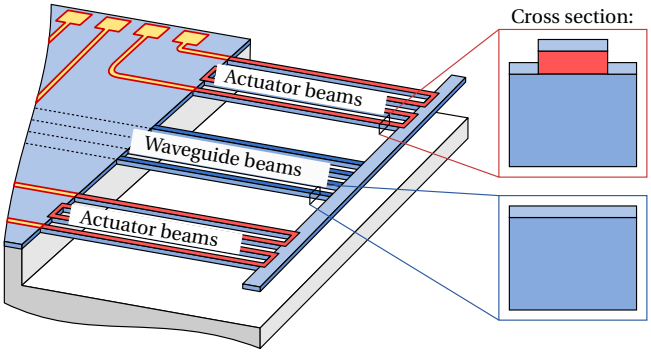


Figure 4.1: The layout of the measured arrays, indicating the cross sections of the waveguide beams and the actuator beams.

actuator beam $m_{\text{act-beam,3}}$ is

$$\begin{aligned} m_{\text{act-beam,3}} &= m_{\text{wg-beam}} + \rho_2 V_2 \\ &= m_{\text{wg-beam}} + \rho_2 L b_2 t_2 \\ &= m_{\text{wg-beam}} + 2320\,\text{kg/m}^3 \times 800\,\mu\text{m} \times 12\,\mu\text{m} \times 3\,\mu\text{m} \\ &= 5.73 \times 10^{-7}\,\text{kg} + 6.68 \times 10^{-8}\,\text{kg} \\ &\approx 6.40 \times 10^{-7}\,\text{kg} \end{aligned}$$

The mass of a single 5 µm actuator beam $m_{\text{act-beam,5}}$ is

$$\begin{aligned} m_{\text{act-beam,5}} &= m_{\text{wg-beam}} + \rho_2 V_2 \\ &= m_{\text{wg-beam}} + \rho_2 L b_2 t_2 \\ &= m_{\text{wg-beam}} + 2320\,\text{kg/m}^3 \times 800\,\mu\text{m} \times 12\,\mu\text{m} \times 5\,\mu\text{m} \\ &= 5.73 \times 10^{-7}\,\text{kg} + 1.11 \times 10^{-7}\,\text{kg} \\ &\approx 6.84 \times 10^{-7}\,\text{kg} \end{aligned}$$

Crossbar The crossbar consists of the same two layers comprising the waveguide beams. The crossbar has a width of 118 µm and a length of 1200 µm. By reducing the width of the crossbar with 32 µm, the loss of mass due to the etch holes is compensated, resulting in an effective crossbar width of 86 µm. The mass of the crossbar m_{cb} is

$$\begin{aligned} m_{\text{cb}} &= \rho_1 V_1 + \rho_3 V_3 \\ &= \rho_1 L b_1 t_1 + \rho_3 L b_3 t_3 \\ &= 2200\,\text{kg/m}^3 \times 1200\,\mu\text{m} \times 86\,\mu\text{m} \times 16\,\mu\text{m} + \\ &\quad 2300\,\text{kg/m}^3 \times 1200\,\mu\text{m} \times 86\,\mu\text{m} \times 2\,\mu\text{m} \\ &\approx 4.11 \times 10^{-6}\,\text{kg} \end{aligned}$$

The out-of-plane stiffness is calculated to be $k_{3\,\mu\text{m}} = 44\,\text{N/m}$ and $k_{5\,\mu\text{m}} = 62\,\text{N/m}$.

The produced actuator force is determined by the stiffness and the deflection of the arrays. The 3 µm system produces a force of about $F = k_{3\,\mu\text{m}}\,\delta_y = 458\,\mu\text{N}$, based on a measured vertical crossbar deflection $\delta_y = 10.4\,\mu\text{m}$. The 5 µm system produces a force of about $F = k_{5\,\mu\text{m}}\,\delta_y = 757\,\mu\text{N}$, considering a crossbar deflection of $\delta_y = 12.3\,\mu\text{m}$.

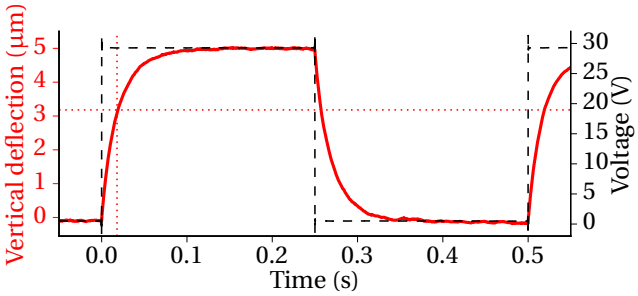
4.4.6. TRANSIENT RESPONSE

The transient thermal response of the actuators is explored, again using the *Polytec MSA-400*. By measuring the position of the free end of the actuator beams, the response to switching the state of the actuator (on/off) can be obtained. The out-of-plane displacements induced by an applied low frequency (2 Hz) square wave are presented in Figure 4.2a (3 µm actuators) and Figure 4.2b (5 µm actuators). An amplitude of 29 V was used for the 3 µm actuators and 16 V for the 5 µm actuators in order to obtain a deflection close to 5 µm.

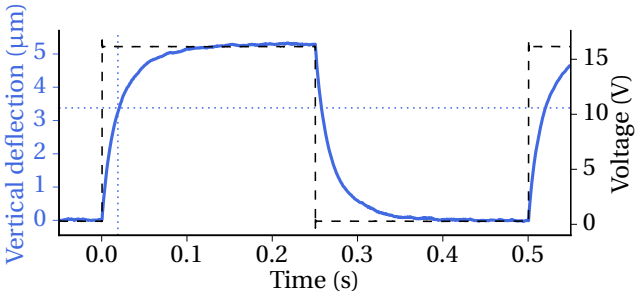
According to the measurements, the vertical deflection changes exponentially with time. The thermal response of the bimorph actuators is governed by heat transfer taking predominantly place through convection and conduction, since the effect of radiation is negligible at the scale of the actuators. A steady temperature distribution is obtained after roughly 0.1 s, for the two types of tested actuators. The 63.2 % time constant of the 3 µm variant was found to be 18 ms. For the 5 µm system, the 63.2 % time constant was measured to be 19 ms. No significant difference between rise and fall times was observed, indicating that the time required for heating and cooling is about the same.

4.5. DISCUSSION AND CONCLUSIONS

The fabricated positionable waveguide arrays have a curved crossbar, which introduces a vertical misalignment in case more than two waveguides need to be aligned with two



(a) Actuators with 3 µm poly-Si thickness.



(b) Actuators with 5 µm poly-Si thickness.

Figure 4.2: The vertical deflection (solid line) of a point on the crossbar resulting from an applied square wave voltage (dashed line). The plots indicate the 63.2 % level (horizontal dotted line) and the corresponding time value (vertical dotted line).

other waveguides. This crossbar curvature can be prevented by adjustments in the design/fabrication. By covering the waveguide beams with a layer of poly-Si similar to the layer on the actuator beams, all beams will have the same curvature. The consequence of this will be that the total structure becomes stiffer, and a smaller deflection will be obtained with the same actuators. Another cause for the crossbar curvature is residual stress, resulting from the PECVD SiO_2 layer that is deposited on top of the TriPleX crossbar. In the presented designs, the PECVD SiO_2, which aims to protect the poly-Si from being etched, is exclusively removed at the bondpad locations. By also removing the PECVD SiO_2 layer from the crossbar (except where it is needed to protect poly-Si), the crossbar will not be curved by residual stress in the PECVD SiO_2/TriPleX combination.

The bimorph actuators are measured to provide a downward deflection of approximately 11 µm when operated simultaneously at 60 mW per actuator side. The expected maximum deflection that can be obtained, based on extrapolation of the measured data, is about two times as large, as the actuators can be driven to approximately 125 mW before reaching the thermal runaway point.

The analytical model and the experimental results reveal that the design of the bimorph beams affects the actuator stroke and the postrelease deflection in a similar way. For example, it was shown that a poly-Si thickness that optimizes the stroke also maximizes the

postrelease deformation. The coupling between the postrelease deformation and the actuator stroke can be conflicting for some applications.

For the alignment concept, a postrelease deformation in the order of 10 μm and an actuator stroke of about 4 μm would be ideal. The 10 μm postrelease deformation ensures that, when the two PICs are flip-chip bonded, the opposing waveguide cores have an appropriate initial vertical offset such that driving the actuators reduces this offset. The 4 μm actuator stroke is sufficient to compensate any vertical misalignment introduced in the pre-alignment. The presented positionable waveguide array design results in an actuator stroke which is more than sufficient to perform the fine-alignment, whereas the postrelease deformation is about seven times larger than required. As a result, the postrelease deformation causes the crossbar to have a vertical offset of approximately 70 μm with respect to the waveguides of the PIC, preventing a decent photonic alignment.

Actuator design improvements can be implemented to make the bimorph actuators better suited for specific applications. For example, covering only a particular region of the actuator beams with poly-Si significantly reduces the postrelease deformation, while the actuator stroke only decreases slightly [8]. Another approach to adjusting the postrelease deformation is by controlling the stress and the stress gradient within the poly-Si layer, which is demonstrated in [17]. For certain applications, the associated increase in complexity of the fabrication process might well be a justifiable investment.

This chapter presented a thorough characterization of the vertical (out-of-plane) translation of the positionable waveguide arrays, based on driving both actuator sides simultaneously. By actuating one actuator side more than the other, the crossbar can be moved downward while it simultaneously is slightly rotated around the propagation direction of the light. This kind of actuation is beneficial for the photonic alignment concept, in case of rotational misalignment resulting from the pre-alignment step. Moreover, the photonic alignment concept will require horizontal (in-plane) translation of the positionable waveguide array, as acceptable coupling loss between the photonic waveguides can only be attained with submicrometer in-plane alignment precision.

The experiments revealed a difference in resistance of the actuators on the left and the right side, probably due to the length difference of the electrical leads. Driving both actuators with an equal voltage might result in an imbalance in the deflection of both sides. Regarding the photonic alignment, this resistance dissimilarity is not expected to be problematic, because active alignment will be applied to obtain the optimal alignment. For applications that do not provide any feedback on the position, the electrical leads are best designed to have equivalent resistance values.

No strict requirements are imposed on the time constant, in case the bimorph actuators are utilized for fine-aligning purposes, as in the alignment concept. For other SiO_2 MEMS applications however, it can be beneficial to have a small time constant. With 63.2 % time constants smaller than 20 ms, both the 3 μm and 5 μm system are able to switch between 0 μm and 5 μm vertical deflection roughly five times per second. When operated at the resonance frequency (13.8 kHz and 16.2 kHz), even higher frequencies can be achieved.

In conclusion, this chapter presented the integration of electrothermal actuators with a photonic material platform that predominantly consists of thick SiO_2. Using a special silicon reinforcement method, fracturing was prevented and suspended SiO_2 beam structures were fabricated. Positionable arrays of photonic waveguides were realized by integrating

thermal out-of-plane bimorph actuators. The actuators were created using two different poly-Si thicknesses on top of SiO_2 beams, enabling the comparison of the different poly-Si thickness variants.

The positionable waveguide arrays have a significant postrelease out-of-plane deflection. The crossbars of the arrays with a beam length of 800 µm are located 60 µm and 80 µm above the chip surface of the 3 µm and 5 µm variant, respectively.

The bimorph actuators, when operated simultaneously, provide an out-of-plane deflection of the crossbar of approximately 11 µm at 60 mW dissipated power per actuator side, corresponding to a temperature in the order of 240 °C. Analytical model results of single bimorph beams give a reasonable estimate of positionable waveguide array deflections. The actuators deliver an estimated force of 450 µN and 750 µN for the 3 µm and 5 µm poly-Si thickness, respectively. The time constants were found to be 18 ms for the 3 µm and 19 ms for the 5 µm variant. By adjusting the design of the actuators, their performance can be tuned to meet application-specific requirements.

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5

WAVEGUIDE ARRAY POSITIONING

In the previous chapter, the feasibility of actuator fabrication was investigated and the actuator performance was characterized. This chapter presents a more thorough investigation of positionable waveguide arrays with respect to the alignment concept. The design space of positionable photonic waveguide arrays (WGAs) is explored in Section 5.2 and a way to quantify the positioning performance is presented. In Section 5.3, the effect of relevant design parameters on the positioning performance is studied on the basis of a finite element model (FEM), and is substantiated by measurements on realized WGAs. In Section 5.4, a number of waveguide arrays with differing design parameters is fabricated and characterized, and the results are compared to the outcome of the FEM. This way, design conditions for sub-micrometer precise alignment are established. In addition, optical chip-to-chip alignment using the proposed concept is demonstrated in Section 5.5.

Based on
T.-J. Peters, M. Tichem, *On-Chip Positionable Waveguides for Submicrometric Photonic Alignment,* Journal of Microelectromechanical Systems 26 (6), 1259-1271 (2017)
(with modifications to Section 5.4.2)

5.1. INTRODUCTION

PACKAGING, which is the integration of components in a housing, is a large contributor to the overall cost of photonic end products. Photonic integrated circuits (PICs) used to be the most expensive components of photonic packages. As the design and manufacturing technology of PICs have evolved over the past decades, fairly complex chips can now be produced against reasonable cost. However, the developments in packaging are lagging behind. As a result, particularly when multiple optical and electrical connections are required, the packaging costs become dominant.

Particularly the precision alignment of photonic components amounts to a substantial part of the packaging costs. Realizing electrical connections to a PIC benefits from the established field of microelectronics, whereas making optical connections is less straightforward because of the tight alignment tolerances required for low optical loss. Because of the variety in PIC material platforms and package configurations, the photonic alignment commonly relies on tailor-made solutions.

This lack of standardization hampers photonic applications to make the transition from a research state to a commercial product [1–3]. Automation of photonic alignment is challenging and the use of dedicated robotic assembly systems may lead to substantial cycle times. A cycle-time (including process setup time) in the order of one hour is mentioned in [4] for the active alignment of a single mode fiber with a grating coupler.

For the future of PICs, it is crucial that photonic alignment technology catches up with the developments of photonics in general. As integrated photonics technology matures, the number of optical ports grows, increasing the difficulty of photonic alignment even further.

A novel alignment concept [5], offering an increased level of automation, has the potential to replace the customized alignment solutions applied in many photonic applications. The essence of this alignment concept is to integrate mechanically flexible waveguides and positioning functions into a single PIC. This combination results in positionable waveguides that can be fine-aligned with the waveguides of another PIC. Once they are fine-aligned, the waveguides are to be locked in their optimal position for the lifetime of the product. This paper is limited to actuation in two directions: out-of-plane translation and rotation around the propagation direction of the light. For a fully functional system, also in-plane translation needs to be dealt with, as well as the position locking after alignment. Solutions for these functions are part of ongoing work and are not treated in this paper.

The research into integrating actuator technology and optical waveguides started more than two decades ago. In a review paper, Chollet distinguishes three types of co-integration: monolithic, hybrid and stacked co-integration [6]. The combinations mentioned in this review paper show a variety of waveguide materials, e.g. GaAs [7], InP [8], polymer [9], and Si [10]. The co-integration presented in the current paper falls in the stacked category, as thermal MEMS actuators are integrated by depositing extra material on top of a silicon nitride (Si_3N_4) / silicon dioxide (SiO_2) waveguide material platform.

5.2. DESIGN PARAMETERS AND POSITIONING REQUIREMENTS

Positionable photonic waveguide arrays are developed and realized in photonic chips, based on the TriPleX Si_3N_4/SiO_2 waveguide technology. The fabrication process consists of two consecutive sequences, as illustrated in Figure 5.1. First, photonic waveguides are created by the formation of a $SiO_2/Si_3N_4/SiO_2$ (lower cladding / core / upper cladding) layer stack on a silicon wafer. After that, the MEMS fabrication sequence creates mechanically flexible, suspended waveguide structures. The suspended waveguide structures consisting mostly of SiO_2 tend to fracture due to compressive residual stress in the SiO_2. The temporary reinforcement method from Chapter 3 is implemented to prevent the waveguide structures from fracturing at the moment they are released.

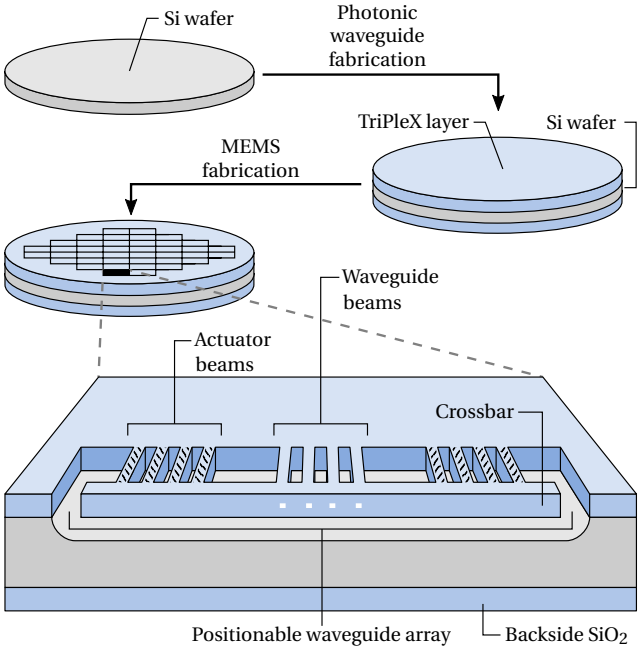


Figure 5.1: Schematic overview of the fabrication of positionable WGAs. Top: the optical waveguide functionality is realized first, followed by the MEMS fabrication. Bottom: a close-up view of a single positionable WGA.

First, the photonic layer stack is plasma etched to obtain the desired waveguide structure pattern. The same pattern is then anisotropically etched into the underlying silicon. Next, an isotropic silicon etch releases the waveguide structures. By locally applying a passivation layer on the silicon sidewalls prior to this etch, the suspended waveguide structures are reinforced by a layer of silicon. This silicon reinforcement reduces the expansion and buckling, preventing the structure from fracturing. Electro-thermal actuators are integrated with the suspended structures by depositing and patterning poly-Si on top of the TriPleX material. More details on the fabrication process can be found in Appendix A.

Positionable WGAs consist of waveguide beams and actuator beams that are designed with the same length and which are mechanically connected at their free ends by a crossbar, as illustrated in Figure 5.1. A number of waveguide beams, four in the figure, is situated at

the center. A set of thermal actuator beams is placed on both sides of the waveguide beams, for out-of-plane motion and rotation around the propagation direction of the light.

The photonic waveguide beams are based on single stripe Si_3N_4 waveguide cores that are embedded in a SiO_2 cladding. These Si_3N_4 cores are 220 nm in thickness and up to 1.5 µm in width, ensuring they are mostly single-mode at a wavelength of 1550 nm. Moreover, 220 nm is a standard Si_3N_4 layer thickness for many applications that are based on the SiO_2 / Si_3N_4 material platform. The waveguide beams have a total thickness of 16 µm and a total width of 18 µm. The actuator beams consist of SiO_2 beams (without waveguiding cores) with the same cross-sectional dimensions as the waveguide beams. To create thermal bimorph actuators, a strip of poly-Si is patterned on top of the beams. The poly-Si also functions as a resistive heater, the resistivity of which is determined by the level of boron doping applied.

The fabrication requires a total of six photolithography masks. A single 100 mm wafer comprises 140 chips, each measuring 6 mm × 6 mm. Every chip contains one or two positionable arrays, depending on the width of the array.

Figure 5.2 shows the layout of a typical positionable WGA, indicating the design parameters that define a particular configuration. An even number of actuator beams is located on every side of the waveguide beams. For one set of actuator beams, the poly-Si is designed in a meandering shape, i.e. all actuator beams on one side are electrically connected in series, creating a two-terminal element.

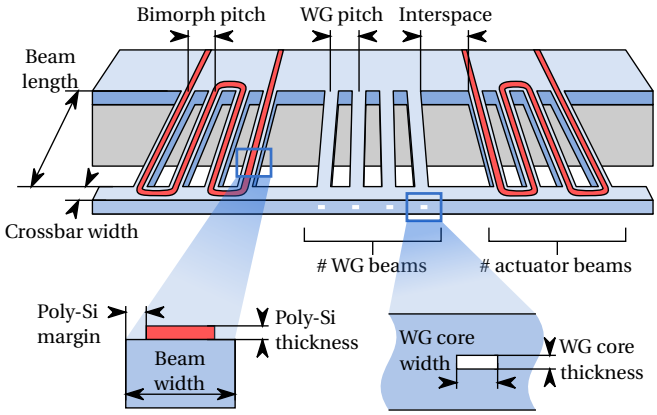


Figure 5.2: Typical WGA layout, showing the design parameters of the system.

Positioning requirements can be specified based on the residual misalignment resulting from the assembly. In the final assembly configuration, the chips are mounted through flip-chip technology exploiting eutectic gold tin (AuSn) thin film solder layers, providing an expected vertical precision of ±1 µm per chip [11]. As a result, the expected maximum vertical misalignment from chip to chip is roughly 2 µm. Taking into account some margin, we target for 4 µm vertical motion range of the WGA. Additionally, the actuators must be able to compensate a rotational misalignment of up to approximately 0.05°, based on a 4 µm vertical height difference over a chip size of 5 mm. Furthermore, as the positionable WGAs are designed for alignment to a counter PIC of which the waveguides are located in a

flat plane, the WGA's waveguide core positions should not deviate more than 100 nm from a straight line to keep the loss level of all channels acceptable.

The positioning performance is quantified by the introduction of positioning indicators, which are all based on the linear approximation of the positions of the waveguide cores, G, as shown in Figure 5.3. Initially, so without any actuation, the vertical deflection of the crossbar is represented by Y_{off}, which is measured between the points in the center of the segments where the waveguides are located. Due to the curved shape of the crossbar, the waveguide cores have a certain vertical deflection, V, measured perpendicular to G_{off}. The range of the waveguide cores, R, is defined as the maximum distance between the cores above and below G, or $V_{\text{max}} - V_{\text{min}}$. In the specific situation without actuation, we refer to this range as R_{off}.

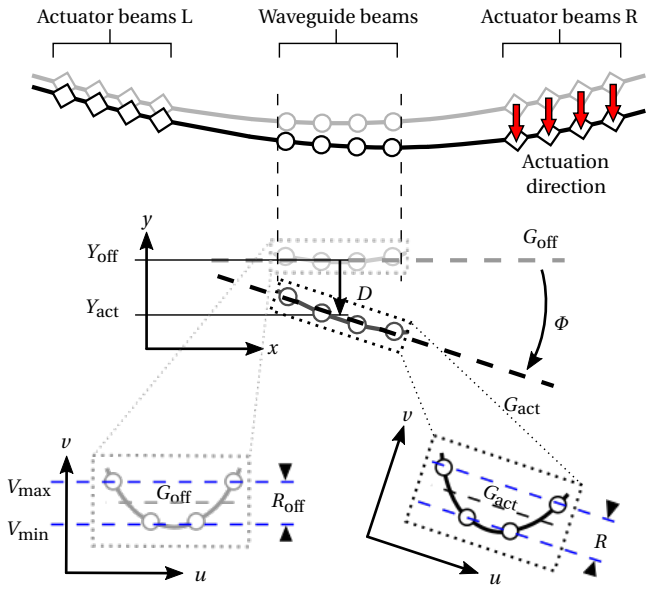


Figure 5.3: Schematic representation of a WGA's crossbar shape with one activated actuator side. The positioning of the crossbar is quantified using three positioning indicators: deflection D, angle Φ, and waveguide core range R.

In actuation mode, additional positioning indicators are required to describe the performance of the system. The vertical deflection of the crossbar is now represented by Y_{act}. The range, R, is now measured perpendicular to G_{act}. For this reason, a moving coordinate system (u, v) is introduced, and similar to the intitial situation we define $R = V_{\text{max}} - V_{\text{min}}$. Positioning parameter D represents the change in vertical deflection with respect to the non-actuated situation, or $Y_{\text{off}} - Y_{\text{act}}$. Angle Φ is the angle between G_{off} and G_{act}.

Table 5.1: The material properties as used in the finite element model.

Material	Coefficient of thermal expansion (1/K)	Young's modulus (GPa)	Poisson's ratio	Density (kg/m^3)
SiO_2	0.5×10^{-6}	70	0.17	2200
Poly-Si	$\alpha_{Si}(T)$	160	0.22	2320

5.3. MODELING

A 3D finite element model is developed in order to comprehend the relation between the WGA design parameters and the positioning indicators. The model takes into account the residual thermal stress from the fabrication process, based on the deposition temperatures of the different materials. This way, the model produces the post-release deformation of the WGA at room temperature. Without actuation, the actuator beams push the outer parts of the crossbar upward while the waveguide beams pull the center of the crossbar downward. The actuator operation of the WGA is also implemented in the model, by imposing a uniform temperature on the actuator beams. When activated, the actuator beams move the crossbar downwards. At the same time, this will also reduce the curvature of the crossbar.

Since we are interested in discovering trends rather than developing a very detailed model, the model is kept as simple as possible, which helps to reduce the calculation time. The most important approximations of the model are discussed here. The waveguide beams are approximated by SiO_2 beams, and the Si_3N_4 waveguide cores are not included. Furthermore, all the beams in the model have a rectangular cross-section, while the fabricated devices have slightly slanted sidewalls (due to the etching process). Additionally, the model does not include the layer of SiO_2 that is deposited on top of the poly-Si in order to protect it from being etched (see Section 4.3 for more details on this). For the thermal actuators, a uniform temperature is applied to the poly-Si strips and the supporting SiO_2 beams, rather than implementing Joule heating. The crossbar is provided with etch holes similar to the ones in the fabricated devices, in order to accurately emulate the stiffness of the crossbar.

The material properties that are used in the model are presented in Table 5.1. The coefficient of thermal of expansion of poly-Si is implemented as a function of temperature, based on the empirical formula by Okada [12]:

$$\alpha_{Si}(T) = c_1\left(1 - e^{-c_2(T-c_3)}\right) + c_4 T, \tag{5.1}$$

with

$$\begin{aligned} c_1 &= 3.725 \times 10^{-6}/\mathrm{K}, \\ c_2 &= 5.88 \times 10^{-3}/\mathrm{K}, \\ c_3 &= 124\,\mathrm{K}, \\ c_4 &= 5.548 \times 10^{-10}/\mathrm{K}^2. \end{aligned}$$

In order to distinguish the effect individual design parameters have on the deformation of the WGA, a benchmark WGA is defined. By varying only one of the design parameters of

this benchmark at a time, its isolated influence on the deformation can be determined. The benchmark WGA consists of four waveguide beams and two sets of four actuator beams with a beam length of 800 µm, a waveguide beam pitch of 127 µm, an actuator beam pitch of 50 µm, a poly-Si thickness of 5 µm and a crossbar width of 118 µm. Figure 5.4 includes a graphical representation of the finite element model of the benchmark WGA.

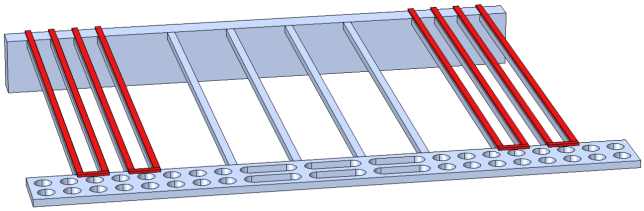


Figure 5.4: Representation of the finite element model of the benchmark WGA. This design has four actuator beams (with poly-Si in red) on each side and four waveguide beams in the middle. The WGA includes etch holes in the crossbar, similar to the fabricated WGAs.

The predicted effect of the beam length on Y, R, and Φ is presented in Figures 5.5a to 5.5c, respectively. The postrelease deformation (the state at room temperature without actuation) is indicated by the grey curve (labeled 'Off' and with filled circles as marker symbol). Two actuated situations are included in the graphs, the blue curve (labeled 'L' and with crosses as marker symbol) representing actuation of the left side and the red curve (labeled 'R+L' and with plusses as marker symbol) representing simultaneous actuation of both sides. For the actuated state, an actuator temperature of 220 °C is applied.

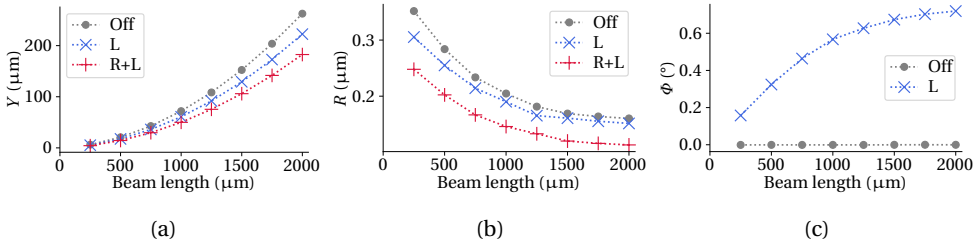
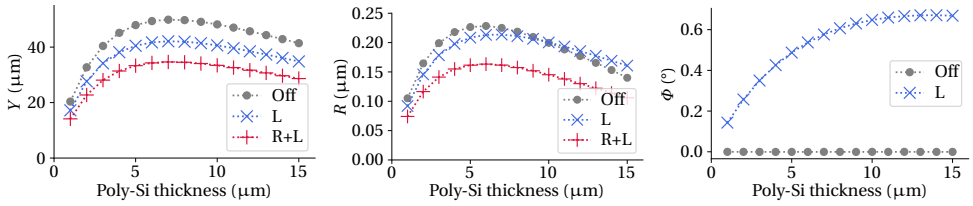


Figure 5.5: The modeled (a) postrelease deflection Y, (b) range R, and (c) angle Φ as a function of the beam length.

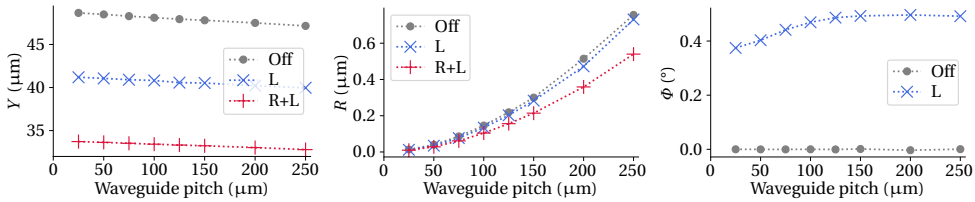
The plots in Figure 5.5 show that the various positioning indicators have clear trends as a function of beam length. In order to quantify these trends, values are extracted from the plots indicating the effect on the initial situation and on the situation with actuation. For the initial deformation, the curves labeled 'Off' are relevant. From Figure 5.5a we see that the initial deflection Y_{off} changes from almost zero (at the shortest beams) to more than 250 µm (at the longest beams), amounting to $\Delta Y_{\text{off}} = Y_{\text{off}}^{\text{max}} - Y_{\text{off}}^{\text{min}} =$ an increase of 256 µm. Similarly, Figure 5.5b provides (based on the grey curve labeled 'Off') $\Delta R_{\text{off}} = R_{\text{off}}^{\text{min}} - R_{\text{off}}^{\text{max}} =$ a decrease of 191 nm.

For the effect of actuation, the difference between the initial ('Off') and actuated ('R+L or L') curves is analyzed. Looking at Figure 5.5a again, we see that the difference between



(a) (b) (c)

Figure 5.6: The modeled (a) postrelease deflection Y, (b) range R, and (c) angle Φ as a function of the poly-Si thickness.



(a) (b) (c)

Figure 5.7: The modeled (a) postrelease deflection Y, (b) range R, and (c) angle Φ as a function of the waveguide beam pitch.

the initial deflection ('Off') and the deflection due to simultaneous actuation ('R+L') changes from almost zero (at the shortest beams) to 78 µm (at the longest beams). In other words: $\Delta D = D_{max} - D_{min} = (Y_{off}^{max} - Y_{R+L}^{max}) - (Y_{off}^{min} - Y_{R+L}^{min}) = 78\,\mu m - 0\,\mu m$ amounting to an increase of 78 µm. The change of the range R as a function of beam length is extracted from Figure 5.5b by also looking at the minimum and maximum difference between the initial range ('Off') and the range at simultaneous actuation ('R+L'). The range R decreases more with short beams as it does with longer beams: $\Delta R = (R_{off}^{min} - R_{R+L}^{min}) - (R_{off}^{max} - R_{R+L}^{max})$ = a decrease of 57 nm. Finally, a value for the change in angle Φ is obtained from Figure 5.5c. At the shortest beam length, actuation of the left side rotates the crossbar by almost 0.2°, while a rotation of more than 0.6° is achieved with the longest beams. Hence, the actuated angle Φ increases by 0.56° over the modeled beam length range, or $\Delta\Phi = (\Phi_{off}^{max} - \Phi_{L}^{max}) - (\Phi_{off}^{min} - \Phi_{L}^{min}) = 0.56°$.

Additionally, the trends of Y, R, and Φ as a function of the poly-Si thickness, the waveguide pitch, the crossbar width, the number of waveguide beams, and the number of actuator beams are presented in Figures 5.6 to 5.10. Values representing the trends are acquired in a similar way as it was done for the beam length.

Table 5.2 includes the acquired values, providing a quantitative representation of the effect of the different design parameters on the positioning indicators. Every row represents a design parameter that is increased over the specified range, whereas the columns display the corresponding change in positioning indicators. The poly-Si thickness is split into two regions, because of the peak in D and R around 7 µm. The values in Table 5.2 can be used to compare the influence of different design parameters on a single positioning indicator. In order to accentuate the most dominant relations, a threshold value is introduced, spec-

ified as half the average of the absolute values in the same column. Only the values that exceed this threshold value are regarded as significant (++ or - -) relations.

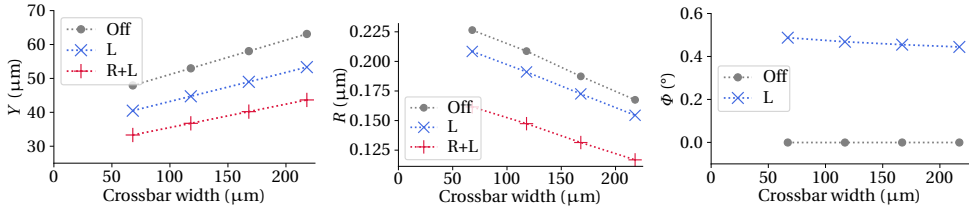


Figure 5.8: The modeled (a) postrelease deflection Y, (b) range R, and (c) angle Φ as a function of the crossbar width.

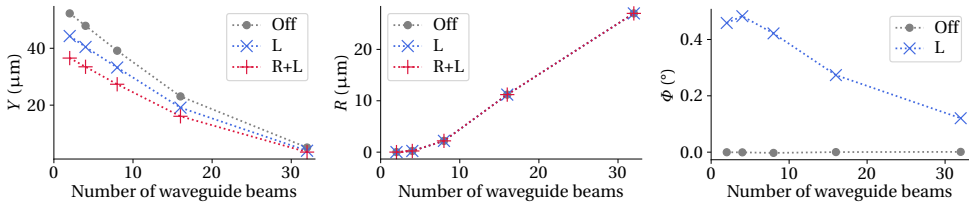
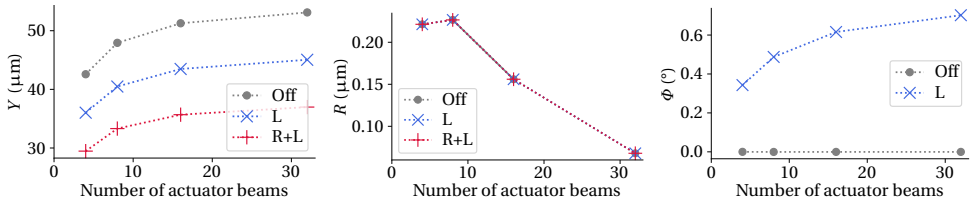


Figure 5.9: The modeled (a) postrelease deflection Y, (b) range R, and (c) angle Φ as a function of the number of waveguide beams.

In Table 5.2, the most dominant correlations are indicated by shaded cells. A correlation is considered to be dominant if a cell's absolute value is larger than half of the average of all the absolute values of the corresponding column. For the row representing the number of waveguide beams, the value corresponding to R_{off} is neglected in calculating the average value, as this value has an extreme deviation from the average. According to the shaded cells, the most significant design parameters are the beam length, the poly-Si thickness, the waveguide beam pitch, the number of waveguide beams, and the number of actuator beams. However, as for functional systems the number of actuator beams usually scales with the number of waveguide beams, the effects of individually increasing waveguide beams and actuator beams are attenuated, and we do not consider them to be dominant design parameters. Below, the trends of the beam length, the poly-Si thickness, and the waveguide beam pitch are discussed.

Increasing the beam length significantly elevates Y_{off}, D, and Φ, improves R_{off}, but reduces R, according to the model. This is as can be expected. Longer beams have the same beam curvature over a longer distance, amounting to an increased Y_{off} as a function of beam length. When actuated, the curvature decreases, and this effect is amplified with longer beams, leading to Y and Φ increasing as a function of beam length. Moreover, as longer beams are more compliant than shorter beams, the crossbar will be less deformed



(a) (b) (c)

Figure 5.10: The modeled (a) postrelease deflection Y, (b) range R, and (c) angle Φ as a function of the number of actuator beams.

Table 5.2: Modeled quantitative effect of individual design parameters on WGA performance. The values indicate the correlations with respect to design parameter changes. Increasing a design parameter leads to a change of positioning indicators. The most dominant correlations are indicated by the shaded cells.

		Initial deformation		Deformation by actuation		
Design parameter	Parameter values	ΔY_{off} (µm)	ΔR_{off}(nm)	ΔD (µm)	ΔR (nm)	$\Delta\Phi$ (°)
Beam length	250 µm to 2000 µm	256.2	191	78.0	57	0.56
Poly-Si thickness	1 µm to 7 µm	29.5	123	9.0	34	0.43
Poly-Si thickness	7 µm to 15 µm	8.5	85	2.5	29	0.09
Waveguide pitch	25 µm to 250 µm	1.5	742	0.6	212	0.12
Crossbar width	68 µm to 218 µm	15.2	59	4.8	14	0.04
Number of wg beams	2 to 32 beams	47.2	26 999	14.1	0	0.36
Number of actuator beams	4 to 32 beams	10.5	159	3.0	0	0.36
Half the average of the absolute values		26.3	113	8.0	25	0.14

by the waveguide beams and actuator beams as the beam length increases. This results in R_{off} and R decreasing as a function of beam length.

For the poly-Si thickness, only the trends below a value of 7 µm are considered. The model predicts that increasing the poly-Si thickness has a positive and significant effect on all positioning indicators. This is in agreement with the theoretical models (e.g., the Timoshenko composite beam theory [13]) describing the curvature of bilayer beams.

Increasing the waveguide beam pitch has a significant positive effect on R_{off} and R, and a less significant effect on the other positioning indicators, according to the model. As the waveguide beam pitch increases, the length of the crossbar grows. The longer the crossbar, the more compliant it will be. In the non-actuated state, the actuator beams will push the sides of the crossbar upwards, while the waveguide beams tend to pull the center of the crossbar down. Hence, it can be expected that, as the waveguide pitch increases, the crossbar will be more deformed, and R will increase. In the actuated situation, a crossbar that is more compliant and deformed due to a larger waveguide pitch is easier to straighten by actuating both sides simultaneously as compared to a crossbar that is less deformed but stiffer due to a smaller waveguide pitch.

In Table 5.3, a qualitative representation of the effect of the different design parameters on the performance of the WGA is provided. The symbols in the table (which are based on the data in Table 5.2) indicate how positioning indicators are affected by design parameters. Individual design parameters are increased, causing the positioning indicators to either in-

Table 5.3: Modeled qualitative effect of individual design parameters on WGA performance. The symbols indicate the correlations with respect to design parameters changes. Increasing a design parameter leads to a strong increase (++), moderate increase (+), moderate decrease (-), strong decrease (- -) or no change of positioning indicators.

	Initial deformation		Deformation by actuation		
Design parameter	ΔY_{off}	ΔR_{off}	ΔD	ΔR	$\Delta \Phi$
Beam length	++	- -	++	- -	++
Poly-Si thickness (< 7 µm)	++	++	++	++	++
Waveguide pitch	-	++	-	++	+
Crossbar width	+	-	+	-	-
Number of wg beams	- -	++	- -	0	- -
Number of actuator beams	+	- -	+	0	++

crease (+ and ++), decrease (- and - -), or remain unaltered (0). Two symbols indicate a stronger response compared to a single symbol. It must be noted that only column-wise comparison of the symbols is valid. The most dominant design parameters are the beam length, the poly-Si thickness, and the waveguide beam pitch. The influence of the crossbar width, the number of waveguide beams, and the number of actuator beams was also investigated, but for these design parameters the model outcome indicated a non-significant effect on the WGA performance. According to the model, with increased beam length the crossbar will have a higher initial out-of-plane deflection (Y_{off}), and the waveguide cores will be confined to a smaller range (R_{off}). Also, with larger beam length the motion ranges will increase (D and Φ). The range upon actuation R will reduce less when beam length is increased, i.e. the curvature the crossbar initially has will be reduced upon actuation, but the magnitude of this effect reduces as the beam length increases. Additionally, the model predicts that increasing the poly-Si thickness (<7 µm) leads to a significant increase of all positioning indicators. Finally, the waveguide beam pitch significantly affects the out-of-plane bending stiffness of the crossbar. Hence, with increasing pitch it can be expected that the initial waveguide core range R_{off} increases, which is confirmed by the model. Also, the model indicates that there is a positive correlation between R and the waveguide beam pitch. The model suggests that the positioning performance can be optimized by tuning these design parameters; however, there are trade-offs to be taken into account. For instance, a small Y_{off} in combination with a large D is a conflicting demand, as these cannot be optimized in one design. A very important demand is the high precision in waveguide alignment, which suggests to minimize the values for R_{off}. The model indicates that this can be achieved particularly by reducing the waveguide pitch, and by reducing the poly-Si thickness as well as increasing the beam length.

5.4. RESULTS I, EFFECT OF DESIGN PARAMETERS

Figure 5.11 shows a realized photonic MEMS chip that is singulated, mounted on a custom PCB, and electrically connected to the PCB by wirebonds. Ten waveguide cores are visible, only the middle four of which are used by this specific WGA.

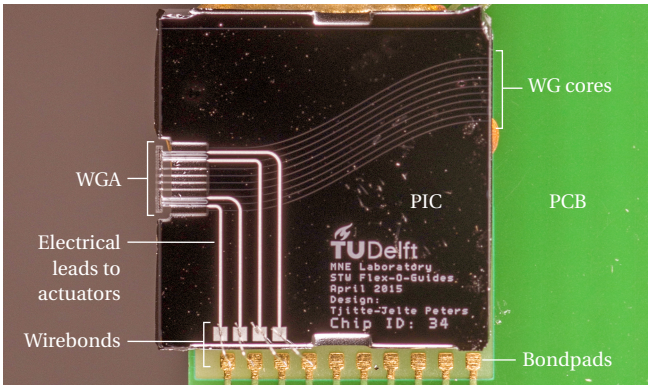


Figure 5.11: Photograph (topview) of a realized PIC with positionable waveguide array (type A), mounted on a PCB and electrically connected by wirebonds.

5

5.4.1. METHOD

The performance of selected realized WGAs is determined by operating the actuators with a *Keithley 2611 system sourcemeter*, while simultaneously measuring the surface contour of the WGA using a *Bruker Contour GT-K 3D* optical (white light) profilometer. Simultaneous measurement of the crossbar top-surface and a nearby positioned reference surface are performed for different levels of dissipated power in the actuators.

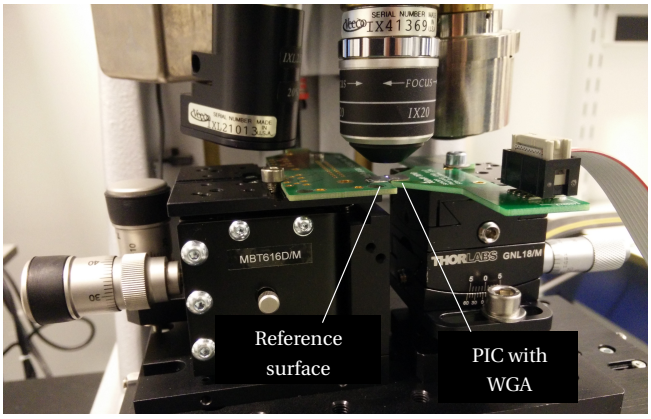


Figure 5.12: Photograph of the measurement setup as used for the actuation measurements. The reference surface (left) and the PIC (right) are located on stages for manual alignment. The out-of-plane surface contour is measured using a white light profilometer, of which the lenses are pictured. The position of the WGA is controlled by an external power source.

The reference surface is used to calibrate the sequential crossbar measurements by providing a common height reference. Figure 5.13 shows an example of a surface measurement, in which black and white rectangle outlines indicate the regions of the crossbar and reference surface that are used for further analysis. Only the crossbar areas of the WGAs are measured, in order to keep the runtime of the measurement at an acceptable level. A

consequence of measuring crossbars (as opposed to measuring the full WGA including the beams) is that only the relative deflection is known, and not for example the initial vertical deflection of the crossbar.

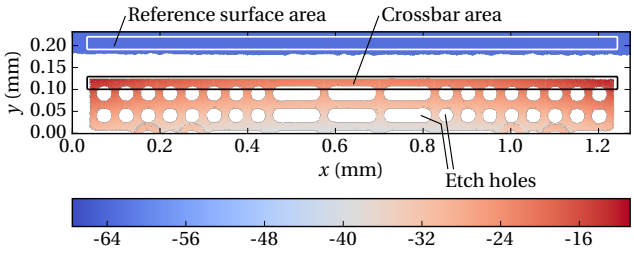


Figure 5.13: Surface contour measurement (top view) of a WGA, with the height data in µm. The crossbar area (within the black rectangular outline) is calibrated by subtracting the reference surface area (within the white rectangular outline). The calibrated crossbar profile is obtained by extracting a mean profile over the length of the calibrated crossbar area.

Figure 5.14 shows three exemplifying calibrated crossbar profiles. The presented profiles are obtained from three different measurements: without actuation, actuation of the right side only, and actuation of the left side only. The profiles illustrate the crossbar moves downward upon actuation. Moreover, the noise level of the profiles is higher than the expected surface roughness. The standard deviation of the noise of the calibrated profiles is calculated to be 0.2 µm. Among the sources of noise are the spikes that occur at a regular pitch, which are a result of the Si_3N_4 cores affecting the measurements of the optical profilometer.

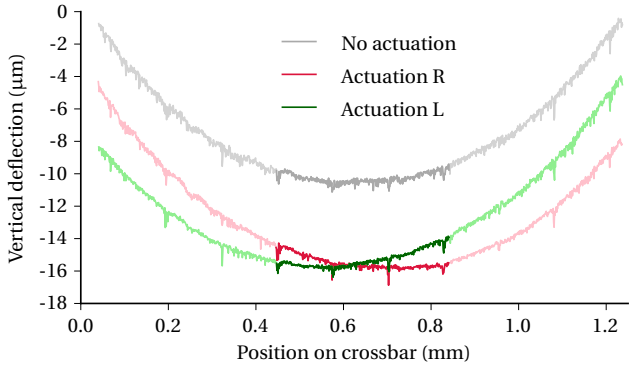


Figure 5.14: Three exemplifying calibrated profiles extracted from three surface contour measurements. The darker areas indicate the regions within the two outer waveguide beams.

The measured WGAs are operated using three actuation modes, which are defined as follows. **Right:** Operating the actuator beams on the right side of the waveguide beams. **Left:** Operating the actuator beams on the left side of the waveguide beams. **R + L:** Simultaneously operating the actuators on both sides of the waveguide beams. The positioning

indicators D, Φ, and R are determined using these three actuation modes, so that they can be plotted as a function of dissipated power.

5.4.2. EFFECT OF DESIGN PARAMETERS

From the finite element analysis we have an estimation of how the design parameters influence the positioning indicators. A benchmark system is defined with the following design parameters: four waveguide beams and eight actuator beams with a beam length of 800 µm, waveguide pitch of 127 µm, poly-Si thickness of 5 µm and a crossbar width of 118 µm. By varying only one of the design parameters at a time, the expected influence of that specific parameter on the positioning indicators is determined. Measurements of two benchmark WGAs that only differ in actuator layer thickness are used to verify the predicted effect of the poly-Si thickness on the deformation. These two WGAs will be referred to as WGA A (3 µm thick poly-Si) and WGA B (5 µm thick poly-Si).

The model outcome of WGA A and WGA B is presented in Figure 5.15. The vertical deflection D, crossbar angle Φ, and vertical range of the waveguide core positions R are plotted as a function of actuator temperature. The measurement results of WGA A and WGA B are presented in Figure 5.16, showing the vertical deflection D, crossbar angle Φ, and vertical range of the waveguide core positions R as a function of power dissipated in the actuator(s). A positive D corresponds to a downward movement of the crossbar. In Chapter 4 it was estimated that 60 mW of dissipated power corresponds to an actuator temperature of 240 °C.

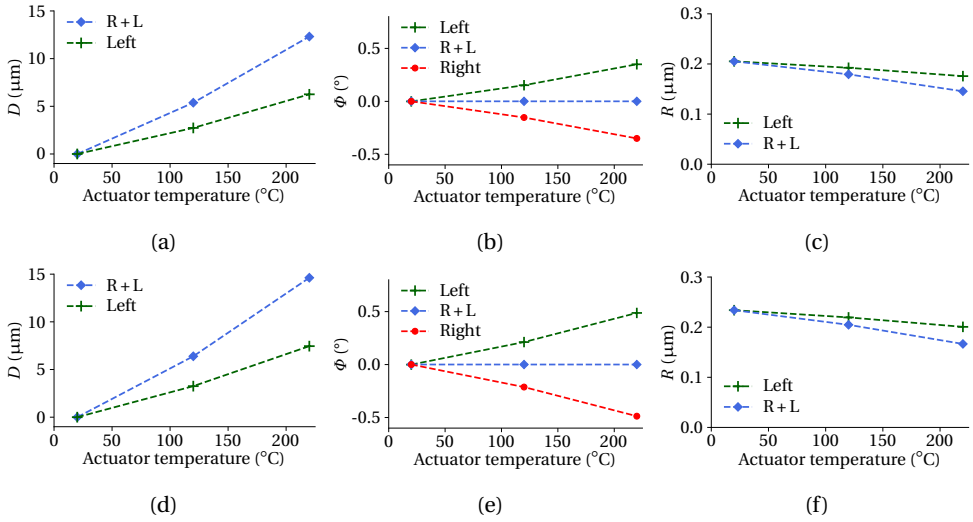


Figure 5.15: The modeled positioning performance of WGA A (3 µm poly-Si thickness, (a),(b), and (c)) and WGA B (5 µm poly-Si thickness, (d), (e), and (f)).

D and Φ are zero in the non-actuated state. Since the crossbar does have an initial curvature, the value for R_{off} is not zero. Both the model and measurement results show that WGA B has increased values for D and Φ as compared to WGA A. Furthermore, the R values of WGA B are higher than those of WGA A, in the model as well as in the measurements.

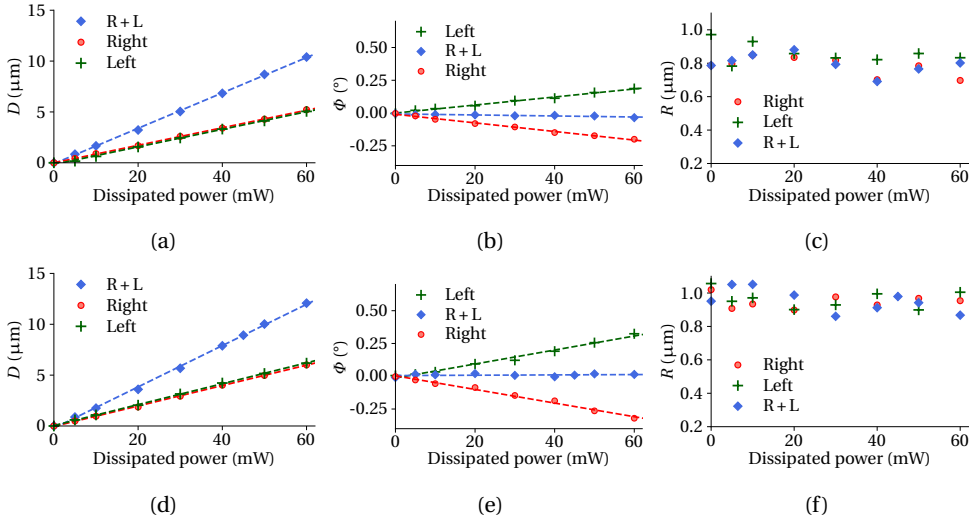


Figure 5.16: The measured positioning performance of WGA A (3 µm poly-Si thickness, (a), (b), and (c)) and WGA B (5 µm poly-Si thickness, (d), (e), and (f)).

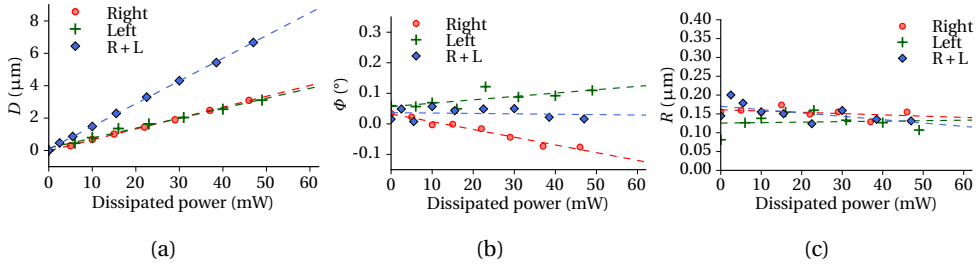


Figure 5.17: The measured positioning performance of WGA C as a function of power dissipated in the actuator(s) with (a) vertical deflection D, (b) crossbar angle Φ, and (c) vertical range of the waveguide core positions R.

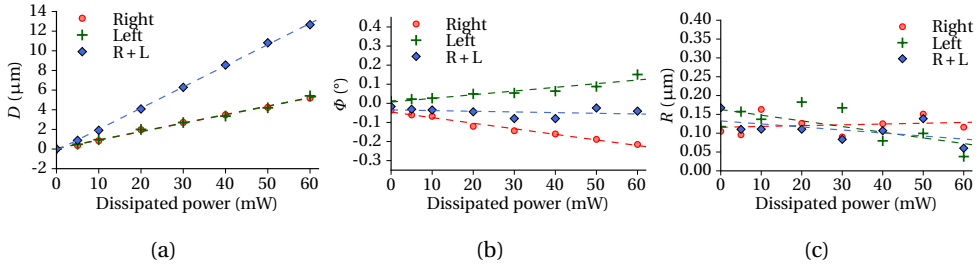


Figure 5.18: The measured positioning performance of WGA D as a function of power dissipated in the actuator(s) with (a) vertical deflection D, (b) crossbar angle Φ, and (c) vertical range of the waveguide core positions R.

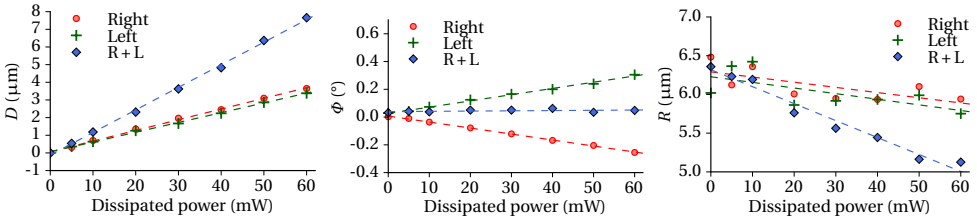


Figure 5.19: The measured positioning performance of WGA E as a function of power dissipated in the actuator(s) with (a) vertical deflection D, (b) crossbar angle Φ, and (c) vertical range of the waveguide core positions R.

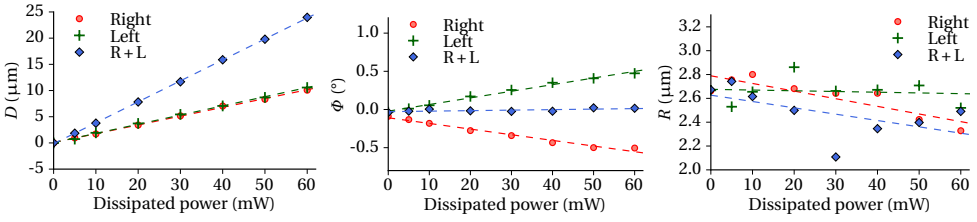


Figure 5.20: The measured positioning performance of WGA F as a function of power dissipated in the actuator(s) with (a) vertical deflection D, (b) crossbar angle Φ, and (c) vertical range of the waveguide core positions R.

These observations are also in agreement with the data in Table 5.3, where an increase in poly-Si thickness corresponds to an increase of all the positioning indicators.

One aspect where the model and measurement differ is the magnitude of the values on the vertical axes. This difference is a direct result of the model differing from the actual WGA. As explained above, the protecting layer of SiO_2 is not incorporated in the model. Absence of this layer will lead to deviations, the extent of which varies per positioning indicator. For example, the measured D and Φ being slightly smaller than the modeled D and Φ can be explained by the extra stiffness that follows from the thin layer of SiO_2. The R on the other hand, is larger in the measurements than in the model results. This is explained by the residual compressive stress in the SiO_2 layer, increasing the curvature of the crossbar.

Table 5.4 summarizes the measured positioning performance of the WGAs. A relevant measure for comparison is the power sensitivity (PS) of the positioning indicators. The PS is essentially the slope of the data shown in Figures 5.15 and 5.16.

The modeling suggested dependencies of positioning performance on other design parameters as well. Four additional WGAs, C through F, were available to experimentally verify these dependencies.

An optimal design has maximum PS for D and Φ, whereas the initial postrelease range R_{off} is minimal. WGAs C through F provide indications how design parameters can be used for optimization. It must be noted that in these WGA designs sometimes multiple design parameters are changed, hence comparison must be done with some care. However, a few observations can clearly be made.

Table 5.4: The measured power sensitivities of the tested WGAs.

	T_{Poly}	W_{Poly}	WG pitch	Beam length	Beam config:	W_{CB}	Power sensitivity of D (µm/W)			PS of Φ (°/W)		R_{off}	PS of R (µm/W)
ID	(µm)	(µm)	(µm)	(µm)	wg,act (#)	(µm)	Left	Right	L+R	Left	Right	(µm)	L+R
A	3	12	127	800	4,8	118	86	86	174	3.1	-3.3	0.83	-1.1
B	5	12	127	800	4,8	118	103	100	203	5.3	-5.2	1.02	-2.1
C	3	10	50	800	4,8	68	62	67	140	1.1	-2.5	0.17	-0.9
D	3	12	50	1000	4,12	118	86	86	216	1.9	-2.9	0.13	-0.8
E	5	12	250	800	6,12	68	55	61	128	4.5	-4.3	6.32	-21.9
F	5	12	250	1400	4,12	68	175	168	400	8.7	-7.4	2.63	-5.3

MAXIMIZE PS OF D

The modeling results indicated that maximum PS for D is particularly achieved with longer beams. The effect of waveguide beam pitch is not significant. This is supported by the measurements. WGA C and D have smaller pitch compared to WGA A, while they have the same poly-Si thickness. The values for D are in a similar range, however. WGA F, on the other hand, has very long beams, and the measurements clearly indicate that this is dominant for the PS of D, even though the waveguide pitch is much larger (which has a small negative effect on PS of D).

MAXIMIZE PS OF Φ

The maximum PS for Φ is mostly driven by beam length and poly-Si thickness, according to the modeling results. In the measurements, the smallest PS of Φ is observed for WGA C, which is indeed the design with the shortest beams and the thinnest layer of poly-Si. The largest values for the PS of Φ are measured with WGA F. As suggested by the model, this particular WGA has the longest beams and thickest poly-Si layer of the devices that were measured.

MINIMIZE POSTRELEASE R_{off}

Apart from the poly-Si thickness, it is particularly the waveguide pitch and number of waveguide beams that is dominating the waveguide range R_{off}. It must be observed in Table 5.4 that the PS for R is in µm/W. This means that with operation powers of ~100 mW the value for R is affected by roughly 0.1 µm (WGA A, C, D) or 0.2 µm (WGA B). This indicates that a well-performing design needs to have values for R_{off} (i.e. only determined by the initial postrelease deformation) in the order of or less than 0.1 µm to 0.3 µm. Table 5.4 shows that WGA C and D have by far the best performance for R_{off}. These are indeed the designs with the smallest waveguide pitch (50 µm) and the smallest poly-Si thickness. Moreover, WGA D, which is 200 µm longer than WGA C, has a smaller R_{off}, which corresponds with the model outcome.

5.5. RESULTS II, PHOTONIC ALIGNMENT EXPERIMENTS

This Section investigates two more aspects that are relevant to the operation of the WGAs in an active alignment scheme: actuator stability, and mode fields of etched facets. Finally, optical coupling of a positionable WGA with a counter PIC is demonstrated and measured.

5.5.1. ACTUATOR STABILITY

The stability of WGA D is studied by operating the actuators with the system sourcemeter at a constant voltage, while performing a surface contour measurement with the white light profilometer every ten minutes, for a total duration of one hour. A single measurement takes approximately five seconds. The obtained Y and Φ results provide a figure of merit for the stability of the actuators over time.

WGA D is subjected to stability measurements which are performed at the three different operation modes, using 50 mW of dissipated power. Section 5.5.1 includes the measured Y as a function of time. The vertical deflection of every actuator mode's first measurement (time=00:00) is aligned with the zero point of the vertical axis. All three actuation modes show the same trend: Y first increases a little bit, and then decreases. The measurements reveal a maximum change in deflection of 92 nm, 64 nm, and 71 nm for the Right, Left, and R + L actuation respectively.

The measured Φ as a function of time is presented in Section 5.5.1. The angle Φ of every actuator mode's first measurement (time=00:00) is aligned with the zero point of the vertical axis. The measurements reveal a maximum change in Φ of 0.023°, 0.011° and 0.028°, for the Right, Left, and R + L operation mode respectively.

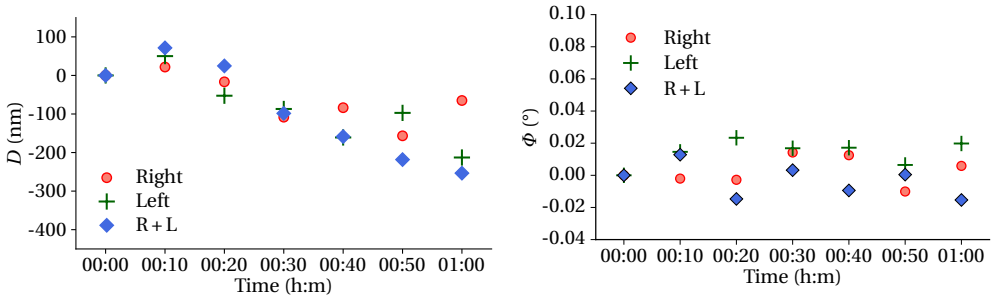


Figure 5.21: The deflection D and angle Φ of WGA D in the three operation modes, measured over a total duration of one hour.

A precise alignment requires stability in the position of the crossbar until it is mechanically fixed. For most fixing methods, the fixation will be accomplished in a matter of seconds, resulting in far less than 10 nm deviation from the aligned optimum. Regardless of the fixing method, an active alignment approach enables small adjustments of the actuators until the fixation is finished in order to maintain an optimal optical alignment. The stability of the positionable WGAs is acceptable.

5.5.2. MODE FIELD ANALYSIS

The fabricated waveguides differ from conventional Si_3N_4 / SiO_2 waveguides on two fronts. Firstly, material alongside and underneath the waveguide beams is removed, resulting in suspended waveguide beams. Secondly, the end-facets are etched, leading to a topography on the facet. This Subsection measures the mode field profiles of the fabricated suspended waveguides to have a first verification of their quality.

The mode field intensity distribution of the waveguides is studied by coupling light into the waveguides of a photonic MEMS chip through a fiber array unit (FAU). The photonic MEMS chip is first mounted to a PCB, after which the FAU is mounted to it with a UV-curable epoxy. A photonic MEMS chip with eight channels (900 µm beam length and 127 µm waveguide pitch) is selected in combination with an eight-channel FAU (with similar 127 µm waveguide pitch). The waveguide cores measure 1 µm × 220 nm (width × thickness). Figure 5.22 shows the assembly of the PCB on which the photonic MEMS chip is mounted, to which the FAU is mounted.

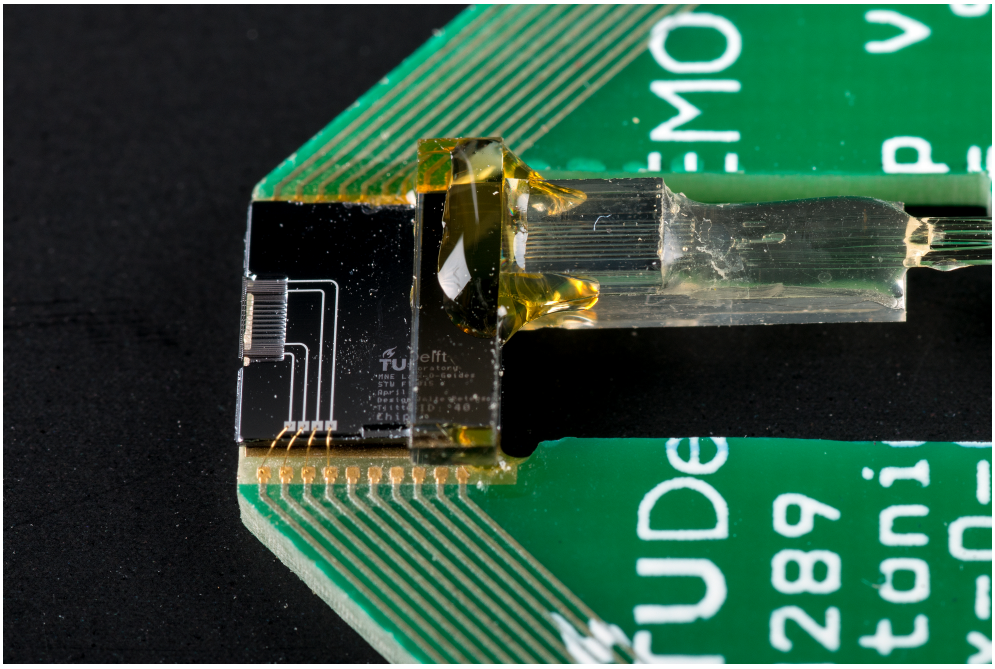


Figure 5.22: Assembly of a FAU mounted to a photonic MEMS chip which is mounted and wirebonded to a PCB. Photograph by Hans de Lijser.

Using a *Keysight 8163B* tunable laser and a *Xenics Xeva XC-132* infrared (IR) camera, near field profiles of all the photonic channels are obtained consecutively. The schematic of the experimental setup is presented in Figure 5.23. The tunable laser, operating at 1550 nm, is connected to one of the channels, while the IR camera and a 50× objective (*Olympus 1-LM550*) are used to capture the mode field intensity distribution at the end facet of the suspended waveguide corresponding to the active channel.

Figure 5.24 includes the measured mode field profile of the first waveguide channel. The measured mode field profiles of the remaining waveguide channels are available as supplemental material. With a specified focal length of 3.6 mm and a measured distance between objective and camera of 61 cm, the magnification of the optical system is calculated to be approximately 168 times, resulting in one camera pixel (measuring 30 µm by

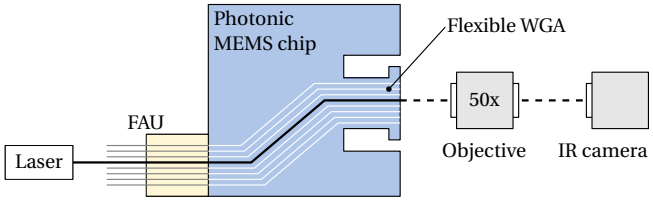


Figure 5.23: Schematic representation of the experimental setup used for the mode field analysis. The laser source is operated at 1550 nm.

Table 5.5: The mode field diameters corresponding to the measured mode field intensity distributions

Waveguide	MFD_x (nm)	MFD_y (nm)
1	2955	2597
2	2750	2605
3	2844	2611
4	2750	2617
5	2771	2541
6	2829	2713
7	2800	2731
8	2787	2618

30 µm) corresponding to 178 nm by 178 nm. Based on Figure 5.24, the Gaussian $1/e^2$ mode field diameters can be estimated. Waveguide 1 is measured to have a horizontal mode field diameter (MFD_x) of about 2.9 µm and a vertical MFD_y of 2.6 µm. For all eight channels, mean values for MFD_x and MFD_y of 2.81(6) µm and 2.63(6) µm were measured, respectively. The measured mode field profiles do not show any abnormalities and demonstrate that the partly suspended waveguide beams function properly.

Table 5.5 presents the Gaussian $1/e^2$ mode field diameters in horizontal and vertical direction (MFD_x and MFD_y, respectively) of all the measured waveguides. The values in the table are estimations that are based on the profiles along the horizontal and vertical lines.

5.5.3. PHOTONIC ALIGNMENT EXPERIMENT

Finally, the suitability of a positionable WGA for photonic alignment is evaluated by means of a photonic alignment experiment. For this experiment, a waveguide pitch of 50 µm was selected, as this is the only configuration that allows for simultaneously aligning more than two waveguides. Figure 5.32 presents the schematic of the experimental setup, consisting of a photonic MEMS chip, an indium phosphide (InP) PIC, a 10× objective, and an IR camera.

For monitoring the coupled power, the 10× objective and the IR camera are used, providing an image of the end-facets on the opposite side of the photonic MEMS chip. Using this configuration, the IR camera can capture three adjacent 50 µm-pitched waveguide spots simultaneously in a single frame. First, for pre-alignment, the laser sources (operating at a wavelength of 1550 nm) on the InP PIC are activated, and the actuators on the photonic MEMS chip are temporarily set to approximately 50 % of their maximum range.

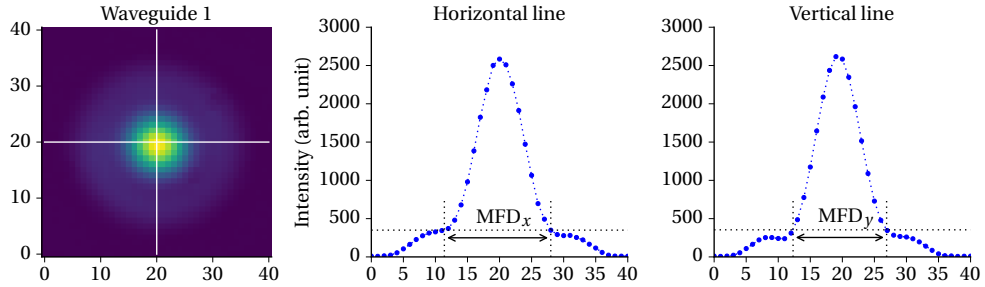


Figure 5.24: The measured mode field intensity distribution of waveguide 1. The 2D image as measured with the IR camera is shown on the left, with the values at both axes corresponding to camera pixels. The profiles along the horizontal and vertical white lines are shown in the two graphs on the right, with the Gaussian $1/e^2$ mode field diameters indicated.

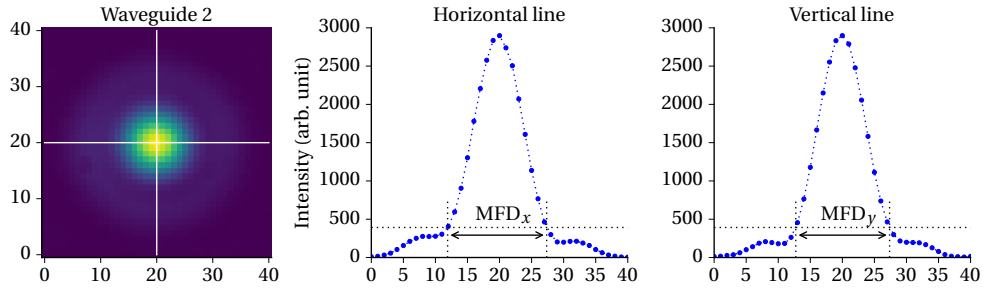


Figure 5.25: The measured mode field intensity distribution of waveguide 2, showing MFD$_x$ and MFD$_y$.

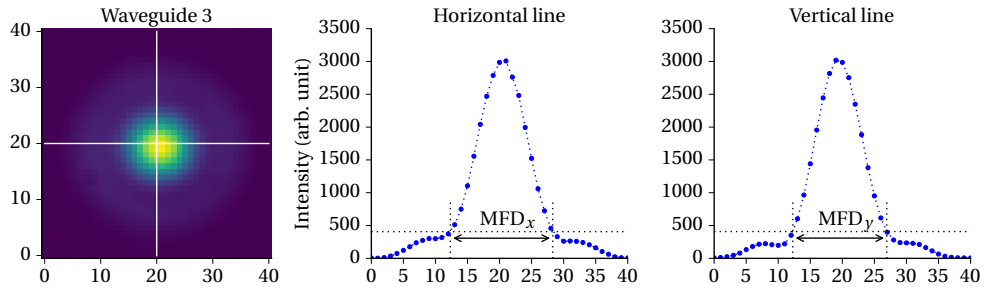


Figure 5.26: The measured mode field intensity distribution of waveguide 3, showing MFD$_x$ and MFD$_y$.

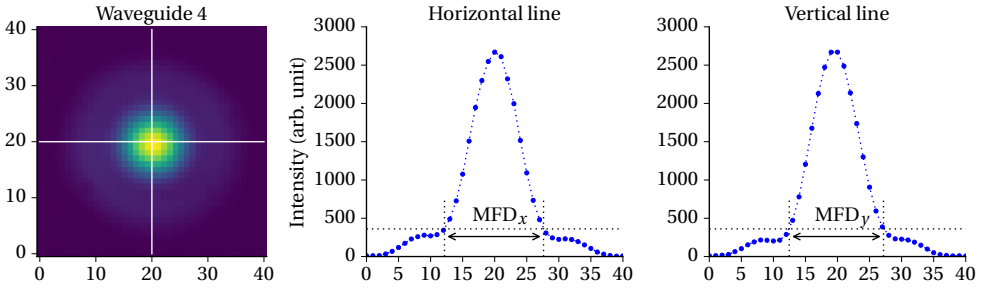


Figure 5.27: The measured mode field intensity distribution of waveguide 4, showing MFD$_x$ and MFD$_y$.

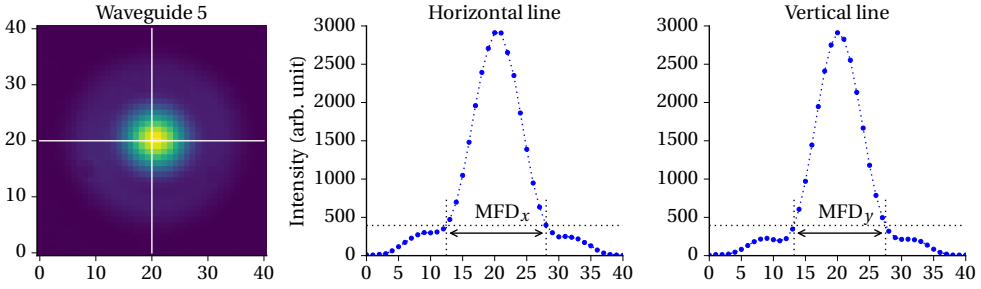


Figure 5.28: The measured mode field intensity distribution of waveguide 5, showing MFD$_x$ and MFD$_y$.

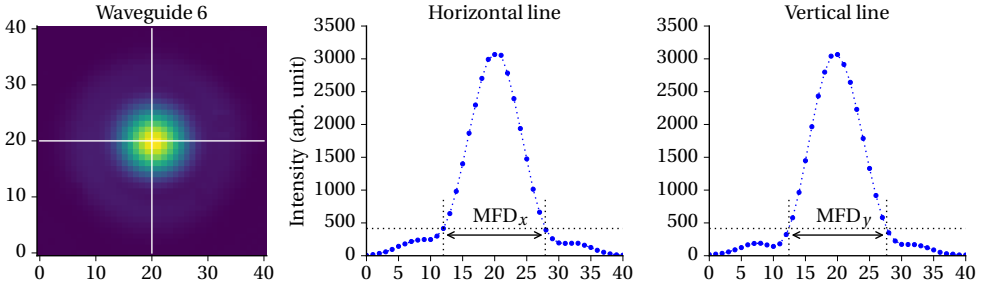


Figure 5.29: The measured mode field intensity distribution of waveguide 6, showing MFD$_x$ and MFD$_y$.

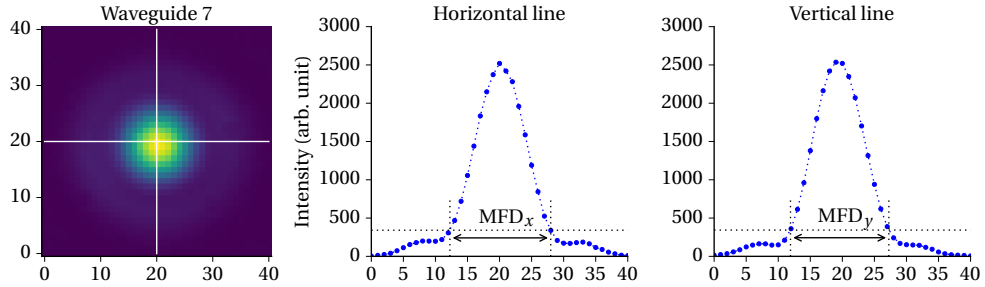


Figure 5.30: The measured mode field intensity distribution of waveguide 7, showing MFD$_x$ and MFD$_y$.

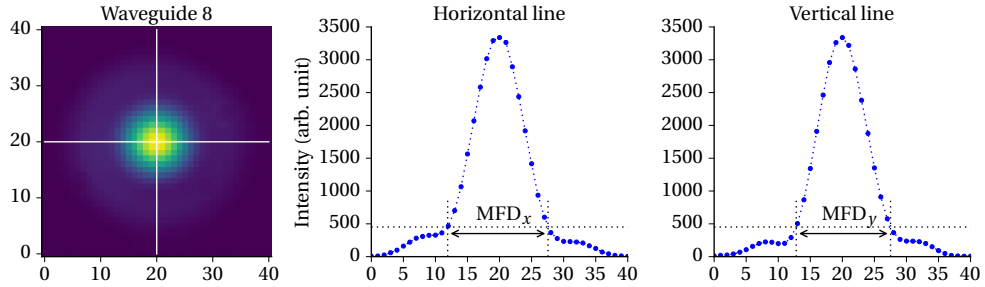


Figure 5.31: The measured mode field intensity distribution of waveguide 8, showing MFD$_x$ and MFD$_y$.

Then, using manual microstages, the InP PIC is aligned with respect to the WGA side of the photonic MEMS chip, aiming for maximum light coupling through the waveguides that are in the field of view.

Traversing the complete actuator range in a scan-like fashion from 0 V to 55 V in steps of 1 V provides a total of 3136 frames, each one representing the mode field intensity distribution of the three waveguides within the field of view of the camera. From every frame, the intensity amplitude of the three spots is extracted using a two-dimensional gaussian fit. Figure 5.33 presents the resulting normalized intensity scans for the three waveguide spots.

For all three spots, no light was measured at a voltage of 0 V across both actuators. At this voltage, the waveguide cores at the free end of the flexible WGA are located above the InP waveguide cores. Similarly, also at an actuator voltage of 55 V, no light was measured at the three spots. This corresponds to the situation in which the positionable waveguide cores are located below the InP waveguide cores. At intermediate actuator voltages, alignment of the positionable waveguide cores with the InP waveguide cores is achieved, where the maximum intensity amplitude indicates an optimal alignment (see Figure 5.33).

By combining the individual intensity scans, a representation of the overall alignment is obtained, which is presented in Figure 5.34. The combined colormap is obtained by multiplying the normalized intensities of the three waveguide spots. The best alignment of

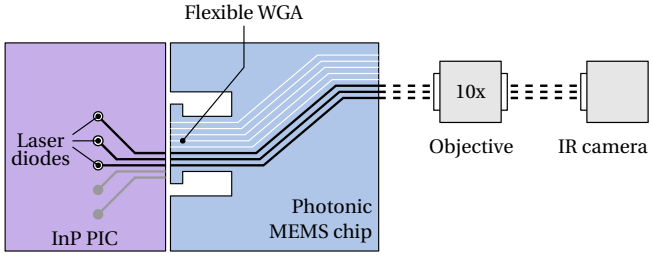


Figure 5.32: Schematic representation of the experimental setup used for the photonic alignment experiment.

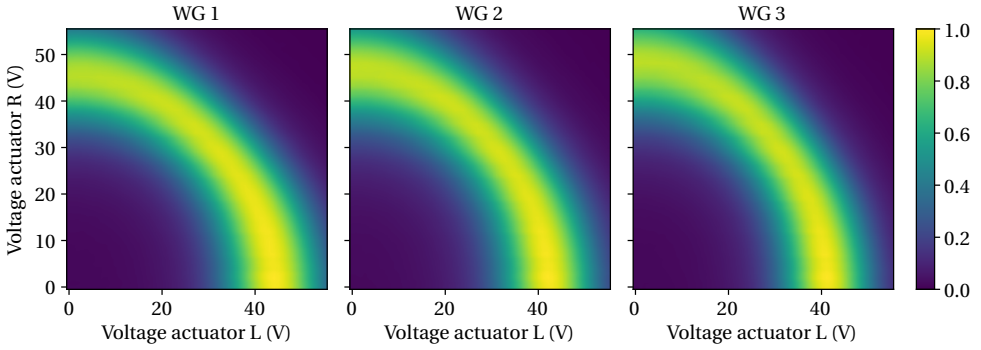


Figure 5.33: Colormap of the normalized intensity amplitude as a function of left and right actuator voltage, measured at the three waveguides.

all three waveguides within the traversed actuator range occurs at a voltage of 42 V and 2 V, for the left and right actuator respectively.

5.6. FINAL DISCUSSION AND CONCLUSIONS

Positionable photonic waveguide arrays were developed for a novel chip-to-chip alignment concept. A finite element model of the positionable waveguide arrays was created in order to understand how the design influences the performance of the WGA. This investigation provides insights that are not only relevant to the WGAs as applied in the proposed alignment concept, but are also valuable for the development of similar systems. The model outcome is validated by means of measurements performed on fabricated WGAs.

The main design parameters that affect the performance are the poly-Si thickness, the beam length and the waveguide pitch. The power sensitivities of D, R, and Φ particularly increase with longer beams and thicker poly-Si. R_{off} improves with longer beams, smaller waveguide beam pitch and thinner poly-Si. It is apparent that for example the requirements for a small R_{off} and a large PS of D conflict with respect to the poly-Si thickness. However, the modeling results provide guidelines for the design parameters, directing towards an optimal positionable WGA design.

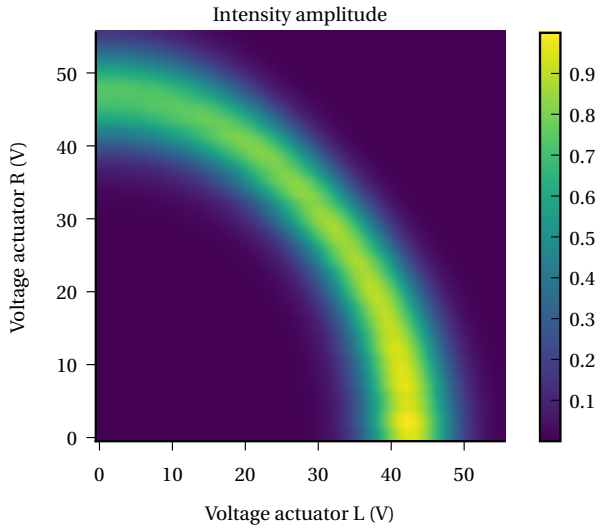


Figure 5.34: The normalized amplitude of the combined measured intensity as a function of actuator voltage.

For a WGA to have a large PS of D, a large PS of Φ, and a small R_{off}, a feasible design has a poly-Si thickness of 3 μm, a waveguide pitch of 50 μm, and a beam length of 1000 μm. Measurements revealed that a WGA with this design meets the requirements by achieving an out-of-plane deflection D and rotation Φ that are sufficiently large while the initial waveguide core range R_{off} is small enough. At the same time, this WGA design results in a relatively large initial deflection Y_{off}, which makes planar photonic alignment with another PIC difficult. This issue can be solved by a smart design of the total system, which is part of ongoing research in our lab.

Drifts of 10 nm/min and 0.003 °/min were determined for deflection and angle, based on measurements spanning one hour in total. Moreover, mode field analysis of an eight-channel WGA confirms that the partly suspended Si_3N_4 / SiO_2 waveguides provide proper photonic functionality. An average MFD of 2.63 μm × 2.81 μm was measured for suspended waveguide beams having 220 nm × 1 μm sized waveguide cores. Finally, it was shown that a working WGA can be designed which can accomplish submicrometer photonic alignment. To this end, three adjacent channels of a selected WGA were actively aligned with three channels of another PIC.

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6

CONCLUSIONS AND RECOMMENDATIONS

The continuous development of photonic technology and Photonic Integrated Circuits (PICs) leads to new kinds of applications in the fields of telecom, datacom, healthcare, optical sensing and visible light applications. The advances in packaging of PICs are lagging behind, making packaging a large contributor to fabrication costs. Improvement in optical packaging and interconnect technology is of great importance for the future of PIC-based applications.

The research in this thesis aimed to advance optical interconnect technology by investigating a novel alignment concept. This chapter summarizes the implications of the research findings. Section 6.1 highlights the main contributions that the research in this thesis brings. In Section 6.2, the actual lessons learned are stated. Recommendations for further research are provided in Section 6.3.

6.1. CONTRIBUTIONS

TWO-STAGE ALIGNMENT CONCEPT

THE research in this thesis signifies important progress in the development of a novel concept for the alignment of an InP PIC with a TriPleX interposer chip. A positionable waveguide array is realized within the TriPleX interposer chip, consisting of mechanically flexible waveguide beams and an integrated actuation mechanism to facilitate fine-alignment at the PIC – interposer chip interface. Photonic alignment is achieved in two stages. In the first stage, the PIC and interposer chip are coarsely pre-aligned and fixed. At this stage, a selection of the degrees of freedom is aligned with sufficient accuracy. In the second stage, the alignment in the remaining degrees of freedom is improved by fine-aligning the positionable waveguide array of the interposer chip with respect to the waveguides of the PIC. Then, the positionable waveguide array is fixed in its position.

SiO_2 PHOTONIC MEMS

A major innovation is the realization of MEMS-functions in an SiO_2-based waveguiding platform. The majority of research on positionable waveguides is limited to silicon photonic devices. For the first time, we have demonstrated the powerful combination of suspended SiO_2 waveguides and microactuators, or 'SiO_2 photonic MEMS'. While this thesis has focused on the use in a photonic alignment concept, many other applications can benefit from SiO_2 photonic MEMS, like optical switches, optical attenuators, waveguide cantilever scanners, and (e.g. wafer-level) optical probes.

FABRICATION PROCESS

A comprehensive microfabrication process was developed for Else Kooi Laboratory (EKL) equipment, based on post-processing of TriPleX wafers. What started out as a process flow for fabricating suspended SiO_2 beams has evolved into an extensive fabrication process for positionable waveguide arrays with integrated thermal actuators. The paramaterized design approach revealed to be very beneficial, making it possible to individually set every design parameter of every waveguide array.

MODEL-BASED DESIGN OPTIMIZATION OF WGA SYSTEM

The large number of design parameters (waveguide beam length, waveguide beam pitch, number of waveguide beams, number of actuator beams, etc.) resulted in a large number of WGA design variations. Finite element modeling was used to identify the most relevant parameters. Additionally, the finite element analysis provides guidelines for the design parameters of a positionable photonic waveguide array with optimal performance.

6.2. CONCLUSIONS

The alignment concept is feasible, as long as the following two prerequisites are met:

- suspended SiO_2 waveguide structures are manufacturable,
- an alignment mechanism, preferably using microactuators, can be implemented, and
- an optimal combination of the design parameters of the positionable waveguide array is used.

SUSPENDED SiO_2 WAVEGUIDE STRUCTURES ARE MANUFACTURABLE

Because of the intrinsic compressive stress in the SiO_2, the suspended beams buckled and fractured upon release, as was shown in Chapter 3. This problem was solved by developing a special silicon reinforcement method, which ensures that the SiO_2 beams are supported by a layer of silicon until the whole structure is released. Once suspended, the supporting silicon is no longer required and is removed by etching. For ~15 μm thick thermal SiO_2 beams, an initial silicon thickness of 70 μm resulted in suspended beams ranging in length from 10 μm to 1000 μm with a 97.8 % fabrication yield. The supporting silicon limits the expansion of the SiO_2, which results in lower stress concentrations, reducing the chance of beam failure during fabrication. The reinforcement method proved of the utmost importance for reliably fabricating suspended structures and positionable waveguide arrays.

MICROACTUATORS CAN BE IMPLEMENTED

In Chapter 4 it was shown that patterning poly-Si on top of SiO_2 beams is an elegant way to integrate thermal actuators for out-of-plane displacement. The three advantages of this approach are a large actuator stroke (~22 μm), due to the (~ factor 7) difference in CTE of SiO_2 and poly-Si, the layer of poly-Si acting as heater as well as one of the bimorph materials, and an acceptable increase in fabrication complexity. The integrated alignment needs to be improved by reducing the significant initial deflection of the crossbar, the bimorph beams and by developing solutions for actuators with pure in-plane motion.

THE WGA DESIGN CAN BE OPTIMIZED

The WGA design consists of a set of waveguide beams and, adjacent to the waveguide beams, two sets of actuator beams with a layer of poly-Si on top. A crossbar mechanically connects the waveguide beams and the actuator beams. Parameters in the design are the number of waveguide beams, the number of actuator beams, the beam length, the (waveguide and actuator beam) pitch, the poly-Si thickness, and the crossbar width. By exploring the design space in Chapter 5, it was found that the main design parameters that affect the performance are the poly-Si thickness, the beam length and the waveguide pitch. A WGA with very long beams and a thick layer of poly-Si will produce a large out-of-plane deflection, a large rotational motion range of the crossbar, but will also have a significantly curving crossbar. The model predicted that the waveguide core range R is improved with longer beams, smaller waveguide beam pitch and thinner poly-Si. For a WGA to have a large power sensitivity (PS) of deflection D, a large PS of angle Φ, and a small intitial waveguide core range R_{off}, a feasible design has a poly-Si thickness of 3 μm, a waveguide pitch of 50 μm, and a beam length of 1000 μm. Overall, the modeling results provide guidelines for the large set of design parameters, directing towards an optimal positionable waveguide array, which is confirmed by measurements on fabricated designs.

6.3. RECOMMENDATIONS FOR FUTURE RESEARCH

The work in this thesis provides a first step in the development of the proposed alignment concept. For the first time, alignment of multiple waveguides using integrated out-of-plane actuators is demonstrated. The most important next steps are

- Implementation of in-plane actuation

- Locking the positionable waveguides in place after fine-alignment
- Combining in-plane actuation, out-of-plane actuation and locking into single system
- Integrating flip-chip based pre-assembly process

Research of all four steps is part of a European follow-up project, called PHASTFlex. The implementation of in-plane actuation is challenging with the same material configuration as used for the out-of-plane actuators. The SiO_2 and Poly-Si differ in CTE by almost a factor 7. While beneficial for out-of-plane motion, this makes a pure in-plane motion of for example a chevron actuator challenging. Additional investigations should be performed on alternative solutions for in-plane motion (e.g., alternative actuator materials).

An additional recommendation is to investigate how to further improve the fabrication yield. The Si-reinforcement method significantly improved the yield of single cantilevers. A better understanding is required for high yield fabrication of more complex shapes.

Moreover, it would be interesting to explore the minimum required cladding thickness for mechanically flexible waveguides to have acceptable optical loss. Reducing the cladding directly reduces the height and width of the beam, reducing the mechanical stiffness and lowering the demand on the actuator force.

In the presented research, waveguide arrays with up to six waveguide beams have been characterized. While the alignment concept is scalable, creating high port-count (>8) positionable waveguide arrays requires further investigations. For example, the most suitable configuration for large waveguide arrays might include a set of actuator beams for every four waveguide beams.

As a final recommendation, it is proposed to assess the field reliability of the alignment concept. It will be interesting to investigate the effect of environmental conditions like temperature, humidity, mechanical vibrations, mechanical shock, and particles. For example, the sensitivity of aligned and locked waveguide arrays to variations in temperature is relevant. Because thermal actuators are used, external temperature changes will induce mechanical stresses in the actuator beams and on the locking mechanism.

A

PROCESS FLOW

This appendix provides the process flow for fabrication of waveguide structures with out-of-plane actuators presented in Chapters 4 and 5. For a process description the reader is referred to Section 4.3 and the schematic fabrication sequence as depicted in Figure 4.6.

Part of this process flow was also reported in: "Modelling of the Initial Deformation of TriPleX Based Bimorph Actuators Used in Alignment of Optical Waveguides", T.A. Nooren, M.Sc. thesis (2015). This M.Sc. thesis resulted from the work by a M.Sc. student I supervised, and for which I provided the process flow and carried out the fabrication processing.

This process flow is known within EKL under identification code *WB1993*.

1. STARTING MATERIAL

Use single side polished wafers with the following specifications:

Type:	p-type
Orientation:	{100}
Resistivity:	31
Thickness:	525 ± 2 µm
Diameter:	100.0 ± 0.2 mm

2. DEPOSIT TRIPLEX STACK

Processing is done by LioniX.
Layer stack on frontside:

- Bottom cladding layer: thermal oxide, thickness = 8 µm
- Waveguide core: silicon nitride, thickness = 200 nm
- Top cladding: PECVD oxide, thickness = 8 µm

Stack on backside of wafer is either similar to frontside or without the (complete) top cladding layer.
Zero layer alignment markers for contact aligner (FWAMs) are patterned in the silicon nitride layer!

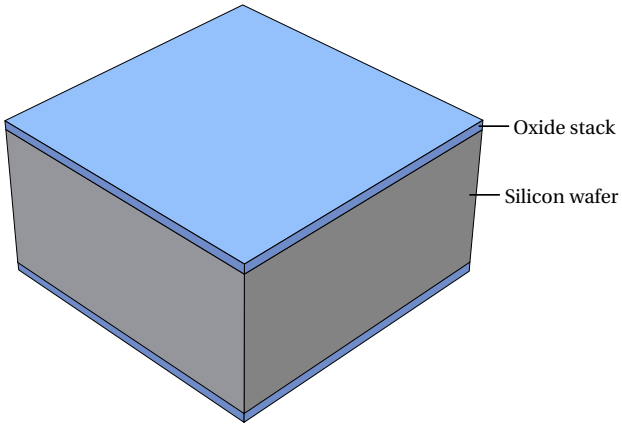

Figure A.1: Silicon wafer with 16 µm TriPleX stack

3. CLEANING OF WAFERS FROM OUTSIDE DIMES

CLEANING IN MEMS LAB: HNO_3 100% AND 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Fill the container with HNO_3 100%
Rinse	Rinse in DI water
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Fill the container with HNO_3 65%.
Rinse	Rinse in DI water
Drying	Use the dry-spinner.

ENTER CLASS 100 CLEANROOM

Change waferbox to a standard Dimes black box.

4. CLEANING PROCEDURE: HNO_3 100% AND 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

5. MEASUREMENT: CURVATURE

Use Tencor Flexus instrument to measure the curvature of the wafer.
This is a reference measurement.

Measurement: thickness (frontside and backside)

Use the Leitz MPV-SP measurement system to measure the oxide thickness on the *frontside* of Lionix wafers:
Program: Th. Sio2 on Si >50 nm auto5pts
Expected oxide thickness: 16 µm

Use the Leitz MPV-SP measurement system to measure the oxide thickness on the *backside* of Lionix wafers:
Program: Th. Sio2 on Si >50 nm auto5pts
Expected oxide thickness: 16 µm

6. Deposit poly-Si @ frontside

LPCVD of poly-Si: seedlayer

Tempress LPCVD tube E3 poly, recipe: LPolyBin.
Duration: 1 h. Expected thickness: 130 nm.

Perform test WB1993-P01

Determine time required to etch 130 nm of poly-Si with recipe 'Leon_1'

Remove LPCVD poly-Si from backside

Trikon Omega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine. The process parameters of the etch program may not be changed. Recipe: 'Leon_1'. Duration: 90 s.

7. Cleaning Procedure: HNO_3 100% and 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

Remove native oxide from poly-Si

Perform this step right before starting the epitaxy. After waiting for too long, native oxide will reappear. !

Etching	4 minutes in 0.55 % HF solution (Merck: HF 0.55 % VLSI selectipur) at ambient temperature. Use wet bench 'HF (0.55 %)' and the carrier with the black dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the orange carrier with a red dot.

Epitaxy of poly-Si

Use ASMI Epsilon One.
Recipe names: WB1993_3muB4e16 for 3 µm thickness, WB1993_5muB4e16 for 5 µm thickness.
Boron doping with a target sheet resistance of 45 Ω/□.

Measure sheet resistance

Use the CDE Resmap 4-points probe with the silicon probe (ask Tom Scholtes for help).
Expected sheet resistance: 45 Ω/□

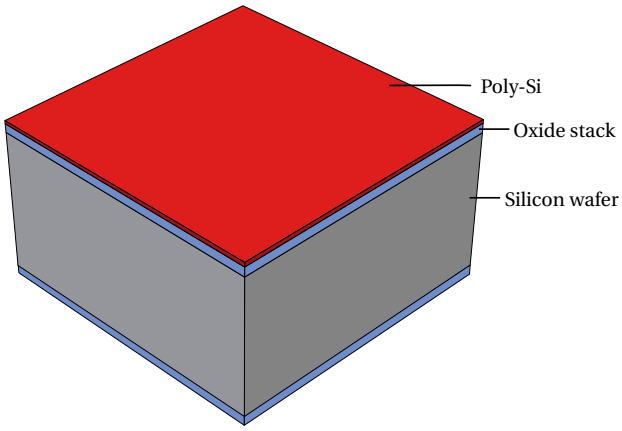

Figure A.2: Result after growing 5 µm epi-polysilicon on frontside

8. OPEN FWAM RECTANGLES IN POLY-SI

COATING (FRONTSIDE)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co-3012-1.4um'** on the coating system (resist thickness: 12 µm at 48% RH). After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

ALIGNMENT AND EXPOSURE (FRONTSIDE)

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.
Expose mask 'COMURK' with job 'clearFWAM' and the correct exposure energy of 150 mJ

! Make sure that alignment is disabled (optical alignment = N, prealignment type = Z). Furthermore, a double exposure is required: one without translation and one with a translation of 1000 µm over the X-axis. This results in open rectangles at the location of the FWAMs.

DEVELOPING

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using ShipleyMF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.
Use program 'Dev-SP' on the developer station.

INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

ETCH POLY-SI

Use the Rapier etcher.
Follow the operating instructions from the manual when using this machine.
The process parameters of the etch program may not be changed!

Use recipe 'Straightdown2'

Strip photoresist using Tepla

Strip resist	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use **'program 1'**: 1000 W power and automatic endpoint detection + 2 min overetching.

9. Cleaning Procedure: HNO_3 100% and 65%

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

10. Deposit and pattern 6 µm photoresist mask @ backside

Coating (backside)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with AZ9260 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co-Syr-9260-6um-no EBR'** on the coating system (resist thickness: 12 µm at 48% RH). After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.
Wait at least 20 minutes after coating for dehydration before exposure! !

Prebake

One hour of baking in the Memmert oven (110 °C) to harden the resist layer. This has two objectives: (1) increase density of resist for etching and (2) prevent sticking to the clamp of the Drytek.

Alignment and exposure (backside)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask 'BS' (located in box 468) using an exposure energy of 1200 mJ. This is achieved with a duration of 60 seconds.
Wait at least 20 minutes after exposing before developing! !

Developing

Manual developing of photoresist. Use 1 part of AZ400K diluted with 2 parts of DI water. For development time: start with 1 min 30 sec. Depending of the result (optical inspection) another 30 sec.

Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

A

ETCH OXIDE (BACKSIDE)
Etch depth: 16 µm, stop on silicon.
Drytek Triode for RIE
Recipe: StdOxide
Etchrate SiO_2: 500 nm/min
Etchrate AZ9260: 145 nm/min

Drytek Triode T384 etch parameters. Recipe: **'StdOxide'**

Step	**Gasses & flows**	**Pressure**	**RF power**	**He pressure**	**Etch time**
1. Oxide (RIE)	C_2F_6 @ 36 sccm CHF_3 @ 144 sccm	180 mTorr	300 W	12 Torr	~ 32 min

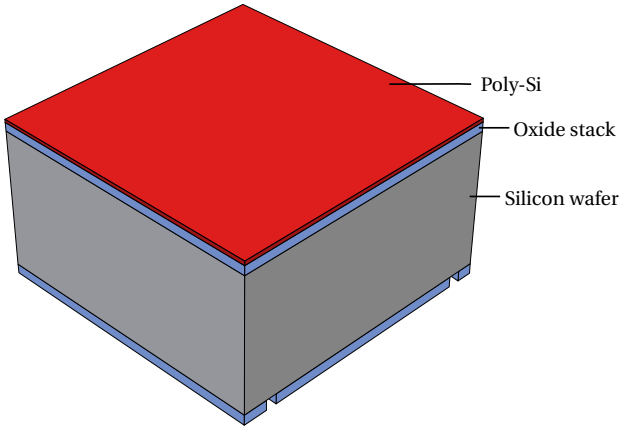

Figure A.3: Result after patterning the backside SiO2 layer

11. CLEANING PROCEDURE: TEPLA + HNO_3 100% AND 65%

Strip resist	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use **'program 1'**: 1000 W power and automatic endpoint detection + 2 min overetching.
Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Cleaning	10 minutes in concentrated nitric acid (Merck: HNO_3 65% selectipur) at 110 °C. This will dissolve metal particles. Use wet bench 'HNO_3 (65%)' and the carrier with the red dot.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Semitool 'rinser/dryer' with the standard program, and the white carrier with a red dot.

12. Deposit, open FWAM and pattern Al-1%Si @ frontside

0.675 µm thick Al-1%Si deposition

Use Trikon Sigma sputter coater to deposit a 0.675 µm thick layer.
Recipe: 'Sigma#AlSi_675nm_350C'.

Coating (frontside)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co-3012-1.4um'** on the coating system (resist thickness: 12 µm at 48% RH). After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

Alignment and exposure (frontside)

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.
Expose mask 'COMURK' with job 'clearFWAM' and the correct exposure energy of 150 mJ
Make sure that alignment is disabled (optical alignment = N, prealignment type = Z). Furthermore, a double exposure is required: one without translation and one with a translation of 1000 µm over the X-axis. This results in open rectangles at the location of the FWAMs. !

Developing

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using ShipleyMF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.
Use program 'Dev-SP' on the developer station.

Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

Etch Al-1%Si (dry)

Use the Trikon Omega 201 plasma etcher. Recipe: Al06r350.
Automatic endpoint detection does not work due to small surface area in mask.

Strip photoresist using Tepla

Strip resist	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use **'program 1'**: 1000 W power and automatic endpoint detection + 2 min overetching.

13. Cleaning Procedure: HNO_3 100% for green metals

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%) metaal' and the carrier with the yellow and red dots.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger 'rinser/dryer' with the standard program, and the white carrier with a black dot.

No HNO_3 65% at 110 °C cleaning step, because this will etch metals. !

COATING (FRONTSIDE)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co-edg-3012-1.4um'** on the coating system (resist thickness: 1.4 µm at 48% RH).
After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

ALIGNMENT AND EXPOSURE (FRONTSIDE)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask 'Al' (located in box 468) using an exposure energy of 110 mJ. This is achieved with a duration of 5.5 seconds.

DEVELOPING

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment.
The process consists of a post-exposure bake at 115 °C for 90 seconds, followed by a development step using ShipleyMF322 with a single puddle process, and a hard bake at 100 °C for 90 seconds.
Use program 'Dev-edg-SP' on the developer station.

INSPECTION: LINEWIDTH AND OVERLAY

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

ETCH AL-1%SI (DRY)

Use the Trikon Omega 201 plasma etcher. Recipe: Al_poly2. Different recipe than the one used before to etch Al-1%Si because of larger open area.

STRIP PHOTORESIST USING TEPLA

Strip resist	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use **'program 1'**: 1000 W power and automatic endpoint detection + 2 min overetching.

14. CLEANING PROCEDURE: HNO_3 100% FOR GREEN METALS

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%) metaal' and the carrier with the yellow and red dots.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger 'rinser/dryer' with the standard program, and the white carrier with a black dot.

! No HNO_3 65% at 110 °C cleaning step, because this will etch metals.

15. PATTERN POLY-SI @ FRONTSIDE

COATING (FRONTSIDE)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Shipley SPR3027 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

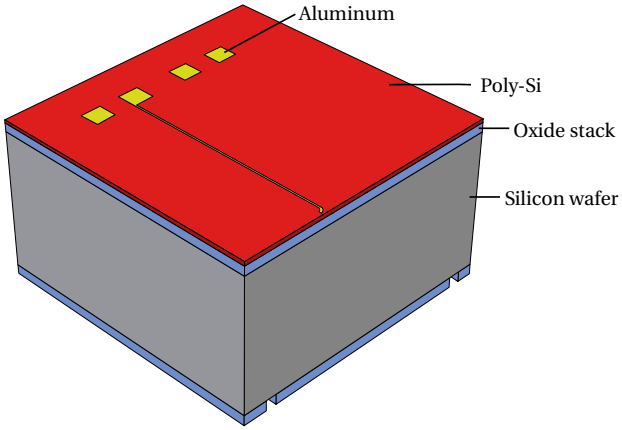

Figure A.4: Patterned aluminium layer

Use coating program **'Co-edg-3027-4.0um'** on the coating system (resist thickness: 3.1 µm at 48% RH).
After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

Alignment and exposure (frontside)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask 'Poly' (located in box 468) for a duration of 26.4 second (value is obtained from table).

Developing

The wafers are developed by a combination of EVG120 processes and manual development.
When using the EVG120 system, follow the instructions specified for this equipment.

1. Use program 'Dev_PEB' on the developer station. This performs a post-exposure bake at 115 °C for 60 seconds.
2. Manually develop in MF322. Duration: 1 min
3. Rinse thoroughly with DI water
4. Use program 'Dev_HB' on the developer station. This performs a hard bake at 100 °C for 60 seconds.

Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

Remove Al precipitates

To prevent micromasking, all aluminum precipitates need to be removed.
Use the Trikon Omega 201 plasma etcher. Recipe: Al06TS. Different recipe than the one used before to etch Al-1%Si because of larger open area.

A

ETCH POLY-SI

Use the Rapier etcher.
Follow the operating instructions from the manual when using this machine.
The process parameters of the etch program may not be changed!

Use recipe 'Straightdown2'
For 3 µm use 20 cycles, for 5 µm use 25 cycles.

STRIP PHOTORESIST USING TEPLA

Strip resist — Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use **'program 23'**: plasma with CF_4 gas. Duration: 3 min CF_4 strip, 10 min O_2 strip.

16. CLEANING PROCEDURE: HNO_3 100% FOR GREEN METALS

Cleaning — 10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%) metaal' and the carrier with the yellow and red dots.

QDR — Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying — Use the Avenger 'rinser/dryer' with the standard program, and the white carrier with a black dot.

! No HNO_3 65% at 110 °C cleaning step, because this will etch metals.

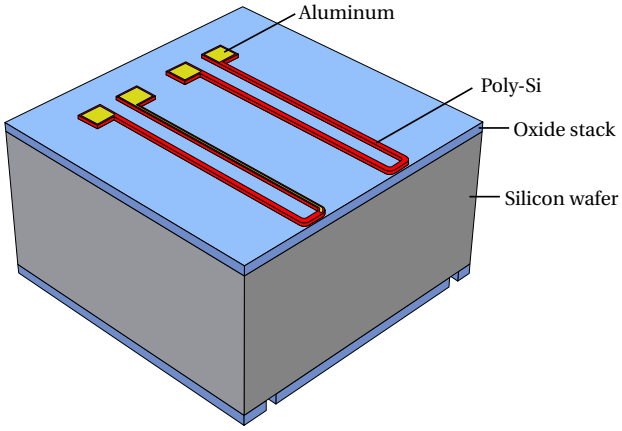

Figure A.5: Result after patterning the poly-Si layer

17. PROTECT POLY-SI WITH PLASMA OXIDE, BUT OPEN BONDPADS

DEPOSIT >1 µM PLASMA OXIDE @ FRONTSIDE

Use Novellus. Perform PECVD of SiO_2, target thickness: 2 µm (depends on the amount of oxide etched in the Si etching steps).
Recipe: 2.0musio2.

COATING (FRONTSIDE)

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin

coating with Shipley SPR3012 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co-topo-3027-4.0um'** on the coating system (resist thickness: 1.4 µm at 48% RH).
After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

Alignment and exposure (frontside)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.
Expose mask 'bpad' (located in box 468) for a duration of 24.7 s (value is obtained from table).

Developing

The wafers are developed by a combination of EVG120 processes and manual development.
When using the EVG120 system, follow the instructions specified for this equipment.

1. Use program 'Dev_PEB' on the developer station. This performs a post-exposure bake at 115 °C for 60 seconds.
2. Manually develop in MF322. Duration: 1 min
3. Rinse thoroughly with DI water
4. Use program 'Dev_HB' on the developer station. This performs a hard bake at 100 °C for 60 seconds.

Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

Etch plasma oxide

Use Drytek Triode, two consecutive recipes.
1. Recipe: 'stdOxide'. Time: 180 s.
2. Recipe: 'Plasmox'. Time: 90 s.

Strip photoresist using Tepla

Strip resist	Use the Tepla plasma system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier. Use **'program 1'**: 1000 W power and automatic endpoint detection + 2 min overetching.

18. Cleaning Procedure: HNO_3 100% for green metals

Cleaning	10 minutes in fuming nitric acid (Merck: HNO_3 100% selectipur) at ambient temperature. This will dissolve organic materials. Use wet bench 'HNO_3 (100%) metaal' and the carrier with the yellow and red dots.
QDR	Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.
Drying	Use the Avenger 'rinser/dryer' with the standard program, and the white carrier with a black dot.

No HNO_3 65% at 110 °C cleaning step, because this will etch metals. !

19. Deposit second layer of plasma oxide, full wafer coverage

Deposit 250 nm plasma oxide @ frontside

Use Novellus Concept 1 PECVD system. Perform PECVD of SiO_2, target thickness: 290 nm (depends on the amount of oxide etched in the Si etching steps).

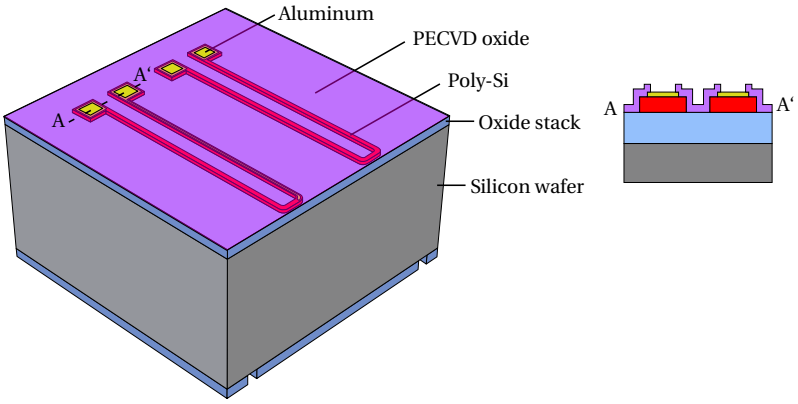

Figure A.6: Result after depositing the first PECVD oxide layer and opening the bond pads

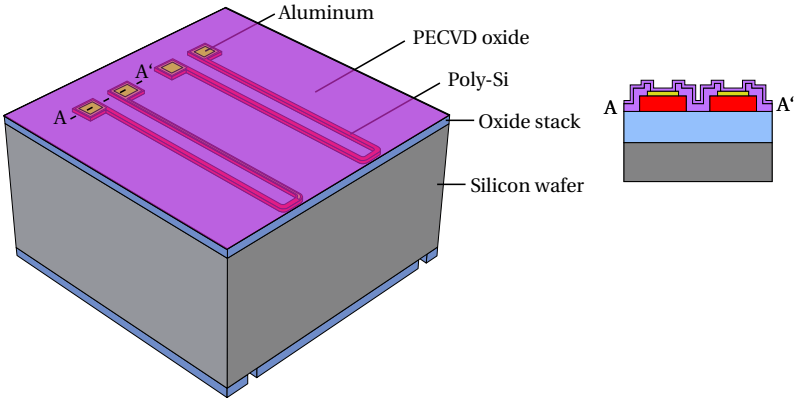

Figure A.7: Result after depositing the second PECVD layer

20. PATTERN AND RELEASE WAVEGUIDE BEAMS @ FRONTSIDE

SPINCOAT (FRONTSIDE)

On top of the spraycoated resist, spincoat a layer of AZ9260. Thickness: 12 µm
Wim Wien created a customized process to spincoat a thick layer of AZ9260 using the topo dispension.
Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.
The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with AZ9260 positive resist, and a soft bake at 95 °C for 90 seconds. The resist is dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use coating program **'Co_Edg_Syr_Topo_9260_12um'** on the coating system (resist thickness: 12 µm at 48% RH). After coating, check on the back part of the wafers that there are no resist residues. If there are, clean them with a cotton bud and acetone.

! Wait at least 30 minutes after coating for dehydration before exposure!

ALIGNMENT AND EXPOSURE (FRONTSIDE)

Processing will be performed on ELVIS / EVG420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Expose mask 'Ox' (located in box 468) for a duration of 90 s.
Wait at least 30 minutes after coating for dehydration before exposure! !

Bake photoresist
Bake the wafers in Memmert oven at a temperature of 110 °C for a duration of 90 min.

Developing
Manual developing of photoresist. Use 1 part of AZ400K diluted with 2 parts of DI water. For development time: start with 1 min 30 sec. Depending of the result (optical inspection) another 30 sec.

Inspection: Linewidth and overlay
Visually inspect the wafers through a microscope, and check the linewidth and overlay. No resist residues are allowed.

Etch Oxide (16 µm, stop on Silicon)
Drytek Triode for RIE
Recipe: StdOxide
Etchrate SiO_2: 500 nm/min
Etchrate AZ9260: 145 nm/min

Drytek Triode T384 etch parameters. Recipe: **'StdOxide'**

Step	**Gasses & flows**	**Pressure**	**RF power**	**He pressure**	**Etch time**
1. Oxide (RIE)	C_2F_6 @ 36 sccm CHF_3 @ 144 sccm	180 mTorr	300 W	12 Torr	~ 32 min

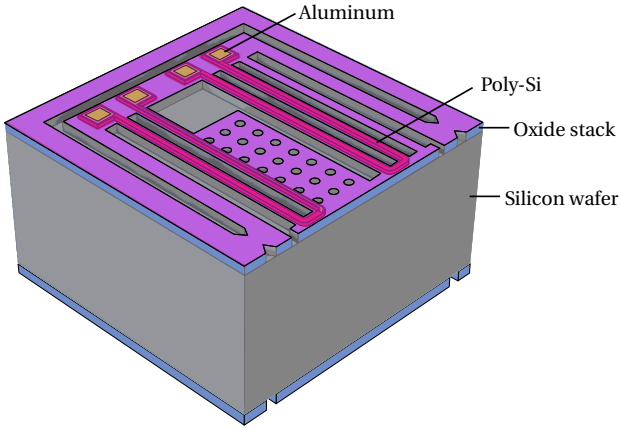

Figure A.8: Etching of the (frontside) oxide layer, stop on/in silicon. Not visible is the protective layer of plasma oxide on the frontside.

A

21. ETCH SILICON @ FRONTSIDE

ETCH SILICON ANISOTROPICALLY (60 µM)

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_Smooth_20C' to anisotropically etch the pattern into the silicon.
Etch rate: ~ 6 µm/min.
Etching 60 µm of Si requires around 300 loops.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_Smooth_20C'**

Step	Gasses & flows	Pressure	Source 1 Power	Source 2 power	Platen HF power	Process time
1. Strike	Ar @ 300 sccm C_4F_8 @ 220 sccm	40 mTorr	2500 W	500 W	0 W	2.0 s
2. Depo	C_4F_8 @ 220 sccm	40 mTorr	2500 W	500 W	0 W	1.2 s
3. Etch_1a	SF_6 @ 400 sccm	30 mTorr	2500 W	500 W	175 W	1.0 s
4. Etch_1b	SF_6 @ 400 sccm	30 mTorr	2500 W	500 W	60 W	2.5 s

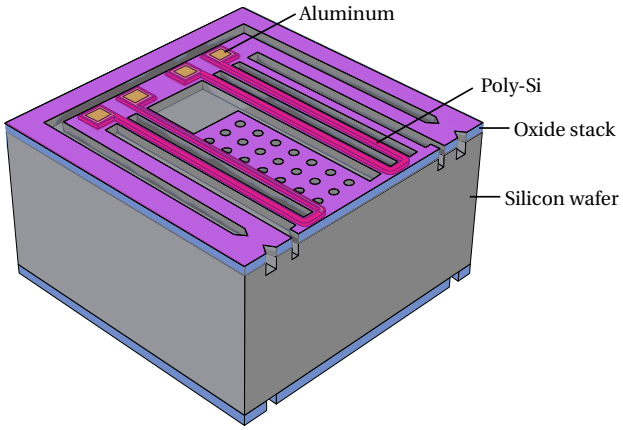

Figure A.9: Anisotropic etching of silicon. Not visible is the protective layer of plasma oxide on the frontside.

DEPOSIT PASSIVATION LAYER AND LOCALLY REMOVE IT

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_Depo_And_Pasiv_Etch' to deposit and subsequently locally remove the passivation layer.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_Depo_And_Pasiv_Etch'**

Step	Gasses & flows	Pressure	Source 1 Power	Source 2 power	Platen HF power	Process time
1. Strike	Ar @ 300 sccm C_4F_8 @ 220 sccm	40 mTorr	2500 W	500 W	0 W	2.0 s
2. d1	C_4F_8 @ 220 sccm	40 mTorr	2500 W	500 W	0 W	400.0 s
3. E1	SF_6 @ 350 sccm	25 mTorr	2500 W	0 W	75 W	100.0 s

22. Etch trenches in Si @ backside

Etch backside

Using the patterned SiO_2 as mask, etch 365 µm deep trenches in the backside.
Recipe: Rapier#No_endp_Si_Etch_Bosch.
Target etch depth: 330 µm. Number of cycles: 235.

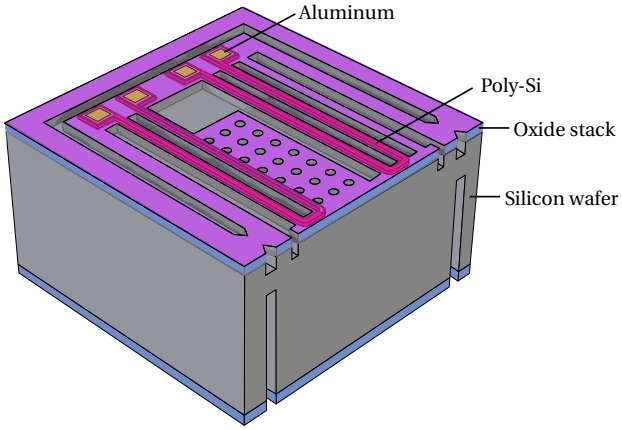

Figure A.10: Result after etching trenches in the Si (backside). Not visible is the protective layer of plasma oxide on the frontside.

23. Etch silicon @ frontside

Etch Silicon isotropically (35 µm): release

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch and passivation program may not be changed!
Use recipe 'DTC_IsoEtch_PS_01' to isotropically etch the silicon.
Etch rate: ~ 7 µm/min.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_IsoEtch_PS_01'**

Step	Gasses & flows	Pressure	Source 1 Power	Source 2 power	Platen HF power	Process time
1. Strike1	Ar @ 250 sccm C_4F_8 @ 1 sccm	50 mTorr	2500 W	0 W	0 W	5.0 s
2. Strike2	Ar @ 250 sccm C_4F_8 @ 250 sccm	75 mTorr	2500 W	0 W	0 W	5.0 s
3. IsoEtch1	SF_6 @ 500 sccm	100 mTorr	2500 W	0 W	0 W	300.0 s

Strip photoresist and passivation layer using Tepla

Strip resist — Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use **'program 04'**: 1000 W power and 15 min etching, and then repeat, for a total time of 30 min.

Etch Silicon isotropically (35 µm): remove supporting Silicon

Use the SPTS Rapier Omega i2L plasma etcher. Follow the operating instructions from the manual when using this machine. The process conditions of the etch and passivation program may not be changed!

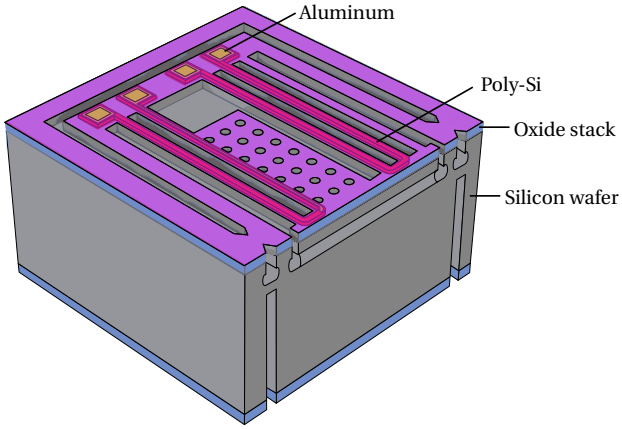

Figure A.11: The result after the first isotropic silicon etch. Not visible is the protective layer of plasma oxide on the frontside.

Use recipe 'DTC_IsoEtch_PS_01' to isotropically etch the silicon.
! Put process wafer on top of a carrier wafer to prevent etching into the chuck.
Etch rate: ~ 7 µm/min.

SPTS Rapier Omega i2L etch parameters. Recipe: **'DTC_IsoEtch_PS_01'**

Step	Gasses & flows	Pressure	Source 1 Power	Source 2 power	Platen HF power	Process time
1. Strike1	Ar @ 250 sccm C_4F_8 @ 1 sccm	50 mTorr	2500 W	0 W	0 W	5.0 s
2. Strike2	Ar @ 250 sccm C_4F_8 @ 250 sccm	75 mTorr	2500 W	0 W	0 W	5.0 s
3. IsoEtch1	SF_6 @ 500 sccm	100 mTorr	2500 W	0 W	0 W	300.0 s

ETCH TEMPORARY PECVD OXIDE PROTECTION

Use the Alcatel GIR 300 F etcher.
Use the standard oxide recipe. CF_4 @ 50 sccm, CHF_3 @ 25 sccm, and He @ 40 sccm.
Pressure: 0.05 mbar
Power: 60 W
Etch time: 10 min 30 s.

24. END OF PROCESS, FINAL INSPECTION

INSPECTION WITH SEM

Inspect the end-result using the SEM.

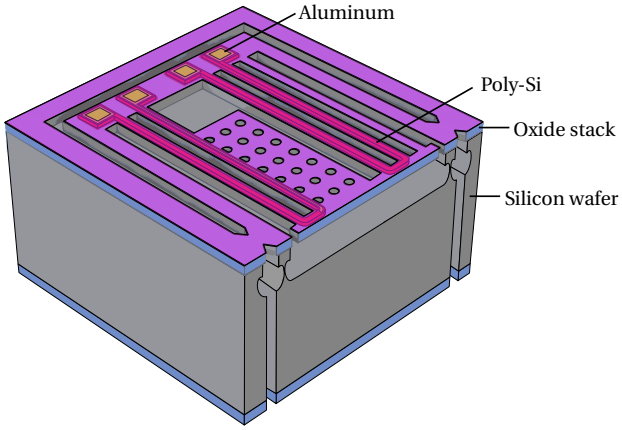

Figure A.12: The result after the second isotropic silicon etch.

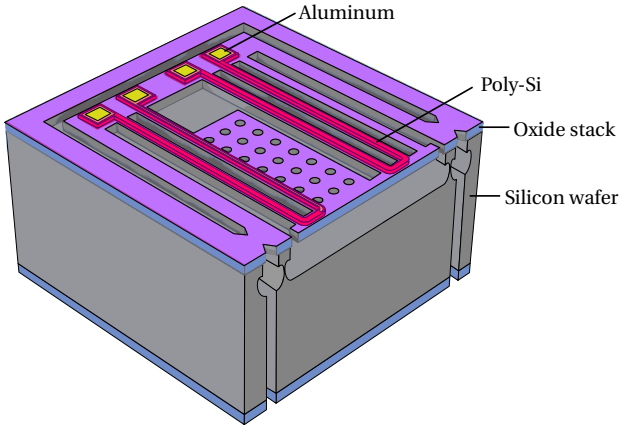

Figure A.13: The result after etching the PECVD oxide protective layer to open the aluminum bond pads

B

MASK LAYOUT

This appendix provides the mask layout that was used to fabricate the positionable waveguide arrays.

B.1. DESIGN PARAMETERS OF THE INDIVIDUAL CHIPS

The mask layout is created using a parameterized approach. In total, the mask design includes 31 design parameters. Table B.1 lists all the design parameters and includes a short description of every parameter. Parameters that are not in this list are driven by other design parameters. The design parameter values of all the chips on the mask/wafer are presented in Table B.2. The actual mask layout is provided in Figures B.2 to B.8.

B

Table B.1: List and description of design parameters

Design parameter	Description
# WGAs/chip	Depending on the size of the WGA, a single chip contains either one or two (identical) WGA's
# waveguides	The number of waveguide beams in the WGA
WG core width	The width of the Si_3N_4 core embedded in the waveguide beams
Small pitch, y	The waveguide pitch on the side of the chip where the WGA is located
Small pitch, x	The pitch of the crossbar beams that are perpendicular to the waveguides
Large pitch	The waveguide pitch on the side of the chip opposite to the side of the WGA
WG length	The length of the suspended part of the waveguides within the WGA
WG endwidth	The width of the waveguide beams
CB width	The width of the crossbar, expressed in crossbar beams
CB earsize	The extension of the crossbar from the outer actuator beam, expressed in crossbar beams
EH fillet	The fillet of the etch holes within the crossbar
WGA fillet	The fillet of the corners of the WGA, except for the etch holes within the crossbar
WGA offset	The offset between the edge of the chip and the center of the WGA
Chip edge cut	The contribution of the current chip to the singulation trench width
# bimorph beams	The number of bimorph actuator beams. Two sets with this number of beams are located adjacent to the waveguide beams
Bimorph pitch	The pitch of the bimorph actuator beams
# omissions	The number of omitted actuator beams between the outer waveguide beam and the inner actuator beam
Poly margin	The distance between the poly-Si and the edge of the SiO_2 actuator beam
Poly path width	The width of the poly-Si path (not the width of the poly-Si heaters)
Bondpad size	The size of the poly-Si part of the bondpads
Metal margin	The distance between the edge of the metal (aluminum in this case) and the edge of the poly-Si
Include U-beam	Determines whether a U-beam actuator (a type of in-plane actuator) is included in the WGA design, or not
# hot arms	The number of hot arms within the U-beam actuator
Hot arm width	The width of the hot arm(s)
Cold arm width	The width of the cold arm
Hot arm trench width	The width of the trench on the side of the hot arm(s)
Cold arm trench width	The width of the trench on the side of the cold arm
U-beam flex length	The length of the flexure within the U-beam
WGA flexure length	The length of the flexure connecting the U-beam to the WGA
WGA flexure width	The width of the flexure connecting the U-beam to the WGA
Breakout beam width	The width of the breakout beams placed between the chips

Table B.2: Overview of the design parameters as used in the mask layout

Chip ID	# WGAs/chip	# waveguides	WG core width (µm)	Small pitch, y (µm)	Small pitch, x (µm)	Large pitch (µm)	WG length (µm)	WG endwidth (µm)	CB width	CB earsize	EH fillet (µm)	WGA fillet (µm)	WGA offset (µm)	Chip edge cut (µm)	# bimorph beams	Bimorph pitch (µm)	# omissions	Poly margin (µm)	Poly path width (µm)	Bondpad size (µm)	Metal margin (µm)	Include U-beam	# hot arms	Hot arm width (µm)	Cold arm width (µm)	Hot arm trench width (µm)	Cold arm trench width (µm)	U-beam flex length (µm)	WGA flexure length (µm)	WGA flexure width (µm)	Breakout beam width (µm)
1	2	4	1.5	25	25	127	800	16	1	1	5	15	750	50	4	25	1	3	50	250	2	yes	1	18	5	10	10	160	30	10	800
2	2	4	1.5	25	25	127	1000	16	1	1	5	15	750	50	4	25	1	4	50	250	2	yes	1	18	5	10	10	200	30	10	900
3	2	6	1.5	25	25	127	1000	16	1	1	5	15	750	50	6	25	1	3	50	250	3	yes	1	18	5	10	10	200	30	10	900
4	2	4	1	25	25	127	1000	16	1	1	5	15	750	50	6	25	1	4	50	250	3	yes	1	18	5	10	10	200	30	10	850
5	1	6	1	250	50	127	500	18	1	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	600
6	1	6	1	250	50	127	700	18	1	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	700
7	1	6	1	250	50	127	800	18	1	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	800
8	1	8	1	250	50	127	1000	18	1	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	900
9	1	2	1	250	50	127	1000	18	1	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	900
10	1	6	1	250	50	127	800	18	1	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	850
11	1	6	1	250	50	127	900	18	1	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	750
12	1	6	1	250	50	127	1000	18	1	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	650
13	2	4	1.5	25	25	127	1000	16	1	1	5	15	750	50	4	25	1	3	50	250	2	no	0	0	0	0	0	0	0	0	0	600
14	2	8	1.5	25	25	127	500	16	1	1	5	15	750	50	4	25	1	3	50	250	3	no	0	0	0	0	0	0	0	0	0	700
15	2	8	1.5	25	25	127	700	16	1	1	5	15	750	50	4	25	1	3	50	250	2	no	0	0	0	0	0	0	0	0	0	800
16	2	8	1.5	25	25	127	800	16	1	1	5	15	750	50	4	25	1	3	50	250	3	no	0	0	0	0	0	0	0	0	0	900
17	2	8	1.5	25	25	127	900	16	1	1	5	15	750	50	6	25	1	3	50	250	2	no	0	0	0	0	0	0	0	0	0	900
18	2	8	1.5	25	25	127	1000	16	3	1	5	15	750	50	6	25	1	3	50	250	3	no	0	0	0	0	0	0	0	0	0	850
19	2	8	1.5	25	25	127	1200	16	1	1	5	15	750	50	6	25	1	3	50	250	2	no	0	0	0	0	0	0	0	0	0	750
20	2	8	1	25	25	127	1400	16	1	1	5	15	750	50	6	25	1	3	50	250	3	no	0	0	0	0	0	0	0	0	0	650
21	2	4	1	50	50	127	500	18	1	1	5	15	750	50	4	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	0	400
22	2	4	1	50	50	127	700	18	1	1	5	15	750	50	4	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	0	500
23	2	4	1	50	50	127	800	18	1	1	5	15	750	50	4	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	0	600
24	2	4	1	50	50	127	900	18	1	1	5	15	750	50	4	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	0	700
25	2	4	1	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	4	50	250	2	yes	2	18	3	10	10	100	25	19	800
26	2	4	1	50	50	127	1200	18	1	1	5	15	750	50	4	50	1	4	50	250	3	yes	2	18	3	10	10	120	3	0	900
27	2	4	1	50	50	127	1000	18	3	1	5	15	750	50	6	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	0	900
28	2	4	1	50	50	127	1000	18	1	2	5	15	750	50	6	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	0	850
29	2	4	1	50	50	127	900	18	1	1	5	15	750	50	6	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	0	750
30	2	4	1	50	50	127	800	18	1	1	5	15	750	50	6	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	0	650
31	2	4	1	50	50	127	700	18	1	1	5	15	750	50	6	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	0	550

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Table B.2: Overview of the design parameters as used in the mask layout

Chip ID	# WGAs/chip	# waveguides	WG core width (µm)	Small pitch, y (µm)	Small pitch, x (µm)	Large pitch (µm)	WG length (µm)	WG endwidth (µm)	CB width	CB earsize	EH fillet (µm)	WGA fillet (µm)	WGA offset (µm)	Chip edge cut (µm)	# bimorph beams	Bimorph pitch (µm)	# omissions	Poly margin (µm)	Poly path width (µm)	Bondpad size (µm)	Metal margin (µm)	Include U-beam	# hot arms	Hot arm width (µm)	Cold arm width (µm)	Hot arm trench width (µm)	Cold arm trench width (µm)	U-beam flex length (µm)	WGA flexure length (µm)	WGA flexure width (µm)	Breakout beam width (µm)
32	2	4	1	50	50	127	500	18	1	1	5	15	750	50	6	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	450
33	1	2	1	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	400
34	1	4	1	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	500
35	1	6	1	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	600
36	1	8	1	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	700
37	1	2	1	127	50	127	900	18	1	2	13	15	3000	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	800
38	1	4	1	127	50	127	900	18	1	2	13	15	3000	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	900
39	1	6	1	127	50	127	900	18	1	2	13	15	3000	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	900
40	1	8	1	127	50	127	900	18	1	2	13	15	3000	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	850
41	1	2	1.5	127	50	127	1000	18	3	2	13	15	3000	50	6	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	750
42	1	4	1.5	127	50	127	1000	18	3	2	13	15	3000	50	6	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	650
43	1	6	1.5	127	50	127	1000	18	3	2	13	15	3000	50	6	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	550
44	1	8	1.5	127	50	127	1000	18	3	2	13	15	3000	50	6	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	450
45	1	2	1.5	250	50	127	1000	18	1	4	15	15	2500	50	4	50	4	3	50	250	2	yes	1	18	3	10	10	100	30	19	300
46	1	4	1.5	250	50	127	500	18	1	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	400
47	1	4	1.5	250	50	127	700	18	1	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	500
48	1	4	1.5	250	50	127	800	18	1	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	600
49	1	4	1.5	250	50	127	800	18	1	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	700
50	1	4	1.5	250	50	127	900	18	1	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	800
51	1	4	1.5	250	50	127	900	18	1	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	900
52	1	4	1.5	250	50	127	1000	18	1	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	900
53	1	4	1.5	250	50	127	1000	18	1	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	850
54	1	4	1.5	250	50	127	1200	18	1	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	750
55	1	4	1.5	250	50	127	1400	18	1	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	650
56	1	4	1.5	250	50	127	1000	18	1	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	550
57	1	4	1.5	250	50	127	800	18	1	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	450
58	1	4	1.5	250	50	127	800	18	1	4	15	15	2500	50	4	50	4	3	50	250	3	yes	2	18	3	10	10	160	30	19	400
59	2	2	1.5	50	50	127	800	18	1	1	5	15	900	50	4	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	400
60	2	2	1.5	50	50	127	900	18	1	1	5	15	900	50	4	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	500
61	2	2	1.5	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	600
62	2	6	1.5	50	50	127	900	18	1	1	5	15	900	50	4	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	700

Table B.2: Overview of the design parameters as used in the mask layout

Chip ID	# WGAs/chip	# waveguides	WG core width (µm)	Small pitch, y (µm)	Small pitch, x (µm)	Large pitch (µm)	WG length (µm)	WG endwidth (µm)	CB width	CB earsize	EH fillet (µm)	WGA fillet (µm)	WGA offset (µm)	Chip edge cut (µm)	# bimorph beams	Bimorph pitch (µm)	# omissions	Poly margin (µm)	Poly path width (µm)	Bondpad size (µm)	Metal margin (µm)	Include U-beam	# hot arms	Hot arm width (µm)	Cold arm width (µm)	Hot arm trench width (µm)	Cold arm trench width (µm)	U-beam flex length (µm)	WGA flexure length (µm)	WGA flexure width (µm)	Breakout beam width (µm)
63	2	6	1.5	50	50	127	1000	18	1	1	5	15	900	50	4	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	800
64	2	4	1.5	50	50	127	800	18	1	1	5	15	750	50	4	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	900
65	2	4	1.5	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	900
66	2	6	1.5	50	50	127	800	18	1	1	5	15	750	50	6	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	850
67	2	6	1.5	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	750
68	2	2	1.5	50	50	127	800	18	1	1	5	15	750	50	6	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	650
69	2	2	1.5	50	50	127	900	18	1	1	5	15	750	50	6	50	1	4	50	250	2	no	0	0	0	0	0	0	0	0	550
70	2	2	1.5	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	4	50	250	3	no	0	0	0	0	0	0	0	0	450
71	2	2	2	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	400
72	2	2	2	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	500
73	2	2	2	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	600
74	2	6	2	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	700
75	2	6	2	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	800
76	2	4	2	50	50	127	1000	18	1	1	5	15	750	50	4	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	900
77	2	4	2	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	900
78	2	6	2	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	850
79	2	6	2	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	750
80	2	2	2	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	650
81	2	2	2	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	550
82	2	2	2	50	50	127	1000	18	1	1	5	15	750	50	6	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	450
83	1	6	2	250	50	127	1200	18	2	4	15	15	2500	50	4	50	4	3	50	250	2	yes	2	18	3	10	10	120	3	0	500
84	1	4	2	250	50	127	500	18	2	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	400
85	1	4	2	250	50	127	700	18	2	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	500
86	1	4	2	250	50	127	800	18	2	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	600
87	1	4	2	250	50	127	800	18	2	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	700
88	1	4	2	250	50	127	900	18	2	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	800
89	1	4	2	250	50	127	900	18	2	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	900
90	1	4	2	250	50	127	1000	18	2	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	900
91	1	4	2	250	50	127	1000	18	2	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	850
92	1	4	2	250	50	127	1200	18	2	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	750
93	1	4	2	250	50	127	1400	18	2	4	15	15	2500	50	6	50	4	3	50	250	2	yes	2	18	3	10	10	210	3	0	650

Table B.2: Overview of the design parameters as used in the mask layout

Chip ID	# WGAs/chip	# waveguides	WG core width (µm)	Small pitch, y (µm)	Small pitch, x (µm)	Large pitch (µm)	WG length (µm)	WG endwidth (µm)	CB width	CB earsize	EH fillet (µm)	WGA fillet (µm)	WGA offset (µm)	Chip edge cut (µm)	# bimorph beams	Bimorph pitch (µm)	# omissions	Poly margin (µm)	Poly path width (µm)	Bondpad size (µm)	Metal margin (µm)	Include U-beam	# hot arms	Hot arm width (µm)	Cold arm width (µm)	Hot arm trench width (µm)	Cold arm trench width (µm)	U-beam flex length (µm)	WGA flexure length (µm)	WGA flexure width (µm)	Breakout beam width (µm)
94	1	4	2	250	50	127	1000	18	2	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	550
95	1	4	2	250	50	127	800	18	2	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	450
96	1	4	2	250	50	127	1000	18	2	4	15	15	2500	50	6	50	4	3	50	250	3	yes	2	18	3	15	15	300	30	19	600
97	1	2	1.5	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	400
98	1	4	1.5	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	500
99	1	6	1.5	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	600
100	1	8	1.5	127	50	127	800	18	2	2	13	15	3000	50	4	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	700
101	1	2	2	127	50	127	900	18	2	2	13	15	3000	50	4	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	800
102	1	4	2	127	50	127	900	18	2	2	13	15	3000	50	4	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	900
103	1	6	2	127	50	127	900	18	2	2	13	15	3000	50	6	50	2	3	50	250	2	no	0	0	0	0	0	0	0	0	900
104	1	8	2	127	50	127	900	18	2	2	13	15	3000	50	6	50	2	3	50	250	3	no	0	0	0	0	0	0	0	0	850
105	1	2	2	127	50	127	1000	18	2	2	13	15	3000	50	6	50	2	3	50	250	2	yes	2	18	3	10	10	100	25	19	750
106	1	4	2	127	50	127	1000	18	2	2	13	15	3000	50	6	50	2	3	50	250	3	yes	2	18	3	10	10	100	25	19	650
107	1	6	2	127	50	127	1000	18	2	2	13	15	3000	50	6	50	2	4	50	250	2	yes	2	18	3	10	10	100	25	19	550
108	1	8	2	127	50	127	1000	18	2	2	13	15	3000	50	6	50	2	5	50	250	3	yes	2	18	3	10	10	100	25	19	450
109	2	4	1.5	50	50	127	500	18	2	2	5	15	750	50	4	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	400
110	2	4	1.5	50	50	127	700	18	2	2	5	15	750	50	4	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	500
111	2	4	1.5	50	50	127	800	18	2	2	5	15	750	50	4	50	1	5	50	250	2	yes	2	18	3	10	10	80	25	19	600
112	2	4	1.5	50	50	127	900	18	2	2	5	15	750	50	4	50	1	5	50	250	3	yes	2	18	3	10	10	90	25	19	700
113	2	4	1.5	50	50	127	1000	18	2	2	5	15	750	50	4	50	1	4	50	250	2	yes	2	18	3	10	10	100	25	19	800
114	2	4	1.5	50	50	127	1200	18	2	2	5	15	750	50	4	50	1	4	50	250	3	yes	2	18	3	10	10	120	3	0	900
115	2	4	1.5	50	50	127	1000	18	2	2	5	15	750	50	6	50	1	4	50	250	2	yes	2	18	3	10	10	100	25	19	900
116	2	4	1.5	50	50	127	1000	18	2	2	5	15	750	50	6	50	1	3	50	250	3	yes	1	18	3	10	10	100	25	19	850
117	2	4	1.5	50	50	127	900	18	2	2	5	15	750	50	6	50	1	3	50	250	2	yes	1	18	3	10	10	90	25	19	750
118	2	4	1.5	50	50	127	800	18	2	2	5	15	750	50	6	50	1	3	50	250	3	yes	1	18	3	10	10	80	25	19	650
119	2	4	1.5	50	50	127	700	18	2	2	5	15	750	50	6	50	1	5	50	250	2	no	0	0	0	0	0	0	0	0	550
120	2	4	1.5	50	50	127	500	18	2	2	5	15	750	50	6	50	1	5	50	250	3	no	0	0	0	0	0	0	0	0	450
121	2	4	1.5	25	25	127	1000	16	2	2	5	15	750	50	4	25	10	5	50	250	2	yes	2	18	5	10	10	100	25	19	600
122	2	8	1.5	25	25	127	500	16	1	2	5	15	750	50	4	25	10	5	50	250	3	no	0	0	0	0	0	0	0	0	700
123	2	8	1.5	25	25	127	700	16	1	2	5	15	750	50	4	25	10	5	50	250	2	no	0	0	0	0	0	0	0	0	800
124	2	8	1.5	25	25	127	800	16	1	2	5	15	750	50	4	25	10	5	50	250	3	yes	2	18	5	10	10	80	25	19	900

Table B.2: Overview of the design parameters as used in the mask layout

Chip ID	# WGAs/chip	# waveguides	WG core width (µm)	Small pitch, y (µm)	Small pitch, x (µm)	Large pitch (µm)	WG length (µm)	WG endwidth (µm)	CB width	CB earsize	EH fillet (µm)	WGA fillet (µm)	WGA offset (µm)	Chip edge cut (µm)	# bimorph beams	Bimorph pitch (µm)	# omissions	Poly margin (µm)	Poly path width (µm)	Bondpad size (µm)	Metal margin (µm)	Include U-beam	# hot arms	Hot arm width (µm)	Cold arm width (µm)	Hot arm trench width (µm)	Cold arm trench width (µm)	U-beam flex length (µm)	WGA flexure length (µm)	WGA flexure width (µm)	Breakout beam width (µm)
125	2	8	1.5	25	25	127	900	16	2	2	5	15	750	50	6	25	10	3	50	250	2	yes	2	18	5	10	10	90	25	19	900
126	2	8	1.5	25	25	127	1000	16	3	2	5	15	750	50	6	25	10	3	50	250	3	yes	2	18	5	10	10	100	25	19	850
127	2	8	1.5	25	25	127	1200	16	2	2	5	15	750	50	6	25	10	5	50	250	2	yes	2	18	5	10	10	120	3	0	750
128	2	4	1	25	25	127	1400	16	2	2	5	15	750	50	6	25	10	5	50	250	3	yes	2	18	5	10	10	140	3	0	650
129	1	6	1	250	50	127	500	18	2	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	600
130	1	6	1	250	50	127	700	18	2	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	700
131	1	6	1	250	50	127	800	18	2	4	15	15	2500	50	4	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	800
132	1	8	1	250	50	127	1000	18	2	4	15	15	2500	50	4	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	900
133	1	2	1	250	50	127	1000	16	2	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	900
134	1	6	1	250	50	127	800	18	2	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	850
135	1	6	1	250	50	127	900	18	2	4	15	15	2500	50	6	50	4	3	50	250	2	no	0	0	0	0	0	0	0	0	0	750
136	1	6	1	250	50	127	1000	18	2	4	15	15	2500	50	6	50	4	3	50	250	3	no	0	0	0	0	0	0	0	0	0	650
137	2	4	1.5	25	25	127	800	16	2	2	5	15	750	50	4	25	1	3	50	250	2	no	0	0	0	0	0	0	0	0	0	800
138	2	6	1.5	25	25	127	1000	16	2	2	5	15	750	50	4	25	1	3	50	250	3	no	0	0	0	0	0	0	0	0	0	900
139	2	4	1.5	25	25	127	1000	16	2	2	5	15	750	50	6	25	1	4	50	250	2	no	0	0	0	0	0	0	0	0	0	900
140	2	4	1	25	25	127	1000	16	2	2	5	15	750	50	6	25	1	3	50	250	3	no	0	0	0	0	0	0	0	0	0	850

B.2. FULL WAFER MASK LAYOUT

The full wafer layout with all the six mask layers is presented in Figure B.1. A single 100 mm (4-inch) wafer holds 140 chips, taking into account a chip size of 6.1 mm by 6.1 mm.

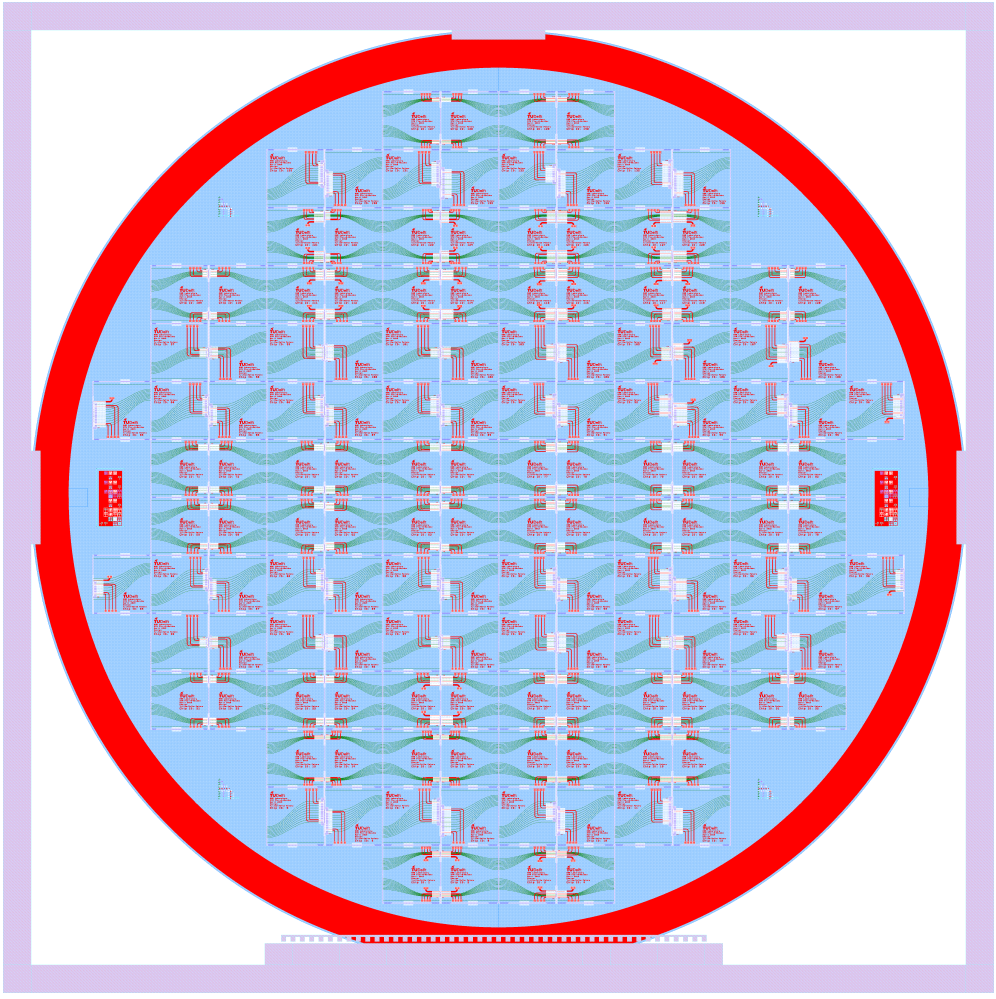

Figure B.1: Mask layout of full wafer, combined view of all the layers.

B.3. SINGLE CHIP MASK LAYOUT

The mask layout of a single chip (chip 34) is provided in Figures B.2 to B.8. Chip 34 is characterized and discussed in Chapter 4 as well as in Chapter 5 (see Figure 4.7 and Figure 5.11). Figure B.2 provides a combined view of all the layers, followed by views of the individual layers. The layer with the waveguide cores is presented in Figure B.3. Figure B.4 shows the mask that defines the poly-Si layer. The pattern of the aluminum is depicted in Figure B.5. Bondpad openings are defined by the mask in Figure B.6. Figure B.7 shows the layer for backside silicon etching, which is used for creating the trenches between the chips. Finally, the pattern for the front side SiO_2 etch is presented in Figure B.8.

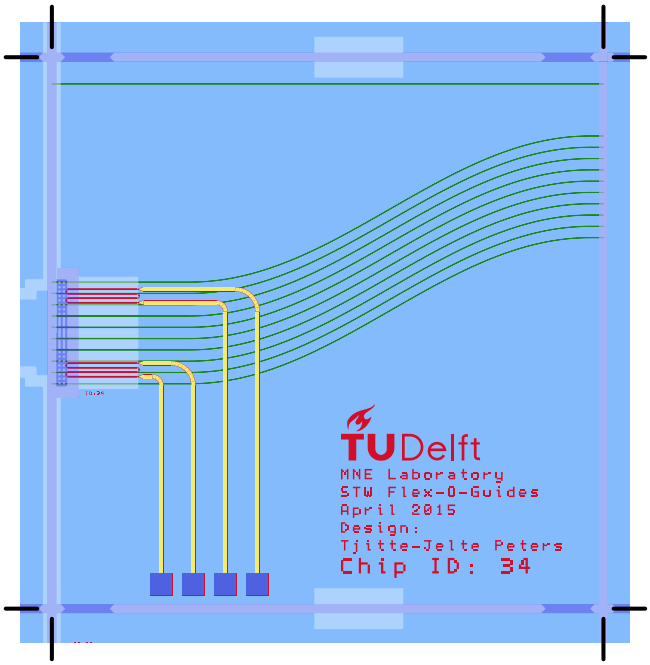

Figure B.2: Mask layout of chip 34, combined view of all the layers.

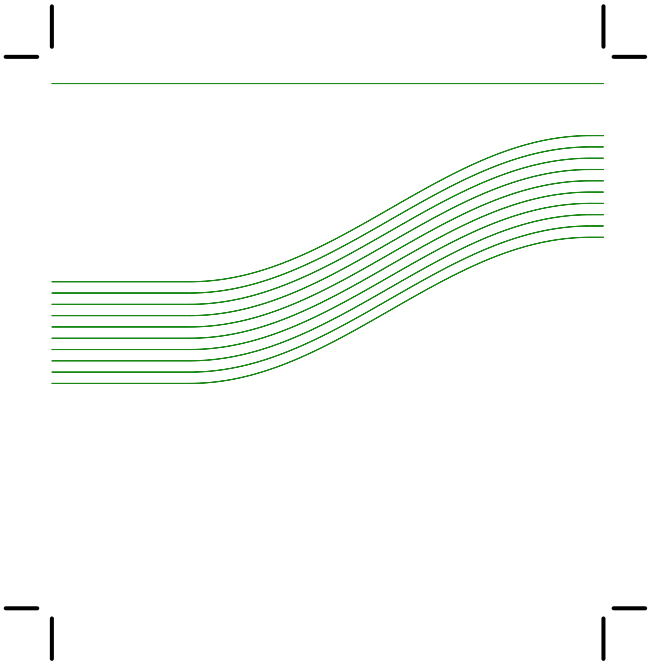

Figure B.3: Mask layout of chip 34, *waveguide* layer only. Drawn features are the Si_3N_4 waveguide cores.

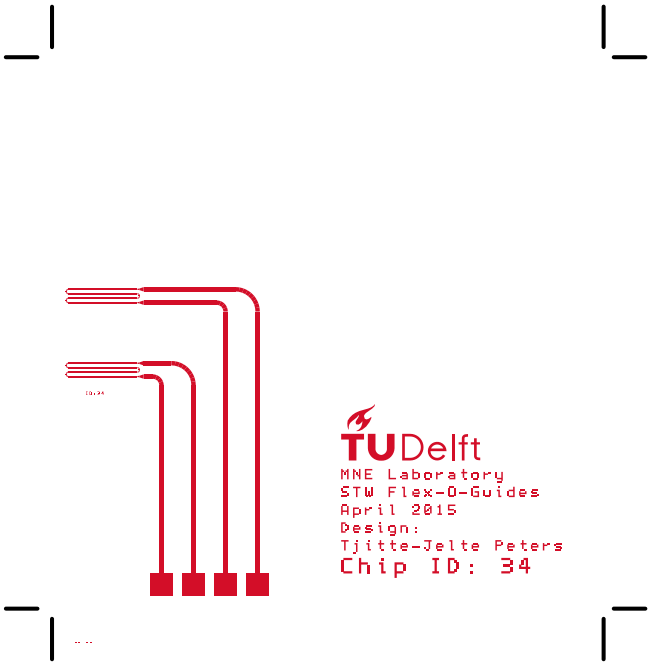

Figure B.4: Mask layout of chip 34, *poly-Si* layer only. Drawn features are poly-Si.

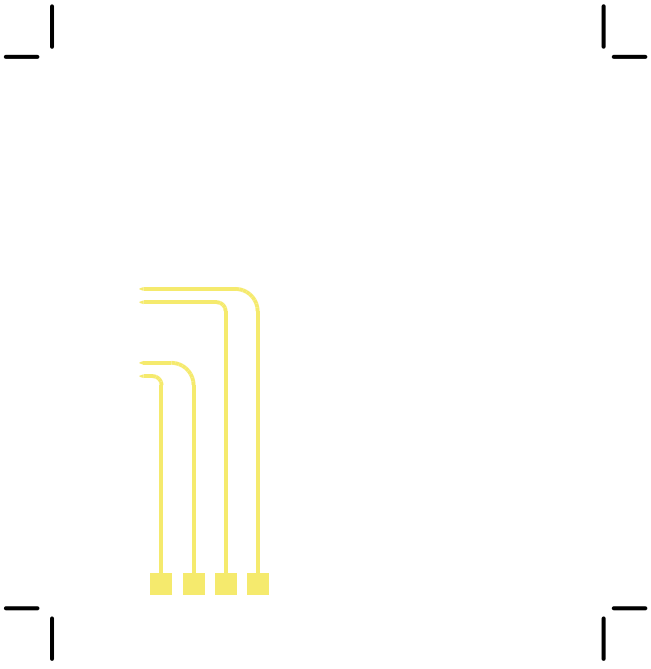

Figure B.5: Mask layout of chip 34, *aluminum* layer only. Drawn features are aluminum.

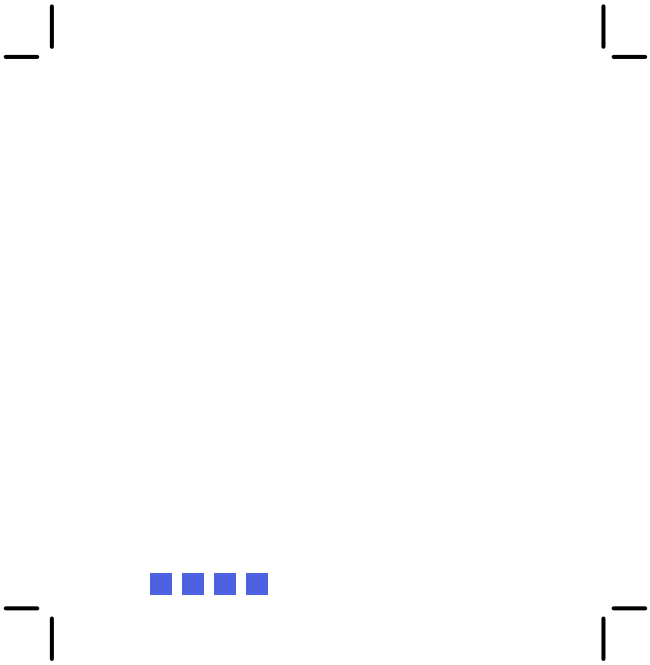

Figure B.6: Mask layout of chip 34, *bondpad opening* layer only. Drawn features are where oxide is opened to contact the bondpads.

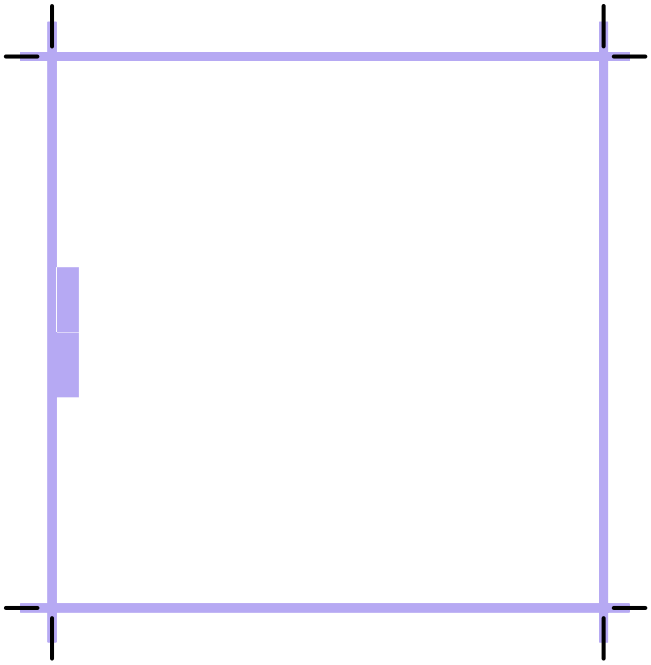

Figure B.7: Mask layout of chip 34, *backside* layer only. Drawn features are etched in silicon from the backside.

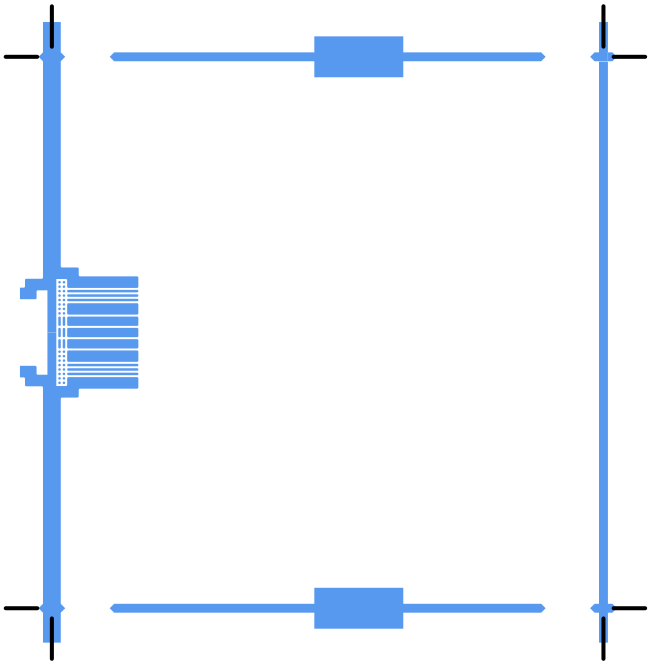

Figure B.8: Mask layout of chip 34, *oxide* layer only. Drawn features are etched in the oxide layer.

SUMMARY

THIS thesis describes the development of a positionable waveguide array realized in a silicon nitride / silicon dioxide (Si_3N_4 core / SiO_2 cladding) photonic platform. The positionable waveguide array is the heart of a novel alignment approach for high precision multi-channel chip-to-chip interconnects. This alignment approach enables submicron accurate alignment of an Indium Phosphide (InP) Photonic Integrated Circuit (PIC) and a TriPleX interposer chip. Mechanically flexible waveguides with integrated alignment functionality are realized within the TriPleX interposer chip. Compared to competing alignment approaches, the proposed concept targets higher accuracy and precision and allows for an increased level of automation to lower assembly time and cost.

The final alignment of the waveguides is achieved in two stages. In the first stage, both chips are flip-chip bonded on a common substrate. The result of this first stage is a coarse alignment of the waveguides of both chips, as well as mechanical fixation and electrical connection of both chips. In the second stage, integrated alignment functionality of the positionable waveguide array within the TriPleX interposer chip is used to optimally align the interposer waveguides with the waveguides of the InP PIC. Once aligned, the alignment function of the positionable waveguide array has served its purpose and the positionable waveguide array is mechanically fixed, providing an optimal alignment for the lifetime of the PIC.

The manufacturability of suspended SiO_2 beam structures has been investigated. A major fabrication challenge is the release of thick (>10 μm) SiO_2 structures with high yield. A microfabrication process based on a special reinforcement method is developed for the reliable release of SiO_2 beam structures. A supporting layer of Si functions as a reinforcing layer during etching and release. This supporting Si layer reduces the bending and stress concentrations in clamped-clamped beams, thereby enabling a high fabrication yield.

The fabrication process is tested on a silicon wafer with a ~ 15 μm thick thermal oxide layer. The obtained suspended structures are mechanically characterized. Two deformation effects can be distinguished: a curvature of the beam and a slope at the base of the beam. These effects are caused by the compressive mean stress and the gradient stress in the thermal SiO_2. The curvature of the SiO_2 – Si beams corresponds to a concave downward profile while the SiO_2 beams without supporting Si reveal a small curvature in the opposite direction (concave upward). The slope at the base is approximately 0.5° for the SiO_2 beams and between 0.5° and 0° for the SiO_2 – Si beams. The acquired bending stiffness of long SiO_2 beams is in the newton per meter range (e.g., 0.8 N/m for a cantilever measuring 1000 μm in length and 13 μm in width).

The fabrication process is extended to include integrated actuators. Electrothermal bimorph actuators consisting of polysilicon on top of ~ 15 μm thick silicon dioxide beams have been designed, fabricated, and characterized. This material platform enables the integration of actuators with photonic waveguides, producing photonic waveguide structures that are mechanically flexible and positionable. The characterization includes measure-

ments of the postrelease deformation (i.e., without actuation) as well as the deflection resulting from quasi-static and dynamic actuation. The postrelease deformation reveals a curvature, resulting in the free ends of 800 μm long silicon dioxide beams with 5 μm thick polysilicon to be situated approximately 80 μm above the chip surface. Bimorph actuators having an 800 μm length and a 5 μm thick polysilicon layer produce an out-of-plane deflection of approximately 11 μm at 60 mW dissipated power, corresponding to an estimated 240 °C actuator temperature. The delivered actuation force of the 800 μm long bimorph actuators having 5 μm thick polysilicon is calculated to be approximately 750 μN at 120 mW.

Finally, positionable photonic waveguide arrays are developed for optical chip-to-chip alignment. Partly suspended photonic structures, based on the Si_3N_4/SiO_2 material platform, are equipped with thermal actuators, enabling the free end of the structures to be positioned with submicrometer accuracy. A crossbar mechanically connects the free ends of the suspended waveguide beams with the free ends of the actuator beams. This crossbar design allows the free ends of the waveguide beams to be positioned as a single array of which the pitch is precisely defined by photo lithography. A finite element model is developed to provide insight in the way the design of the system affects the performance. The modeling results show that the expected vertical deflection and rotation are highly dependent on the array design. Measurements of fabricated devices confirm the trends that follow from the model, and are used to assess the positioning performance. Moreover, the finite element analysis gives guidelines for the design parameters of an optimal positionable photonic waveguide array. By following these guidelines, all the requirements for the intended photonic alignment can be fulfilled, which is validated by measurements. The stability over time of the positioning system is experimentally determined, and is also sufficient. Measured mode field profiles of partly suspended waveguide beams with 1 μm × 220 nm (width × thickness) sized waveguide cores show correct waveguiding functionality. Furthermore, an alignment experiment demonstrates how three adjacent waveguide beams within a positionable waveguide array can be actively aligned with the channels of another photonic chip.

SAMENVATTING

DIT proefschrift beschrijft de ontwikkeling van positioneerbare lichtkanalen, gerealiseerd in een fotonisch platform van siliciumnitride / siliciumdioxide (Si_3N_4 kern in een SiO_2 omhulling). De positioneerbare lichtkanalen vormen de basis van een nieuw uitlijnconcept voor meerkanaals chip-naar-chip verbindingen met een hoge uitlijnnauwkeurigheid. Het uitlijnconcept maakt submicronnauwkeurige uitlijning mogelijk tussen een Indium Phosphide (InP) fotonisch geïntegreerd circuit (PIC) en een TriPleX-interposer-chip. Deze TriPleX-interposer-chip bevat beweegbare lichtkanalen met geïntegreerde uitlijnfunctionaliteit. In vergelijking met andere uitlijnprincipes is het voorgestelde concept ontworpen om een hogere uitlijnnauwkeurigheid te behalen en om automatisering mogelijk te maken, waarmee de uitlijntijd en daarmee de kosten omlaag worden gebracht.

De uiteindelijke uitlijning van de lichtkanalen vindt plaats in twee stappen. In de eerste stap worden de beide chips op een gedeeld substraat bevestigd, waarbij van beide chips het oppervlak met de lichtkanalen naar het substraat gericht is. Na deze stap zijn de lichtkanalen van beide chips grof uitgelijnd, en zijn de twee chips vastgezet en elektrisch aangeloten. In de tweede stap wordt de geïntegreerde uitlijningsfunctionaliteit gebruikt om de interposer-lichtkanalen optimaal uit te lijnen met de lichtkanalen van de InP PIC. Zodra de lichtkanalen uitgelijnd zijn, heeft de geïntegreerde uitlijnfunctionaliteit haar taak volbracht. De positioneerbare lichtkanalen worden dan vastgezet, zodat de optimale uitlijning behouden blijft gedurende de levensduur van de PIC.

De produceerbaarheid van beweegbare SiO_2 lichtkanalen is onderzocht. Bij de fabricage van beweegbare SiO_2 lichtkanalen met een dikte van >10 µm is er een grote kans dat de lichtkanalen knappen. Dit heeft te maken met het groeiproces van het SiO_2, wat plaatsvindt bij een hoge temperatuur. Doordat de uitzettingscoefficient van Si groter is dan die van SiO_2, drukt het Si bij kamertemperatuur het SiO_2 in elkaar. Wanneer het onderliggende Si wordt verwijderd door middel van etsen, zet het SiO_2 uit, en kan buiging zorgen voor knappende lichtkanalen. Er is een microfabricageproces ontwikkeld dat gebruik maakt van een speciale versterkingsmethode voor het veilig fabriceren van beweegbare SiO_2 lichtkanalen. Een ondersteunende laag van Si functioneert als versterking tijdens etsen en losmaken. Deze ondersteunende laag Si vermindert het buigen van de beweegbare lichtkanalen en verlaagt daarmee de spanningsconcentraties in het materiaal, waardoor het afknappen kan worden voorkomen.

Het fabricageproces is getest op een siliciumwafer met thermisch oxide van ~ 15 µm dikte. De verkregen beweegbare structuren (hierna: cantilevers) zijn gekarakteriseerd. Twee vervormings-effecten kunnen worden onderscheiden: een kromming van de cantilevers en een helling aan de basis van de cantilevers. Deze effecten worden veroorzaakt door de mechanische spanning in het thermische SiO_2, welke zowel een constante component heeft als een component met een gradiënt. De SiO_2 – Si cantilevers hebben een neerwaartse kromming over de lengte terwijl de SiO_2 cantilevers zonder Si ondersteuning een kleine kromming in de tegenovergestelde richting hebben (opwaarts). De helling aan de basis is

ongeveer 0.5° voor de SiO_2 cantilevers en tussen 0.5° en 0° voor de SiO_2 – Si cantilevers. De gemeten buigstijfheid van lange SiO_2 cantilevers ligt in de Newton-per-meter orde (bijvoorbeeld 0.8 N/m voor een 1000 μm lange en 13 μm brede cantilever.

Het fabricageproces is vervolgens uitgebreid met geïntegreerde actuatoren. Elektrothermische bimorf actuatoren bestaande uit ~ 15 μm dikke siliciumdioxide cantilevers met polysilicium erop zijn ontworpen, gefabriceerd en gekarakteriseerd. Dankzij dit materiaalplatform kunnen actuatoren geïntegreerd worden met fotonische lichtkanalen, waardoor deze positioneerbaar worden. De karakterisatie bestaat uit metingen van zowel de neutrale statische vervorming (d.w.z. zonder elektrische aansturing) als de buiging resulterend uit quasi-statische en dynamische elektrische aansturing. De neutrale vervorming laat een kromming zien, waardoor de vrije uiteinden van 800 μm lange siliciumdioxide cantilevers met 5 μm dik polysilicium zich ongeveer 80 μm boven het chipoppervlak bevinden. Bimorfe actuatoren met een lengte van 800 μm en een 5 μm dikke polysiliciumlaag produceren een uit-het-vlak verplaatsing van ongeveer 11 μm bij 60 mW verbruikt vermogen, wat overeenkomt met een geschatte actuatortemperatuur van 240 °C. Volgens berekeningen kunnen de bimorfe actuatoren van 800 μm met polysilicium van 5 μm dik een kracht leveren van ongeveer 750 μN bij 120 mW.

Ten slotte zijn positioneerbare lichtkanalen ontwikkeld voor optische uitlijning op chip niveau. Gedeeltelijk vrijhangende fotonische structuren die gebaseerd zijn op het Si_3N_4/SiO_2 materiaalplatform zijn uitgerust met thermische actuatoren, waardoor het vrije einde kan worden gepositioneerd met submicrometer nauwkeurigheid. Een eindig elementenmodel is ontwikkeld om inzicht te krijgen in de manier waarop het ontwerp van het systeem de prestaties beïnvloedt. Uit de resultaten van het modelleren blijkt dat de verwachte verticale buiging en rotatie in hoge mate afhankelijk zijn van het ontwerp van het gehele systeem. Metingen van gefabriceerde chips bevestigen de voorspellingen die volgen uit het model, en zijn gebruikt om de positioneringprestaties te beoordelen. Bovendien geeft de eindige elementenanalyse richtlijnen voor de ontwerpparameters van een optimale positioneerbaarheid van lichtkanalen. Door deze richtlijnen te volgen, kan aan alle eisen voor de beoogde fotonische uitlijning worden voldaan, wat wordt bevestigd door metingen. De stabiliteit als functie van tijd van het positioneringssysteem is experimenteel bepaald en is voldoende. Gemeten optische veldprofielen van gedeeltelijk vrijhangende lichtkanalen met kernen van 1 μm × 220 nm (breedte × dikte) laten een correct functionerende golfgeleiding zien. Met een uitlijningsexperiment is gedemonstreerd hoe drie naast elkaar liggende positioneerbare lichtkanalen actief kunnen worden uitgelijnd met de lichtkanalen van een andere fotonische chip.

ABOUT THE AUTHOR

Tjitte-Jelte Peters was born on 24-04-1983 in Balk, The Netherlands. He received both his B.Sc. and M.Sc. in Electrical Engineering from the University of Twente, Netherlands. During his education, he specialized in Microsystems and Microelectronics at the Transducers Science and Technology group. After working at mechatronic engineering firm Demcon for almost a year, he joined Delft University of Technology in 2012 as a PhD candidate at the Micro and Nano Engineering Laboratory. In October 2016, he entered the *Talent Incubator Programme* at Bright Society. Within this programme, he was involved in projects at Photon Delta, Technobis, Innoluce/Infineon, and Philips. Since December 2018, he works as process development engineer at Philips Innovation Services through Bright Society. His main field of interest is the microfabrication of MEMS.

List of Publications

Journal Publications

- T.-J. Peters, M. Tichem,
On-Chip Positionable Waveguides for Submicrometric Photonic Alignment,
Journal of Microelectromechanical Systems 26 (6), 1259–1271 (2017).

- T.-J. Peters, M. Tichem,
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- K. Wörhoff, A. Prak, F. Postma, A. Leinse, K. Wu, T.-J. Peters, M. Tichem, B. Amaning-Appiah, V. Renukappa, G. Vollrath, J. Balcells-Ventura, P. Uhlig, M. Seyfried, D. Rose, R. Santos, X. J. M. Leijtens, B. Flintham, M. Wale, D. Robbins,
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