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A Nanopower 95.6% Efficiency Voltage Regulator with Adaptive Supply-Switching for Energy Harvesting Applications

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***Abstract*—A nanopower highly efficient low-dropout (LDO) regulator for energy harvesting (EH) applications is presented in this paper. The LDO is fully autonomous with a bandgap reference (BGR) featuring a novel bandgap supply-switching (SS) topology, an over-voltage protection (OVP), a under-voltage lock-out (UVLO) and control block to obtain stable output and robust cold-start. The system provides configurable voltage supply (1.1 $\sim$ 2 V) for potential loads, while consuming as low as 66 nW power. The entire system achieves a peak power efficiency of 95.6% at V_{out} = 2 V and I_{load} = 100 μA.**

I. Introduction

Energy harvesting (EH) systems have drawn significant attention in recent years due to the accelerating development of Internet-of-Things (IoT) applications, where portable and lightweight energy sources are required. The EH interface circuit can extract energy generated by the harvester into an storage device, usually a super-capacitor. However, the output of the EH interface often varies considerably, hence it cannot directly serve as a power supply for following wireless sensor nodes. Thus, there is a demand for a voltage regulator to convert the harvested unstable DC power into a stable DC supply. Since the generated power of an EH system is typically in the order of microwatt [1]- [5], [9], the voltage regulator needs to be designed to consume ultra-low power, enable cold-start ability for the EH system, achieve high power efficiency, small output ripple and large output voltage range for broader applications.

There are mainly two approaches to obtain a stable voltage supply from the EH interfaces, i.e. to use a DC-DC converter [1]- [3] or to use a low-dropout (LDO) regulator [4]. Inductor-based DC-DC converters can achieve relatively high efficiency (80 $\sim$ 90%) over a wide input range when transforming the energy obtained from the energy harvester to a fixed voltage [1], [2], but they require bulky inductors that are impossible to be integrated. In prior work of [1], the inductor is shared between the DC-DC converter and EH interface to reduce the need of an additional inductor. However, since many recent EH systems started employing inductor-less [4] and fully integrated [5] architectures to meet IoT miniaturization requirement, this approach is not applicable. Switched-capacitor (SC) DC-DC converters is possible to be implemented fully on-chip but still occupy large chip area [3]. In comparison, LDO regulator has a much smaller dimension and output ripple. However, its efficiency decreases linearly when the input-to-output dropout voltage becomes higher. To maintain high efficiency with various input condition and output requirement, the output voltage is expected to be configurable. Considering the nominal power generated by a EH system, the power overhead of the voltage regulator should be limited to sub-μW.

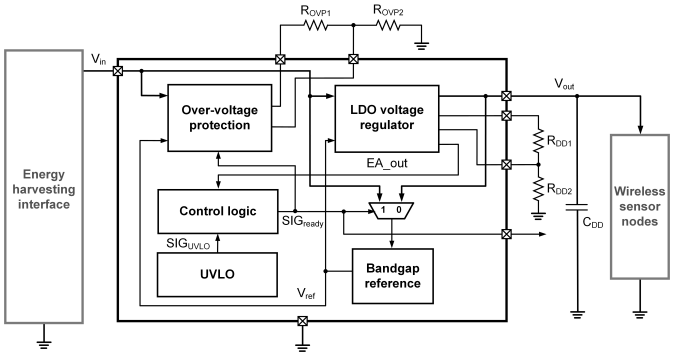

Fig. 1. The block diagram of the proposed voltage regulating system.

In this paper, a nanopower highly efficient voltage regulating system for EH applications is proposed, which achieves a more stable output and dramatically reduced power consumption (by up to 53.5%) by employing a novel supply-switching (SS) topology. To obtain a robust cold-start behavior for energy harvesting applications, an under-voltage lock-out (UVLO) block is designed to generate the SS control signal. The proposed system achieves a configurable V_{out} between 1.1 V and 2 V with power consumption as low as 66 nW. The power efficiency peaks at 95.6% with 2 V output voltage and 100 μA load current.

II. Proposed Architecture

The proposed voltage regulating system architecture is depicted in Fig. 1, which consists of a LDO, a bandgap reference, an over-voltage protection (OVP), an under-voltage lock-out (UVLO) block and a few control blocks. With a input voltage, V_{in}, up to 5 V (configured with OVP via resistors R_{OVP1} and R_{OVP2}), the output voltage V_{out} can be configured from 1.1 V

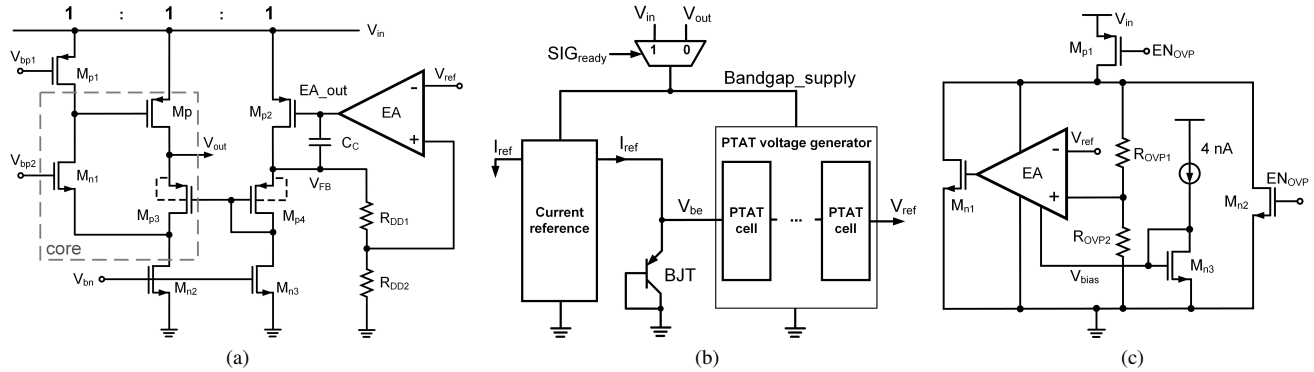

Fig. 2. (a) The schematic of the LDO with off-chip feedback resistors R_{DD1} and R_{DD2}. (b) The block diagram of the bandgap reference with a PTAT voltage generator consisting of 3 PTAT cells in series [7]. (c) The block diagram of the OVP.

to 2 V by altering the ratio of the feedback resistors R_{DD1} and R_{DD2}.

The bandgap adopts a novel SS topology, which dynamically switches the bandgap supply from V_{in} to V_{out} as soon as V_{out} achieves the desired voltage V_{out_set} during the cold-startup period. The switching signal, SIG_{ready}, is generated according to the operating states of the LDO block and UVLO block. Because V_{out} is a regulated voltage and is lower than V_{in}, the bandgap output is more stable while achieving a much lower power consumption. As the bandgap takes up over 1/3 of total quiescent current, the total power consumption could be reduced by up to 30% when V_{in} = 5 V and V_{out} = 1.1 V. The bandgap circuit provides a stable current reference of 4 nA and voltage reference of 1.02 V.

The OVP prevents V_{in} from exceeding the voltage limits that would breaks the devices, which is set to 5 V in this design. The proper operation of OVP is crucial to the systems's cold-startup. Before V_{in} attains 1.1 V, the output from the bandgap, V_{ref}, is lower than the desired value, which is 1.02 V. During this time, in order to let the system be started properly, the OVP should be disabled until the bandgap provides a stable V_{ref}, or the OVP would short V_{in} and ground and prevent the system being starting properly. For a smooth system startup, SIG_{ready} signal is used here again to make sure the OVP is operating correctly during the cold-startup stage. This design is particularly important for energy harvesting application.

III. Circuit Implementation

A. Low-dropout regulator

The schematic of the LDO is shown in Fig. 2a. The LDO structure is based on flip voltage follower [6]. M_p, M_{n1} and M_{p3} form the core of the LDO. The bias currents in M_{n2}, M_{n3} and M_{p1} are set to be 2:1:1 so that the two identical transistors M_{p3} and M_{p4} will have the same V_{gs} and to make $V_{out} = V_{FB} = (1+R_{DD1}/R_{DD2}) \times V_{ref}$. The error amplifier (EA) is implemented with a single stage differential pair to lower the power dissipation.

During cold-startup, the output voltage of the EA (EA_out) rises from 0 to V_{in} – V_{gs} when V_{out} reaches V_{out_set}. Thus

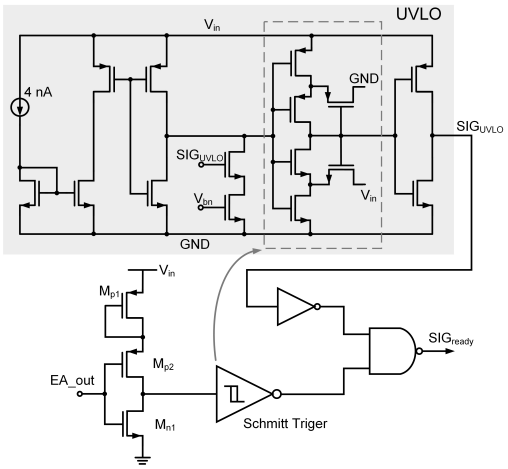

Fig. 3. The schematic of the UVLO circuit and the control logic.

EA_out can be utilized to generate a signal indicating that V_{out} is ready to supply other blocks.

B. Bandgap reference

Fig. 2b illustrates the structure of the low power bandgap based on MOSFET's subthreshold characteristics [7]. It consists of a current reference, a BJT, a multi-stage proportional to absolute temperature (PTAT) voltage generator and a multiplexer. The bandgap reference generates I_{ref} = 4 nA and V_{ref} = 1.02 V. The bandgap begins to work when its supply is above 1.1 V, which sets the minimum allowed value of V_{out_set}. The multiplexer used for SS is implemented with two PMOS-switches and an inverter.

In this design a 3-stage PTAT voltage generator is chosen employed to achieve a good trade-off between power consumption and area, since more PTAT stages result in lower aspect ratio of transistor and higher bias current.

C. Over-voltage protection

Fig. 2c shows the implementation of the OVP circuits. The MOS switch M_{n1} is turned on to short V_{in} and ground when

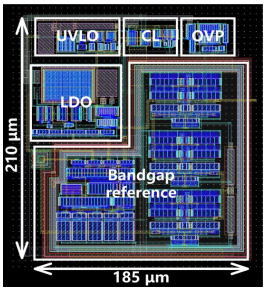

Fig. 4. The layout of the proposed design. CL stands for control logic

TABLE I
POST-LAYOUT SIMULATED CURRENT DISTRIBUTION OF EACH CIRCUIT BLOCK ($V_{out} = 1.1\ V$)

Circuit block	Current (nA)
LDO	18
Bandgap	23
OVP	4
UVLO	14
Control logic	0.04
Total	60

V_{in} exceeds its max allowed value. During off-state, the gat control voltage EN_{OVP} is kept high and the current path fror V_{in} to OVP is blocked by M_{p1}. The NMOS M_{n2} pulls EA's supply to ground so that it draws no current during off-state. When V_{out} is ready, EN_{OVP} goes low and the OVP is then activated.

D. UVLO and control logic

Fig. 3 shows the diagram of the UVLO and control logic, which generate SIG_{ready} to achieve SS by switching bandgap's supply for low-power and stable operations, and activate OVP. When EA_out is high and SIG_{UVLO} is low, the NAND gate outputs an active-low SIG_{ready}. Because EA_out's high voltage level equals to $V_{in} - V_{gs}$, an additional diode-connected M_{p1} is used to prevent leakage current. The UVLO's output SIG_{UVLO} falls from high to low when its power supply V_{in} rises above a threshold V_t, which is set to 1 V. In anotehr word, the UVLO will lock the system in startup phase when the supply voltage V_{in} does not reach the threshold V_t. The UVLO ensures the system can startup with any input ramp-up and with PVT variation when the EA_out signal could become less ideal. Two schmitt triggers are used in UVLO and control logic respectively to avoid ringing during transition.

IV. POST-LAYOUT SIMULATION RESULTS

The proposed voltage regulating system is implemented in 180-nm CMOS BCD process. Fig. 4 shows the layout of the proposed design, occupying an active area of 0.039 mm^2. All the results in the section are based on post-layout simulations.

The voltage regulating system draws a quiescent current of 60 nA when V_{out} = 1.1 V and 72 nA when V_{out} = 2 V. Table I shows the current drawn by each block when V_{out} equals to 1.1 V.

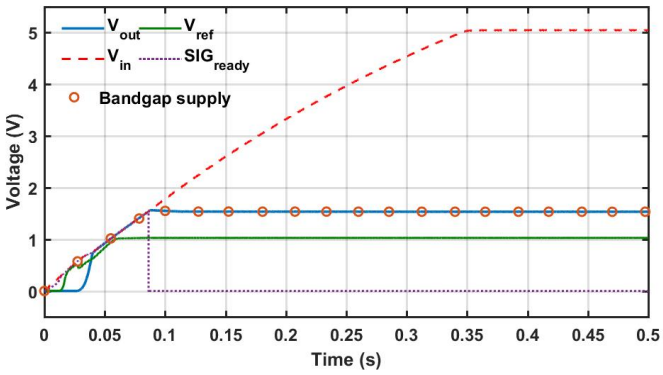

Fig. 5. The cold-start behavior of the proposed voltage regulator.

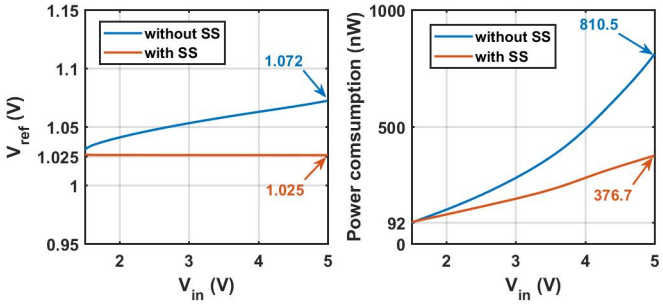

Fig. 6. The comparison of the bandgap output voltage (V_{ref}) (left) and system's power consumption (right) with and without the swithing-supply (SS). (V_{out} = 1.5 V)

The startup behavior of the proposed system, as shown in Fig. 5, has been simulated with a piezoelectric EH interface model originated from [1]. The derised output of the voltage regulating system is set to 1.5 V ($V_{out\_set} = 1.5\ V$). As it can be seen from the waveform, when the input V_{in} ramps up from 0 V at first, the supply voltage of bandgap rises with V_{in} simultaneously. The bandgap is able to generate $V_{ref} = 1.01\ V$ when bandgap supply rises above 1.1 V ($V_{in} = 1.1\ V$). As V_{in} is charged to 1.5 V, V_{out} reaches V_{out_set} and SIG_{ready} falls from high to low, which switches bandgap supply to V_{out}. The switching condition can be adjusted by configuring the V_{out_set} between 1.1 V and 2 V. When V_{in} attains the maximum allowed voltage, the OVP releases the redundant charges to ground, keeping the system safe.

The effectiveness of the bandgap SS topology has been verified by comparing the performance when the system is with and without the SS. As shown in Fig. 6, when adopting the SS, the bandgap output voltage is very stable and the power consumption is significantly reduced by up to 53.5%. Without the SS, the bandgap output voltage shows a drift from 1.030 V to 1.072 V when V_{in} varies from 1.1 V to 5 V while consuming much higher power. The SS topology also enables

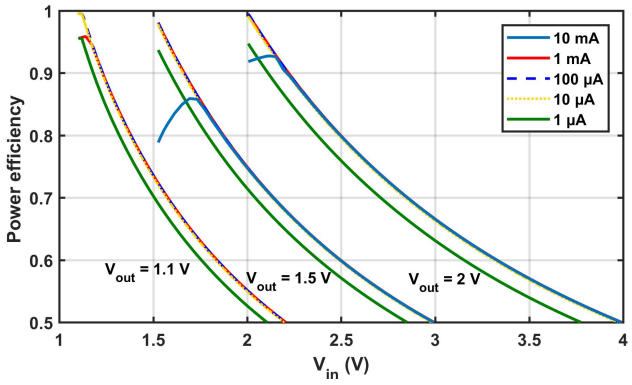

Fig. 7. The power efficiency of the proposed system with various load conditions and V_{out} configurations.

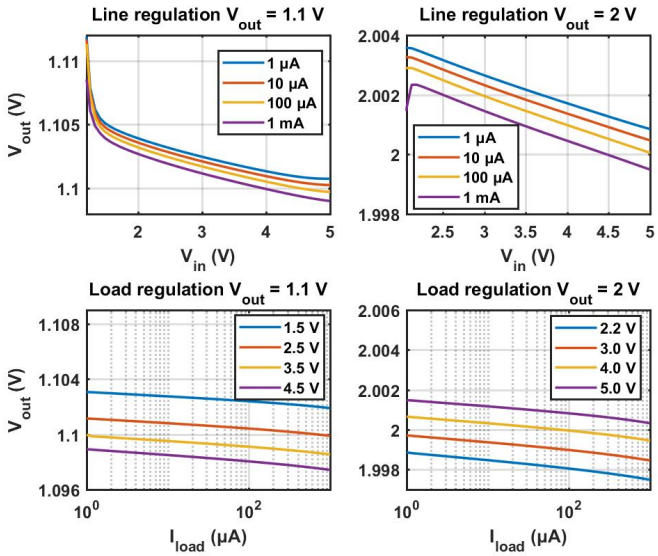

Fig. 8. The simulated line regulation (above) and load regulation (below) of the LDO regulator when V_{out} are set to 1.1 V and 2 V respectively.

the bandgap to be implemented with low threshold MOSFETs, which can further improve the performance by lowering the minimum configurable V_{out_set}.

The system's power efficiencies, which is defined as the output power divided by the total input power, are shown in Fig. 7. The output voltage V_{out} is set to 1.1 V, 1.5 V and 2 V, respectively, and the load varies from 1 μA to 10 mA. For V_{out} = 1.1 V, the maximum load is 3 mA to ensure proper startup. The post-layout simulation results show that the system achieves peak power efficiencies of 92.6%, 94.0% and 95.6% when V_{out} = 1.1 V, 1.5 V and 2 V, respectively. Even with 1 μA load, the efficiencies are still 88.4%, 89.5% and 89.4%, respectively. The power consumption of the system is 66 nW when V_{in} = V_{out} = 1.1 V, and 144 nW when V_{in} = V_{out} = 2 V.

Fig. 8 shows the load regulation and linear regulation performance of the LDO regulator when V_{out_set} equals to 1.1 V and 2 V. The LDO achieves line regulation of 3.36 mV/V (V_{out} = 1.1 V) and 0.93 mV/V (V_{out} = 2 V) and load regulation of 1.49 mV/mA (V_{out} = 1.1 V) and 1.37 mV/mA (V_{out} = 2 V), respectively.

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED SYSTEM WITH EXISTING VOLTAGE REGULATING DESIGNS FOR EH AND IOT APPLICATIONS

Publication	[8]	[9]	[10]	**This work**
Technology	180 nm CMOS	180 nm CMOS	55 nm CMOS	**180 nm CMOS BCD**
Type	LDO	LDO & SC	LDO	**LDO**
Vin (V)	1.35 $\sim$ 1.75	0.7 $\sim$ 2	0.9 $\sim$ 3.6	**1.2 $\sim$ 5**
Vout (V)	1.2	1.2	0.87	**1.1 $\sim$ 2**
I_{load} (mA)	0 $\sim$ 1	0 $\sim$ 0.1	0 $\sim$ 0.1	**0 $\sim$ 10**
I_Q (nA)	15.27×10^3	1300 (SC) 100 (LDO)	64.47	**60**
Output ripple (mV)	1.1	10**	-	**2**
C_L (μF)	0.22	0.8*	20×10^{-6}	**1**
Peak power efficiency	87%*	63% (SC) 88% (LDO)	87.88%	**95.6%**
Line regulation (mV/V)	116.8	32*	2.5*	**3.36**
Load regulation (mV/mA)	6.2	25*	-	**1.49**

*: calculated from corresponding papers.
**: estimated from the measurement results with noise taken into account.

Table II shows the performance comparison to prior voltage regulator designs for EH [8], [9] and IoT [10] applications. Compared with the previous designs, the proposed system achieves a much lower quiescent current and output ripple, as well as better efficiency and voltage regulation.

V. CONCLUSION

An ultralow-power, highly efficient, cold-startup-ready voltage regulating system with a novel bandgap supply-switching (SS) topology is presented for energy harvesting applications. Benefited from the SS, the bandgap generates a stable reference regardless of input voltage, hence a stable output voltage, while achieving lower power consumption. A robust cold-start behavior under PVT variation is guaranteed with the help of the UVLO block. The system operates with a wide input range, and delivers configurable voltage ranges from 1.1 V to 2 V with ultralow quiescent current as low as 60 nA. According to the post-layout simulation results, the system exhibits a peak power efficiency of 95.6% as well as good voltage regulation, showing its great potential for low-power energy harvesting applications.

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