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Molybdenum Oxide in Hole-selective Contacts for Silicon-based Solar Cells

Master Thesis

Molybdenum Oxide in Hole-selective Contacts for Silicon-based Solar Cells

By
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Abstract

Although front and back contact silicon heterojunction solar cells exhibit promising external parameters, they are limited by the front highly absorptive doped layers. Due to their opto-electronic properties, research and development groups have demonstrated that transition metal oxides (TMO) are potential alternatives for doped layers in solar cells. In particular, molybdenum oxide (MoO_x) is a good candidate for the p-contact layers. This thesis presents an investigation of the introduction of MoOx in the front contact of solar cells. To this purpose, the evolution of the passivation is evaluated along the fabrication process together with temperature sensitivity. The application of the layer negatively influences the passivation quality. Moreover, the passivation quality decreases more after annealing and transparent conductive oxide (TCO) deposition. Such issues can be solved thanks to the use of an ultra-tin p-layer before MoOx application, exhibiting implied open-circuit voltage above 715 mV and lifetime 1.57 ms. Finally, the contact stack is optimized by the evaluation of solar cells demonstrators. The best solar cell exhibits a short circuit current density (Jsc) equal to 35.64 mA/cm2, an open-circuit voltage (Voc)¬ of 690 mV, a fill factor (FF) of 77.29% and a total efficiency (η) of 19.01%.

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Nomenclature

Nomenclature	*Meaning*	*Unit*
(i)	Intrinsic	[-]
(n)	Negative	[-]
(p)	Positive	[-]
[-]	Pressure	[mbar]
[-]	Temperature	[°C]
[-]	Energy	[eV]
[-]	Power	[W]
[-]	Power density	[W/cm^2]
[-]	Area	[cm^2]
[-]	Minority carrier density	[cm^{-3}]
[-]	Irradiance	[Watts/m^{2}]
µc-Si	Microcrystalline	[-]
Ag	Silver	[-]
Al_2O_3	Aluminium oxide	[-]
a-Si	Amorphous silicon	[-]
a-Si:H	hydrogen amorphous silicon	[-]
a-SiC:H	Hydrogenated amorphous silicon carbide	[-]
BHF	Buffered hydrofluoric	[-]
CdTe	Cadmium telluride	[-]
CIGS	Copper indium-gallium selenide	[-]
CIS	Copper indium selenide	[-]
c-Si	Crystalline silicon	[-]
EC	Conduction band	[eV]
Ef	Fermi levels	[eV]
Eg	Bandgap	[eV]
EQE	External quantum efficiency	[-]
E_V	Valence band	[eV]
eV_{bi}	Built-in potential barrier	[eV]
E_{VL}	Vacuum level	[eV]
FF	Fill factor	[-]
HF	Hydrofluoric	[-]
HIT	Heterojunction with intrinsic thin layers	[-]
HNO_3	Nitric acid	[-]
IFO:H	Hydrogenated fluorine-doped indium oxide	[-]
IPA	Isopropy alcohol	[-]
ITO	Indium tin oxide	[-]
iV_{oc}	Implied open-circuit voltage	[V]
Jsc	Short circuit current density	[mA/cm^2]
$J_{sc,\ EQE}$	Short circuit current density from EQE	[mA/cm^2]
KOH	Potassium hydroxide solution	[-]

LPCVD	Low-pressure chemical vapour deposition	[-]
mc-Si	Multi-crystalline silicon	[-]
MoO_3	Molybdenum tri-oxide	[-]
MoOx	Molybdenum oxide	[-]
n	Refractive index	[-]
N_2	Nitrogen	[-]
nc-Si:H	Hydrogenated nanocrystalline silicon	[-]
nc-SiO_x:H	Hydrogenated nanocrystalline silicon oxide	[-]
PECVD	Plasma enhanced vapor deposition	[-]
PFF	Pseudo fill factor	[-]
PV	Photovoltaic	[-]
RF	Radio-frequency	[-]
R_s	Series resistance	[Ohm.cm^2]
SCCM	Standard cubic centimeters per minute	[-]
sc-Si	Single-crystalline silicon	[-]
SHJ	Silicon heterojunction	[-]
Si	Silicon	[-]
SiC	Silicon carbide	[-]
SiH_4	Silane	[-]
SiN	Silicon nitride	[-]
SiO_2	Silicon oxide	[-]
STC	Standard test condition	[-]
STC	Standard test condition	[-]
$SunV_{oc}$	Open-circuit voltage from the SunVoc measurement	[V]
TCO	Transparent conductive oxide	[-]
TMAH	Tetramethylammonium hydroxide	[-]
TMO	Transition metal oxide	[-]
V_2O_5	Vanadium pent-oxide	[-]
V_{oc}	Open circuit voltage	[V]
WO_3	Tungsten tri-oxide	[-]
η	Total efficiency	[-]
λ	Wavelength	[nm]
τ_{eff}	Carrier lifetime	[ms]

1. Fundamentals and Motivation

This section will provide the reader some backgrounds about the functioning of a solar cell, especially the physics behind it. It will also give information about the material and the methodology used in this thesis.

1.1. Solar Cell

In order to understand how a solar cell transforms the energy from the sunlight into electrical power, we need to understand the inner physics. Solar cells are based in semiconductor material featuring a positive (p) - negative (n) junction. The p-n junction is built when a negatively charged semiconductor is brought together with a positively charged semiconductor. At the junction, the electrons from the n-region will be attracted by the positive charge from the other side and vice versa. The diffusion of charges will lead to the Fermi levels (E_F) staying constant throughout the p-n junction, bringing the conduction band (E_C) and the valence band (E_V) energies of both p- and n-regions to bend (the slope is related to the presence of the electric field [1]) as shown in *Figure 1*.

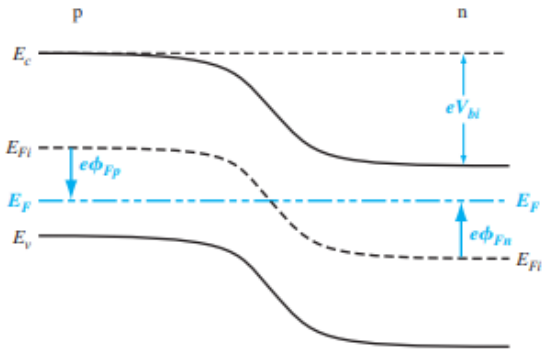


Figure 1: Energy band diagram of a pn junction at thermal equilibrium [2].

The band bending is generating a built-in potential barrier (eV_{bi}) at the junction which separates the photo-generated carriers. Indeed the barrier will block the transfert of the electrons in the conduction band of the n-region to the conduction band of the p-region. The majority carrier will still try to diffuse ; this will lead to a negatively charged region in the p-type and a positively charged region in the n-type. Together they are forming the depletion region (=space charge region) as shown in *Figure 2*.

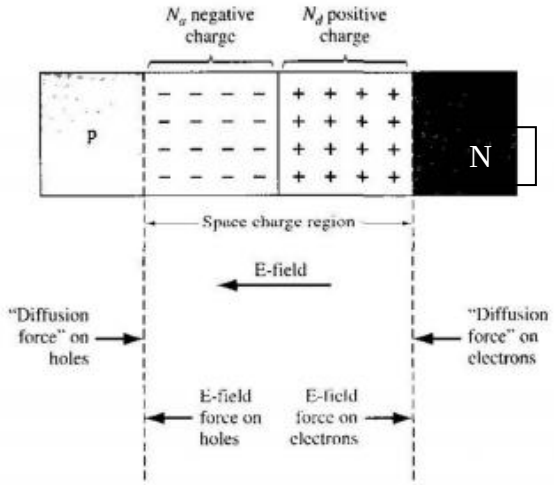


Figure 2: The space charge region, the electric field, and the forces acting on the charged carriers [3].

The presence of the opposite charge in the depletion region produces an internal electric field from the positive charge in the n-region to the negative charge in the p-region. *Figure 1* and *Figure 2* are representing the p-n junction at thermal equilibrium [2].

Solar cells are based on the p-n junction principle. Incident photon illumination creates electron-holes pairs in the space charge region [2]. More precisely, the energy from the photon excites electrons in the valence band able to jump to the conduction band leaving behind a hole [1]. The state of equilibrium is then disturbed by an excess of carrier ; to recover the electron-hole pairs will recombine. While a fraction of the excess electrons will move down the slope of the conduction band (*Figure 1*) successfully to be collected by the contact metal and sent to an external circuit which creates a direct current [1]. A simplified model of the operation of p-n junction solar cells is shown in *Figure 3*.

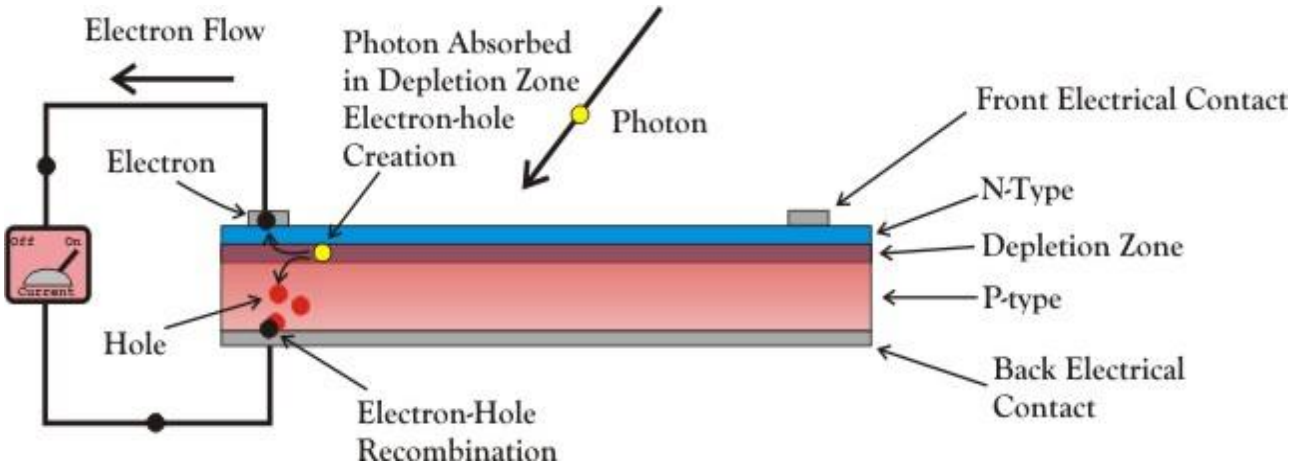


Figure 3: A simplified model of a functioning p-n junction solar cell [4].

1.1.1 The Evolution of Solar Photovoltaic

Over the past decade, the presence of photovoltaic (PV) has been growing sharply as it is targeted that photovoltaics in combination with wind power will supply at least fifty percent of the energy demand by 2050 [5]. In order to achieve this goal, researches have been done to increase their performance; this led to the creation of various designs. The photovoltaic technology can be divided into three distinct categories named "generation" depending on the basic material used and the processing [6].

1. The first generation is including wafers essentially made of crystalline (c-Si), single-crystalline (sc-Si) or multi-crystalline (mc-Si) silicon. This type of PV has already reached a great efficiency, with a current record of 26.6% hold by Kaneka located in Japan [7]. Until now, crystalline silicon represents roughly 80 percent of the market, dominated by single and polycrystalline silicon modules.
2. The second generation is composed of thin-films, their presence increases [8] due to their ability to provide a cheaper solution with low toxicity [9]. The fabrication resides on the juxtaposition of layers on a low-cost basis (glass, polymer or metal). They usually have an efficiency between 12% and 14% [10]. This type of PV can be split into sub-categories.
    a. Amorphous silicon (a-Si) which is considered as a non-crystalline solid and micromorph silicon which consisted of a combination of microcrystalline and amorphous silicon (a-Si/ µc-Si)
    b. Cadmium telluride (CdTe)
    c. Copper indium selenide (CIS) and copper indium-gallium selenide (CIGS)
3. The third generation consists of concentrating PV, organic and perovskite solar cells. They are still under development, only a restricted number of them are being commercialized. This group of solar cells are generally used for locations with really high light intensity or for space application [11].

From all these categories, it can be noticed that silicon plays an important role in the fabrication of semiconductor, indeed it represents more than 90 percent of the total market [12]. For now, it is preferred due to its abundance, high quality and stability. Moreover, it is generally reliable and provides good efficiency.

Strong interest has been shown in silicon heterojunction solar cell because of its ability to provide sufficiently high efficiency at a reduced cost by introducing low-temperature fabrication [13]. The

advantage of decreasing the thermal budget represents a big asset as nowadays PV panels are more expensive than some of the other resources [14].

1.1.2 Silicon Heterojunction Solar Cell (SHJ)

In the past decade, silicon heterojunction has gained a large part of the market thanks to its low cost, low thermal production and good efficiency [13]. *Figure 4* illustrates the composition of the SHJ solar cell. It consists of a texturized n-type crystalline silicon base covered on both surfaces with hydrogen amorphous silicon (a-Si:H) layers; the front surface with a (p)doped layer and the rear side with a (n)doped layer. Optionally intrinsic layers (i) (**Section 1.3**) are added at the interface of the base and the doped layers. The overall is capped with a transparent conductive oxide (TCO) (**Section 2.1.5**) followed by the application of a metal grid (**Section 2.1.6**). [13]

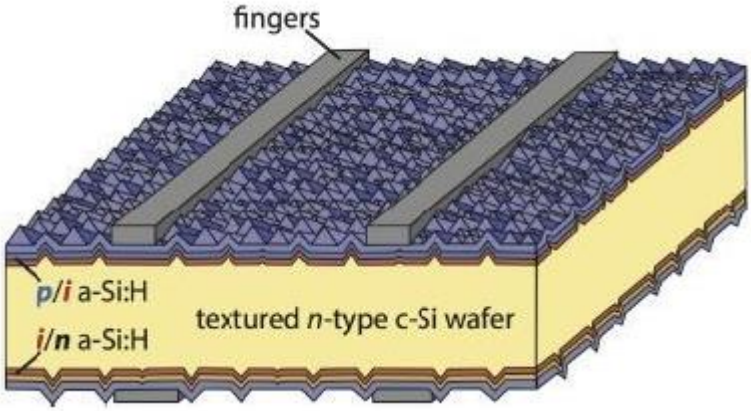


Figure 4: Illustration of a silicon heterojunction solar cell [1].

This kind of solar cell demonstrates a high efficiency; however some improvements are still recommended [13]. Indeed since 2015, a limit in the efficiency equal to 25.1% has been reached [15]. The limitation is partially caused by the application of the dopant layers as they are introducing defects which increase the trap assisted recombination and lead to parasitic losses. Secondly, optical losses occurred in the (p)doped layer as silicon possesses a bandgap in the range of 1.55 to 2.1 eV [16] which causes the absorption of some external energy without the ability to produce any current from it. Additionaly, the transparency of the layer is limited as the (p)doped layer should be thick enough to permit the transfer of holes.
The parasitic losses could be attenuated by replacing the doped layer with alternative materials able to act as carrier selective contacts ; these include transition metal oxides (TMO), organic materials or alkali/alkaline earth metals and/or salt [17].
A high interest has been shown on TMO due to their low price [18], their abundance and the fact that they are not requiring toxic gases or explosive / flammable elements during the fabrication [19].
By replacing the p-doped layer with a TMO having a high work function, the material will operate as hole-selective contact without the disadvantage of introducing defects. Moreover, the dopant free material possesses a wider bandgap than Si which will reduce the optical losses generated on the front surface.

1.2. Transition Metal Oxides (TMO)

Transition metal oxides are a special category of material that can act as insulators due to their strong Coulombic interaction or acquire the metallic properties with high conductivity [20].
The important characteristic of this type of material for this thesis is their possibility to replace the doped layers in silicon heterojunction solar cells. Indeed it is possible to reproduce the action of the (p)doped layer in case of high work function or the (n)doped layer if the material possesses a low work function. This report will only focus on the replacement of the (p)doped layer which is more critical due to its large amount of absorption losses [21].

1.2.1. TMO Hole-Selective Contacts

The main materials of this category are molybdenum tri-oxide (MoO_3), vanadium pent-oxide (V_2O_5) and tungsten tri-oxide (WO_3). They are characterised by their low optical capacity of absorption in the visible spectrum, electronic properties and compatibility with technology as they provide low contact resistivity. The use of these oxides improves the external quantum efficiency (EQE) compared to a-Si:H as it responds to a larger range of wavelengths, from 280 to 1200 nm [19].
They are classified as n-type elements since their Fermi level is closer to the conduction band than the valence band as shown in *Figure 5*.

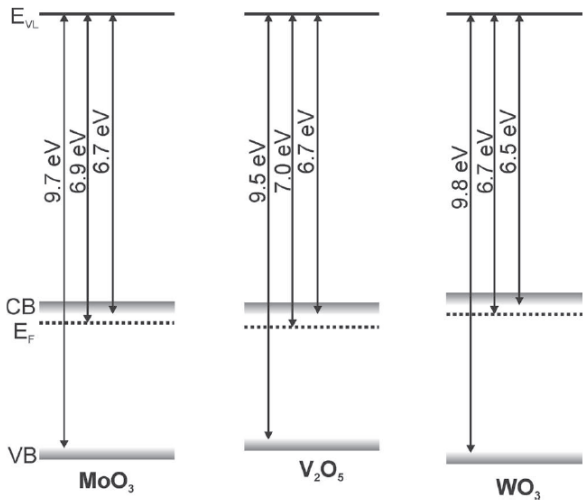


Figure 5: Molybdenum trioxide (MoO_3), vanadium pent-oxide (V_2O_5) and tungsten trioxide (WO_3) with respect to the vacuum level (E_{VL}) [22].

From *Figure 5*, it can be observed that WO_3 shows the highest work function closely followed by MoO_3. The latter has the advantage to be easy to evaporate due to its low-temperature melting point which will help in keeping the cell production to low-temperatures. This attractiveness and its great transparency (the most transparent of the three materials [19]), make it the most appropriate for solar cell production [22]. Anyway this might change, for example, *Gerling et al.* [19] and *Wu et al.* [23] have concluded that the best efficiency should be reached with V_2O_x. While *Khilla et al.* [24] believe in the evolution of WO_x as it possesses the largest bandgap in comparison to the two other materials which should reduce the optical losses even further. However, this kind of verdict can only be reached in the future after a deep investigation of each material.
Figure 6 shows a schematic representation of the E_f alignment when bringing the TMO with (n)c-Si, the first stage consists of electrons leaving the valence band of (n)c-Si and fills the oxygen defect states present in the TMO bandgap. Indeed, the oxygen defects are positive ions which are attracting the excess of electrons present in the (n)c-Si. Through this attraction, the valence band of the (n)c-Si approaches the Fermi level of TMO, producing a high density of defect which results in the increase of carriers recombination close to the interface forming an intrinsic layer (SiO_x). The Fermi level achieved the equilibrium where a positively charged region is generated. TMO is then acting like a hole-selective contact.

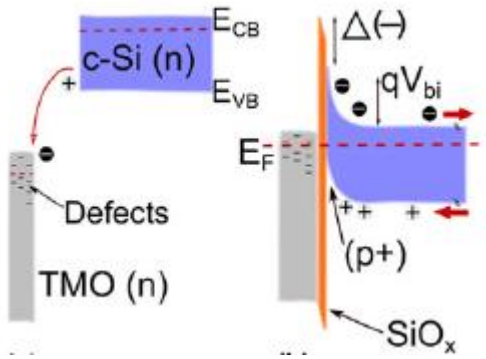


Figure 6: Diagrams of the energy band of TMO in combination with c-Si interface [25].

As a result of band bending, the recombination speed, especially for the trap assisted and the contact resistivity at the interface, is reduced [23].
However, the result of the naturally formed passivation layer is not completely satisfactory according to *Gerling* [25], *Khan* [26] and *Tong* [27], the deposition of a compact passivation layer is preferred. The property can be improved by inserting an intrinsic layer in between the TMO and the doped base which should provide superior efficiency.
The main drawback for the majority of the TMOs is their sensitivity to the atmospheric condition which completely modifies their electronic structure. Indeed, the atmospheric condition reduces the work function of the material due to the apparition of defects.

1.2.2. Molybdenum Trioxide (MoO_3)

The material is a semiconductor with a large bandgap (3 eV [22]). Yet, this one could increase and further reduces the optical losses [28], but then the material will start to act as a semimetal [29].

MoO_x is characterized by its high work function which can reach a value from 5.3 eV to a maximum of 6.9 eV for ultra-clean atmosphere. Unfortunately, this one will decrease as soon as it is exposed to air due to its sensitivity to water vapour. The specific MoO_3 is generally defined with a work function in between 6.8 and 6.9 eV, a bandgap of approximately 3 eV which leads to an ionisation energy of roughly 9.7 eV. The parameters are dependent on the chemical composition which relies on the sample stoichiometric, the density of defects and the condition of the deposition applied [29] [27]. Its electronic structure is also determined by the surface roughness, the crystal structure of the exposed area, the absorption characteristics of the related face and the radiation of the light [30]. However, there is a possibility to roughly control most of these factors.
In the course of aligning the Fermi level of the crystalline silicon with TMO, a Schottky barrier on the front side appears due to the difference in the work function as previously shown in *Figure 6.* The high work function of MoO_x is blocking the holes, acting as a hole selective contact.
In order to see how this concept works, it is easier to illustrate it with a simplified band diagram. *Figure 7* represents the contribution of each layer, the band bending is similar to a standard p-n junction SHJ with a passivation layer. By combining (n)c-Si/(i)a-Si:H and MoO_x, a potential barrier is appearing due to the difference in work function. Thus the carriers are blocked and have to follow a certain path which should provide field-effect passivation with a correct quality accompanied with holes selective contact.

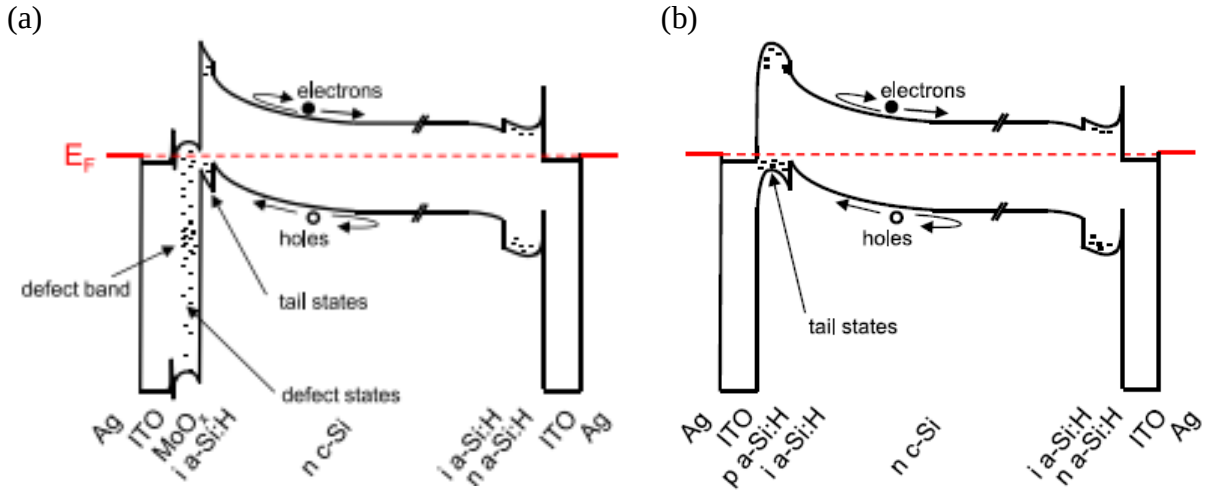


Figure 7: Band diagrams for (a) hybrid Silicon/MoO_x heterojunction solar cell and (b) doped SHJ solar cell [31].

Additionally, due to the fact that MoO_3 possesses a higher bandgap (≈ 3 eV [22]) than p-type a-Si:H (≈1.7 eV [32]), it is possible to reduce the parasitic absorption for a certain range of wavelengths (λ), especially for the blue and visible part of the solar spectrum [33]. Indeed, the energy band gap is related to the wavelength as shown in *equation 1*.

$$E = \frac{hc}{\lambda} \qquad 1$$

E is the minimum energy of the photon required in order for the electron to travel from the valence band to the conduction band. While h corresponds to the Planck's constant and c is the speed of light.
MoO_x is characterized by great transparency, it will reduce the absorption coefficient and increase the short circuit current density (J_{sc}). *Figure 8* compares the absorption coefficient between p-type a-Si:H and MoO_x which shows a much better result. But it must be taken into consideration that the transparency of MoO_x decreases with the thickness.

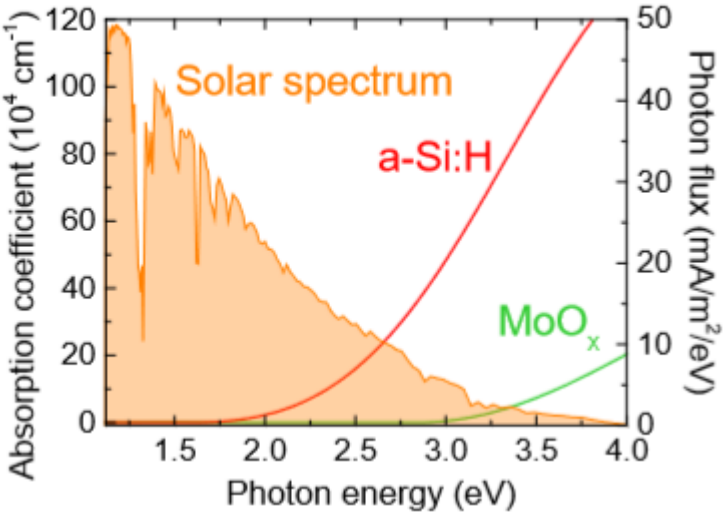


Figure 8: Absorption coefficient of a-Si:H layer and MoOx for the AM1.5g spectrum shown as the red shadow [34].

Nevertheless, the Molybdenum trioxide might not be the material of the future as this one could have some effects on the enzyme required by the fauna and flora if excessively used [35].

a. *Impact of Oxygen Vacancy*

The material brings some challenges as it is characterized by the presence of oxygen vacancies that are mainly dependent on the temperature, exposed atmosphere, the thickness of the layer and the redox condition of the material [36] [37]. The traps (positive ions) are able to capture electrons and act as donors which decrease the energy of the bandgap [37]. Yet the oxygen vacancies can be used advantageously as assisted holes transport but will decrease the Schottky barrier which might reduce the performance [38]. In an ambient environment, the material is in contact with hydrogen which will intercalate into MoO_3 and slowly form water that will accumulate at the surface [37]. This will have an impact on the optical and electronic properties of the material. The chemical reaction is shown in *equation 2*.

$$MoO_3 + H_2 \leftrightarrow MoO_2 + H_2O \qquad 2$$

Due to this property, MoO_x is often amorphous with a sub-stoichiometric structure that possesses an "x" equivalent to approximately 2.73 as the oxygen content decreases [39].
The stoichiometry is dependent on various parameters like the air and oxygen exposure, the temperature and the process used for the deposition.

b. *Storage*

The environment in which the wafer is placed after the deposition is crucial because the material is sensitive to air and oxygen exposure. *Irfan et al.* showed in [36] that this will have an impact on the work function which will decrease gradually as presented in *Figure 9* until reaching saturation at a work function of 5.3 eV. Moreover, *Tong et al.* [40] measured that the minority carrier lifetime degrades when in contact with air as shown in *Figure 10*.

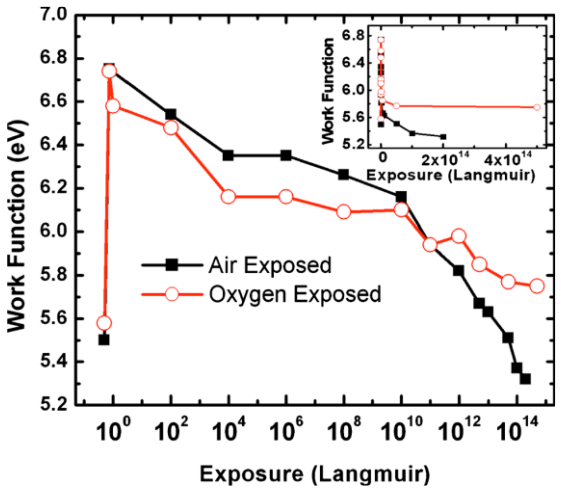


Figure 9: Work function of Molybdenum Trioxide exposed to air and oxygen [36].

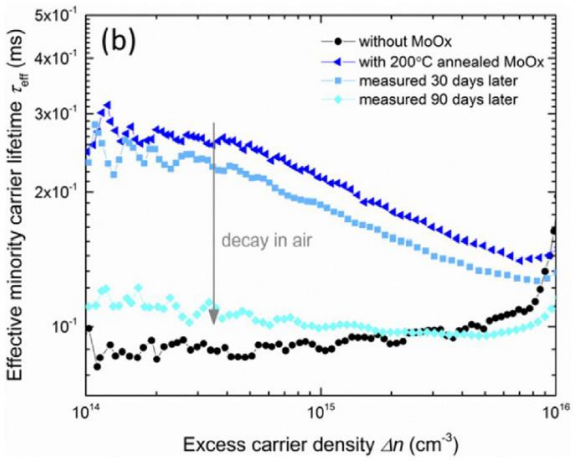


Figure 10: Effective minority carrier lifetime dependent on the excess carrier density and time exposure at ambient air [40] .

To minimize the obstruction, the wafers were stored in a Nitrogen (N_2) box in between the depositions.

1.3. *Surface Passivation for Silicon Heterojunction Solar Cells*

By studying the physics behind a solar cell, it was discovered that the application of carrier-selective passivation layer will reduce the surface recombination as a result of its low defect density. The passivation layer has been proved to carry a crucial role in the manufacturing of the solar cell. Indeed, when the bulk is abruptly stopped, this one will have some dangling bonds at the surface and during the illumination of the c-bulk, the unsaturated bonds (defects) present at the surface will be responsible for recombinations

which limit the V_{oc} and so the efficiency. In order to minimize these losses, it was found that the deposition of an intrinsic thin layer could help by forming Si-Si bonds. This increases the built-in voltage which results in a boost of the V_{oc}, in addition, it acts as a barrier for the electrons at the MoO_x/ (i) a-Si:H interface.
Moreover, it must be noted that by using a texturized wafer, the number of dangling bonds at the surface increases which has the advantage of making the connection between the two layers stronger. As soon the intrinsic layer is deposited, it provides a chemical passivation layer and decouples the electron-hole pair in the contact layer and the metal. Three materials can be used as a passivation layer in combination with (n)c-Si wafer: first, the hydrogenated amorphous silicon (a-Si:H), an ultra-thin silicon oxide (SiO_2) or eventually aluminium oxide (Al_2O_3). Each of them have their own drawbacks [7].
For this project, MoO_x is used and it has already been shown that a-Si:H provides an excellent passivation layer in combination with this metal [19] as it gives a strong hole blocking layer due to its wide bandgap. Moreover, *Zhang et al.* have shown in [41] that the deposition of a-Si:H helps to upgrade the thermal stability of MoO_x. One of the drawbacks of using a passivation layer is the formation of an epitaxial layer due to the presence of H_2 gases and / or the utilization of high temperature (≥140°C) during deposition. Indeed, the formation of a thin layer of SiH_2 in addition with defects could appear at the interface of c-Si and a-Si:H(i) or even a thin (2 nm) amorphous SiO_x could be induced between a-Si:H and MoO_x [42]. The growth of these layers will degrade the cell performance; in any case, a passivation layer is required due to the production of high defect density when putting directly the two materials together [7].

a. Carrier Mechanism

For this thesis, the lifetime of the minority carrier has been deeply investigated as it provides a good approximation of the quality in passivation. As we were unfamiliar with the material; it was important to have an overview of the discovering that has already been done.
Vijayan et al. showed in [43] the type of recombination that happens at the interface of each layer on the front side (cf. *Figure 7*). Inside the c-Si bulk, a float-zone wafer is used and this one has been certified to be defect-free by the manufacturer so no recombination happens inside. There is still the surface of the bulk which is mainly characterized by dangling bond but should be minimized by the introduction of the passivation layer. At the interface of (i)a-Si:H and (n)c-Si, it is assumed that the transport of the carriers occurs only thanks to thermionic emission.
While at the interface of MoO_x and (i)a-Si:H, the mechanism is dependent on the electron affinity of MoO_x which represents the energy from a displacement of an outside electron (vacuum level) to arrive at the conduction band. For a value higher than 5.7eV the transport is dominated by direct band-to-band tunnelling. Indeed, the MoO_x conduction band overlap the valence band of the (i)a-Si:H which creates a surface inversion. It means that an electron from the (i)a-Si:H valence band is then able to tunnel directly to the conduction band without the requirement of traps or the absorption/emission of a photon. While for lower electron affinity (< 5.7eV), the transport mechanism is dominated by trap-assisted tunnelling as the bands are not overlapping anymore. The mechanism depends then on the trap density present close to the conduction band in the MoO_x bulk.

1.4. Thesis Outline

This report will focus on the replacement of the (p)doped layer ((p)a-Si:H) with MoO_x in the faith of reducing the parasitic and optical losses generated on the front surface of silicon heterojunction solar cell. Molybdenum oxide was selected as it already demonstrated great results with a conversion efficiency of 22.5% [21]. In order to accomplish this challenge we started by getting familiar with the subject by doing a literature review about the basic principles, materials (**Chapter 1**) and the various types of equipment used for fabrication and measurements (**Chapter 2**) of the prospective solar cells.
To be time efficient, it was decided in **Chapter 3** to first deposit a stack of layers on a textured wafer to see how the materials would interact and select a range of thicknesses for layers required for the fabrication of solar cells. The choice of this parameter was easily done, however, during the experiments it was discovered that the material was sensitive to annealing and that the application of ITO which is indispensable for the solar cell production had some detrimental impacts on the underneath layers. **Chapter 4** consists of finding a way to attenuate the problem; once this was done, the first solar cells were produced according to the findings made in the previous section. **Chapter 5** starts with the combination of steps required for the rear and the front surface providing two flowcharts. They were then tested and as

soon as satisfactory minority carrier lifetime was obtained, the investigation of the thicknesses and materials was initiated. **Section 5.2** considers various materials for the (p)doped buffer layer. While **Sections 5.3** and **5.4** are demonstrating the importance of selecting the appropriate thickness for the (p)doped buffer layer and MoO_x.
The final chapter (**Chapter 6**) consists of a conclusion and a short statement combining ideas for the future if the project is carried on.

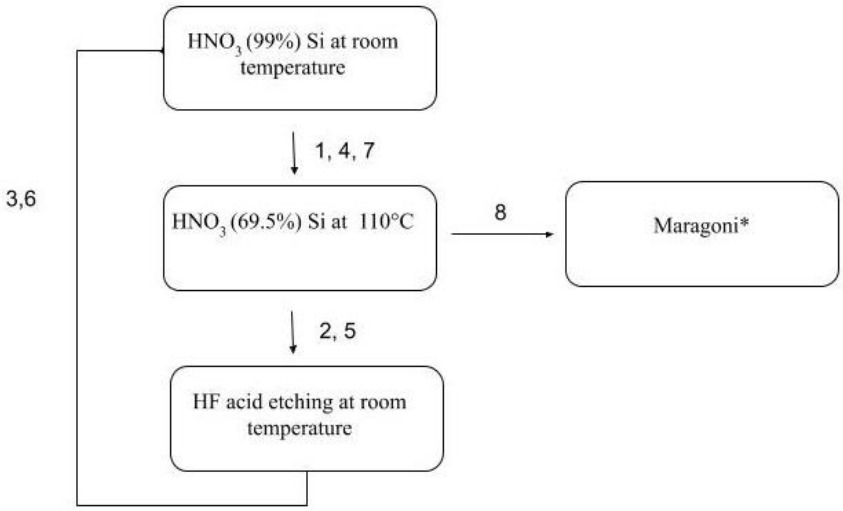
2. Experimental Methods

As we were not familiar with the essential material of this thesis, it was important to start afresh with simple deductions to facilitate the commencement. It was then decided to begin the analysis with the depositions of a stack of layers on top of each other (**Chapter 3** and **4**) and measure how well they will respond to the conjunction. Subsequently, solar cells were produced (**Chapter 5**) according to the outcome of the previous experiments done on wafers.
Section 2.1 provides information about the material and equipment of each deposition of layers used for this thesis. While **Section 2.2** gives instructions about the equipment employed to measure the characteristics of the wafers/ solar cells.

2.1. Samples and Solar Cells Preparation

2.1.1. Wafer Cleaning and Texturing

The choice for the base of the solar cell is really important as it has an impact on its effectiveness. A crystalline silicon substrate was selected as this one provides low impurity and has already proved good capabilities by generating high efficient solar cells. However, the main decision was to go with n-type wafer instead of p-type as this one is less sensitive to degradation caused by light thanks to the absence of boron-oxygen related and metal impurities [44]. The wafers were provided by TU Delft; it consisted of n-type Topsil double-sided polished FZ c-Si wafer. Originally, they had an orientation of <100> ±1° with a thickness of 255-305µm, a diameter of 99.7-100.3mm and a resistivity of 1-5 Ω.cm.
To improve the outcome, some wafers were texturized as it permits to optimize the reflection losses and the improvement of light trapping which will increase the short circuit current density and have a positive impact on the efficiency [45].
To provide randomly distributed pyramidal structures, the (n)c-Si wafer needed to be etched through a mixture of potassium hydroxide solution (KOH) and isopropy alcohol (IPA) called a tetramethylammonium hydroxide (TMAH) solution. IPA is used in order to remove the hydrogen attached to the silicon surface and generate smoothness large size pyramids which improve the impact of reflectivity [46]. The solution is usually set at a temperature of 80°C with a magnetic stir rotating at 100 revolutions per minute; the wafer is dipped in it for 10 to 40 min (until the surface becomes rough). The wafer is then formed with several pyramids composed of a square base with an <111> orientation and four triangular faces with an <100> orientation [47]. The wafer is then cleaned with DI water for 4 minutes to finally be dried.
For this thesis, during the fabrication of solar cells, a flat rear surface was recommended by [48] when SiO_2 /poly-Si was going to be subsequently applied while the front surface required to be texturized. The rear side was then protected with a Silicon Dioxide (SiO_2) or silicon nitride (SiN) thick layer. The layer was deposit through plasma enhanced vapor deposition (PECVD) (**Section 2.1.3**). Once the protecting layer is not required anymore, it is easily removable by dipping the wafer (≈2min) in a buffered hydrofluoric (BHF) acid solution which consists on a mixture of 7 volumes of ammonium fluoride with 1 volume of hydrofluoric (HF), the layer is then completely etched and the surface becomes hydrophobic.
By using a textured wafer, the deposition of the passivation layer is more complicated due to surface recombination at the pyramid valleys and the induced defects [49]. To simplify the deposition and to diminish any defect, contamination or surface roughness present at the surface of the wafer which could lead to a larger recombination density, lower minority carrier lifetime and so limit the open-circuit voltage, this one is required to follow a pre-deposition treatment. In addition, the procedure helps to smooth the shape of the pyramids. The cleaning process has been optimized by a prior student [50]. The method can be found in [50] and is summarized in *Figure 11*.



* 4 min of HF solution, 4 min of DI water + Isopropyl Alcohol gas.

Figure 11: Schematic representation of the cleaning cycle from [50] in order to remove any contamination.

Moreover, to have a more or less uniform deposition, all the future deposition thicknesses were multiplied by a factor of 1.73.

2.1.2. SiO_2 and (n)Poly-Si Deposition

The process provides the (n)doped stack of layers for the rear side by joining SiO_2 with poly-Si materials. The combination of the two materials has the advantage to provide both field-effect and chemical passivation for the c-Si substrate [51]. The validation of the surface passivation was tested through the fabrication of a symmetrical wafer. Due to the satisfying outcome with a minority carrier lifetime of 8.75 ms and an iV_{oc} of 723 mV, this stack of layers was applied for most of the experiment as the (n)doped stack of layers for the rear surface.

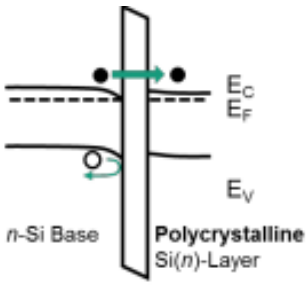


Figure 12: Band diagram using poly-Si with a tunnel oxide on an n-Si base [52].

a. Tunnelling Oxide Formation - Nitride Acid Oxidation of Silicon (NAOS)

With this process, the chemical passivation is done through a thin oxide layer which is grown on top of the wafer to reduce recombination. The layer provides good lattice match with the doped crystalline silicon substrate [51] moreover their differences in the valence band energy level are generating a barrier for the holes while the accumulation of the electrons from the doped substrate is provoking band bending [53] as shown in *Figure 12*. It was decided to use SiO_2 instead of Si_3N_4 or silicon carbide (SiC) as it provides the highest barrier which increases the V_{oc} [53].
To produce this layer, the wafer was dipped in a 69.5% nitric acid (HNO_3) solution for 60 minutes at room temperature in order to grow 1.5 nm of Silicon dioxide (SiO_2) on the surface.

b. Poly-silicon deposition

The layer provides the field-effect passivation thanks to the band-bending generated by the introduction of dopant, the minority carrier is then cut short from diffusing at the interface. The deposition is done by thermal decomposition of silane (SiH_4) at temperatures between 580°C and 650°C and low-pressure [54]. This process is defined as a low-pressure chemical vapour deposition (LPCVD). The quality of passivation for the rear side is dependent on this deposition, it is why the recipe was optimized by TU Delft staff [55] in order to use the right thickness, power, temperature and timing. Indeed, the development of this deposition needs to be taken seriously since for a too thin layer, the dopant will diffuse too much inside the substrate which will reduce the band bending [51]. The ions were implemented through a piece of equipment named "Varian Implanter E500HP". In order to produce a (n)doped layer, phosphorous ions are bombarded with an energy of 20 KeV and at a concentration of $6x10^{15}/cm^3$. To recover from this rough process, the wafer is then annealed at a temperature of 950°C for 3 minutes [56]. Followed by hydrogenation, the hydrogen particles are introduced through the Silicon Nitride (SiN) layer by using PECVD (**Section 2.1.3**). Moreover, SiN provides a small protection as the hydrogenation might damage the poly-Si layer [57]. As soon as the layer is not necessary anymore, it is removed through a BHF solution. As stated before, to improve the passivation quality, hydrogenation is required. This is done by applying a succession of negative high-voltage pulses in a furnace full of hydrogen plasma at a high temperature which accelerates the hydrogen ions and implants them directly into the poly-Si layer. The hydrogen impurities are combining with the Si dangling bond which is modifying the electrical properties of the poly-Si film [58].

2.1.3. Plasma-Enhanced Chemical Vapor Deposition

The deposition of the buffers layer including the surface passivation is typically done by using radio-frequency (RF) PECVD on a contamination-free and clean substrate. Thin layers of various material can be deposited thanks to the generation of a plasma. Gases are introduced in a chamber and as soon as the gas mixture is stabilized; an RF electric field get the material excited through thermal energy and forms a plasma which will accumulate on the substrate surface until becoming solid. This type of deposition has the advantage of not warming up the wafer. A diagram representing the concept is shown in *Figure 13*.

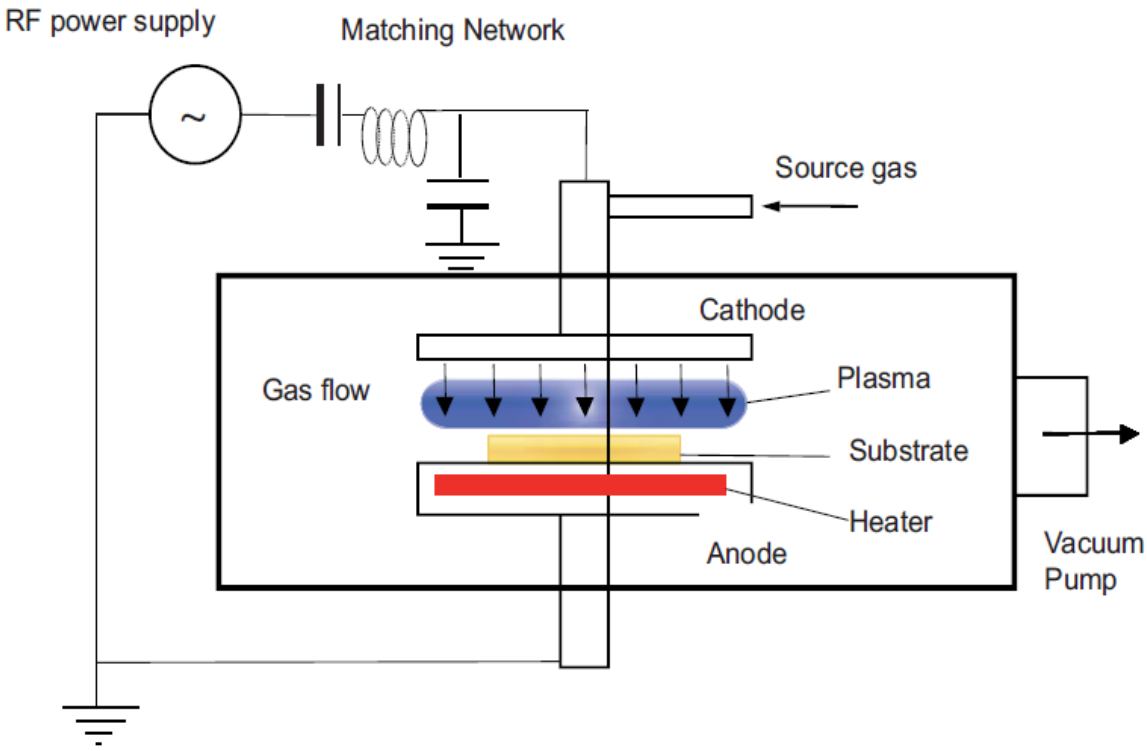


Figure 13: Diagram of RF plasma-enhanced chemical vapor deposition [59].

For this project, the settings used was in accordance with optimized recipes conceived by the students/ PhD from the PVMD group [60] [61]. The laboratory that was used for this thesis possesses three different equipments. To make things easier, the PVMD group gave them names:

- "Novellus Concept 1". The equipment provides multi sequential depositions through 7 chambers. It generates high-quality layer at a temperature of 400°C with a pressure of 2.25 Torr and a power of 1000 W [62]. PECVD of SiO_2 and SiN were applied through this machine. The process follows a precise cycle depending on the selected recipe. This one is downloaded through a computer which controls the equipment.
- "Amor" which is a basic PECVD equipment that needs to be controlled manually. The equipment comprises 4 chambers for different depositions in addition to an enclosure where the wafer can be flipped and a load-lock. Different recipes were applied, *Table 1* is giving an overview of the parameters/materials used for each deposition.

Table 1: Parameters required for the deposition of (i)a-Si:H, (p)nc-Si:H, (p)nc-SiO_x:H, (p)a-Si:H and (p)a-SiC:H through "Amor" PECVD.

Material	(i)a-Si:H	(p)nc-Si:H	(p)nc-SiO_x:H	(p)a-Si	(p)a-SiC
SiH_4 [sccm]	16	1.50	3.8	20	20
CH_4 [sccm]					45
CO_2 [sccm]			1.40		
B_2H_6 (2% in H_2) [sccm]		0.80	0.80	3	3
H_2 [sccm]	48	500	800		
Φtotal	64 sccm	502.3 sccm	806 sccm	23	68
P_{depo}	1.4 mbar	2.2 mbar	2.2 mbar	0.7 mbar	0.7 mbar
$T_{substrate}$	180 °C	180 °C	180 °C	180 °C	180 °C
$P_{RF, meas/set}$	3.2	14.2	11	3	3
Deposition rate	10.175nm/min	1.92 nm/min	1.5168 nm/min	11.94 nm/min	10.776 nm/min

- "Amigo" which consisted of a more sophisticated equipment with 6 chambers and a load-lock. It can administer high power treatment in order to provide better quality for crystallinity. For this process, the wafers and a recipe for each of them just have to be loaded at the beginning and then everything is automatic. The recipes for each layer deposition are shown in *Table 2*. After the intrinsic layer deposition, a hydrogen treatment is applied which will etch approximately 3 nm of the (i)layer followed by a high-frequency treatment. More information about the applied treatments can be found in [63].

Table 2: Parameters required for the deposition of, (p)nc-SiO_x:H and (i)a-Si:H through "Amigo" PECVD.

Material	(i)a-Si:H	(p)nc-SiO_x:H
SiH_4 [sccm]	10	0.8
CO_2 [sccm]		1.40
B_2H_6 (2% in H_2) [sccm]		10
H_2 [sccm]	30	170
Φtotal	40 sccm	182 sccm
P_{depo}	1.4 mbar	2.2 mbar
$T_{substrate}$	180 °C	180 °C
$P_{RF, meas/set}$	3	11
Deposition rate	4.82 nm/min	0.833 nm/min

These equipments have the advantage that as soon as the vacuum condition has been reached, there is no need to break it if various layers need to be deposited. To avoid any contamination, each chamber is

allocated to a type of material ((p), (n) and (i)). Each chamber is equipped with a platen in where the wafer can be placed on. As soon as the right vacuum level has been reached in the chamber, a gas is introduced through a tube; a high voltage RF is then applied and together with the gas they produce a plasma state inside the room. This implies that gas is formed and will deposit as a solid thin film on the wafer. It has the main advantage that it does not require high temperature but a plasma as a source of activation.
Before any process, the carriers and the chamber are seasoned in order to reduce any contamination from the previous deposition. Then the wafers are loaded and are left in the chamber for 30-45 min before any deposition, to be sure that the substrate reaches a temperature of 180°C.
To determine the deposition time, a "test wafer" was measured at different periods of time during the thesis and the thickness was measured in order to determine the deposition rate.
As soon as the deposition is over, the wafer is brought to a distinct location where it is flipped in order to coat the other side if required. If it is not necessary, the wafer is left or in the load lock, in chamber 5 (flipping room) or on the robot arm as these areas are not heated up. The wafer is left there for at least 30 minutes in order to cool down.

2.1.4. MoO_3 Deposition - Thermal Evaporation

Among different methods to deposit MoO_3, this thesis aims at investigating the thermal evaporation approach. The process applied for the deposition can be found in *Figure 14*.

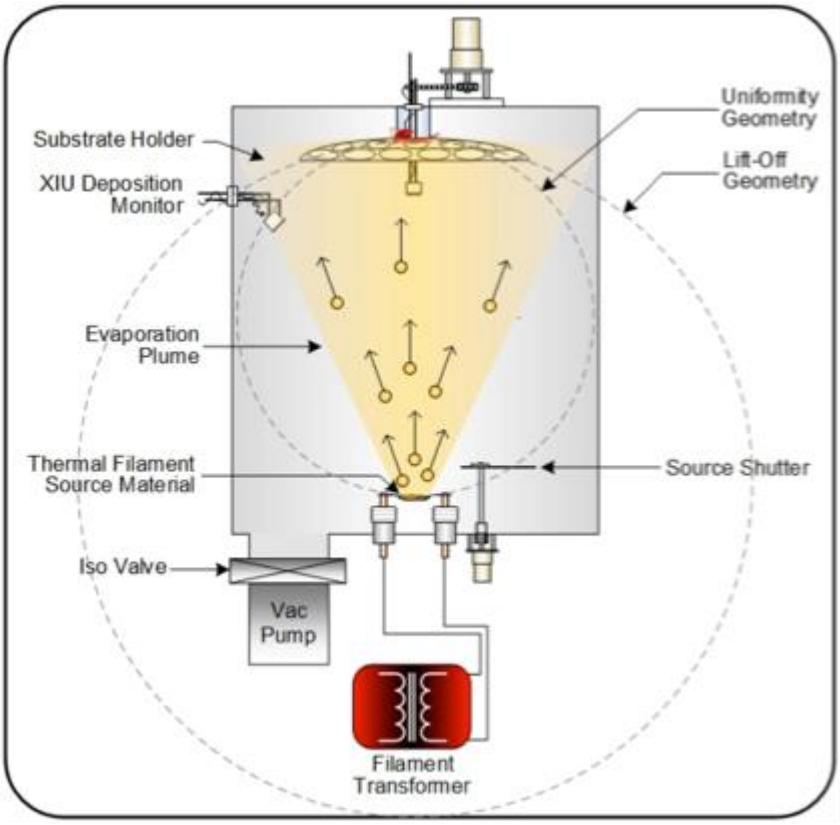


Figure 14: Diagram of Thermal Evaporation Process [64].

Some grey/white MoO_3 powder was placed in a crucible while the wafer was fixed to the ceiling of the equipment with the "to be deposited" surface facing the target material. The set-up finalized, the door is locked up and the machinery can get started. The first step consisted on reaching a high vacuum level, then the powder is heated up by applying a high current until the metal is starting to evaporate, this process only starts at a vapour pressure of $5x10^{-6}$ mbar. Once the melting point of the metal has been reached (795°C [65]), it will start to evaporate and coat the surface.
As molybdenum oxide is getting agitated, it loses some O_2, introducing some oxygen vacancies, which modify the stoichiometry from MoO_3 to MoO_x.
A deposition rate was initially automated by the process engineer in the recipe, this one was not modified through the period of this thesis however its validity was verified and is reported in *Table 3*.

Table 3: Measurement is taken to verify the validity of the deposition rate used during the thermal evaporation.

Thickness targeted (nm)	Spectroscopic ellipsometry thickness (nm)
8.5	9.19±0.010
17	16.33±0.028
25.5	24.06±0.047

2.1.5. Transparent Conductive Oxide - Radio-Frequency Magnetron Sputtering

The main role of a transparent conductive oxide (TCO) is to provide an anti-reflection coating and to transport the charge carriers toward the appropriate electrode terminal [66].
In order to deposit TCO, argon gas is inserted in the chamber and is getting highly energetic, forming ions thanks to radio-frequency from a generator connected to the cathode as seen in *Figure 15*. These ions are then bombarding the target which will release particles that will diffuse on the surface of the wafer [61]. Usually, the deposition is followed by annealing.

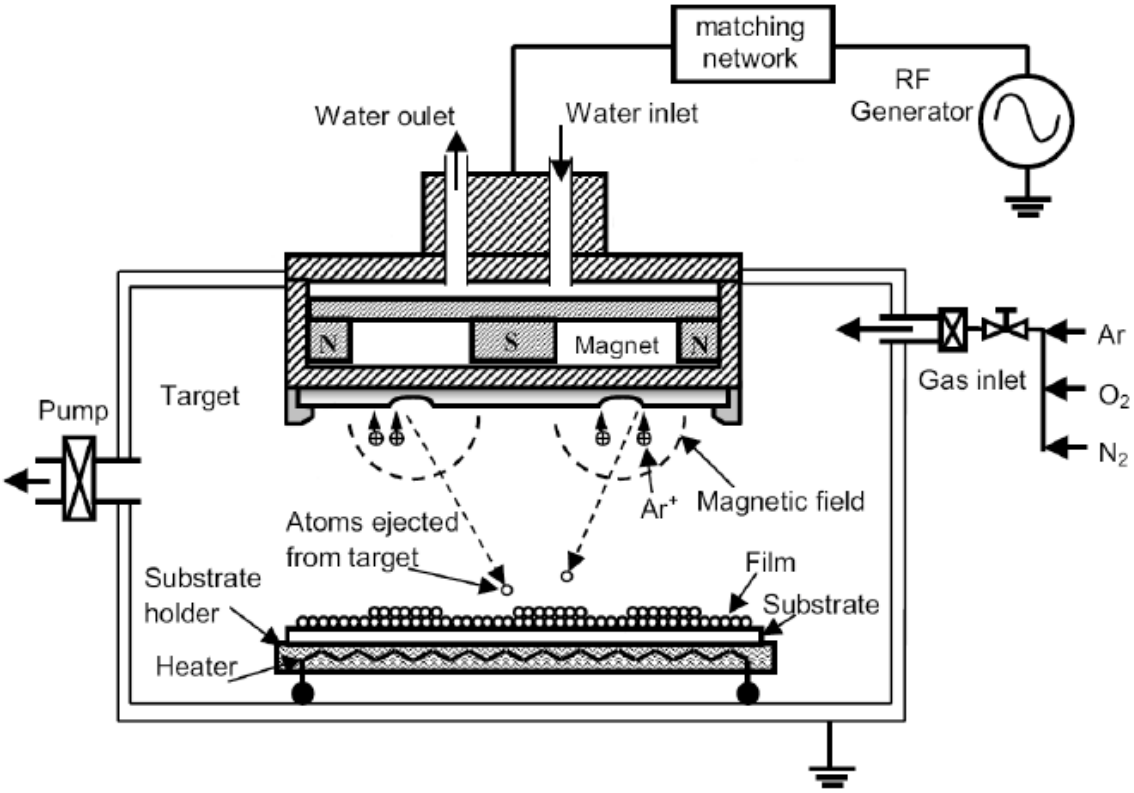


Figure 15: Diagram of the RF magnetron sputtering process [67].

During this thesis, indium tin oxide (ITO) was mostly used, yet, another material consisting of hydrogenated fluorine-doped indium oxide (IFO:H) was tested.

a. ITO

Before the commencement of any deposition, the chamber has to reach a pressure of 2.20E-02 mbar and the substrate has to attain a temperature of 110ºC. Followed by the introduction of 40 standard cubic centimeters per minute (sccm) of Argon at a forward power of 110 W. It must be noted that different recipes have been used through the thesis as it had to be optimized depending on the evolution of the ITO source.

b. IFO:H

For this deposition, the chamber had to reach a pressure of 2.50E-03 Pa and the substrate temperature had to be equal to 105°C. The sputtering will then start with a target that corresponds to a commercial In203-based SCOT. For this process too, Argon is used but here at a concentration of 50 sccm and a power density of 1.8 W/cm^2 while water vapour is joined.

2.1.6. Metallization

The metallization is playing an important role in the efficiency of the solar cell, as it collects the charges and externally transports them. There are different ways to apply it using various materials. The choice of metal is important as it is essential to produce the lowest amount of resistance, for that it is required to select a conductive material that possesses a work function close to the semiconductor in order to have a small potential barrier. Moreover, this one needs to be effective even when only thin fingers are deposited as it is required to have a minimal shading to not impact the short circuit current [68]. During this thesis, two different methods of metallization were applied with distinct materials.

a. Ion Beam Assisted Deposition in Combination with Thermal Evaporation

Both processes are applying the same concept of heating up a metal until it evaporates and deposits on the surface of the wafer. The equipment has the advantage of giving flexibility to the user to select the thickness This kind of deposition uses the same equipment than for MoO_3 deposition and applies exactly the same process for Cr and Al depositions which consist of thermal evaporation (**Section 2.1.4**). However, for Ag coating, the process is different. The deposition is done by electron beam evaporation which consists of heating up the source through ion beam assisted to evaporate it and coat the surface. This is possible by warming the cubicle containing the material through a filament that conducts a high electrical power. Various recipes have been written combining different thicknesses and/or materials. Through this process, there is also the possibility to coat the full area or applying a special design by covering the wafer with a mask.
In order to not heat up the wafer, it was preferred to not deposit a thick layer in one go. When this was required, the deposition was divided into a two- or more steps with a break of 20 minutes cool down while the vacuum level was kept on.

b. Screen Printing Using Silver (Ag) Paste

This process is usually used in the solar cell fabrication industry as this one is fast, robust and well developed. The process consists of placing one wafer on a mobile plate that will slide underneath a frame of thin wire meshed together. The formation of the interwoven is dependent on the deposition requirement (full area or fingers selection). The deposited material is used in the form of sticky glue corresponding to Ag-based polymer paste Dupont PV416 [69]. The paste is placed on top of the framework and as soon as the process started, a brush is sweeping the full area with the paste covering the wafer surface. To harden the Ag, the cell is annealed at 170°C for 40 minutes. Due to the fact that the process requires the use of a paste, it is difficult to control the thickness. Approximately, 67 µm of silver are coating the surface with an aspect ratio of 0.18. The process used for the deposition was optimized by a former student in [70]. During the period of this thesis, two different designs have been used. The replacement was made in order to reduce the losses caused by the metallization as the second design (*Figure 16(b)*) provides thinner busbars with a good quality of the carrier transport. In addition, for the “big” design (*Figure 16(a)*), it was necessary to cut each cell apart which damaged the rear metallization. With *Figure 16(b)*, there was no need to cut them, indeed, they were isolated thanks to the addition of a mask during the ITO deposition. The main difference between the two designs is the area. To make it easier, we will refer to *Figure 16(a)* as the “big” design (Area = 7.84 cm²) and *Figure 16(b)* to the “small” design (Area = 3.92 cm^2).

(a) (b)

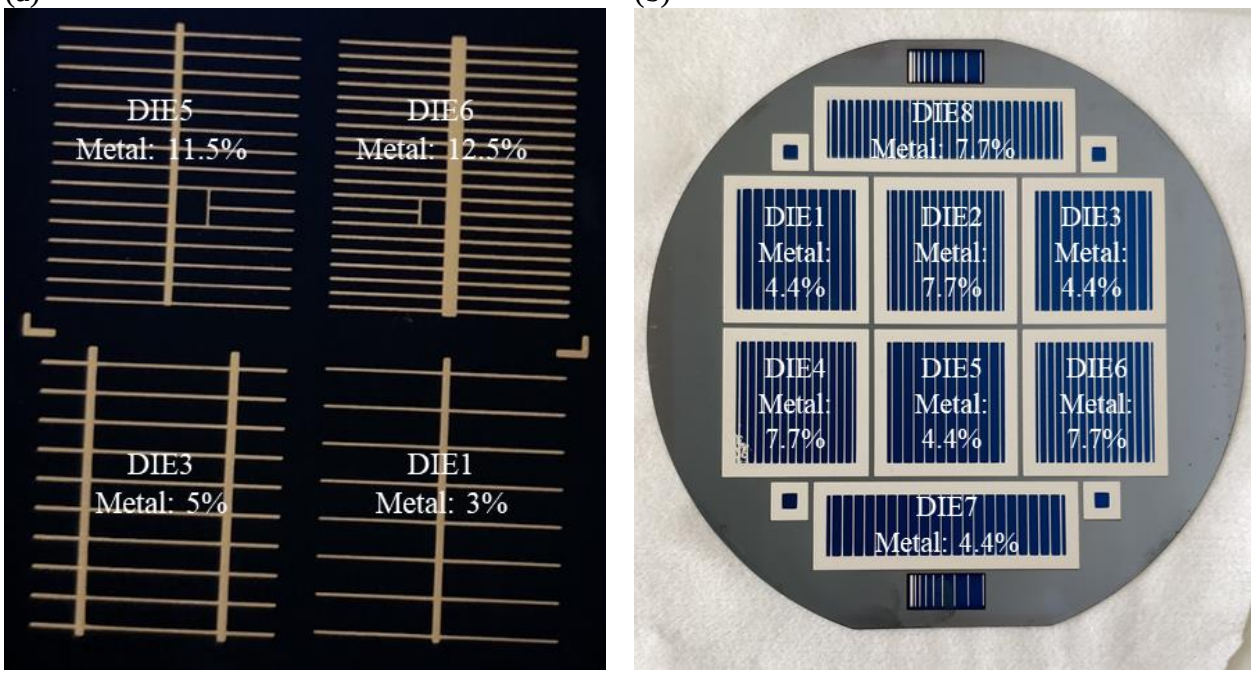


Figure 16: Solar cells made with screen printing (a) "big" design (b) "small" design.

2.2. Characterization

As no solar cell was directly produced, it was not possible to measure the typical parameter; it is why different criterions were measured by using Sinton Consulting WTC-120 (**Section 2.2.1**).
Once the choice of the layer was done, solar cells were produced and their quality was measured using a sun simulator (**Section 2.2.2**), SunsV_{ox} (**Section 2.2.3**) and EQE (**Section 2.2.4**) which are described in this section.

2.2.1. Photo-Conductance Lifetime Tester

This equipment is used to measure the carrier lifetime (τ_{eff}) which gives important information about the quality of the surface passivation and the process applied on the wafer. It is assumed that a high lifetime is equivalent to good quality material [71]. The lifetime of a carrier is defined as the average time it required for carriers to recombine and form an electron/hole pair and define the open-circuit voltage (V_{oc}) for the solar cell. As no solar cells are produced when this measurement is taken, the equipment provides the implied open-circuit voltage (iV_{oc}) which gives an indication of what should be the V_{oc} if a complete solar cell was constructed.
The process uses a nondestructive technique that measures the difference of photo-conductance due to recombination. There are various modes for the measurement, the user has to select the right one depending on the expected minority carrier lifetime The outcome gives the average time it takes for a minority carrier generated by a light source to recombine at the surfaces of the wafers as it is assumed that no recombination happens in the bulk. Therefore the passivation quality is sensible to any impurities or defect deposited on top of the c-Si surfaces. Sensors are recording the difference in photo-conductance and send it directly to the PC as shown in *Figure 17*.

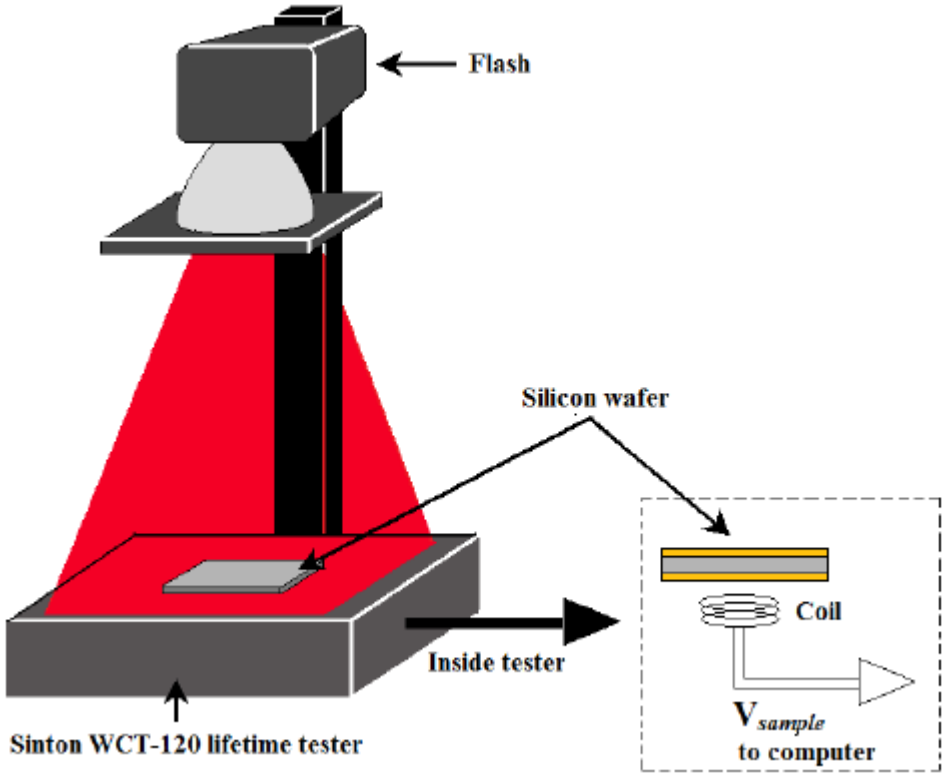


Figure 17: Diagram of photo-conductance lifetime tester [72].

The minority carrier lifetime is extracted at a minority carrier density equal to 1.0E+15 cm^{-3} [73] which corresponds to the excess of carriers present in the (n)c-Si substrate. Furthermore, *Zhang* [74] explains the choice of this selected minority carrier density as the closest value to the injection level for light intensity at one sun and it also coincides with the point in where the radiative and auger recombination, which corresponds to recombination happening in the bulk, are minimal so we can focus on the surface recombination.

The iV_{oc} is obtained at one sun which is defined as the irradiance of the sun outside the atmosphere at a distance of ≈ 1.5E+8 km [75].

2.2.2. Sun Simulator

The quality of a solar cell is determined thanks to different properties that can be measured using a sun simulator, here we used WACOM WXS-156S. The simulator is able to reproduce an illumination equivalent to the standard test condition (STC) (1000 W/m²) with a spectrum identic to the sun (AM1.5) thanks to the utilisation of a halogen and a xenon lamp. The equipment is classified as AAA [76] which means that it provides a spatial uniformity over the surface of the cells, an excellent sun simulation and temporal. The measurement is taken from a certain range of voltage which can be determined by the user. Indeed, the simulator is controlled by a software which also provides a final excel file with all the measured properties.

2.2.3. SunsV_{oc} Measurement

This equipment provides an IV curve excluding the series resistance (R_s). This is possible as the measurements are taken through incident light intensity dissimilarly to WACOM WXS-156S (**Section 2.2.2**) which adjusts the outcome depending to the current [77]. The parameter calculates the SunV_{oc} which is equivalent to the V_{oc} excluding any series resistance (R_s).

For this measurement, no calibration is required as one reference cell is implemented in the trunk.

a. Series Resistance

The R_s represents the losses caused at the interface of the distinct material and will only affect the voltage while it is assumed that the J_{sc} remains constant. Using *equation 3* [78], we can calculate the series resistance.

$$\boldsymbol{R}\ (\Omega.\boldsymbol{cm^2}) = \frac{\boldsymbol{V}}{\boldsymbol{J}} = \frac{\boldsymbol{V_{MPP,SunsVoc} - V_{MPP}}}{\boldsymbol{J_{MPP}}} \quad 3$$

2.2.4. External Quantum Efficiency (EQE)

This parameter represents the ratio of the collected photons incident to the surface able to generate electron-hole pairs. The criterion is measured through a certain range of wavelengths and generate a sort of bell curve. Thanks to this graph it is possible to analyse the electrical and optical losses [79]. The equipment is able to determine the EQE by recording the current when a monochromatic illumination is applied to the un-metalized area of the cell.
The device is controlled through a Labview interface which required the user to start with calibration. Once it is ready to use, the first step consisted in placing the solar cell in a frame while moving it in order to have the polychromatic light directing a metal free-area. Once everything is assembled, the software is automatically taking all the measurements thereupon the last task is for the user to save the data.

a. Active Efficiency

A J_{sc} of the active area (surface uncovered with metal) is provided by the EQE equipment and helps to provide an efficiency of the active area by establishing the percentage of the area that is metal-free. The active efficiency can be calculated thanks to *equation 4.*

$$\boldsymbol{\eta_{active}} = \boldsymbol{\eta_{total}} * \frac{\boldsymbol{J_{sc,EQE}}}{\boldsymbol{J_{sc,solar\ simulator}}} \quad 4$$

3. Passivation Optimization of the (i)a-Si:H/MoO_x interface

In this chapter, we investigate how the (i)a-Si:H and MoO_x would respond to each other for the application in SHJ solar cells. As conventional for silicon heterojunction, an intrinsic hydrogenated amorphous silicon ((i)a-Si:H) layer is adopted to provide passivation to the (n)c-Si surfaces. To make it straightforward, it was decided to deposit the two layers stated above on top of each other and see how they interact; instead of producing a complete solar cell which requires additional fabrication steps so more time. For this chapter, we will also find the optimum thickness for MoO_x in a combination of an (i)a-Si:H to obtain outstanding surface passivation and hole selectivity contact, as it is important to select wisely the thickness of each layer that will be present in the final fabrication of the solar cell.

3.1. Experimental Details

For this first experiment, we fabricated double-sided texturized (n)c-Si wafers dedicated for surface passivation with a good quality as described in **Section 2.1.1**.
The wafers were ready for deposition, thus the intrinsic a-Si:H material was the first layer to be deposit through “Amor” PECVD (**Section 2.1.3**).
As only the front surface needed to be investigated, the intrinsic layer ((i)a-Si:H) providing good passivation was deposited on the back which consisted of 20 nm of thickness as nothing else will be deposited on it.
To validate the surface passivation quality applied on the rear side, a symmetrical sample coated with 20 nm of (i)a-Si:H on both surface was produced. The minority carrier lifetime (τ_{eff} of 3.8 ms) and the V_{oc} (716 mV) were satisfactory to establish this thickness as the constant width for the rear surface.
As a result of the excellent passivation on the rear surface, various layers could finally be applied to the front surface and analysed, knowing that any changes in the parameters are coming from the front modification.
The other side of the (n)c-Si is covered with the stack we intend to deposit on the final device which consisted of a thin (i)a-Si:H (7 nm) and a MoO_x layer. As previously stated, the deposition times were adapted using a corrective factor of 1.73 to take into account the coating of a textured surface. The carrier lifetime was measured directly after the (i)a-Si:H deposition (**Section 2.1.3**). Then the wafer was cut in four quarters as shown in *Figure 19*; to deposit MoO_x film with different thicknesses via thermal evaporation (**Section 2.1.4**) and investigate which one will provide optimal results.
Subsequently, the optimum layer stack was deposited on another wafer to test how the material will respond to certain temperatures that might be required for further deposition.
However, for the usual solar cell fabrication, it is necessary to deposit a TCO layer as MoO_x cannot provide a sufficient lateral conductivity. Therefore, a 75 nm ITO layer was sputtered (**Section 2.1.5**) on top of the (i)a-Si:H/MoO_x stack as shown in *Figure 18*.
The entire set of samples were introduced in an oven for 15 minutes at 130°C to investigate the effect of the temperature.

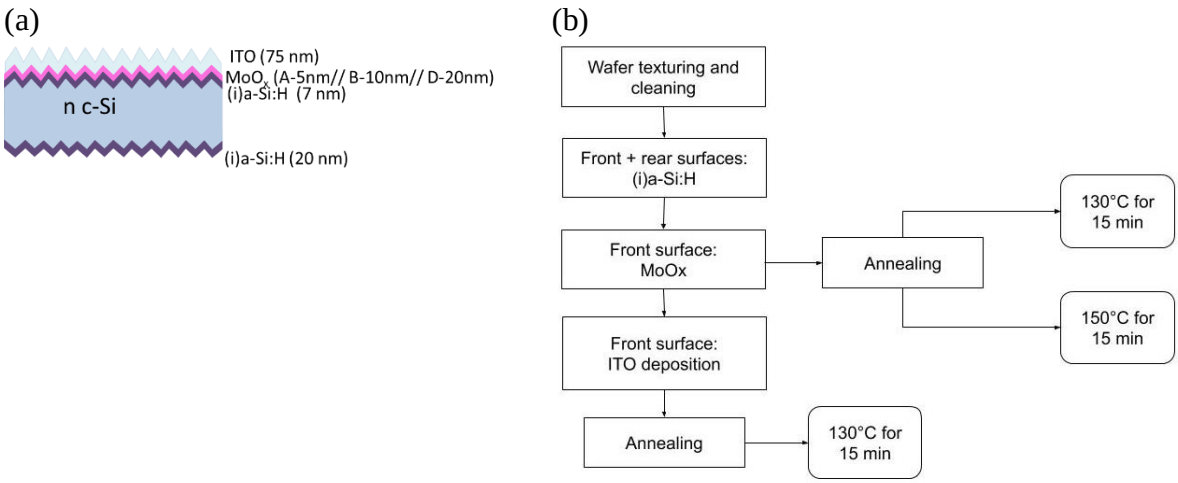


Figure 18: Experimental for the passivation optimization overview (a)diagram of the deposition (b)simplified flowchart of the process applied for the deposition of each layer.

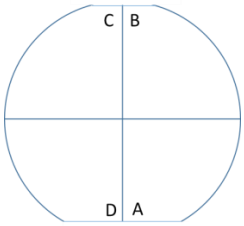


Figure 19: Representation of sample labelling after cutting.

Table 4 summarizes the individual structure of each quarter. It must be enlightened, we deposited the intrinsic layers and ITO at the same time for all the quarters, while the MoO_x depositions are processed in different deposition runs to obtain the indicated thickness.

Table 4: Summary of layers thicknesses for the investigation of passivation quality optimization.

Sample	(i)a-Si:H (back) (nm)	(i)a-Si:H (front) (nm)	MoO_x (front) (nm)	ITO (front) (nm)
A	20	7	5	Yes
B	20	7	10	Yes
D	20	7	20	Yes

3.2. Effect of MoO_x Thickness and Response to Annealing

Firstly, we verified that the MoO_x deposition will not affect the passivation quality of (i)a-Si:H. Samples with (i)a-Si:H/MoOx:H stack were fabricated as described above (see *Figure 18*). *Figure 20* shows the response of the carrier minority lifetime depending on the minority carrier density for high and low injection (refers to the minority carrier density). The curvature is keeping its initial shape after MoO_x deposition.

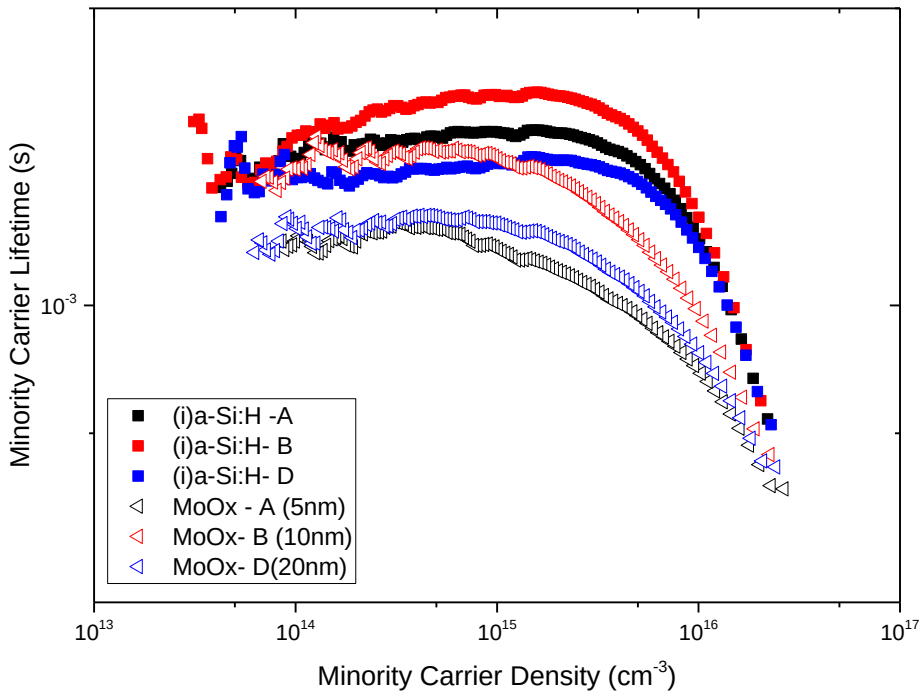


Figure 20: Minority carrier lifetime as a function of minority carrier density before and after the MoO_x deposition with variable MoO_x thicknesses. The corresponding sample's sketch is reported in Figure 18 (excluding ITO deposition).

In *Figure 20*, we observed that each quarter is giving similar shape right after the deposition of the intrinsic layer with a small deviation mainly in the low minority carrier density. The difference can be caused by a non-uniformity during the PECVD. As soon as MoO_x is deposited, we observed a shift to a lower minority carrier lifetime; for a width of 5 and 20 nm the reduction is more important than for 10 nm. However, for any thickness, the shape of the curve is not affected and the reduction remains proportional to the initial trajectory which gives a good indication about the non-detriment of the deposition.
Figure 21 shows the minority carrier lifetime and iV_{oc} in the as-deposited condition and after MoO_x deposition. The purple columns represent the wafer right after the (i)a-Si:H deposition followed by the values of each quarter after being cut. We measure a τ_{eff} above 2 ms for all the quarters with an iV_{oc} in the range 724-728 mV. While the magenta columns show the results of each quarter after MoO_x deposition where a reduction in both τ_{eff} (1.3-2.2 ms) and iV_{oc} (706-709 mV) happens.

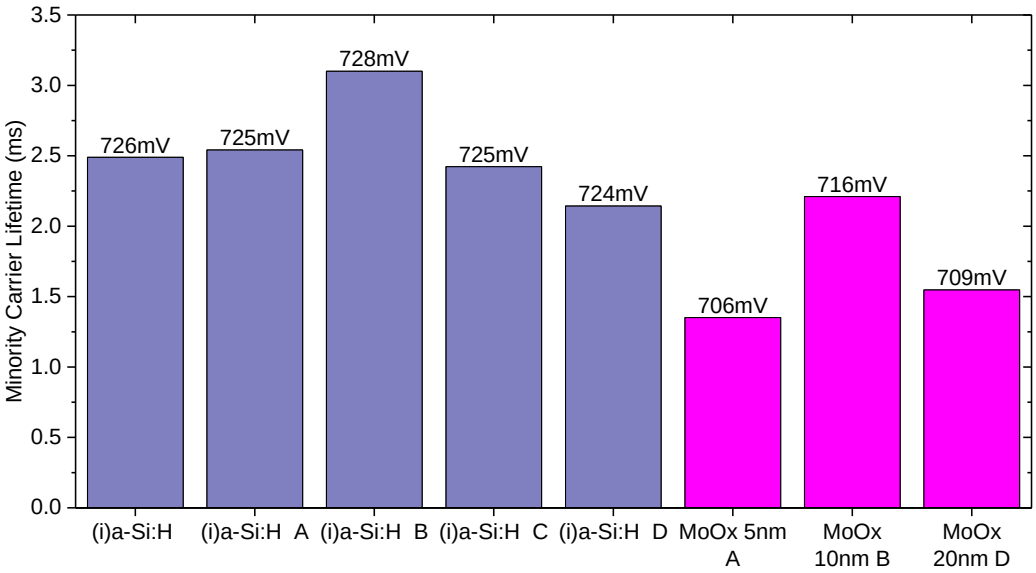


Figure 21: Minority carrier lifetime and iV_{oc} before and after the MoO_x deposition with variable thickness. The corresponding sample's sketch is reported in Figure 18 (excluding ITO deposition).

Figure 21 shows that MoO_x is slightly reducing the quality of the passivation, but this one is required in order to act as holes selectivity contact. The small decline could also be due to the fact that (i)a-Si:H and MoO_x are degrading after exposure in ambient condition due to the presence of oxygen and humidity in the environment [80].

In the next step, we investigated the effect of the MoO_x thickness on the passivation quality and identify the optimum thickness to be used for solar cell fabrication. This study was important as it is necessary to have a layer providing hole selective contact without being too thick as we do not want to excessively affect the transparency of the material. In other words, we want to obtain the perfect trade-off between the layer thickness and electrical properties.

Figure 20 and *Figure 21* are in concordance. They are both showing that 10 nm is providing the best outcome with a small deviation from the intrinsic layer for the minority carrier lifetime as a function of minority carrier density (*Figure 20*) and a sufficient iV_{oc} (716 mV) at one sun and minority carrier lifetime of 2.21 ms at a carrier density of 1E+15 cm^{-3}. By increasing or decreasing the thickness, the minority carrier lifetime (5 nm of MoO_x = 1.35 ms and 20 nm of MoO_x = 1.55 ms) and iV_{oc} (5 nm of MoO_x = 706 mV and 20 nm of MoO_x = 709 mV) are diminishing compared to the 10 nm of MoO_x. *Tong et al.* [27] suggested that the thickness should be kept as thin as possible (less than 11 nm) in order to:

- maximize the extraction of the holes carriers,
- decrease the parasitic losses caused by light absorption and
- reduce the tunnelling of minority charge carriers [66].

A new wafer was then fabricated with 10 nm of MoO_x and the halves were annealed at 130°C and 150°C for 15 minutes to see how the material is reacting. These conditions were investigated as the future TCO deposition might require these range of temperatures.

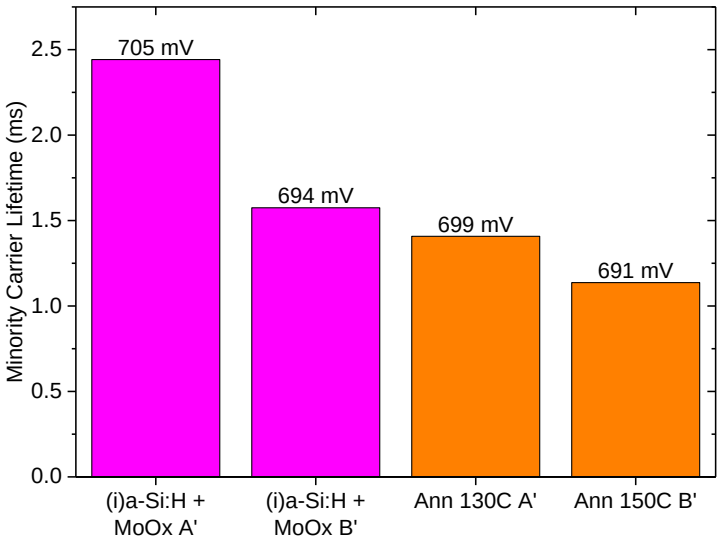


Figure 22: Minority carrier lifetime and iV_{oc} for the stack of layers corresponding to the sample's sketch reported in Figure 18 (excluding ITO deposition) after 15 min of annealing at 130°C and 150°C.

Figure 22 shows that the degradation caused by the annealing is different for 130°C and 150°C. The deterioration of the minority carrier lifetime at an annealing temperature of 130°C (MoO_x = 2.44 ms, after ann = 1.41 ms) is more important than for 150°C (MoO_x = 1.57 ms, after ann = 1.14 ms). For the iV_{oc} we observe a reduction by 6 mV and 3 mV for 130°C and 150°C, respectively. It is difficult to affirm that the difference in reduction is for sure caused by the variation in annealing temperature. Indeed, the minority carrier lifetime and the iV_{oc} is dissimilar directly after the MoO_x deposition for half A' (2.44 ms, 705 mV) and B' (1.57 ms, 694 mV) even if they are supposed to be similar. The contrast can be due to non-uniformity generated by any deposition done until this point. At the same time, the results are in concordance with *Kobori et al.* [81] which state that MoO_x is affected by low-temperature annealing as it causes the development of oxygen carriers and will affect the carrier transport properties. While *Essig et al.* [82] explain the origin of this deterioration as the hydrogen located in the intrinsic layer is starting to release and interact with the MoO_x already at a very low temperature (>100°C).

3.3. Effect of ITO Sputtering Deposition on the Passivation Quality

For the future fabrication of solar cell, a TCO is needed; this deposition is not soft as it requires plasma luminescence and ion bombardment which might damage the passivation. This effect has been reported by *Demaurex et al*. [83]; sputtering could impact the interface between (i)a-Si:H/c-Si which will disturb the carrier transport.
The quarters of the wafer from *Figure 21* were then deposited with ITO as shown in *Figure 23*, which represents the minority carrier lifetime and implied open-circuit voltage after each deposition.

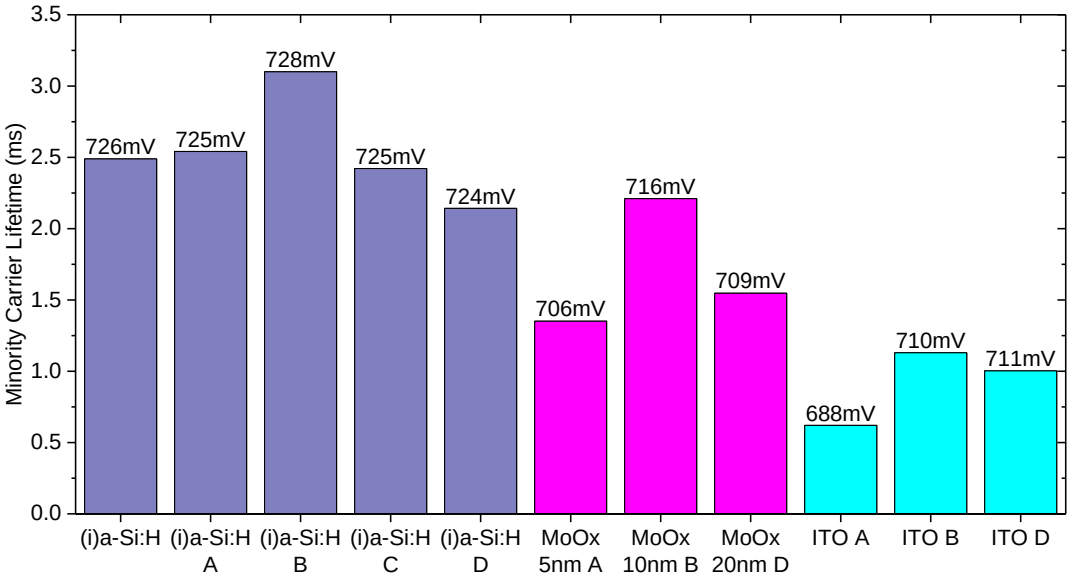


Figure 23: Minority carrier lifetime and iV_{oc} corresponding to the sample's sketch that is reported in Figure 18.

Figure 23 shows that the introduction of ITO damages the passivation quality more or equally than MoO_x deposition. For 5 nm of MoO_x, the decrease in iV_{oc} from intrinsic to TMO deposition is equal to 19 mV while after sputtering it decreases further by 18 mV. Concerning the minority carrier lifetime, the 5 nm layer is a bit more affected by MoO_x deposition ((i)a-Si:H = 2.54 ms, MoO_x = 1.35 ms and ITO = 0.62 ms). It shows that for a thin layer of MoO_x, the quality of passivation is affected by both deposition (MoO_x and ITO). For 10 nm of MoO_x, the iV_{oc} is more moved by the MoO_x deposition ((i)a-Si:H = 728 mV, MoO_x = 716 mV and ITO = 710 mV) while the minority carrier lifetime is similarly affected by both deposition ((i)a-Si:H = 3.1 ms, MoO_x = 2.21 ms and ITO = 1.13 ms). The real difference happens when MoO_x has a thickness of 20 nm, indeed for this design, the iV_{oc} is not affected by ITO deposition ((i)a-Si:H = 724 mV, MoO_x = 709 mV and ITO = 711 mV) while the minority carrier lifetime gradually decreases after each deposition ((i)a-Si:H = 2.14 ms, MoO_x = 1.55 ms and ITO = 1.02 ms).
Figure 23 illustrates that the wafer with an MoO_x thickness of 10 nm should be selected as it provides the right balance between performant iV_{oc} and minority carrier lifetime after ITO deposition with the ability to keep the transparency of the material. Thus *Figure 24* shows the minority carrier lifetime curve after the deposition of each layer for the quarter of wafer coated with 10 nm of MoO_x.

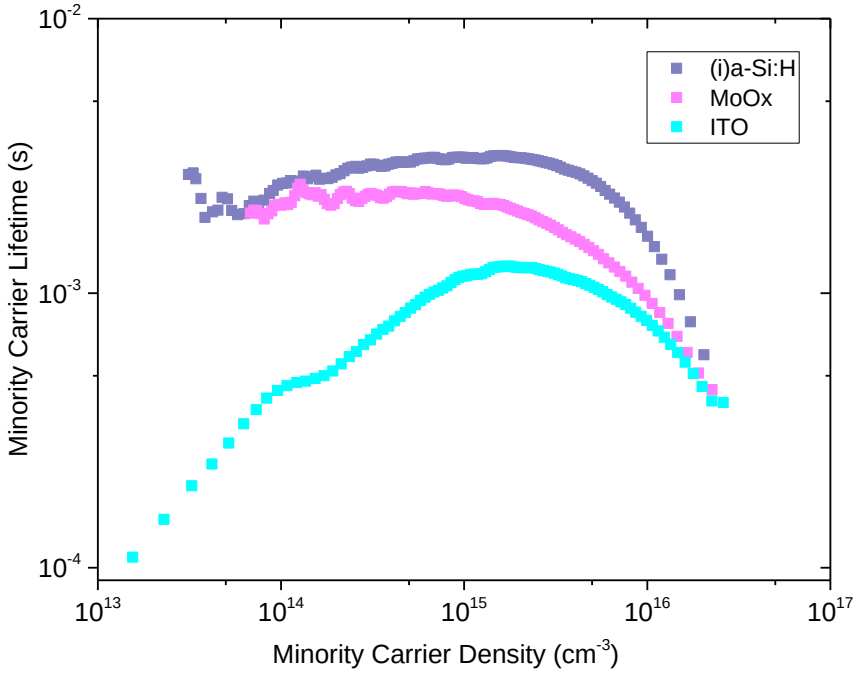


Figure 24: Minority carrier lifetime as a function of minority carrier density before and after each deposition for the quarter of wafer having 10 nm of MoO_x. The corresponding sample's sketch is reported in Figure 18.

Figure 24 demonstrates that disruptions are coming after the deposition of the ITO for the stack of layers composed of 11 nm of (i)a-Si:H and 10 nm of MoO_x. The curve is completely diverging from a range of 1E+14 to 1E+15 cm^{-3} of minority carrier density; this reactiveness is also observed for HIT solar cells [84]. However, there was a possibility that the MoO_x would have the ability to protect the layer beneath but this was not the case; the outcome is in concordance with [42].
Finally, we investigated the effect of thermal annealing of the complete stack (*Figure 18*) and see the response of the passivation quality at a temperature of 130°C (*Figure 25*).

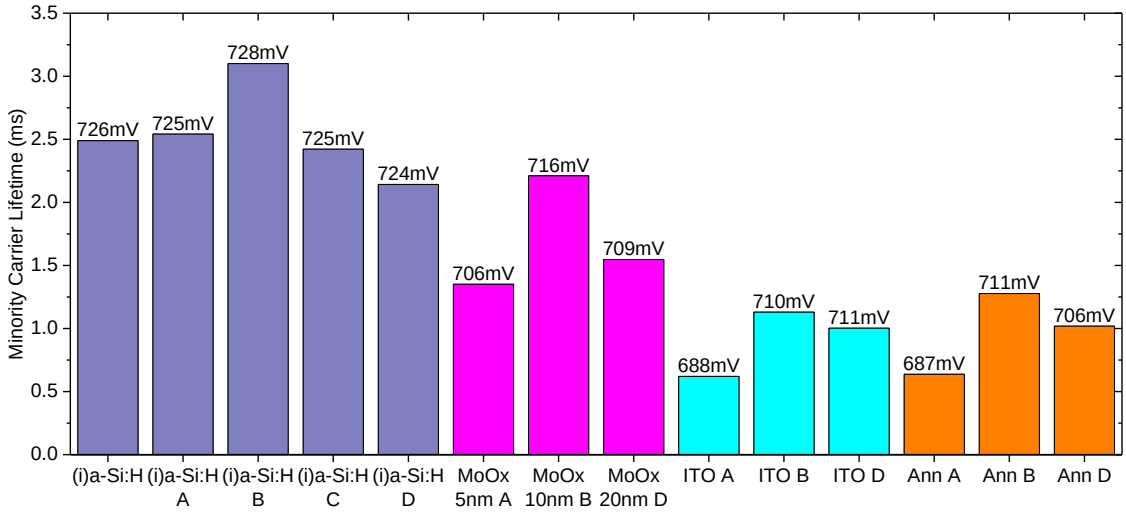


Figure 25: Minority carrier lifetime and implied V_{oc} corresponding to the sample's sketch that is reported in Figure 18 after 15 min of annealing at 130°C.

Figure 25 proves that the introduction of the ITO layer also procures another main asset which is the protection against temperature sensitiveness. Indeed the minority carrier lifetime and the iV_{oc} are remaining roughly constant after annealing for each MoO_x thicknesses. The minority carrier lifetime slightly increases for 5 and 10 nm of MoO_x after annealing (5 nm of MoO_x = 0.64 ms and 10 nm of MoO_x = 1.28 ms). Concerning the iV_{oc}, this one is affected by 5 mV for a thickness of 20 nm of MoO_x while for 5 and 10 nm it improves by 1 mV.

Through this experiment, we concluded that 10 nm of MoO_x is providing the right balance between keeping the material transparent and providing a decent minority carrier lifetime and iV_{oc} after ITO deposition (1.13 ms and 710 mV). However, the results are not satisfactory and there is a belief that they can be improved. This will be investigated in **Chapter 4**.

3.4. Conclusions

For this first experiment, we investigated the minority carrier lifetime and iV_{oc} of a stack of layers composed by a thin (i)a-Si:H, MoO_x and ITO deposited on top of textured (n)doped crystalline silicon wafers. Various thicknesses (5, 10 and 20 nm) for MoO_x layer were tested to analyse how they would affect the outcome. Firstly, it was decided to study the effect of MoO_x on the surface passivation generated by the intrinsic material ((i)a-Si:H) through its deposition. During these experiments, it was confirmed that molybdenum oxide would reduce the quality of passivation however, the material is required to act as a hole selectivity contact. The analysis showed that 10 nm was the right choice of thickness as it generated only a small reduction on the minority carrier lifetime (before MoO_x = 3.1 ms and after MoO_x = 2.21 ms) and iV_{oc} (before MoO_x = 728 mV and after MoO_x = 716 mV).
However, it was also noticed that the combination of (i)a-Si:H/MoO_x is sensible to low-temperature annealing like 130°C or 150°C which will bring complications for further deposition. In addition to the temperature sensitiveness, the layer is affected by the RF magnetron sputtering process required for ITO deposition and MoO_x is not able to protect the intrinsic layer against deterioration.
After the ITO deposition, the passivation quality was degraded with a poor minority carrier lifetime and iV_{oc} equal to 1.13 ms and 710 mv for wafer deposited with 10 nm of MoO_x. The main advantage is that as soon as the ITO layer is present, the underneath stack of layer is not sensitive to low-temperature annealing (130°C) anymore.
It is then imperative to find a way to attenuate the damages caused by ITO and MoO_x deposition. Various options to resolve this problem are being discussed and tested in **Chapter 4**.

4. Strategies to Improve/Stabilize the Passivation Quality

The precedent experiments (**Chapter 3**) showed that by annealing MoO_x on top of (i)a-Si:H or by introducing ITO on the stack of layers, the passivation quality is affected and degrades. It is then imperative to find a way to attenuate the damages. Other groups suggested various solutions that could be tested. The first alternative was reported by *Essig et al.* in [82]; they related the origin of the degradation to the hydrogen effusion from (i)a-Si:H/MoO_x. Hydrogen will interfere with MoO_x layer and slowly form water that will accumulate at the surface [37]. This drawback could be attenuated by annealing the intrinsic layer before MoO_x deposition. The purpose of it is to reduce the hydrogen content in the intrinsic layer. The hydrogen starts to be released at a temperature of 100°C with a peak at 360°C on the other hand, dehydrogenation will lead to a degradation of the passivation quality thus the pre-annealing temperature should be kept at low temperature [82]. Hydrogen is required to saturate the bulk defects present in the silicon base [85].
Besides the above-mentioned approach, we investigated the use of a protecting layer consisting in a thin (p)doped hydrogenated nanocrystalline silicon oxide ((p)nc-SiO_x:H) that can improve at the same time field-effect passivation. The (p)nc-SiO_x:H material is a mixture of doped nanocrystalline silicon and amorphous silicon oxide [48]. The material possesses many advantages, like its versatility which means that it can be tuned depending on the requirement of the experiment. Moreover, it has good optical properties and will not bring too much parasitic absorption thanks to its larger bandgap compared to (i)a-Si:H and its thin thickness. In addition, by adding this layer in our front stack, the refractive index (n) will be reduced more gradually from silicon to MoO_x [86]. By using a layer having oxygen, this should not bring too many defects as the Si-O (4.685 eV) energy bond is strong, in comparison to Si-Si (3.524 eV) and Si-H (4.073 eV) [87] [88]. The theory is that the (p)doped layer will act as a buffer layer and should improve the carrier transport by smoothing the band bending.

4.1. Experimental Details

This part is divided into two sub-sections, the first consists on testing the effect of pre-annealing the (i)a-Si:H layer and the second one addresses to the addition of a thin (p)nc-SiO_x:H in between the (i)layer and the MoO_x.

4.1.1. Annealing Before MoO_x Deposition

As mentioned above, we tested the annealing of the intrinsic layer before the MoO_x deposition and we monitored the passivation quality after each step of fabrication. *Figure 26* represents the flowchart that was applied to this experiment.

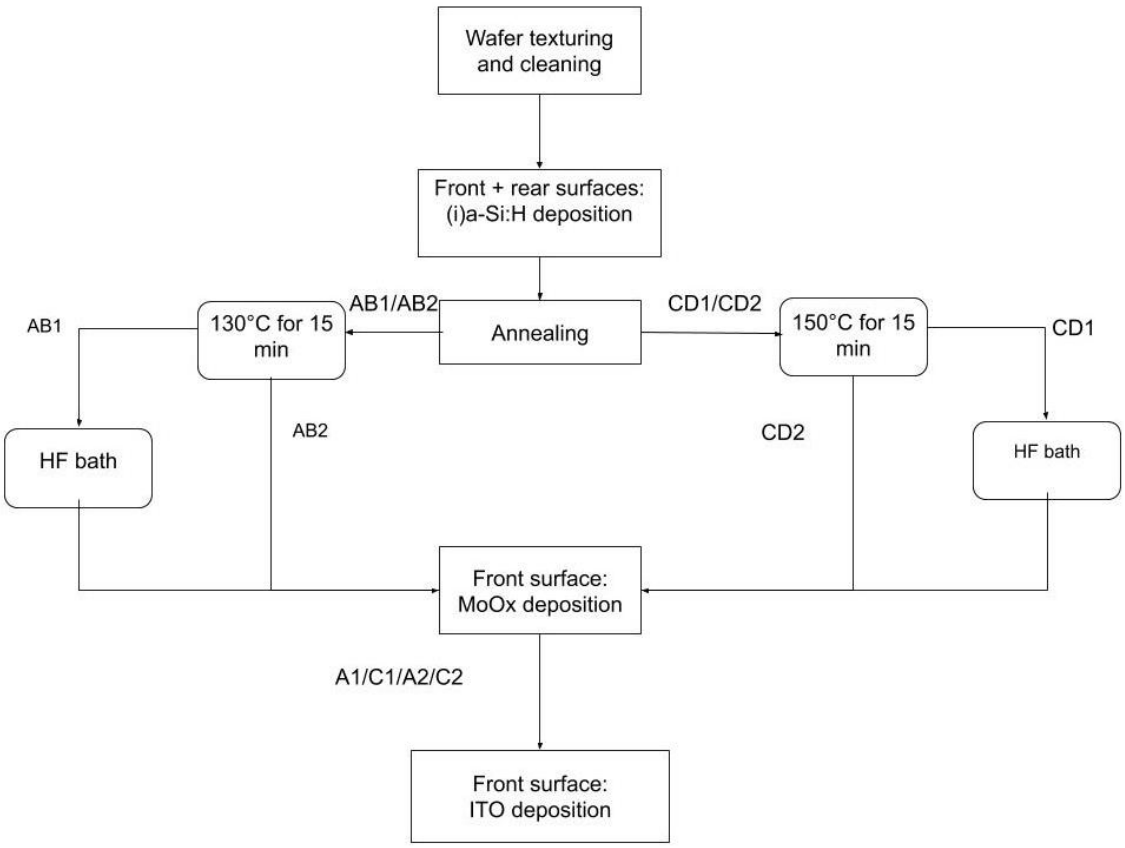


Figure 26: Diagram representing the flowchart applied for the "pre-annealing" experiment.

To start with, two wafers were textured and an intrinsic layer was deposit through "Amor" PECVD (**Section 2.1.3**). The substrates were covered with 20 nm of (i)a-Si:H on one side while 7 nm was applied on the front. The wafers were then cut into half (called A/B and C/D) as illustrated in *Figure 19* so that different treatments could be applied to each of them. It was then important to verify that by breaking the wafer into half, it would not damage the outcome for this purpose the minority carrier lifetime and the iV_{oc} were re-measured. Therefore, the first half (A/B) of each wafer was annealed for 15 minutes at 130°C with a 10 minutes cool down before taking a new measurement. While the second half was treated for 15 minutes but this time at a temperature of 150°C and had a 10 minutes cool down. What differentiates the two wafers is the next step, as one halve was dipped in a 0.55% HF bath for 4 minutes (until becoming hydrophobic) in order to etch the intrinsic layer from any native silicon oxide, while the other one jumped directly to the next stage. A layer of 10 nm of MoO_x was then deposited on the front surface by thermal evaporation (**Section 2.1.4)**. The halves were then cut again in 2 in order to have quarters similar to *Figure 19*, and only one quarter of each half was covered with ITO (**Section 2.1.5**). Finally all the samples were annealed at 130°C for 15 minutes with a 10 minutes cool down.

4.1.2. Insertion of (p)doped Buffer Layer

A summary of the various step applied on the wafer can be found in *Figure 27*.

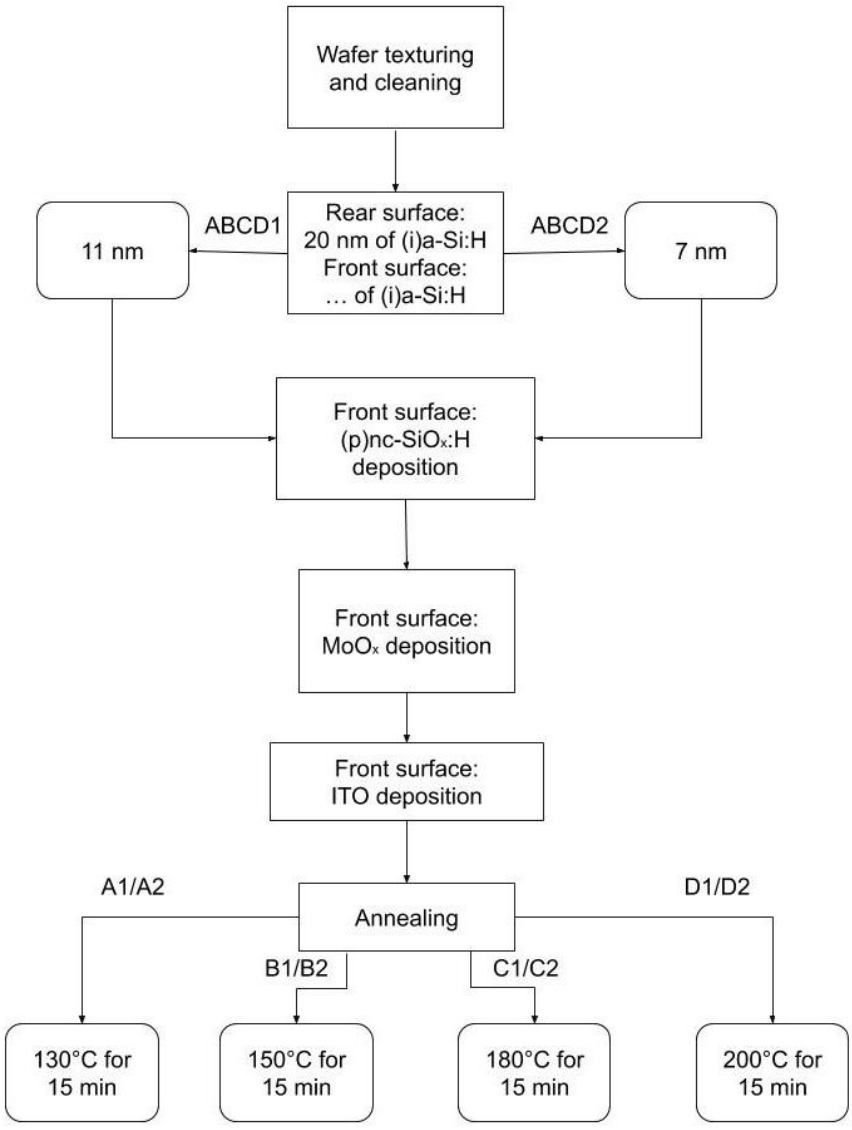


Figure 27: Diagram representing the flowchart applied for the "insertion of (p)doped buffer layer" experiment.

For this experiment, the wafers were texturized and cleaned as described in **Section 2.1.1**. Here two wafers were used, both had a rear side coated with 20 nm of (i)a-Si:H while one wafer had a front side of 11 nm of (i)a-Si:H and the second wafer was coated with a thickness of 7 nm, the difference of thickness was to test the effect of the deposition of the (p)doped layer which required a high hydrogen for silane dilution and a particular power/pressure which are often accompanied with etching [89]. This was followed by the deposition of a 5 nm of (p)nc-SiO_x:H. Both depositions were done using the same "Amor" PECVD system without breaking the vacuum (**Section 2.1.2**). A layer of 10 nm of MoO_x was then deposited through thermal evaporation (**Section 2.1.4**) followed by 75 nm ITO deposition (**Section 2.1.5**). The last step consisted of cutting the wafers in quarters to anneal them at different temperatures and compare the outcomes. This time higher temperatures were applied to review the resistance of ITO layer.

4.2. Effect of Annealing before MoO_x Deposition

Figure 28 shows the quality of the surface passivation through the minority carrier lifetime and iV_{oc} after each step for the wafer on which pre-annealing was followed by HF bath.

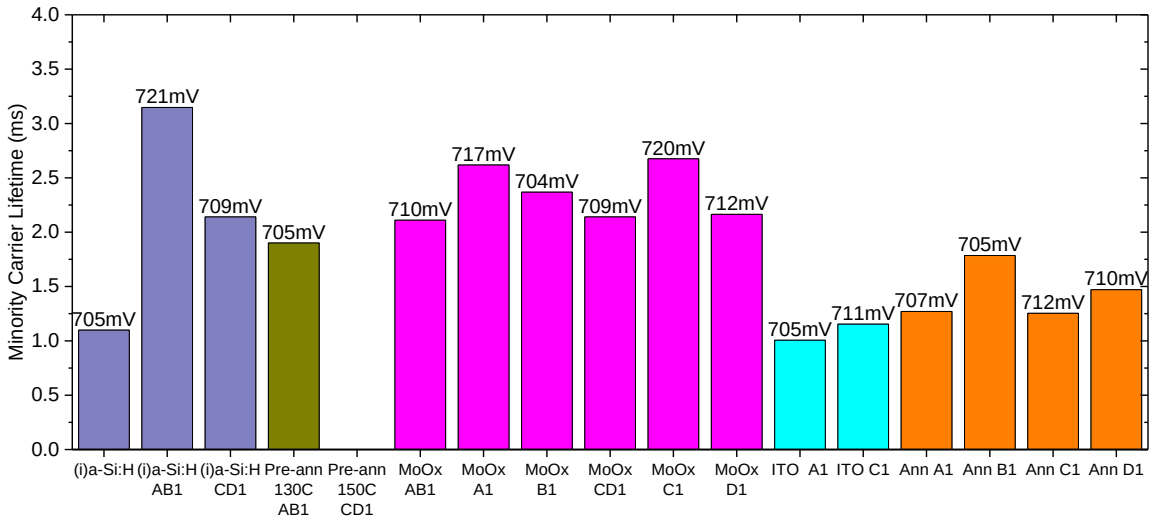


Figure 28: Quality of the passivation for pre-anneal wafer followed by HF dip.

It can be observed that after the intrinsic deposition, the wafer was cut into halves in order to apply different treatments. While being cut in quarters after MoO_x deposition and finally only 2 quarters were completed with ITO deposition while all of them were annealed.

Figure 28 shows that by cutting the wafer into two after the deposition of the intrinsic layer, it is positively modifying the minority carrier lifetime (full wafer = 1.1 ms, halve AB1= 3.15 ms and halve CD1 = 1.9 ms) and the iV_{oc} (full wafer = 705 mV, halve AB1= 721 mV and halve CD1 = 709 mV) of each halve. The change can be related to the homogeneity of the intrinsic layer deposition. However, the minority carrier lifetime and the iV_{oc} of the intrinsic layer decrease by 16 mV and 1.25 ms as it gets warmed up at 130°C for 15 min. For annealing the intrinsic layer at 150°C for 15 minutes, no observation can be done as the measurements were not taken but it is assumed that the layer will react similarly than the lower temperature. We do not observe further degradation after MoO_x deposition. The main reduction in minority carrier lifetime (before ITO = 2.62/2.67 ms, after ITO = 1/1.15 ms and after ann = 1.27/1.25 ms) and iV_{oc} (before ITO = 717/720 mV, after ITO = 705/711 mV and after ann = 707/712 mV) happens after ITO deposition but then slightly increases when annealed. Thus, pre-annealing followed by an HF dip is not achieving the goal of attenuating the deterioration of the passivation quality after ITO deposition.

Compared to *Figure 22* in **Chapter 3**, it can be observed that the minority carrier lifetime (AB1 = 2.11 ms and CD1 = 2.14 ms) and the iV_{oc} (AB1 = 710 mV and CD1 = 709 mV) are more consistent through each halve after MoO_x deposition. The presence of rough uniformity after MoO_x deposition could be explained thanks to *Schulze et al.* [90] by the reconfiguration of the (i)a-Si:H surface in order to be in equilibrium with the bulk.

Figure 29 shows exactly the same process excluding the HF bath after pre-annealing.

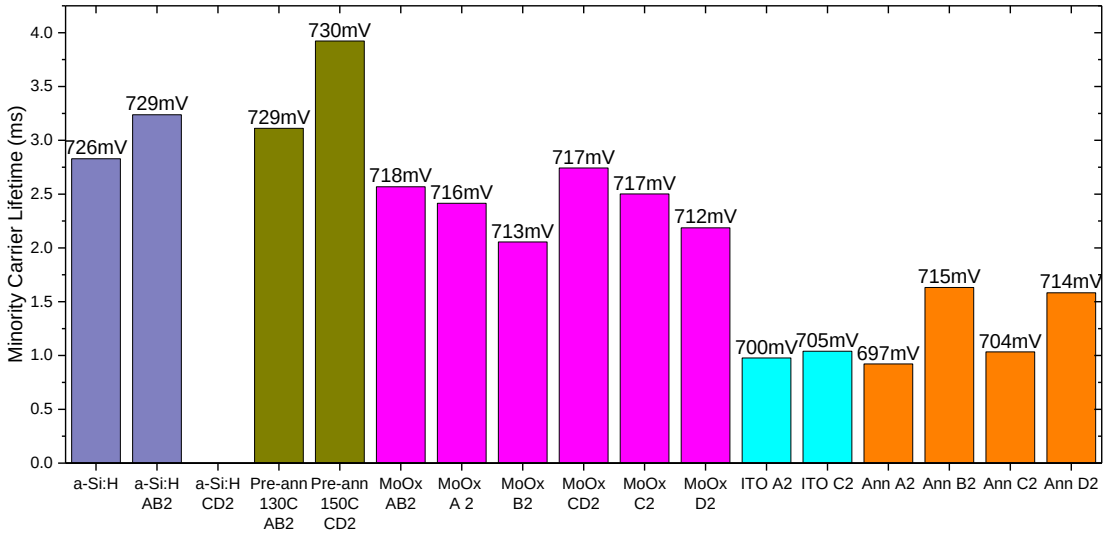


Figure 29: Quality of passivation for the pre-anneal wafer without HF dip.

For *Figure 29*, the changes in minority carrier lifetime and iV_{oc} after each deposition are very similar than *Figure 28*. *Figure 30* is regrouping both results in order to investigate if there are any benefits of adding HF bath after the pre-annealing to remove the presence of native oxides. It shows that in the end, the outcome is similar. However, it can be observed that both wafers did not start with the same quality of passivation. There is no explanation for this initial difference but by using HF bath, the minority carrier lifetime is remaining roughly constant until ITO deposition while by excluding this step, there is a gradual reduction between each step.

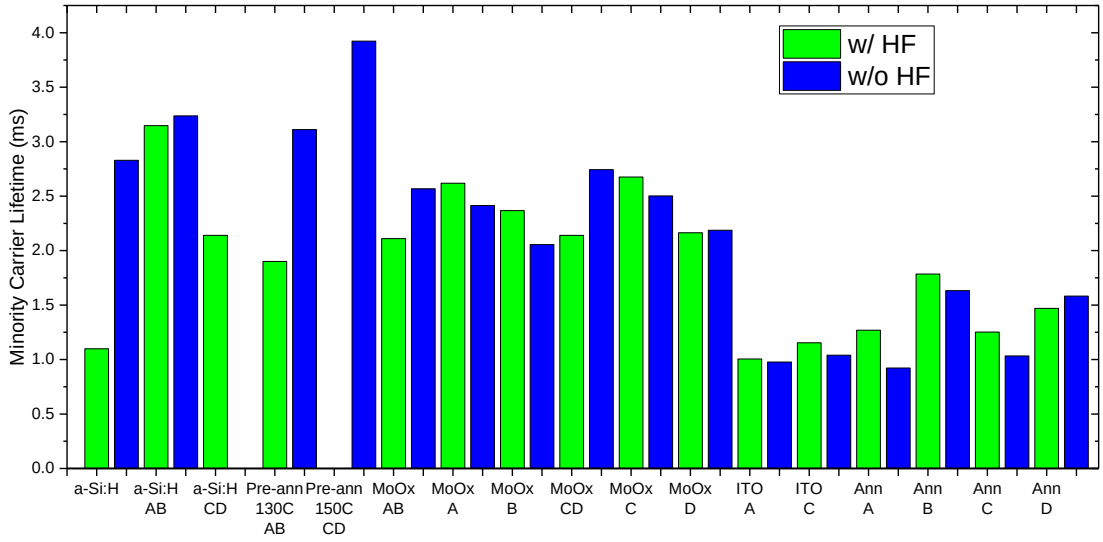


Figure 30: Comparison of samples with and without HF bath after pre-annealing.

The outcome in *Figure 30* also shows that for both wafers the quarters on which no ITO layer was present and were dole out annealing, are providing better minority carrier lifetime and iV_{oc} than quarters having ITO, however, ITO is required for the fabrication of the solar cell. Also, the graphs demonstrate that the ITO layer is providing protection against annealing as a degradation of the minority carrier lifetime happens after annealing when the wafers have no ITO layer. Indeed as soon as the wafer is protected with an ITO layer, it can face larger temperature without an important change in the passivation quality. Despite the importance of ITO deposition, it can be stated that pre-annealing is indeed helping with the MoO_x deposition as it reduces its sensitiveness to temperature and provides a more uniform layer but it is not providing protection against the reduction in the passivation quality caused by the rough ITO deposition.

4.3. *Effect of the Insertion of (p)doped Buffer Layer*

The next experiment consisted of introducing a (p)doped layer of nc-SiO_x:H between (i)a-Si:H and MoO_x interface. Two different wafers were fabricated, the first one had an intrinsic thickness on the front of 11 nm of (i)a-Si:H while for the second wafer a width of 7 nm (i)a-Si:H was applied. The choice of increasing the thickness of the intrinsic layer was due to the fact that the deposition of the (p)doped nanocrystalline layer will etch some of the underneath amorphous materials due to the aggressive plasma conditions such as high power/pressure and high hydrogen for silane dilution.

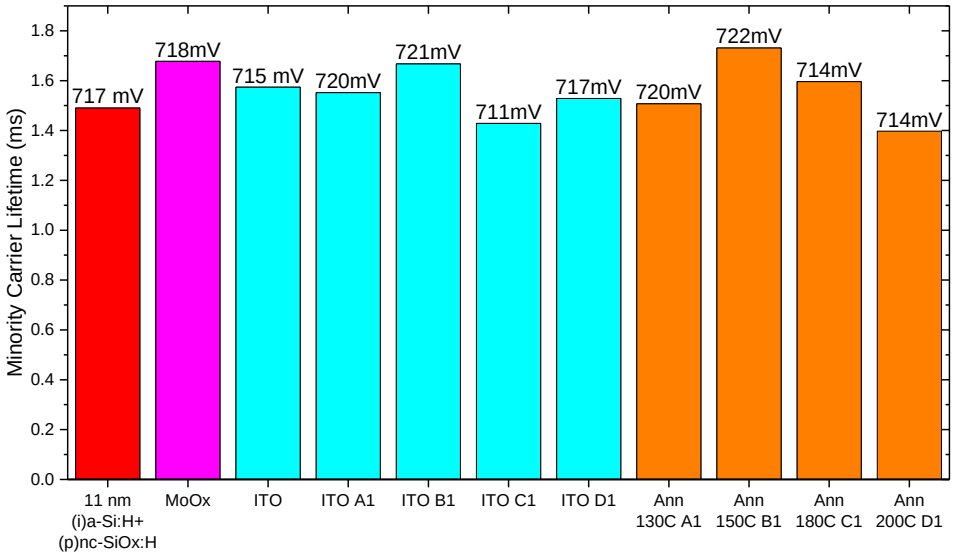


Figure 31: Passivation quality of samples with 11nm of (i)a-Si:H + 5nm of (p)nc-SiO_x:H+ 10 nm of MoO_x + ITO deposition followed by annealing.

Figure 31 represents the measurement taken after the deposition of the intrinsic layer in combination with the buffer layer followed by MoO_x, ITO deposition and the annealing treatment. For this experiment, we increased the temperature for annealing (130°C, 150°C, 180°C and 200°C) in order to verify that the passivation quality will resist to strenuous conditions. The minority carrier and the iV_{oc} are remaining practically constant overall process with a small sensitivity of the iV_{oc} at annealing of 150°C and 180°C. The result for the iV_{oc} is satisfactory with a minimum value of 714 mV for annealing at 180°C/200°C. On the other hand, the minority carrier lifetime is the smallest for annealing at 200°C (ann 200°C = 1.4 ms) but this is due to a lower passivation quality on the halve of wafer (C/D) right after ITO deposition. The outcome of this experiment is still satisfactory.

By trying to reduce the thickness of (i)a-Si:H to 7 nm in order to have a more transparent layer and so less optical losses, *Figure 32* demonstrated that it is then not possible to provide good quality passivation after ITO deposition. Before ITO deposition, the stack of layers with 7 nm of (i)a-Si:H is providing higher minority carrier lifetime compared to 11 nm of (i)a-Si:H. While the opposite occurs for iV_{oc} which has a preference for 11 nm of (i)a-Si:H. After ITO deposition, the passivation quality (minority carrier lifetime and iV_{oc}) is lower for layer having a 7 nm of (i)a-Si:H compared to 11 nm of (i)a-Si:H. Moreover, the results are not consistent through each quarter for 7 nm of (i)a-Si:H after ITO deposition which is different from *Figure 31*.

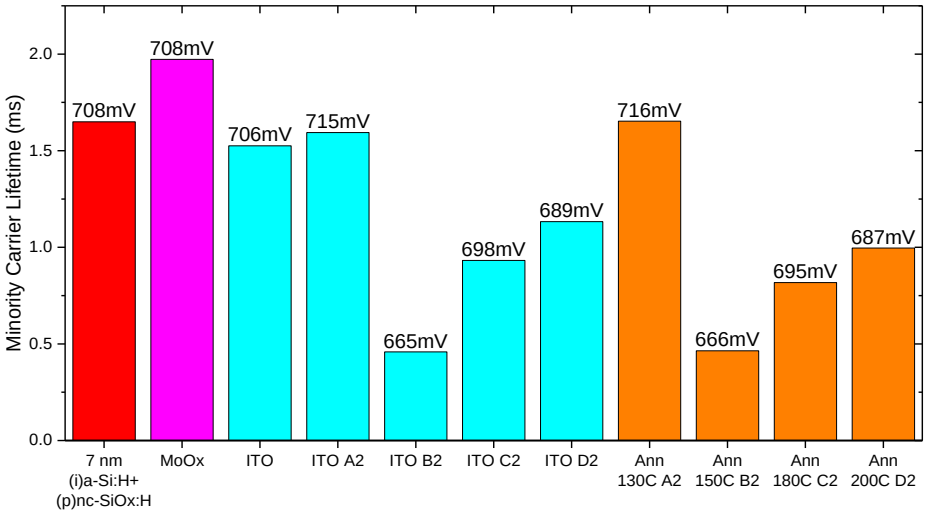


Figure 32: Passivation quality of samples with 7nm of a-Si:H+ 5nm of (p)nc-SiO$_x$:H + 10nm of MoO$_x$ + ITO deposition followed by annealing.

Figure 33 shows a comparison between wafers having 11 nm and 7 nm of (i)a-Si:H, it can be observed that the two wafers have initially a similar quality in passivation with a slight better minority carrier lifetime for thinner (i)a-Si:H layer even after MoO$_x$ deposition. However, as soon as the ITO is applied, the samples with a thin (i)layer are more affected and the minority carrier lifetime will decrease wider after annealing. The addition of a (p)doped buffer layer is then providing the desired outcome for a certain thickness of (i)a-Si:H.

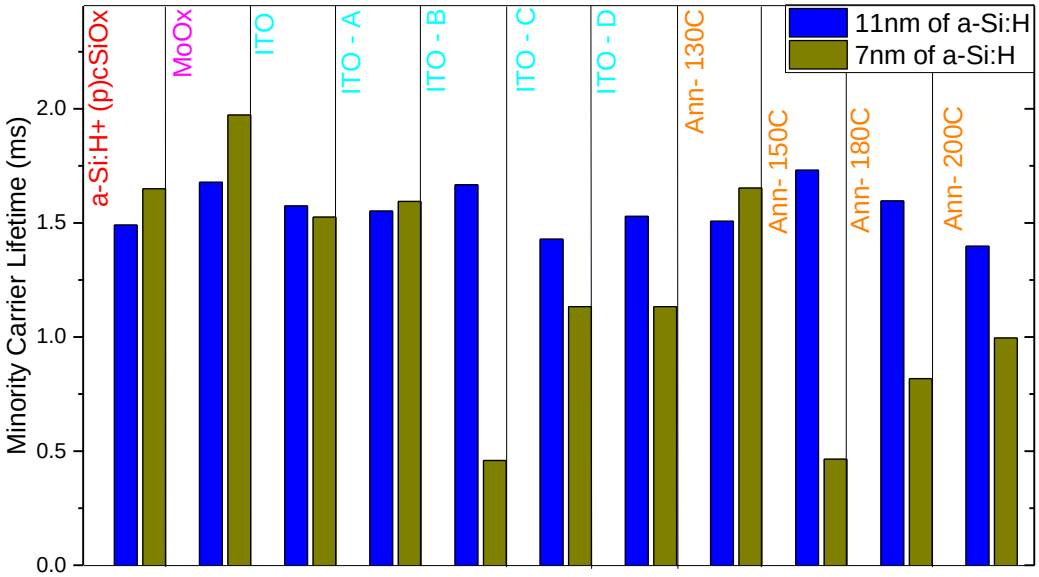


Figure 33: Comparison between two thicknesses of (i)a-Si:H followed by the deposition of 5 nm of (p)nc-SiO$_x$:H+ 10 nm of MoO$_x$ + ITO deposition followed by annealing.

4.4. Conclusions

Through this chapter, two distinct options were tested in order to reduce the sensitivity of MoO$_x$ to the temperature and attenuate the reduction of the iV$_{oc}$ and minority carrier lifetime caused by the deposition of ITO. The test showed that annealing the intrinsic layer helps for the MoO$_x$ deposition. The minority carrier lifetime and iV$_{oc}$ are not affected by the process, moreover the layer quality is uniform. Another advantage is the fact that thanks to the addition of this step, the MoO$_x$ layer is less sensitive to low-temperature annealing. While the addition of the HF solution was not providing any adjustment on the outcome. Unfortunately, pre-annealing is not helping in the attenuation of ITO deposition damages. A

major reduction in the minority carrier lifetime happens, before the ITO deposition, the value is equal to 2.62/2.67 ms while after it is equivalent to 1/1.15 ms. The iV_{oc} is also slightly affected with a value equal to 717/720 mV before ITO deposition and 705/711 mV after ITO deposition. Pre-annealing the intrinsic layer before MoO_x is helping with the temperature sensitiveness of the material but it is not providing a protection against the damages caused by ITO deposition.
Concerning the addition of (p)nc-SiO_x:H as a buffer layer, it clearly responds to the demand. The minority carrier lifetime and iV_{oc} are remaining constant and uniform through each deposition. It also restrains the MoO_x layer sensitiveness for temperature. However, (i)a-Si:H needs to be thick enough in order to still be able to provide passivation as it gets etch during the deposition of (p)nc-SiO_x:H. For a thin intrinsic layer (7 nm), damages are caused after ITO deposition with a large decrease and non-uniformity in the minority carrier lifetime (before ITO = 1.97 ms, after ITO = 1.52 ms, ITO A2 = 1.59 ms, ITO B2 = 0.46 ms, ITO C2 = 0.93 ms and ITO D2 = 1.13 ms) and iV_{oc} (before ITO = 708 mV, after ITO = 706 mV, ITO A2 = 715 mV, ITO B2 = 665 mV, ITO C2 = 698 mV and ITO D2 = 689 mV). By applying an intrinsic layer of 11 nm, it was possible to provide good passivation quality even after the deposition of ITO with an iV_{oc} of minimum 711 mV and a minority carrier lifetime equal to minimum 1.43 ms. Moreover, after ITO deposition the quarters of wafer are only slightly affected by temperature going from 130°C to 200°C, the completed wafer provided a great passivation quality. Ultimately, this option will be used as our solution for the fabrication of solar cells.

5. Integration of MoO_x on Front Surface of the Poly-SiO_x and Si-HJT

In **Chapter 3**, the characteristics of MoO_x in combination with (i)a-Si:H were investigated. The experiments showed that the stack of layers was severely affected by the deposition of ITO which is required for conductivity. In **Chapter** 4, we tested two different options to attenuate this issue and concluded that by including a (p)doped buffer layer between (i)a-Si:H and MoO_x it is possible to provide a protection for the passivation quality and prevent the deterioration caused by certain temperature and/or ITO deposition. As the outcome of the previous experience was positive, in this chapter we implement the optimized stack in the fabrication of a complete silicon-based solar cell. Furthermore, we tested different materials for the (p)doped buffer layer to examine which one should be adopted and what thickness should be applied. To obtain a fully optimized front surface, the thickness of the MoO_x layer was investigated too.
For this thesis, only the front side of silicon-based solar cells is investigated. To study the effects of the MoO_x and (p)doped buffer layer on the front surface of the solar cells, it was necessary to have good quality and stable surface passivation in combination to an electron selective contact on the rear side. This was accomplished through the deposition of SiO_2/poly-Si or (n)stack of layers on the rear surface. These types of rear side have already shown great result and have been optimized by the PVMD group [55] [61]. By having a performant and fixed rear side, any change in the photoconductance lifetime measurements will be caused by a modification made on the front surface.

5.1. Approval for the Solar Cell Fabrication

Due to the requirement of assymetrical deposition on the rear and front surface, the fabrication of the solar cell brought some challenges. Indeed the flowchart was modified accordingly.
For the rear side of the device, namely the (n)doped contact, we selected a high-temperature contact previously developed in the PVMD group which consists of 1.5 nm of SiO_2 capped with 250 nm of (n)poly-Si on a flat surface [91]. The stack of layers is providing good passivation and electrons selective contact [92]. The validity of the combination of layers for the rear surface was tested on a symmetrical sample which provided exceptional surface passivation with an iV_{oc} equivalent to 723 mV and minority carrier lifetime of 8.75 ms. By applying (n)poly-Si layers for the rear side, it gives the opportunity to completely focus on the front side and analyse any change found in the parameters knowing that it comes from any modification done on the top surface. In consistence with [92], the rear side was kept flat for the deposition of a tunnelling oxide and a poly-Si layer followed by ion implantation, annealing, oxidation and hydrogenation while the other surface required texturizing. A first experiment following the stages stated in *Flowchart 1* (*Figure 34*) was completed. However, the minority carrier lifetime after the deposition of the intrinsic (11 nm) and (p)doped buffer (3 nm) layer was not satisfactory with a minority carrier lifetime of 0.411 ms. It was necessary to find a way to combine all these steps together without affecting the quality of passivation. For this purpose, *Flowchart 2* (*Figure 34*) was designed in the hope of increasing the minority carrier lifetime after the intrinsic (11 nm) and (p)doped (3 nm) layer deposition. By modifying the organization of the flow chart, the minority carrier lifetime increased to 2.83 ms.

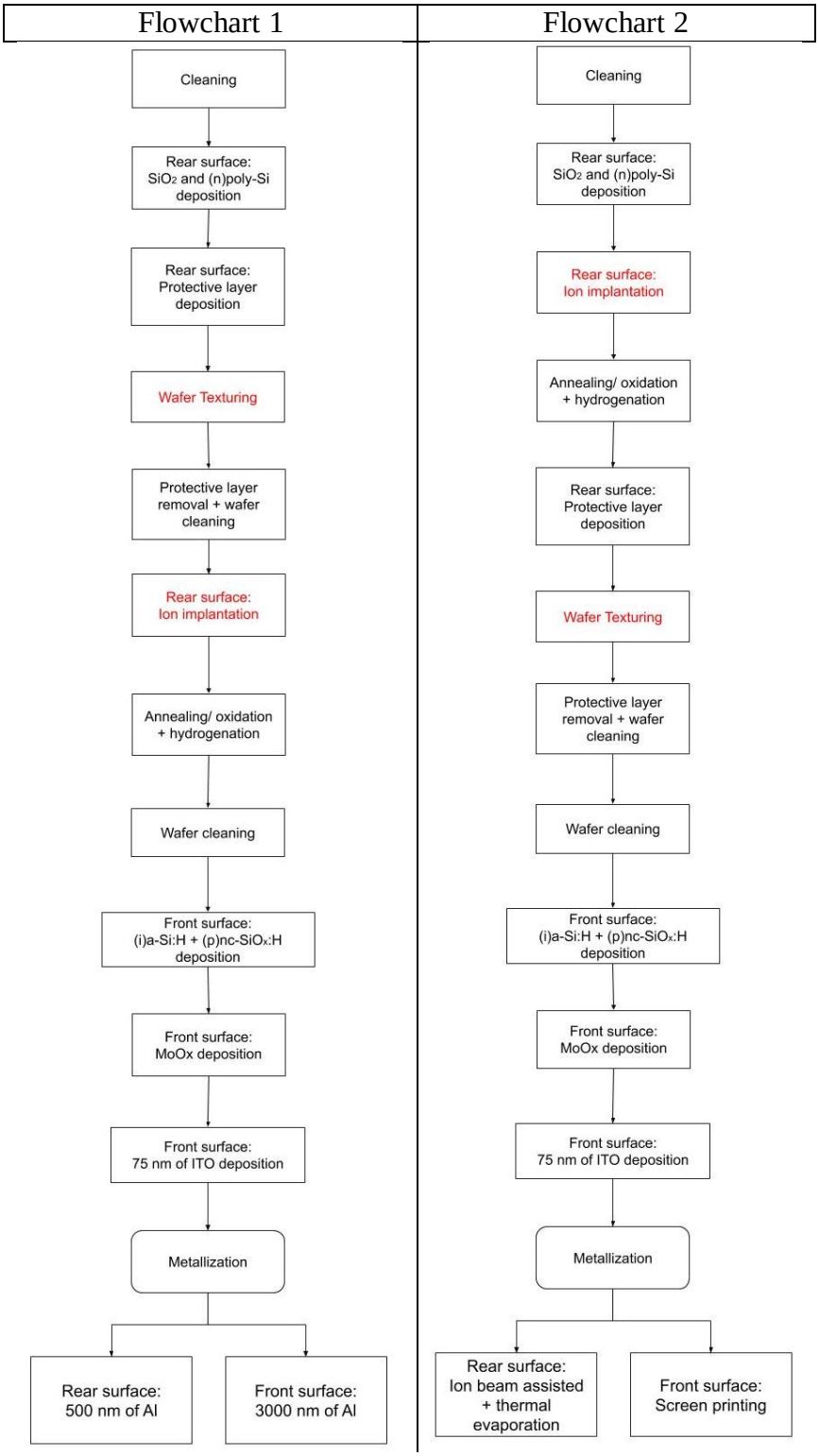


Figure 34: The applied procedure for the fowchart to combine the deposition requirement for the rear and front surfaces.

Figure 34 shows the distinct arrangement for the decisive steps while *Figure 35* illustrates the importance of the process order of the flowchart. The two flowcharts are providing a dissimilar outcome. *Flowchart 1* is characterized with a J_{sc} = 27.8 mA/cm^2, V_{oc} = 0.61V and a FF = 62.1%. While, *Flowchart 2* has a J_{sc} = 29.96 mA/cm^2, V_{oc} = 0.702V and a FF = 69.6%.

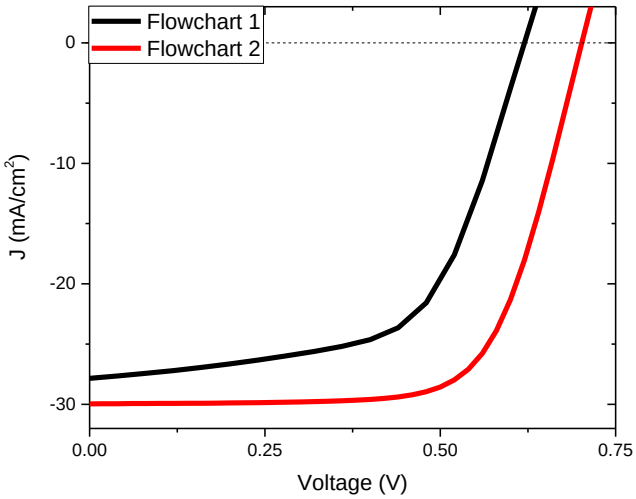


Figure 35: J-V curve for the different flowchart which combines the actions required on the rear and front surfaces

The improvement for the entire parameters in *Flowchart 2* demonstrates the importance of implementing the ion before texturing the front surface of the wafer; this procedure was then followed for the fabrication of solar cells.

5.2. Material Variation for the (p)doped Buffer Layer

5.2.1. Experimental Details

Chapter 4 showed the improvement of the passivation quality thanks to the addition of a (p)doped buffer layer between (i)a-Si:H and MoO_x. In the previous chapter only (p)nc-SiO_x:H was tested as buffer layer, while here we investigate the use of (p)doped hydrogenated nanocrystalline silicon (nc-Si:H), (p)doped hydrogenated amorphous silicon carbide (a-SiC:H) and (p)a-Si:H. Each material is tested through the fabrication of solar cells following the flowchart illustrated in *Figure 36*.

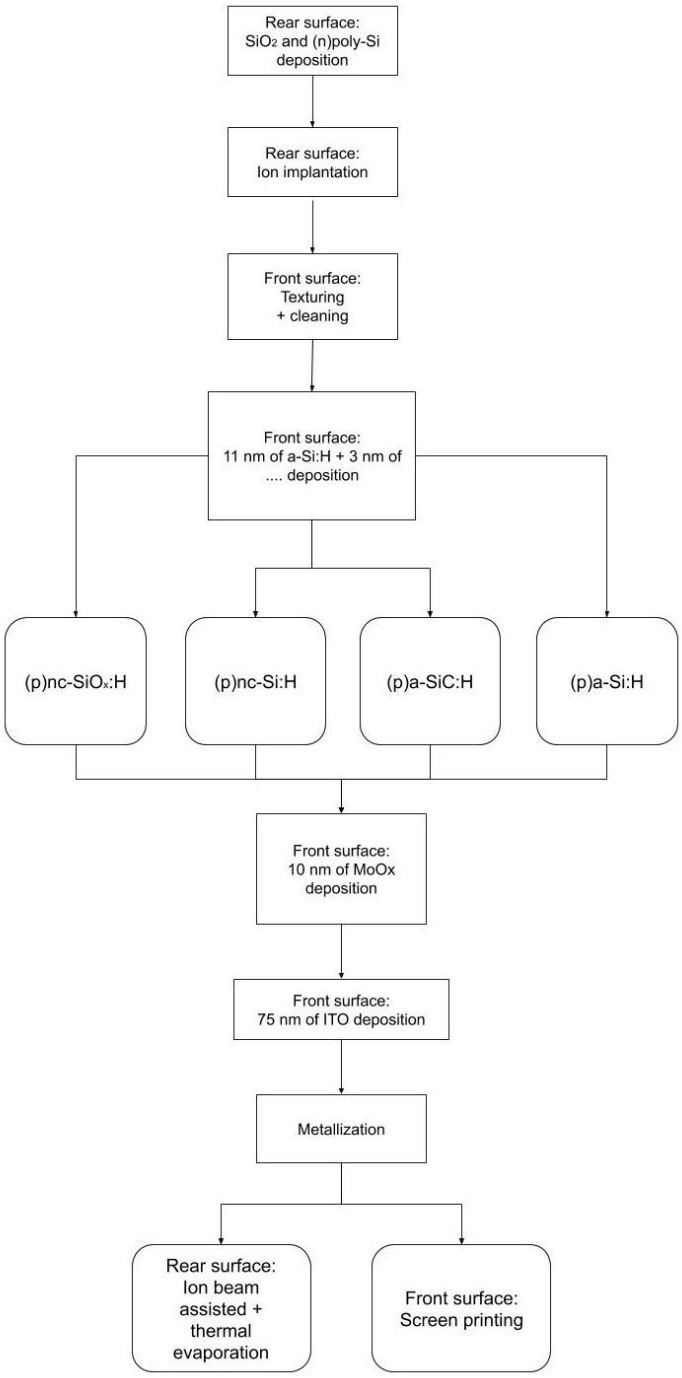


Figure 36: Diagram representing the flowchart applied for the variation of material for the (p)doped layer.

The deposition on the rear surface is done according to **Section 2.1.2** while the front surface was completed with 11 nm of (i)a-Si:H and 3 nm of (p)doped buffer layer using "Amor" PECVD (**Section 2.1.3**). The choice of the thickness for MoO_x layer was done according to **Section 3.2** but will be investigated again later in this chapter. Besides the fact that the thickness might not be optimized, the experiment should still provide an appropriate overview of which materials should be adopted for the (p)doped buffer layer.

The wafer was coated with 10 nm of MoO_x by thermal evaporation (**Section 2.1.4**) and 75 nm of ITO layer by RF magnetron sputtering (**Section 2.1.5**). The metallization on the rear side was completed through thermal and ion beam evaporation (**Section 2.1.6a**), consisting of 100 nm of Ag, 30 nm of Cr and 1 µm of Al. For the front side, metal grid was screen printed (**Section 2.1.6b**), using the design reported in *Figure 16(a)* with a cell area of 7.84 cm² and 12.5% of metal on the total area.

5.2.2. Solar Cell Results

For this section, it was decided to test various materials as buffer layers. Each of the selected materials has some advantages:

- (p)nc-SiO_x:H helps to reduce the parasitic absorption especially for the low range of wavelength. The addition of oxygen has been proven to reduce absorption losses [93]. It has been demonstrated to provide also excellent electrical properties along the layer direction due to the presence of elongated nanocrystals [94] [95]. Moreover, the material possesses a refractive index (n= 2.7 [96]) which is in between c-Si (n=3.97 [97]) and the MoO_3 (n=1.88 [98]).
- (p)nc-Si:H is characterized by low parasitic absorption and good conductivity. Its difference from the previous material is the absence of oxygen which will have an impact on the band bending. It will change the absorption and conductivity of the layer. The material has low activation energy which may facilitate the tunnelling probability and allow transport of the carriers [93]. For this material, the refractive index is equal to 3.5 [99] which is roughly similar to c-Si, so it provides a lighter gradation compared to (p)nc-SiO_x:H.
- (p)a-SiC:H is characterized by a bandgap between 1.76 and 2.2 eV which should contribute to an increase in the J_{sc} [100]. The introduction of the carbon has demonstrated to have a positive impact on the passivation quality [101]. The material posses a refractive index similar to (p)nc-SiO_x:H equal to approximately 2.3 [102].
- (p)a-Si:H is the (p)doped equivalent of the intrinsic material employed thus by combining them together we should have an excellent electrical quality as stated in [103]. For this material, the refractive index is very close to the substrate (n)c-Si and is equal to ≈3.7 [104].

It was decided, to mostly work with nanocrystalline silicon layers as they have shown better surface passivation compared to amorphous layers [93]. Additionally, all the selected materials are deposited with high hydrogen; it was shown in [105] that good crystallinity is generated with high hydrogen dilution in combination with low power density.

In order to provide the best combination for solar cells, measurements were recorded for each of the material in between each step of the fabrication. Information about the recombination is shown in *Figure 37*. This facilitates the investigation of how each material is interacting with (i)a-Si:H and MoO_x.

In *Figure 37*, it can be observed that the (p)a-SiC:H is the material interacting the best with (i)a-Si:H closely followed by (p)nc-SiO_x:H and (p)nc-Si:H while (p)a-Si:H is presenting the lowest iV_{oc}. However, the ranking of the iV_{oc} of each material changes as soon as the MoO_x is deposited with an important increase in iV_{oc} for the (p)a-Si:H. As soon as ITO is deposited, the wafer with (p)a-Si:H will be more affected than the other wafers and provides the lower iV_{oc}. For the other materials, the iV_{oc} remains roughly constant through the whole process. At the time that the solar cell is completed, a drop can be observed on the graph, this can be caused by the application of the metal which might bring some series resistance and/or the deposition could have damaged the underneath layer as it requires short annealing after the screen printing for the front surface. Additionally, the metallization for the rear side using e-beam for Al deposition employs energetic radiation that might penetrate inside the present layer modifying the atoms bond and generating defects [106]. To attenuate this potential damage thin layers of Ag and Cr were deposit before Al by thermal evaporation assuming that it will provide protection to the underneath layers but this might not be the case. To isolate the deterioration that could have been brought by the metallization in addition to the losses caused by the association of the various materials (together they represent the series resistance), the $SunsV_{oc}$ (**Section 2.2.2**) was measured. *Figure 37* shows us that the iV_{oc} classification of the different materials is remaining similar than the one measured with the solar simulator.

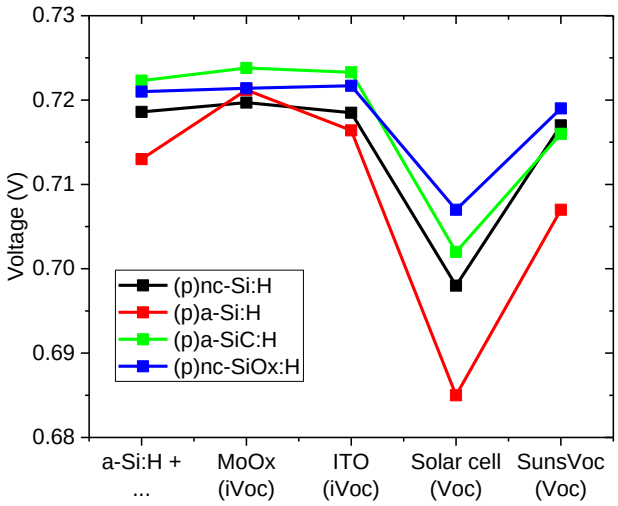


Figure 37: Variation of iV_{oc}, V_{oc} and $SunsV_{oc}$ dependent on the (p)doped buffer layer for hybrid MoO_x/ silicon-based solar cells.

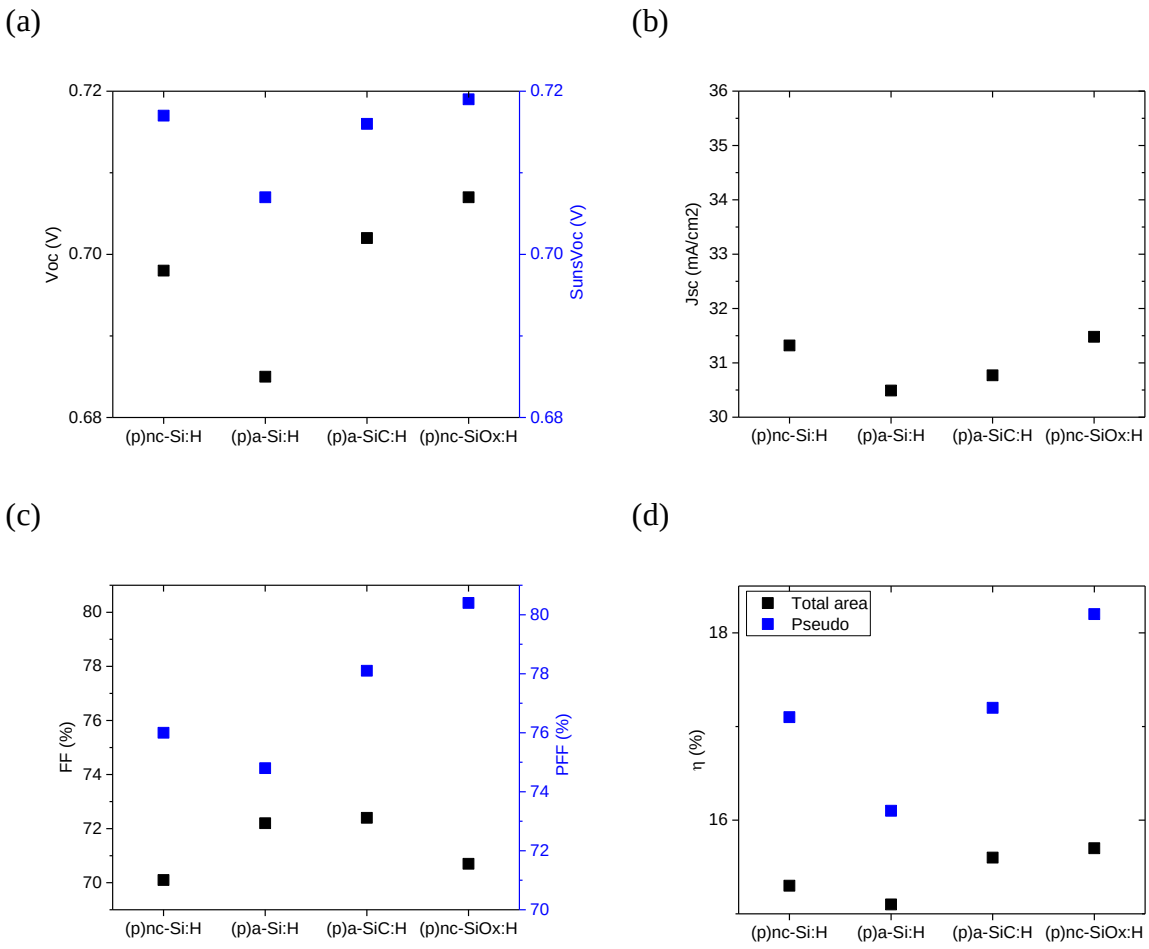


Figure 38: (a) V_{oc}, $SunV_{oc}$ (b) J_{sc} (c) FF, PFF and (d) η (total and pseudo) for various (p)doped buffer layer for hybrid MoO_x/ silicon-based solar cells.

Figure 38 shows the solar cell's parameters using various material. The graphs also demonstrate the superiority of crystallised layers compared to amorphous even after the inclusion of carbon which increased the V_{oc} and J_{sc} compared to (p)a-Si:H as projected by *Tawada et al*. in [100]. Firstly, *Figure 38(a)* shows that (p)nc-SiO_x:H buffer layer gives the highest open-circuit voltage, indeed, by adding oxygen

to the (p)nc-Si:H to form (p)nc-SiO_x:H, fewer recombinations are experienced which increases the V_{oc}. Moreover, (p)nc-SiO_x:H provides the best J_{sc} thanks to its transparency as shown in *Figure 38(b)*. The fact that J_{sc} (*Figure 38(b)*) is higher for (p)nc-SiO_x:H than for the other solar cells could be explained by the fact that the (p)nc-SiO_x:H is generating more collectable carriers at lower wavelength (280 nm to 440 nm [93]). Concerning the low J_{sc} for (p)a-Si:H, it is related to the absorption coefficient of the layer which was already demonstrated in *Figure 8*.
In *Figure 38(c),* the fill factor shows a preference for the amorphous material while the pseudo FF (PFF) which provides a measurement excluding the series resistance exhibits completely different results. The solar cell made with (p)nc-SiO_x:H is showing the best PFF, efficiency for the total area and pseudo efficiency. *Figure 38(d)* displays two different efficiencies, the pseudo represents the efficiency excluding the series resistance which demonstrates the superiority of (p)nc-SiO_x:H (18.2%) followed by (p)a-SiC:H (17.2%) and (p)nc-Si:H (17.1%). The total area efficiency represents the efficiency measured with a solar simulator, this one provides the same trends as the pseudo efficiency; only with a lower deviation between the efficiencies: (p)nc-SiO_x:H (15.7%), (p)a-SiC:H (15.6%), (p)nc-Si:H (15.3%) and (p)a-Si:H (15.1%). We observe that the two favourite materials are the ones providing a gradual refractive index between the (n)c-Si and the MoO_x.
For the SunV_{oc} (*Figure 38(a)*), each solar cells are equally affected by the series resistance (R_s) for the V_{oc}, while this is not the case for the PFF(*Figure 38(c)*),. The fact that the V_{oc} on each solar cell is equally affected by the resistance is explained in [107] for the reason that there is no current flowing when these measurements are taken. However, the fill factor is dependent on the maximum power point (MPP) which is dependent on the current. According to *Leilaeioun* [107], the reduction in MPP can be caused by the inability of the stack of layers to provide holes selective contact; this one should then be kept minimal. The series resistance is calculated in accordance with **Section 2.2.3a** and reported in *Figure 39*.

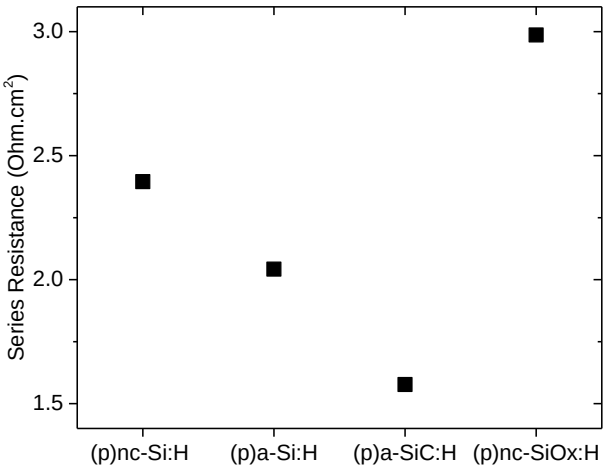


Figure 39: Series resistance for various materials of (p)doped layer for hybrid MoO_x/ silicon-based HIT solar cells.

Figure 39 shows that the largest series resistance is produced by (p)nc-SiO_x:H (R_s = 2.99 ohm.cm^2) followed by (p)nc-Si:H (R_s = 2.39 ohm.cm^2) and (p)a-Si:H (R_s = 2.04 ohm.cm^2) while the (p)a-SiC:H (R_s = 1.58 ohm.cm^2) has the lowest series resistance. Even with the large R_s, (p)nc-SiO_x:H still achieves the best performance (η_{total} = 15.7%) as illustrated in *Figure 38(d)*, tightly followed by (p)a-SiC:H (η_{total} = 15.6%).
Figure 40(a) exhibits the parameters that have been discussed above. It can be observed that the J-V curve of each material is showing acceptable results with a preference for the FF of the (p)nc-SiO_x:H layer. Yet when we increase the scale of the x-axis (*Figure 40(b)*), a S-shape arises on the J-V curve. The display of this S-shape could be caused by a hole-blocking behaviour [21].

(a) (b)

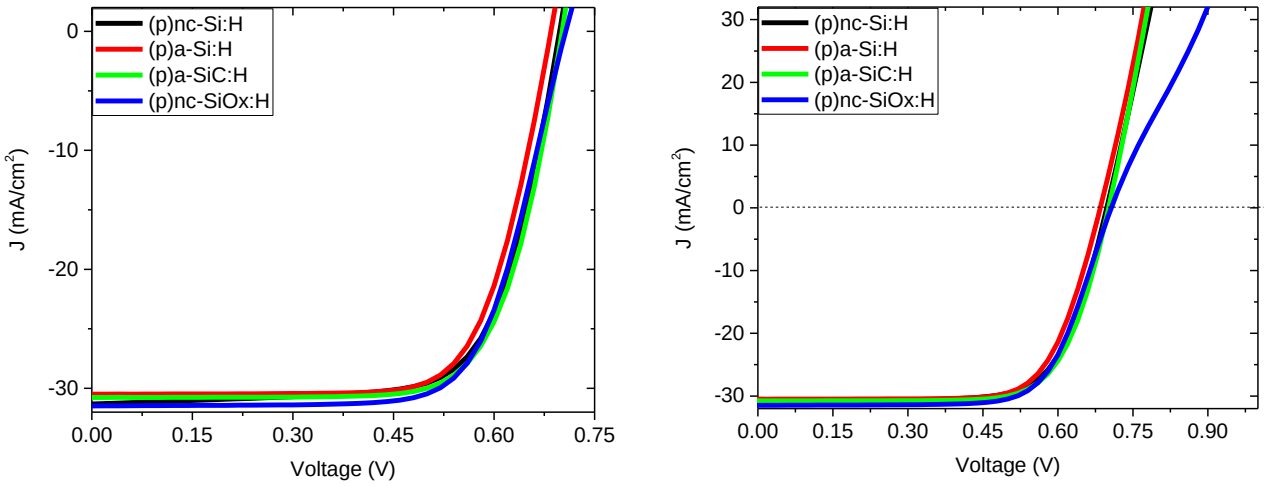


Figure 40: J-V curve for various materials of (p)doped layer for hybrid MoO_x/ silicon-based HIT solar cells (a) from 0 V to V_{oc} (b) from 0 V to 1 V.

This type of curvature was already observed in different papers [31], [42] and [108]. Despite all the investigations, the origin of it is still not fully understood; but it is usually related to an obstruction in the hole extraction caused by a band offset/ Schottky barrier.

Table 5 exhibits the V_{oc}, J_{sc}, FF and efficiency for each material. From this table, it can be declared that the best efficiency is reached by using (p)nc-SiO_x:H (15.7%) as the (p)doped buffer layer closely followed by (p)a-SiC:H (15.6%), (p)nc-Si:H (15.3%) and (p)a-Si:H (15.1%).

Table 5: Parameters for various materials of (p)doped layer for hybrid MoO_x/ silicon-based solar cells.

3 nm of …	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	η (%)
(p)nc-Si:H	698	31.32	70.1	15.3
(p)a-Si:H	685	30.49	72.2	15.1
(p)a-SiC:H	702	30.77	72.4	15.6
(p)nc-SiO_x:H	707	31.48	70.7	15.7

Even with the presence of the S-shape, it was decided to continue the further experiments with (p)nc-SiO_x:H as it provided the best result.

5.3. Variation on the Thickness of (p)doped Buffer Layer

In the attempt to increase the performance of the solar cells and attenuate the presence of the S-shape, a more advanced PECVD equipment (“Amigo”) was tested for the next deposition. “Amigo” provides treatments using hydrogen plasma treatments in between depositions and high-frequency layers which might help the nanocrystal growth and improve the passivation quality of the (i)a-Si:H layer.

5.3.1. Experimental Details

Figure 41 provides a simplified diagram of the step applied to the wafers in order to fabricate solar cells.

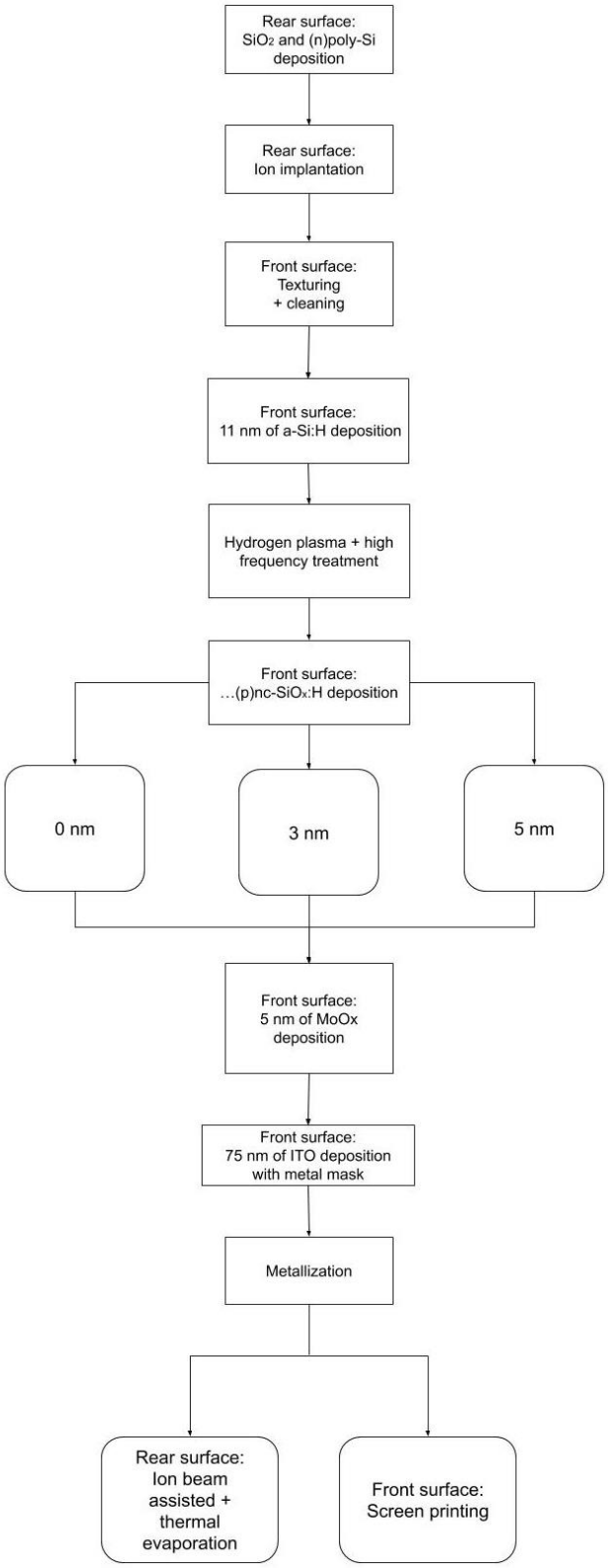


Figure 41: Diagram representing the flowchart applied for the variation on the thickness of the (p)doped buffer layer for hybrid MoO_x/ silicon-based solar cells.

To start with, the same rear side as previously was employed as reported in **Section 2.1.2**. The front surface was then texturized and cleaned (**Section 2.1.1**). The main difference compared to the previous sections is the fact that a more advanced equipment for the (i) and (p)doped layers deposition was employed. It consisted of a different PECVD called “Amigo” (**Section 2.1.3**). The cells are completed by the deposition of 5 nm of MoO_x and 75 nm of ITO on the front surface. The thickness of MoO_x was changed from **Section 5.2** as an experiment made in between this period of time demonstrated that it could be

reduced to 5 nm. The results from this experiment are not presented in this thesis as **Section 5.4** will provide the same kind of investigation but for more advanced solar cells.
Moreover, to reduce the series resistance and grid metal coverage, we used a new design for screen printing (*Figure 16(b)*) for the front surface. To isolate each cell present on the wafer without having to cut them, a metal mask was applied during the ITO deposition. The metal grid design provides 8 cells per wafer with metal coverage of 4.4% or 7.7%.
Concerning the rear metallization, the full surface was coated with 100 nm of Ag, 30 nm of Cr and 1 µm of Al.

5.3.2. Solar Cell Results

This section will investigate if there is a possibility to improve the outcome by modifying the thickness of (p)nc-SiO_x:H.
Figure 42 illustrates the variation of parameters for distinct thicknesses of (p)nc-SiO_x:H. The squares on each graph are representing the average of the 4 cells having the same non-active area represented in *Figure 16(b)* in addition to their standard deviation.

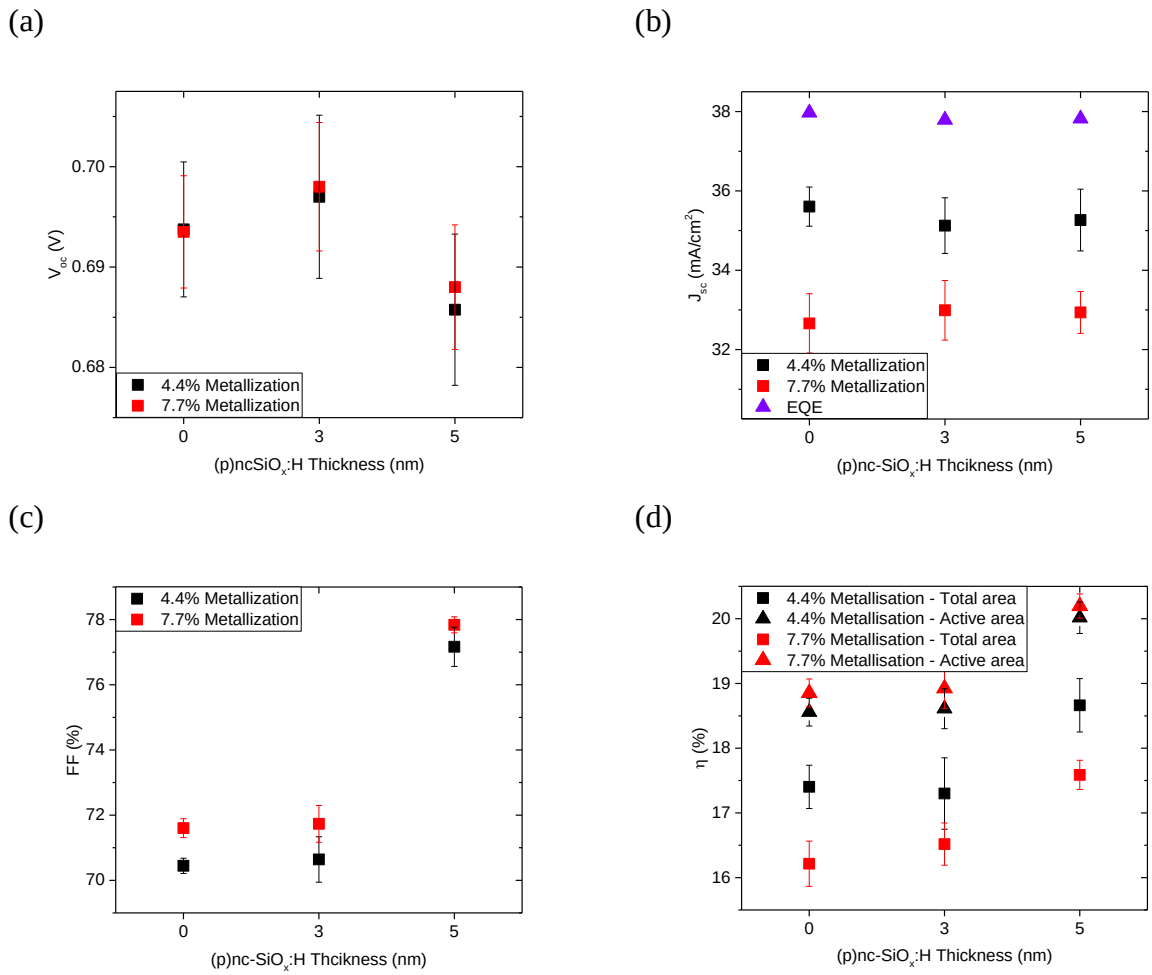


Figure 42:(a) V_{oc}, (b) J_{sc}, $J_{sc,\,EQE}$, (c) FF and (d) η (total and active) for hybrid MoO_x/ silicon-based solar cells with various (p)doped buffer layer thicknesses.

Figure 42(a) shows the dependence of V_{oc} on the thickness of the (p)doped buffer layer generating a band offset as demonstrated later in *Figure 46*. The 3 nm of (p)nc-SiO_x:H will provide a good band offset to reduce the recombination. *Figure 42(a)* demonstrates the gain in V_{oc} with the addition of the (p)doped buffer layer, however, this one should be kept thin as V_{oc} decreases when the thickness is enlarged to 5 nm. The V_{oc} gives an overview of the recombination however it does not allow to interpret where these recombination are occurring. Concerning the J_{sc} (*Figure 42(b)*), the parameter is not affected by the difference in thicknesses as it remains roughly constant. However, J_{sc} (*Figure 42(b)*) is sufficiently affected

by the difference in the percentage of metallisation present on the surface as it will contribute to the shading, it is then preferable to limit the metal coverage. On the other hand, the metallization will also slightly influence the fill factor (*Figure 42(c)*), this can be observed through the deviation between the black and red square for each thickness of the (p)doped buffer layer. The percentage of metallization on the total area plays a role in the electrical properties, especially in the series resistance. The consequences are more important for J_{sc}. It is then preferable to keep the metallization to 4.4% of the total area. The FF is further affected by the thickness of the (p)doped buffer layer. Indeed, we observe in *Figure 42(c)* that it is possible to reach a FF of 78% by applying a thickness of 5 nm for the (p)doped buffer layer. As a consequence of its superiority in the fill factor, the efficiency of the solar cell with 5 nm of (p)nc-SiO_x:H attains an average of 18.66% for the total area. By reducing the thickness of the (p)doped buffer layer to 3 nm, the average efficiency is decreasing to 17.68% and is comparable to the solar cells without (p)doped buffer layer. *Figure 42(d)* provides the efficiency of the total and active area. We observe that the total efficiency is larger for solar cells having a metal grid covering only 4.4% of the total area, while the active efficiency represents the efficiency without any metallization. The parameter is calculated thanks to *equation 4* and is dependent on the J_{sc} recorded with the solar simulator. In the way that the solar cells with similar (p)doped buffer layer thickness are coming from a unique wafer, it was expected that the active efficiency will be equal for both designs which is approximately the case as demonstrated in *Figure 42(d)*. *Figure 43* provides the EQE of each solar cell, we observe that increasing the thickness of the (p)doped buffer layer from 0 nm to 5 nm will not affect the transparency of the layer as the EQE remains almost unchanged.

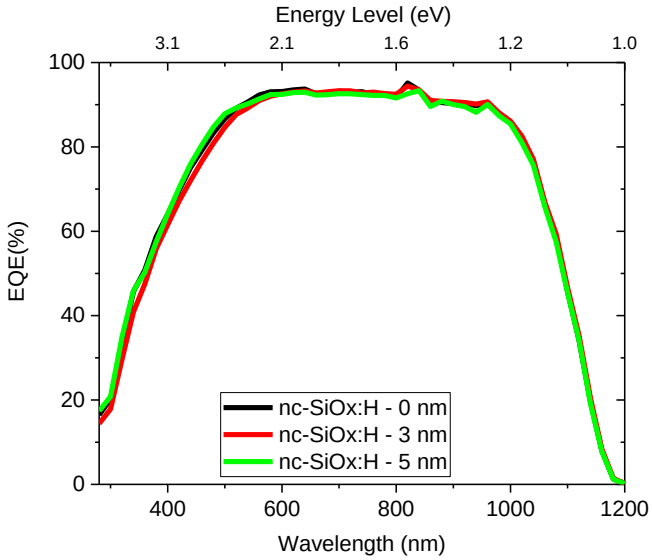


Figure 43: External Quantum Efficiency vs wavelength for hybrid MoO_x/ silicon-based solar cells with a variation of the thicknessfor the (p)doped buffer layer.

Figure 44 gives us the J-V of the solar cells and it can clearly be observed that the thinner layers are strongly affected by the S-shape. The thickness of 5 nm for (p)nc-SiO_x:H layer is providing a perfect width for the right amount of carriers to tunnel through the barrier which will not overwhelm the carrier transport and generates the S-shape.

(a) (b)

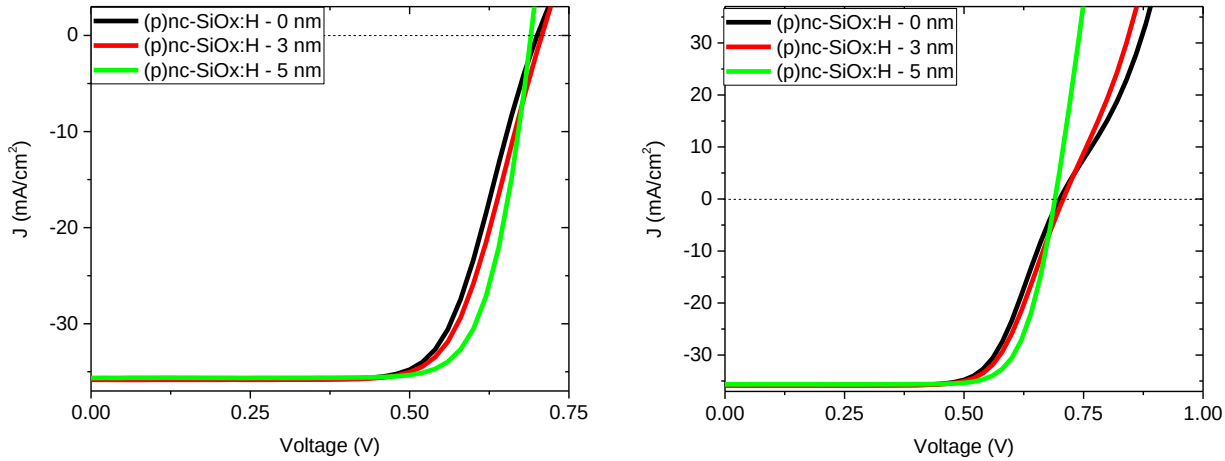


Figure 44: J-V curve dependent on the (p)doped buffer layer thickness for hybrid MoO_x/ silicon-based solar cells (a) from 0 V to V_{oc} (b) from 0 V to 1 V.

To understand better what is happening inside, some solar cells made according to *Figure 36* with a (p)doped buffer layer of 0 and 8 nm of (p)nc-SiO_x:H were heated at various temperatures when measurements were taken. The first measurement started at the standard test condition (STC), the requirements are very specific with a temperature of the solar cell equal to 25°C, a total irradiance of 1000 Watts/m^2 and a mass of the air equivalent to 1.5 [1]. Measurements were then taken with the solar simulator decreasing the temperature of the trunk from 50°C to 15°C. *Figure 45* represents how solar cells behave when receiving thermal energy.

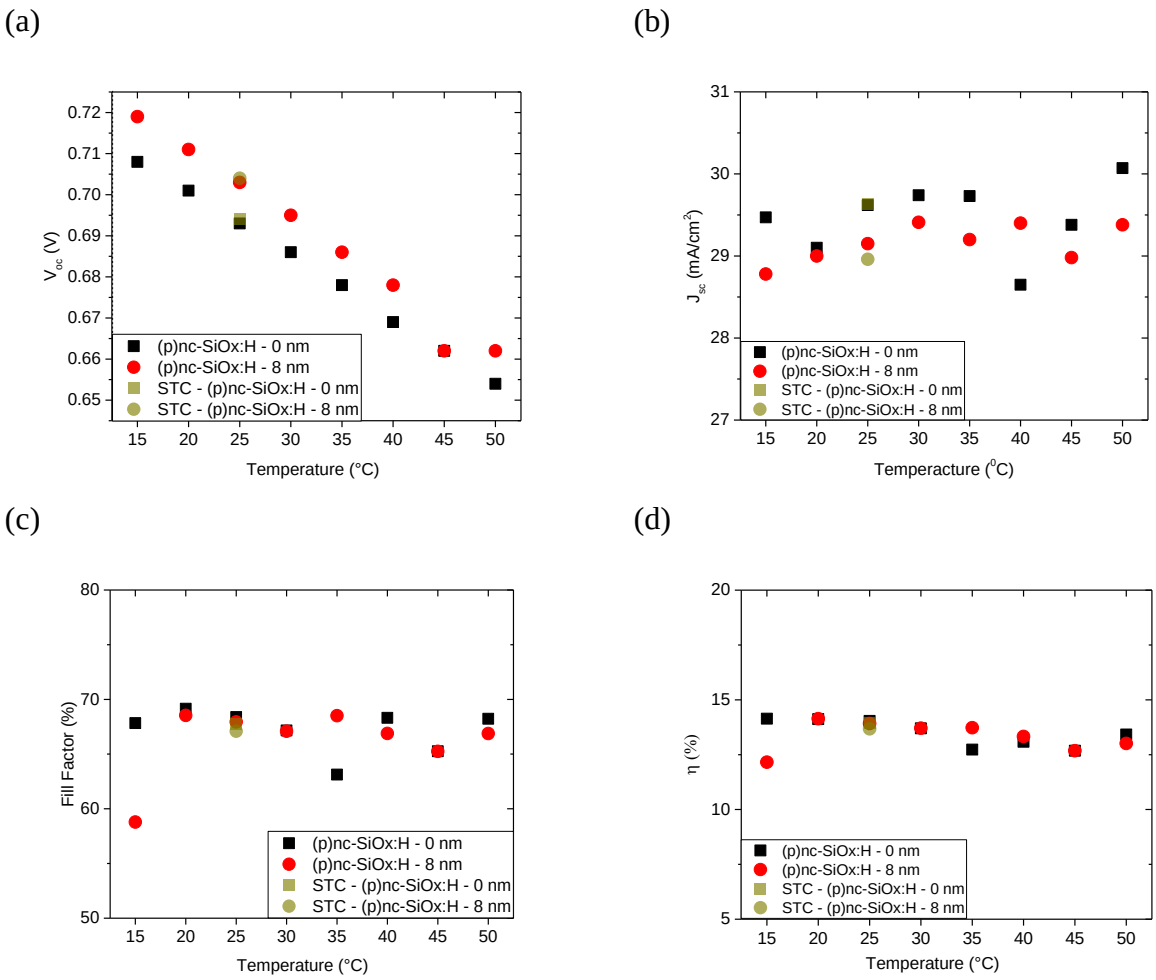


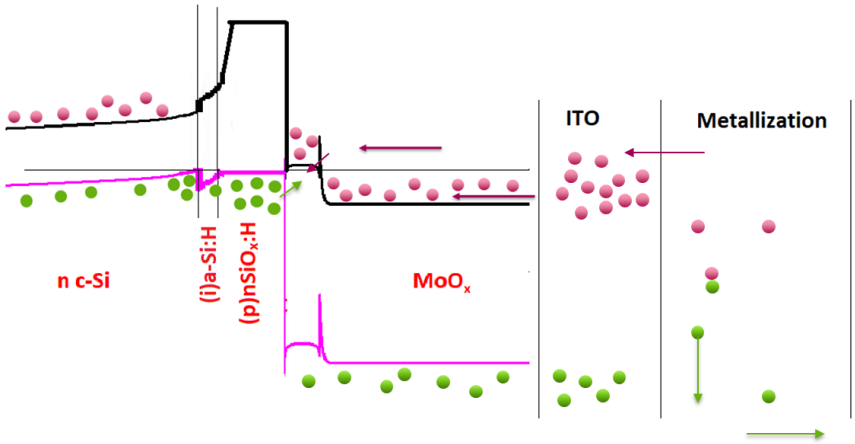
Figure 45: (a) V_{oc}, (b)J_{sc}, (c) FF and (d)η response to temperature change for solar cells with distinct (p)doped buffer layer thickness for hybrid MoO_x/ silicon-based solar cells made according to Figure 36.

Figure 45(a) demonstrated that a thicker (p)doped buffer layer is providing a wide barrier for the electrons present in the conduction band of the (n)c-Si as illustrated in *Figure 46*. This will then reduce the recombination and increase the V_{oc}. Yet, *Figure 45(d)* shows that the efficiency is similar for both thicknesses which might be due to an equilibrium of the difference in V_{oc} with the decrease of the J_{sc} for thicker layer. Indeed, *Figure 45(b)* shows that the layer with 8 nm of (p)nc-SiO_x will absorb more of the light hitting the surface. The theory can be confirmed thanks to *Figure 43* which shows the same behaviours but with lower intensity as the difference in thickness is minim.

The dependence of the parameters due to the temperature is similar for both thicknesses. The V_{oc} (*Figure 45(a)*) is decreasing when intensifying the temperature while the fill factor (*Figure* 45(*c*)) and the efficiency (*Figure 45(d)*) are remaining roughly constant. Concerning the V_{oc} at high-temperature, recombination increases which provides a lower V_{oc}, for both solar cells. Significant carrier lifetime change is happening at (n)c-Si/ (i)a-Si:H interface due to temperature as demonstrated by *Vasudevan et al.* in [109]. For the solar cell having a (p)doped buffer layer of 8 nm, it is difficult to draw any conclusion as there is no change in the efficiency through the temperature dependence. Some speculations were done about the electrons from the (n)c-Si conduction band receiving enough thermal energy to tunnel the wide (p)doped buffer layer for higher temperature ; which increases the recombination without changing the efficiency

In order to help the reader's understanding, a simplified diagram with our speculations about the carrier transport is represented in *Figure 46*, that illustrates the conditions at STC.

(a)



(b)

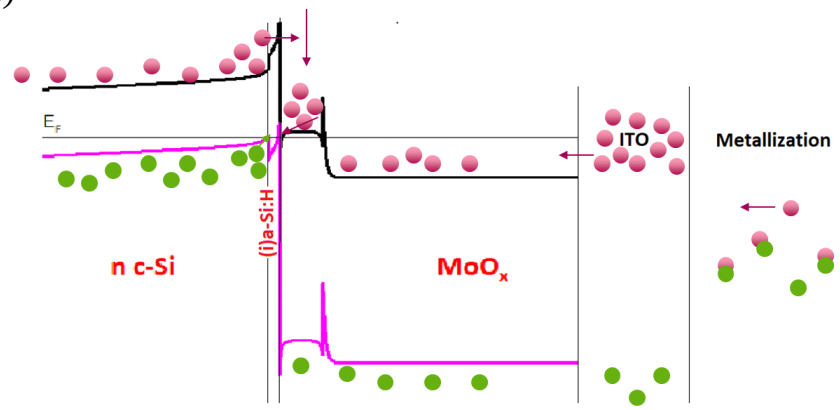


Figure 46: Simplified band diagram with the carriers transport of the front surface of the fabricated solar cell made of (a) (n)c-Si/(i)a-Si:H/ thick (p)nc-SiO_x:H/MoO_x/ITO/metallization and (b) (n)c-Si/(i)a-Si:H/MoO_x/ITO/metallization

Figure 45 demonstrated that the difference in recombination according to the temperature does not have a particular effect on the efficiency of both solar cells with distinct (p)doped buffer layer. On the other hand, this variation in recombination will have an effect on the intensity of the S-shape curvature in the J-V curve for the solar cell made with 8 nm of (p)doped buffer layer as shown in *Figure 47*.

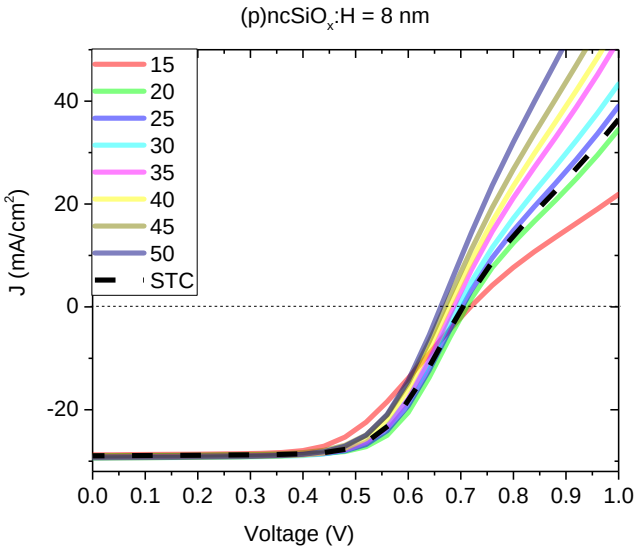


Figure 47: Intensity of the S-shape curvature dependent on the temperature variation for hybrid MoO_x/ silicon-based solar cells characterized by a (p)doped buffer layer of 8 nm.

Through the outcome of this experiment and *Figure 47*, we came with the theory that the (p)doped buffer layer is bringing an excess of carrier too important for the system to be handled. The transport of the carrier is then disrupted which generates an S-shape. Nevertheless, as soon as the temperature is increased, more recombination are occurring which are helping to reduce the excess of carrier and improve their transport. This leads to an attenuation of the S-shape intensity.
This is not the first time we face the presence of the S-shape. The curvature was already identified in **Section 5.2.2** and has been explained as a cause of carriers transport. The S-shape was also experienced in [21] where they interpreted the appearance of this type of curvature as a band mismatch between the MoO_x and TCO layers. A different type of TCO was then tested on the front side. It consisted of hydrogenated fluorine-doped indium oxide (IFO:H). It differs from ITO by its largest optical bandgap which is equal to 3.85 eV. More details about the deposition conditions can be found in (**Section 2.1.5**).

(a) (b)

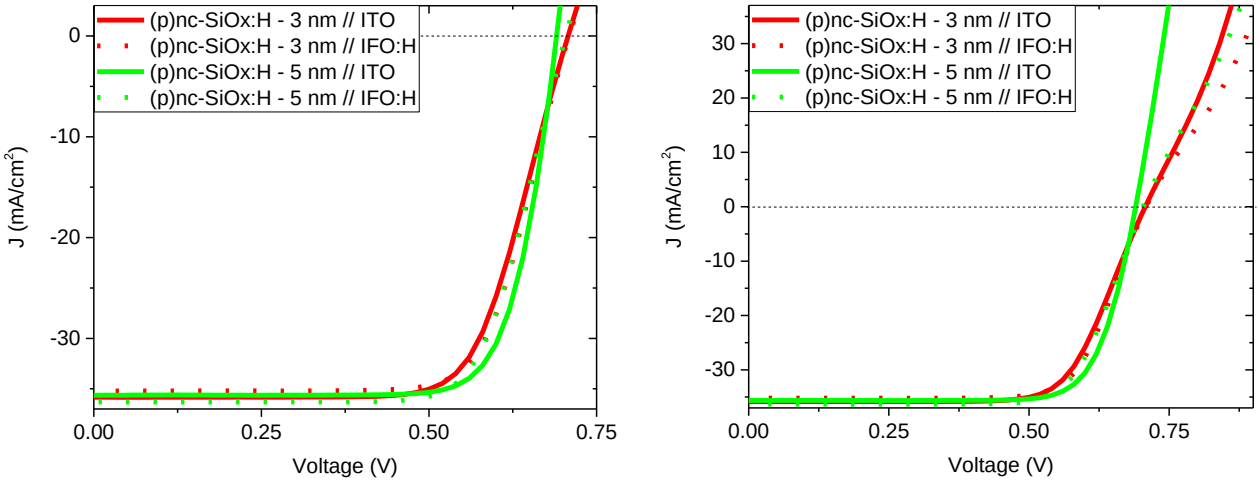


Figure 48: J-V curve for 3 and 5 nm of (p)nc-SiO_x:H for hybrid MoO_x/ silicon-based solar cells having IFO:H (a) from 0 V to V_{oc} (b) from 0 V to 1 V.

Figure 48(a) shows the comparison of the most performant solar cells on each wafer featuring ITO and IFO:H on the front side. Also the (p)nc-SiOx:H buffer layer is varied in thickness. For the layer of 3 nm the

change helps to increase the J_{sc} and FF. However, *Figure 48(b)* proves that it is not a good idea to substitute for IFO:H as this one intensifies the presence of the S-shape.
Table 6 provides the V_{oc}, J_{sc}, FF and η of the solar cells represented in *Figure 44* and *Figure 48*. These are the best solar cells present on each wafer. It can be noticed that they are corresponding to DIE1 or DIE3 (***Figure 16****(b)*), both of these DIEs have an area with 4.4% of metal on the total area. *Table 6* shows that the best solar cells are providing great results especially thanks to the large V_{oc}; however, the FF is reasonably small, excluding the solar cell highlighted in green. The solar cell made with 5 nm of (p)nc-SiO_x:H with ITO on the top has a smaller V_{oc} but provides a FF of 77.29% which increased the efficiency to 19.01%. Concerning the J_{sc}, this one remained roughly constant through the different thicknesses of (p)doped buffer layer.

Table 6: Parameters for hybrid MoO_x/ silicon-based solar cells cells with a variation in the thickness for the(p)doped buffer layer made of (p)nc-SiO_x:H.

(p)nc-SiO_x:H thickness (nm)	TCO	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	DIE
0	ITO	700	35.79	70.57	17.68	1
3	ITO	707	35.84	71.31	18.08	3
	IFO:H	709	35.21	72.97	18.21	3
5	ITO	690	35.64	77.29	19.01	1
	IFO:H	704	36.31	70.57	17.68	1

In conclusion, this section showed the great performance of 5 nm of (p)nc-SiO_x:H with a total efficiency of 19.01%, yet the V_{oc} can still be increased as now it is only equal to 690 mV.
This experiment was done on our last batch of cells, so the results were not taken into account in **Section 5.4**.

5.4. Variation on the thickness for the MoO_x Layer

5.4.1. Experimental Details

The goal of this experiment was to find the right thickness of MoO_x layer in order to fabricate the most efficient solar cell. *Figure 49* provides a simplified diagram of the flowchart employed for this experiment in order to convert wafers into performant solar cells.

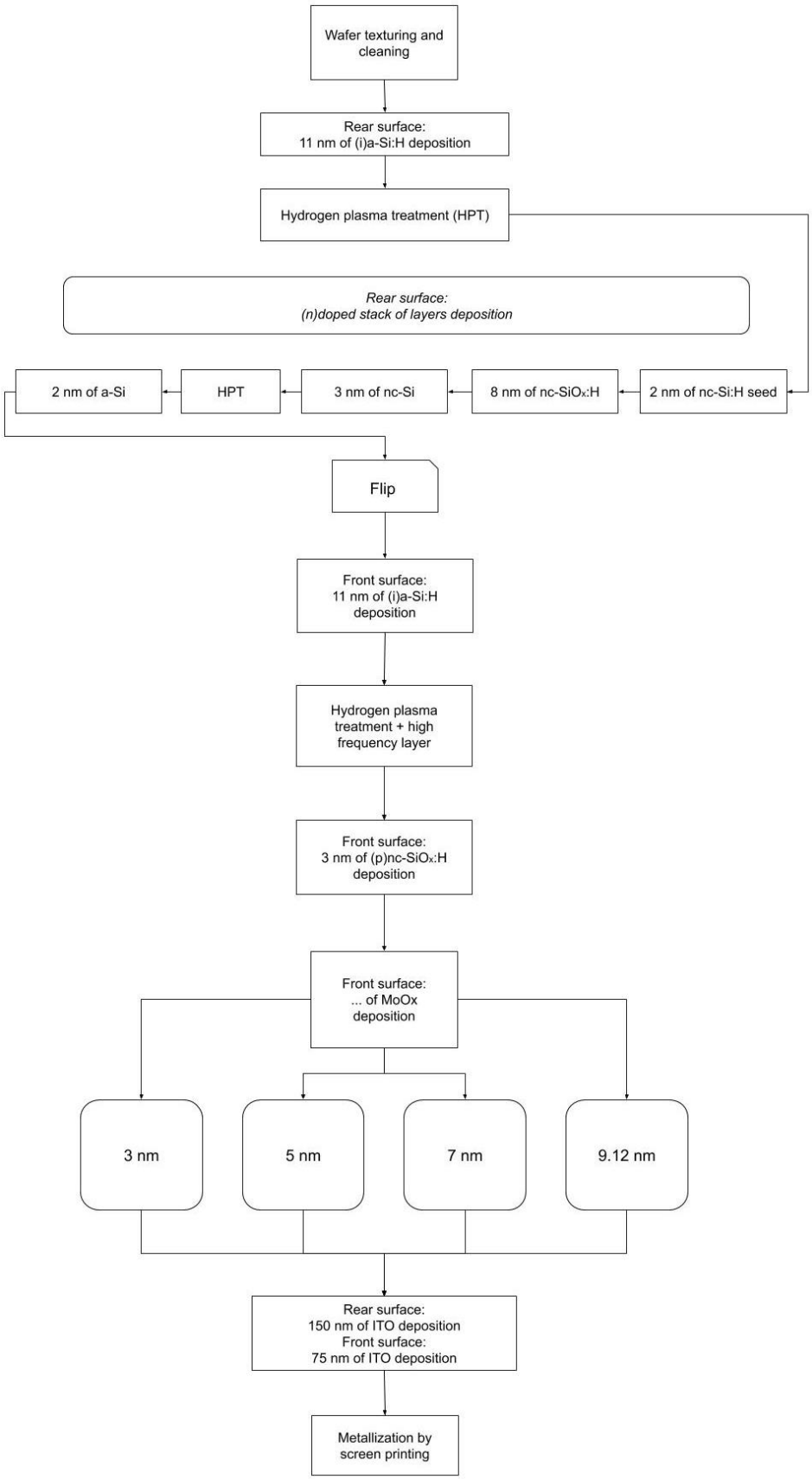


Figure 49: *Diagram representing the flowchart used for the variation on the MoO_x thickness for hybrid MoO_x/ silicon-based HIT solar cells.*

For this experiment, both surfaces of the wafer were textured while the previously used SiO_x/poly-Si as (n)contact; here it was replaced by (i)a-Si:H and an (n)doped stack of layers which were deposit through "Amigo" PECVD (**Section 2.1.3**). After depositing the (i)/(n) stack, the wafer was flipped and the front side

of the wafer was coated with 9 nm of (i)a-Si:H and a thin buffer (3 nm) (p)nc-SiO_x:H layer with the application of hydrogen plasma treatments in between depositions and high-frequency layers. In this thesis, no advanced information about the deposition done on the rear surface is given as it was not the subject of the project, the recipe was optimized and given by Y. Zhao (PhD in the PVMD group of TU Delft [61]).
Unfortunately, this experiment did not take into account the result from **Section 5.3**. Indeed, here thickness of 3 nm of (p)nc-SiO_x:H was applied instead of the optimized one (5 nm) due to the fact that both experiments were done at the same time so they were based on previous results done on less performant solar cells which were showing a different optimized thickness. However, the outcome of these solar cells are not presented in this thesis.
For this experiment, we screen printed both front and rear contacts (*Figure 16(b)*) obtaining cells with an area of 3.92 cm^2. Metal masks were used to define the cell area during the ITO deposition.

5.4.2. Solar Cell Results

The first step was to verify that the addition of MoO_x layer will undeniably increase the performance of the solar cells; then investigate the limit of the MoO_x layer thickness to not deteriorate the efficiency.

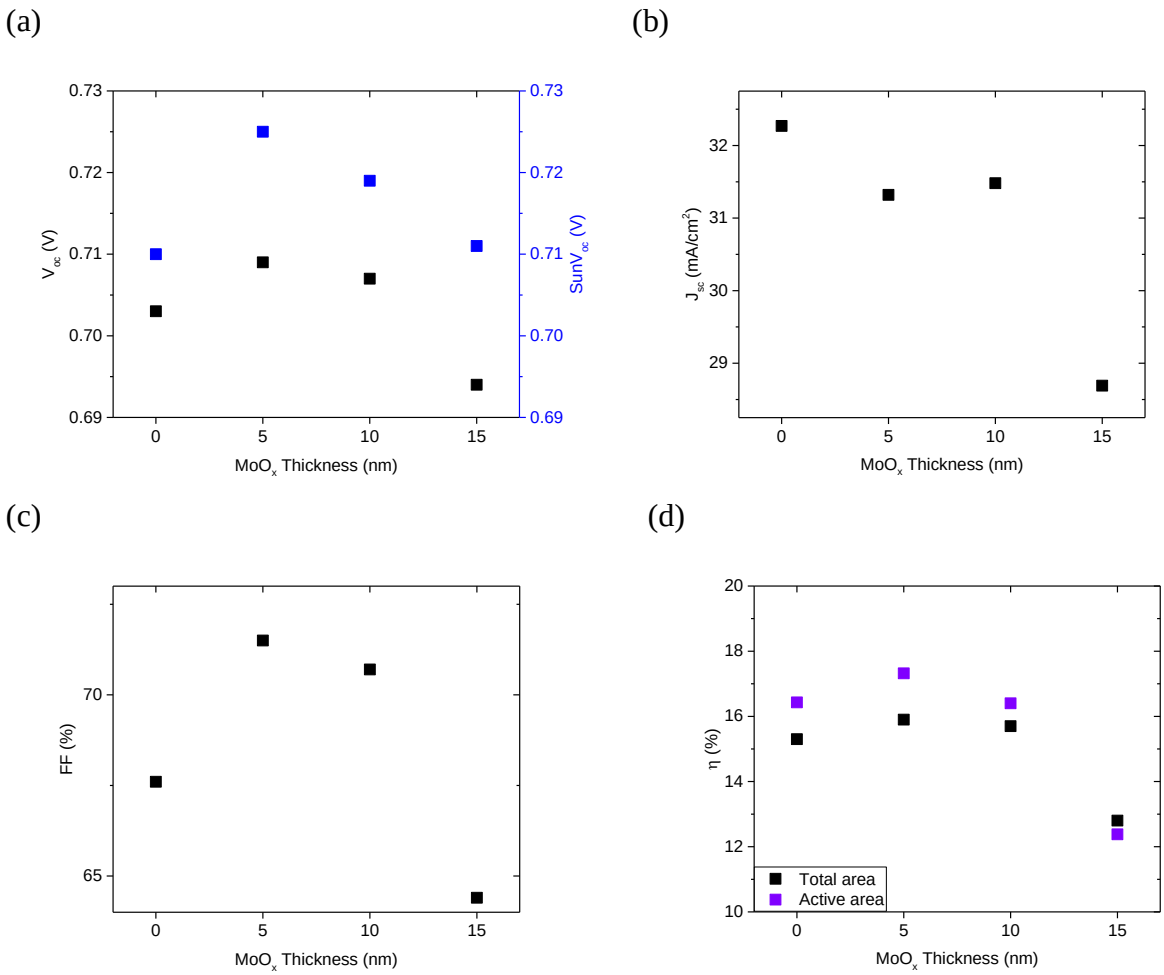


Figure 50: (a) V_{oc}, SunV_{oc} and (b) J_{sc} (c) FF, PFF and (d) total and active efficiency with various MoO_x thicknesses for hybrid MoO_x/ silicon-based solar cells made according to Figure 36.

Figure 50 demonstrates the usefulness of MoO_x on solar cells fabricated according to *Figure 36* with a front side made of 11 nm of (i)a-Si:H/ 3 nm of (p)nc-SiO_x:H and various thickness of MoO_x. *Figure 50(a), (c) and (d)* are showing a similar trend with an increase in the parameters as soon as a layer of 5 nm of MoO_x is introduced. The improvement of the solar cell performance is due to the fact that MoO_x acts as a barrier through a band offset as shown in *Figure 7* which provides a hole selective contact. The 5 nm of MoO_x looks like the optimized thickness, indeed when a thicker layer is applied, V_{oc}, SunV_{oc}, FF and both efficiencies are decreasing. *Figure 50(b)* demonstrates that the addition of a thin MoO_x layer will only

slightly affect the J_{sc} as MoO_x is relatively transparent. For a thicker layer (15 nm of MoO_x) more important optical losses appear.
Moreover, the addition of the MoO_x layer helps to reduce the series resistance (*Figure 51*) which is relatively high when the (p)doped layer is directly in contact with ITO. As soon as the MoO_x layer is introduced, the series resistance drops followed by a linear rise for thicker MoO_x layer.

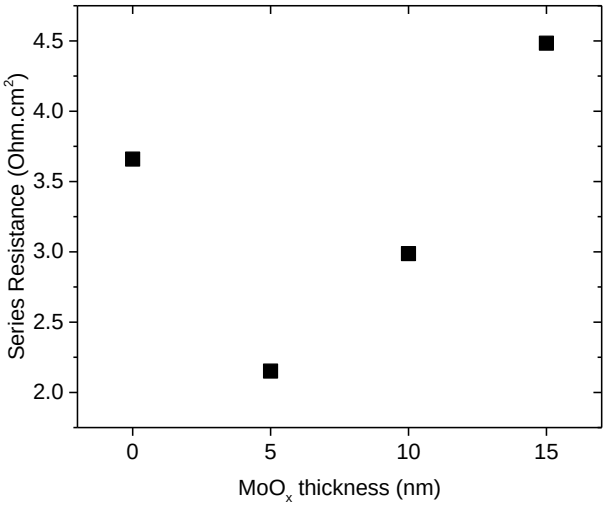
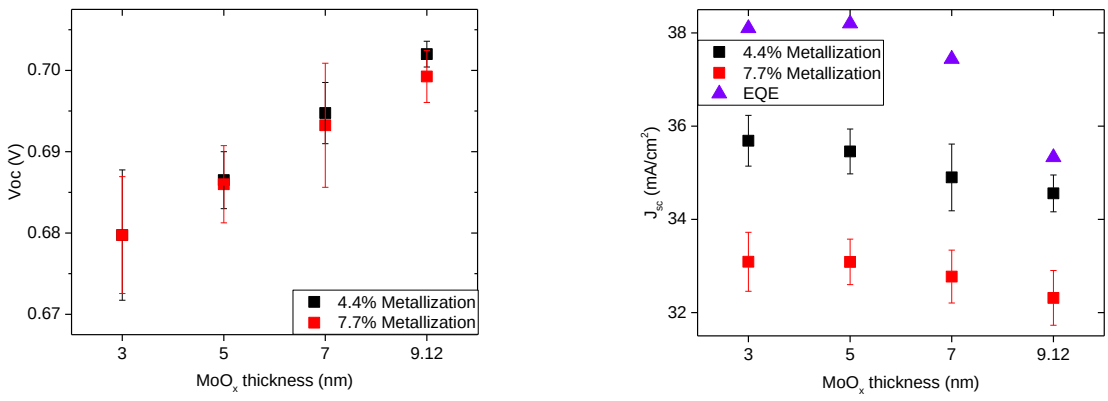


Figure 51: Variation in series resistance depending on MoO_x thickness for hybrid MoO_x/ silicon-based solar cells made according to Figure 36.

Figure 50 and *Figure 51* gave a range of thicknesses for MoO_x layer (0 nm < MoO_x thickness <10 nm) that should be tested in order to optimize the solar cell even more. As mentioned before, the solar cells from *Figure 50* and *Figure 51* were fabricated according to *Figure 36*, where we used the 7.84 cm^2 grid design (*Figure 16(a)*) for screen printing which required the solar cells to be cut apart and led to the damage of the rear metallization.
The same experiment was repeated using both sides texturized wafers which should lead to enhanced in the optical properties. Moreover, the problem about the damages experienced in the rear metallization after cutting the solar cells apart was resolved by applying the grid design (*Figure 16(b),* Area= 3.92 cm^2) for screen printing on the rear and front surface. Then it was possible to take the measurements without cutting the solar cells from the wafer. The process used for the fabrication of these more performant solar cells can be found in **Section 5.4.1**.
The MoO_x layer thickness was varied between 3 nm and 9.12 nm as this provided the best result in *Figure 50*. *Figure 52* shows the average value of the parameters based on 4 cells from the same wafer having equivalent metal coverage. The error bar represents the standard deviation calculated for each parameter.

(a) (b)



(c) (d)

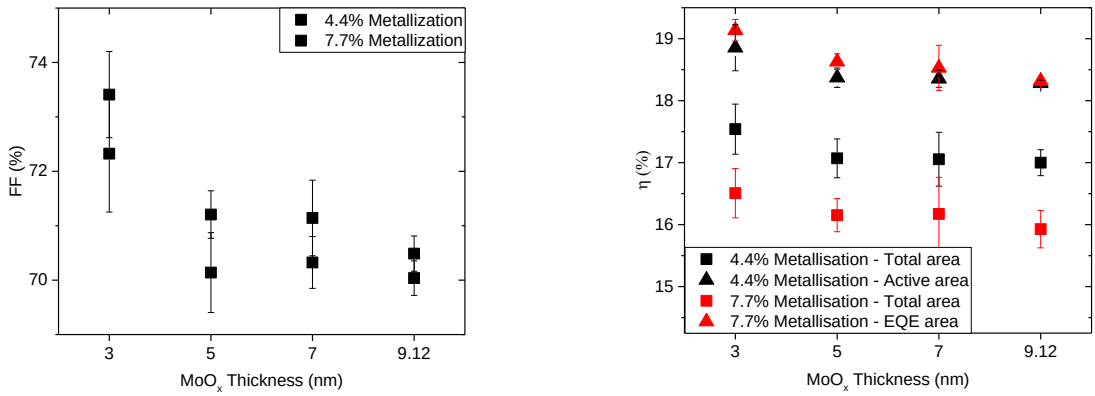


Figure 52: (a) $V_{oc,}$ (b) J_{sc}, $J_{sx,\,EQE}$, (c) FF and (d)η for an active and total area for various MoO_x thicknesses for hybrid MoO_x/ silicon-based HIT solar cells doubly texturized.

Figure 52(a) shows that by increasing the thickness of the MoO_x layer, we observe a linear increase in V_{oc}. While *Figure 52(b)* demonstrates a reduction in the optical properties for thicker MoO_x layers. It is then important to balance the J_{sc} and the V_{oc}. However, the J_{sc} is mainly affected by the percentage of metallization on the surface due to the shading. It is then advantageous to keep the metalization margin as this does not affect the FF considerably as shown in *Figure 52(c)*. The FF provides the best outcome for 3 nm of MoO_x with a light reduction for thicker MoO_x layers. *Figure 52(d)* gives the average efficiency of the solar cells present on each wafer which demonstrates the superiority of the solar cell having a thickness of 3 nm of MoO_x.
It is also important to verify that the selected thicknesses will not affect the transport of the carrier which can be established by looking at the J-V curve.

(a) (b)

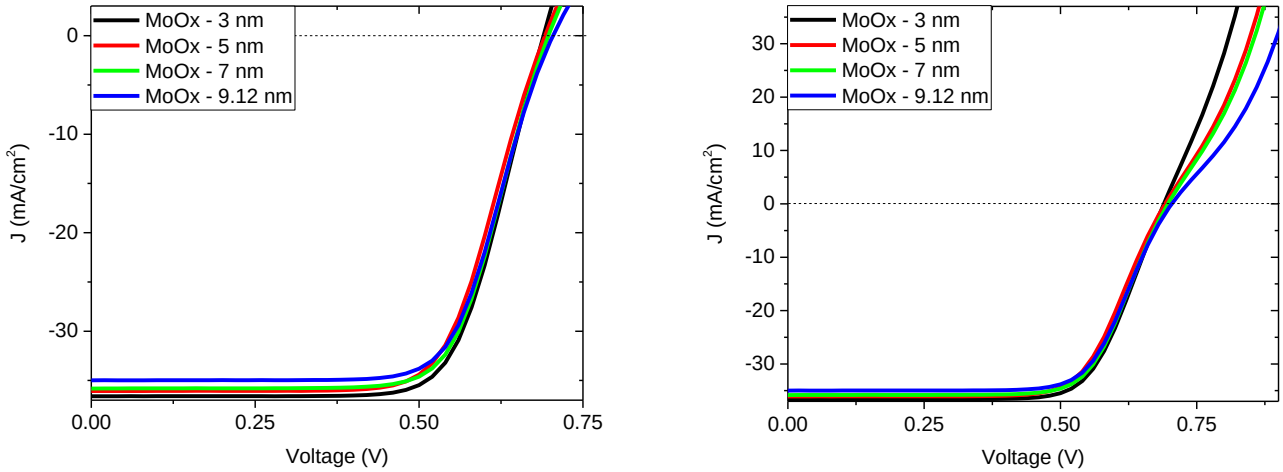


Figure 53: J-V curves with various MoO_x thicknesses for hybrid MoO_x/ silicon-based HIT solar cells (a) from 0 V to V_{oc} (b) from 0 V to 1 V.

Figure 53 presents the J-V curve of the most performant solar cell on each wafer. It can be observed that for thicker MoOx, the S-shape becomes stronger and influence the J-V curve even at a voltage lower than V_{oc} which will have an impact on the fill factor as illustrated in *Figure 52(c)*. Moreover, *Sun et al.* [110] stated that increasing the thickness would impact the FF due to the low conductivity of the material.
Another disadvantage of having a thicker layer of MoO_x is their effect on the transparency of the material. However, *Figure 54* illustrates that this will affect the optical losses only slightly.

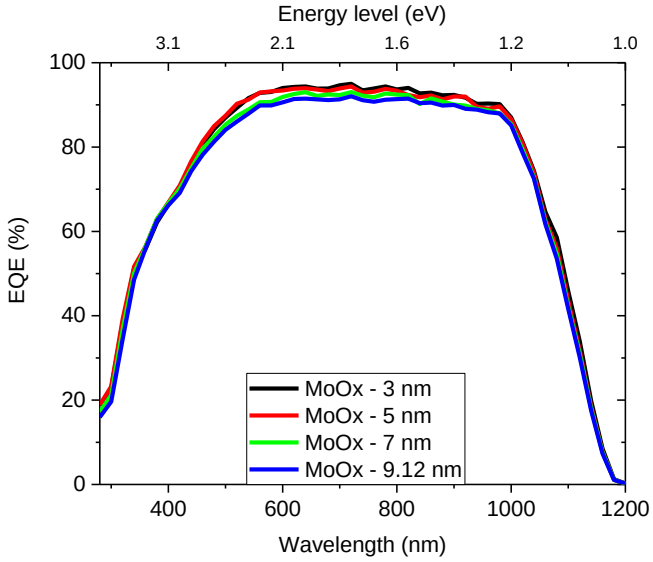


Figure 54: External Quantum Efficiency vs wavelength for a variation of the thickness of MoO_x for hybrid MoO_x/ silicon-based HIT solar cells doubly texturized .

In *Figure 52(b)* and *Figure 54*, we observe that the thickness will only slightly affect the optical losses of the solar cell. The choice of the MoO_x thickness is then more dependent on the V_{oc} and the FF. *Table 7* is regrouping the parameters of the best solar cells of each wafer from *Figure 52.* DIE 5(4.4% of metal on the total area, ***Figure 16****(b)*) provides the best total efficiency for each wafer reaching a maximum efficiency of 18.01% for the solar cell made with 3 nm of MoO_x.

Table 7: Parameters for a variation of the thickness of MoO_x for hybrid MoO_x/ silicon-based HIT solar cells.

MoO_x thickness (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	DIE
3	690	36.61	71.3	18.01	5
5	692	36.08	69.26	17.3	5
7	697	35.82	70.33	17.56	5
9.12	704	34.98	69.63	17.16	5

The results are satisfactory as the selected thickness can provide solar cells having a V_{oc} equal to 690 mV with a J_{sc} of 36.61 mA/cm^2, a fill factor of 71.3% and a total efficiency of 18.01%.

5.5. Conclusions

Chapter 5 is marked by the fabrication of our first solar cell. To start with, we had to select the material for the rear side in order to provide good quality passivation and electron selective contact. The two targets point were reached by applying 1.5 nm of SiO_2 capped with 250 nm of (n)poly-Si on a flat surface. This choice made, we were able to focus on the (p)doped front surface based on the MoO_x material.
Unfortunately, the first batch of solar cell gave an unsatisfactory FF which was equal to 62.1%. After investigation, it was noticed that the problem came from the procedure order before the deposition of MoO_x. By modifying the flowchart, we were able to increase the FF of the solar cell to 69.6%; with a big improvement in the minority carrier lifetime after the deposition of 11 nm of (i)a-Si:H and 3 nm of (p)nc-SiO_x, going from 0.411 ms for *Flowchart 1* to 2.833 ms for *Flowchart 2*. As soon as the base of the solar cell was providing good minority carrier lifetime we started focusing on optimizing the (p)doped stack of layer for the front surface according to the discovery made in **Chapter 4**.
First, we tested various materials for the (p)doped buffer layer in order to find which one combines the best with (i)a-Si:H and MoO_x layers. Through the analyse of various parameters, it was demonstrated that

the solar cell made with (p)nc-SiO_x:H was showing the best efficiency (15.7%) closely followed by the solar cell made of (p)a-SiC:H (15.6%), (p)nc-Si:H (15.3%) and (p)a-Si:H (15.1%). On the other side, the solar cell made with (p)nc-SiO_x:H showed the disadvantage of inducing an S-shape.
In the attempt to attenuate the presence of the S-shape and improve the performance, more advanced equipment was used for PECVD. The equipment provides treatments in between the deposition using hydrogen plasma treatments in between depositions and high-frequency layers to provide a p-doped layer with better quality for the crystallization.
The second step consisted of investigating the thickness of the (p)nc-SiO_x:H in order to produce the highest efficiency. Through the experiment, we were able to remove the S-shape when a thickness of 5 nm of (p)nc-SiO_x:H was applied. Moreover, the selected thickness gave great fill factor (77.29%) with an increase in the efficiency (19.01%) compared to thinner layer (18.08% for 3 nm of (p)nc-SiO_x). Furthermore, we tried to reduce the presence of the S-shape for the other thicknesses of (p)doped buffer layer by using IFO:H as TCO. Unfortunately, it did not provide the desired result; the presence of the S-shape was even more dominant with IFO:H compared to ITO.
Due to the fact that the experiment investigating the thickness of (p)nc-SiO_x:H and MoO_x layer were done simultaneously; the optimization of the (p)doped buffer layer thickness was not taken into account when the thickness of the MoO_x was investigated. The analyse is still providing useful results.
Dissimilar solar cells were produced with a different rear side, the (n)SiO_2/ploy-Si layer was replaced by a (n)doped stack of layers on a texturized surface with additional treatments between the deposition. With an un-optimized (p)nc-SiO_x:H layer, we were able to provide an efficiency of 18.01% for 3 nm of MoO_x. By selecting a thin layer for MoO_x we were also able to increase the J_{sc} to 36.61 mA/cm^2 compared to 36.08 mA/cm^2 for the solar cell made with a 5 nm layer of MoO_x.
In conclusion, this chapter provided the thickness and the material that should be applied for (p)doped buffer layer and MoO_x layer in order to provide the most efficient solar cell.

6. Conclusions and future work

The aim of this thesis is to challenge the limit of the SHJ solar cells efficiency (25.1% [7]) caused by the introduction of defects causing parasitic losses in addition to the optical losses on the front surface generated by the small bandgap of Si (1.55 to 2.1 eV [16]).
To reduce these losses, it was decided to focus on the replacement of the front (p)doped layer with an un-doped transparent material that will be able to act as a hole selective contact.
Researches have shown that this could be accomplished by the introduction of transition metal oxide (TMO). By combining a (n)c-Si with a TMO having a large work function (>6.7 eV), the Fermi-levels of both materials will align. The energy band will bend and the material will provide a hole selective contact without the introduction of dopants. This report will focus on molybdenum oxide which is a TMO with a work function able to reach 6.9 eV. Additionally, the material is characterized by a bandgap equivalent to 3 eV which should reduce the optical losses present on the front surface. MoO_x has already shown great results [21], yet, the material is still in its development phase.
To start with, we investigated the response of the passivation quality for MoO_x in combination to layers that are required for SHJ solar cells fabrication. For this purpose, MoO_x was deposited on an intrinsic layer to verify that it will not affect the surface passivation provided by the thin (7 nm) intrinsic hydrogenated amorphous silicon film. Unfortunately, the addition of MoO_x reduced the quality of passivation with a diminution of the iV_{oc} and minority carrier lifetime. The analysis showed that 10 nm of MoO_x was the preferred thickness to minimize the losses on the minority carriers lifetime (before MoO_x = 3.1 ms and after MoO_x = 2.21 ms) and iV_{oc} (before MoO_x = 728 mV and after MoO_x = 716 ms). Moreover, the choice of this thin thickness has the advantage that it will not excessively reduce the transparency of the material. Regrettably, it was noticed through annealing (130°C and 150°C for 15 min) that the combination (i)a-Si:H/ MoO_x is sensitive to low-temperature which will bring issues for the further steps required for the solar cell fabrication.
The experiment was followed by the investigation of the effect generated by ITO deposition; the introduction of this layer also brought some issues as the process required plasma luminescence and ion bombardment which impacted the quality of the passivation, with a reduction in the iV_{oc} (MoO_x = 716 mV and ITO = 710 mV) and minority carriers lifetime (MoO_x = 2.21 ms and ITO = 1.13 ms) for 10 nm of MoO_x.
To attenuate the reduction in the minority carrier lifetime and iV_{oc} from both (MoO_x and ITO) depositions, two strategies were tested:

I. pre-annealing the intrinsic layer before the deposition of the MoO_x layer
II. the addition of a (p)doped buffer layer in between the intrinsic and the MoO_x layer

The first option did not fully respond to the demand. Pre-annealing the intrinsic layer did help for the deposition of MoO_x as no reduction happened for the iV_{oc} and minority carrier lifetime. Additionally, the sensitiveness of MoO_x against low-temperature annealing was attenuated. However, as soon as ITO was deposited, a major reduction happened in the minority carrier lifetime (before ITO = 2.62/2.67 ms, after ITO = 1/1.15 ms and after ann = 1.27/1.25 ms) and iV_{oc} (before ITO = 717/720 mV, after ITO = 705/711 mV and after ann = 707/712 mV) with a small boost after annealing.
The second option did respond to the demand when a minimum thickness of the intrinsic layer was applied (>11 nm). The addition of the 11 nm of (p)doped buffer layer provided a constant and excellent surface passivation through each deposition (after MoO_x and ITO deposition). The minority carrier lifetime and an iV_{oc} had a minimum of 1.43 ms and 711 mV.
The selected strategy was then tested on solar cells. The first step consisted of the selection of a material and thickness for the (p)doped buffer layer followed by the optimization of the MoO_x layer thickness.
To start with, it was decided to investigate 4 different materials for the (p)doped buffer layer which consisted of (p)nc-SiO_x:H, (p)nc-Si:H, (p)a-Si:H and (p)a-Si:H. The solar cell made with (p)nc-SiO_x:H as (p)doped buffer layer generated the best total efficiency (15.7%).
The second experiment consisted of optimizing the thickness for the (p)nc-SiO_x:H layer. By testing thicknesses for (p)doped buffer layers of 0, 3 and 5 nm, it was observed that the best total efficiency (19.01%) is achieved with a layer of 5 nm. The solar cell was able to provide excellent results thanks to its large FF (77.29%) and J_{sc} (35.64 mA/cm^2). However, the V_{oc} still required some improvements as it only reached 690 mV.
In the hope of improving the efficiency, two different TCO were tested, it was demonstrated that the ITO (η = 19.01%) is more attractive than IFO:H (η = 17.68%).

The last experiment consisted of optimizing the MoO_x thickness. Due to the fact that the last two experiments (investigation of the MoO_x and the (p)doped buffer layer thicknesses) were done at the same time, it was not possible to combine the result. The optimization of MoO_x thickness was then accomplished with a 3 nm of (p)nc-SiO_x:H. We were still able to provide a satisfactory total efficiency of 18.01% with a J_{sc} of 36.61 mA/cm^2 and a fill factor of 71.3% while the V_{oc} once again only reached 690 mV.
The results are almost competing with the doped SHJ solar cells produced by the PVMD group. Indeed, the best SHJ solar cell based on doped nc-SiO_x:H layers [111] presented by the PVMD group (Y. Zhao (PhD)) reached a V_{oc} of 716 mV, a J_{sc} equal to 38 mA/cm², a fill factor of 79.3%, the overall provided an active efficiency of 21.6%.
To go for the gold, improvement in the total efficiency are still required. For this purpose, the first action would be to combine the two optimized thicknesses for the (p)nc-SiO_x and MoO_x layers. In the case that the result are not meeting the expectation, an option would be to replace the (p)nc-SiO_x:H layer with (p)a-SiC:H as the material also provided performant efficiency (15.6%).
Moreover, it could be a good idea to anneal for 15 minutes at 130°C the (p)doped buffer layer before MoO_x deposition to attenuate the hydrogen effusion as it was proven that this concept improved the interaction between the two layers.
Concerning the choice of the TMO material, *Werner et al.* declared in [112] that MoO_x should be replaced with WoO_x which provides an improvement in the optical losses.
As soon as the front surface is optimized similar investigation actions should be accomplished for the rear side and replace the (n)doped layer with a dopant free stack of layers to suppress any parasitic losses generated by the dopant.

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This thesis would not have been possible without the help of a lot of people.
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My last sentence goes to my meimei and my mom who always believed in me even when I did not.

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