Multiplexed thermal-diffusivity-based temperature sensors

By

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Abstract

Due to the precise lithography and highly pure silicon used in IC technology, thermal-diffusivity (TD) temperature sensors can achieve high accuracy without the need for trimming. TD sensors employ electrothermal filters (ETFs) to measure the thermal diffusivity of silicon, i.e. the rate at which heat diffuses through silicon, which is a well-defined function of temperature. This thesis presents two approaches to improve the accuracy and resolution of TD sensors. The first approach investigates the effect of variations in ETF geometry on sensor resolution and proposes a multiplexing scheme to utilize a single readout circuit for reading out multiple ETFs. The second approach aims to investigate the effect of improvements in CMOS technology on sensor accuracy by scaling two ETFs to the 65nm process from the 180nm process. A first-order phase-domain delta-sigma modulator is designed for the readout of the ETFs in the 65nm process, and the previously designed multiplexing scheme is used for cost and time-efficient tape-out. Based on the estimated lithographic error of the 65nm process, the two ETFs are expected to achieve untrimmed inaccuracies of 0.18℃(3σ) and 0.36℃(3σ), respectively.

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1 Introduction

Temperature changes in the environment can affect the operation and accuracy of the integrated circuits. Therefore, temperature sensors are widely used to monitor ambient temperature and compensate for possible performance loss. In recent years, integrated temperature sensors realized in CMOS technologies have been the preferred choice in many applications, due to their small size, low cost, and easily interpretable digital output.

1.1 Temperature sensors in CMOS Technology

There are several ways to realize temperature sensors in CMOS processes. The differentiation is based on the sensing element used in the temperature sensor. BJT-based sensors exploit the temperature dependency of the base-emitter voltage, V_{BE}, which exhibits a Complementary-To-Absolute-Temperature (CTAT) behavior. Furthermore, when two BJTs are biased at a well-defined collector current ratio, the difference between their base-emitter voltages (ΔV_{BE}) is Proportional-To-Absolute-Temperature (PTAT). By combining ΔV_{BE} and V_{BE}, a temperature-independent reference voltage can be created, which can then be compared to a PTAT or CTAT voltage to determine absolute temperature. After a one-point trim, BJT-based temperature sensors can offer high accuracy (0.1°C (3σ)) over a large temperature range (-55°C to 125°C) with μW-level power consumption [1]. However, the need for trimming increases their fabrication cost. Also, V_{BE} is around 0.7V at room temperature, which creates a voltage headroom problem that is hard to meet in advanced CMOS processes due to their low supply voltages (<1V).

When they are biased in weak inversion, MOSFETs can replace BJTs as sensing elements because of the exponential relationship between gate-source voltage and drain current. Moreover, since the threshold voltage of a MOSFET decreases in advanced technologies, the voltage headroom issue is solved. On the other hand, the untrimmed inaccuracy of a MOSFET-based sensor is worse than a BJT-based one due to the increase in the parameters that suffer from process spread [2], further increasing the need for trimming.

Resistors are also used as sensing elements in temperature sensors. They have a strong temperature dependency and can be designed for high energy efficiency (10fJ.K^2in [3]). Resistor-based sensors can also scale well with technology since they can operate under low-voltage headroom. However, they exhibit more spread than BJTs. After a one-point trim, their untrimmed accuracy (0.4°C (3σ)) is worse than that of BJT-based sensors [3]. Two-point calibration can improve accuracy at the expense of higher costs.

Temperature sensors using electro-thermal filters (ETFs) as the sensing element rely on a temperature-dependent property of silicon called thermal diffusivity, D_{Si}. In an ETF, a heater generates a periodic heat wave that travels through the silicon substrate, causing temperature fluctuations that can be detected by a neighboring temperature sensor. With a well-defined distance, *s*, between the heater and the sensor, the thermal delay in the signal can be used to

determine absolute temperature. Due to the precise lithography and highly pure silicon used in IC technology, thermal-diffusivity (TD) temperature sensors can achieve high accuracy without the need for trimming [4]. However, they have poor energy efficiency, because the sensor's resolution is directly proportional to the received signal, which is only in the order of a few mV even with mWs of heater power dissipation. Reducing *s* will increase signal amplitude but will also degrade the ETF's accuracy by increasing its sensitivity to lithographic errors. Hence, a trade-off exists between resolution and accuracy regarding the choice of *s*. However, due to the improved lithography with CMOS technology scaling, the distance *s* can be reduced without losing the sensor's accuracy. Furthermore, D_{Si} is a process-independent property, which makes ETFs easily scalable.

This project aims to optimize the ETF design for better resolution and accuracy. This will be done by investigating the tradeoffs associated with varying the distance *s* and scaling the ETFs from a 180nm process to a 65nm process.

1.2 Thermal-diffusivity temperature sensors

1.2.1 Working Principle

The thermal diffusivity of a material is a measure of the rate at which heat waves travel through it. For the silicon substrate of an integrated circuit, D_{Si} is proportional to $1/T^{1.8}$ [5]. This relation to the absolute temperature *T* is mainly caused by phonon scattering in crystalline semiconductors.

Then by observing the thermal delay between two points spaced at a known distance on silicon, temperature information can be retrieved. These two points can be realized by a heater and a temperature sensor, spaced at distance *r*, as shown in Figure 1.1. Such a structure is called an Electrothermal Filter (ETF).

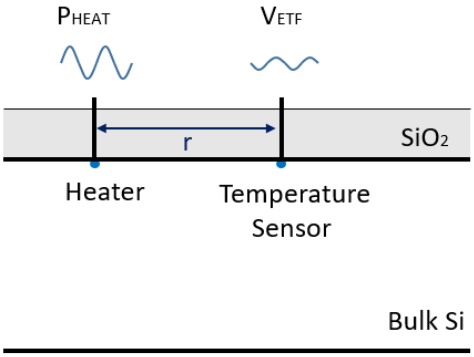


Figure 1.1: A basic electrothermal filter structure.

The operation of an ETF can be better understood by considering what happens when an electrical signal with an angular frequency ω is applied to the point heater. This signal will be transformed into a heat wave that diffuses through the silicon substrate in a semi-spherical manner. The temperature profile can be obtained by solving [6]:

$$\frac{d^2\big(rT(r)\big)}{dr^2} - q^2 rT(r) = 0, \tag{1.1}$$

where r is the distance to the point heater, $\mathrm{T(r)}$ is the temperature increase at a distance r and $\mathrm{q}^2 = j\omega/D$. The temperature profile defines a thermal impedance, $\mathrm{Z_{th}(\omega, r)}$, which relates $\mathrm{T(\omega, r)}$ to the dissipated power at the heater, $\mathrm{P_{heat}(\omega)}$:

$$Z_{th}(\omega, r) = \frac{T(\omega, r)}{P_{heat}(\omega)} = \frac{1}{2\pi k_{Si} r} exp\left(-r\sqrt{\frac{\omega}{2D_{Si}}}\right) exp\left(-jr\sqrt{\frac{\omega}{2D_{Si}}}\right) \tag{1.2}$$

In which k_{Si} is the thermal conductivity of silicon. From Eq. 1.2, the magnitude and phase components of the thermal impedance are expressed as follows:

$$\begin{aligned} |Z_{th}(\omega, r)| &= \frac{1}{2\pi k_{Si} r} exp\left(-r\sqrt{\frac{\omega}{2D_{Si}}}\right) \\ \phi(\omega, r) &= -r\sqrt{\frac{\omega}{2D_{Si}}} \end{aligned} \tag{1.3}$$

From Eq. 1.3, the thermal impedance decreases in magnitude as the angular frequency increases. Hence, ETFs behave like low-pass filters in the thermal domain.

Regarding the output of the ETF, the point temperature sensor at a distance *r* from the heater receives the heat wave. If the sensor has a sensitivity $\mathrm{S_t}$, the output amplitude V_{ETF} can be expressed as:

$$V_{ETF} = \frac{P_{HEAT} S_t}{2\pi k_{Si} r} exp\left(-r\sqrt{\frac{\pi f_{drive}}{D_{Si}}}\right) \tag{1.4}$$

And the phase component of the ETF output is given by:

$$\phi_{ETF} = -r\sqrt{\frac{\pi f_{drive}}{D_{Si}}} \tag{1.5}$$

Where $\mathrm{f_{drive}}$ is the frequency of the electrical signal driving the heater. To observe the temperature dependency of the output phase, the relation between D_{Si} and the absolute temperature can be integrated into Eq. 1.5 as follows:

$$\phi_{ETF} \propto -r\sqrt{\pi f_{drive} T^{1.8}} \tag{1.6}$$

Both the amplitude and the phase components of the ETF output signal have a temperature dependency. This implies that either one could be used to process the temperature information. Comparing Eq. 1.4 and 1.5, $\mathrm{V_{ETF}}$ depends on more parameters than $\mathrm{\phi_{ETF}}$, such as heater power and the sensitivity of the temperature sensor. This makes it less attractive since the extra parameters introduce additional temperature spread. Furthermore, $\mathrm{\phi_{ETF}}$ is

proportional to $T^{0.9}$, and this near-linear relation will be more convenient while extracting the temperature information from the ETF output.

1.2.2 ETF designs

In the previous section, both the heater and the temperature sensor are assumed to be points. Even though this is not possible to realize in a practical implementation, certain design choices can be used to approximate this behavior.

1.2.2.1 Heater Design

For a point heater, the applied electrical signal will heat an infinitesimally small volume, concentrating all the heat at one point. This will result in a high amplitude output signal. However, as the heater's surface area increases, the heat due to the applied electrical signal would spread more. Consequently, the output signal amplitude decreases.

The geometry of the heater also depends on the targeted heater power $\mathrm{P_{heat}}$. If the heater is realized as an n+ diffusion resistor, the dissipated power will be determined by the supply voltage, $\mathrm{V_{DD}}$, and the sheet resistance of the resistive layer, $\mathrm{R_{sh}}$. For typical $\mathrm{P_{heat}}$, $\mathrm{V_{DD,}}$ and $\mathrm{R_{sh}}$ values, the length of the heater needs to be longer than its width, as shown in Figure 1.2(a). To make this resemble a point heater, it can be folded to form the U-shaped heater shown in Figure 1.2(b).

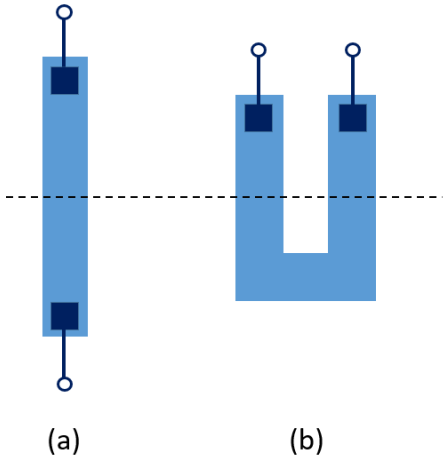


Figure 1.2: Longitudinal (a) and U-shaped (b) heater designs.

1.2.2.2 Temperature Sensor Design

There are several ways to implement the temperature sensor of an ETF. Diffusion resistors, MOSFETs, or BJTs can all be used for this purpose since they are all implemented in the substrate and are sensitive to temperature changes. However, they all require biasing, thus causing extra power consumption. Also, the distance *s* in Figure 1.1 directly affects the phase output as seen in Eq. 1.5. With these components, the effective location of the diffusions will be sensitive to process spread due to implantation, thus, the effective *s* value will be process-dependent, resulting in poor accuracy.

A better implementation of the temperature sensor is to create integrated thermocouples. Due to the Seebeck effect, if two, ohmically connected, but different conductors are subjected

to a temperature difference between their ends, there will be a voltage output proportional to this temperature difference. When aluminum interconnect and p+ diffusion resistors are used to form an on-chip thermocouple, a sensitivity, S_t, of about 0.5mV/K is achieved [7]. And by connecting them in series, a thermopile can be formed and used as the temperature sensor of an ETF.

Another advantage of thermophiles is that they are passive sensors, meaning that they do not need biasing. Furthermore, the distance *s* is determined only by lithography and is independent of the process variations. Hence, a thermopile is the most suitable option for the relative temperature sensor required in ETFs.

The ETF designs with thermophiles have gone through modifications to provide better performance specifications over the years. The first proposed design in [8] is a bar ETF similar to that presented in Figure 1.3.

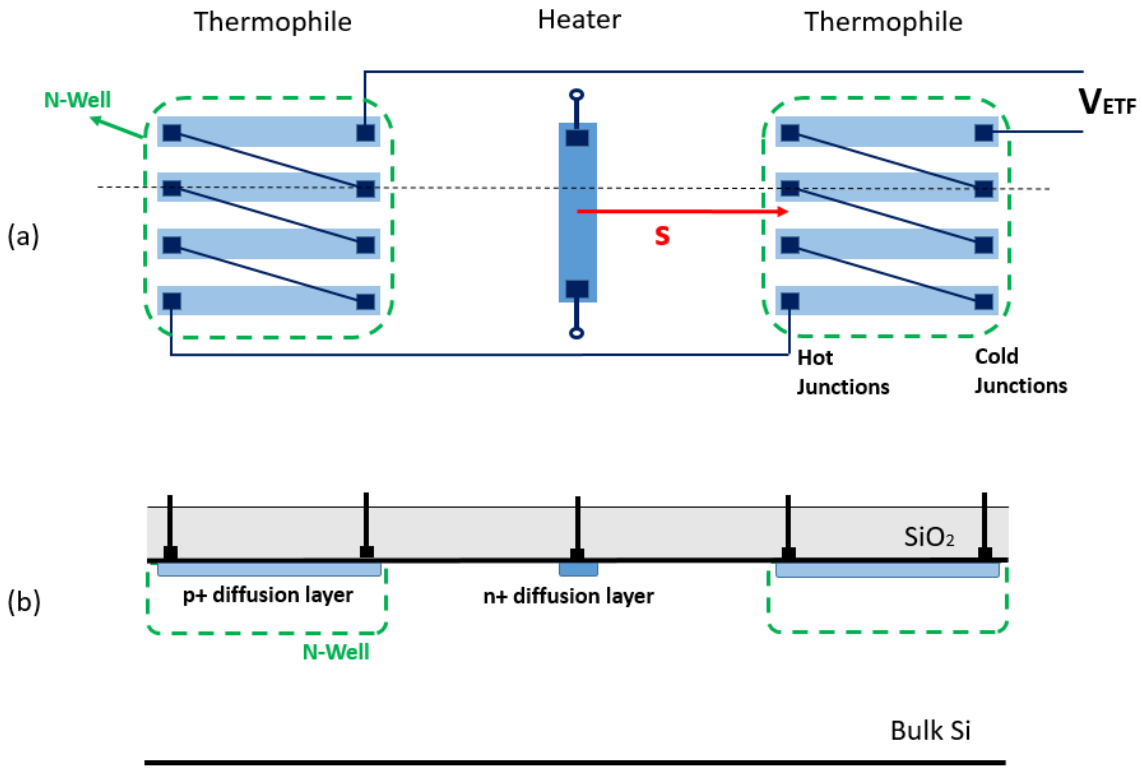


Figure 1.3: A bar ETF (a) and its cross-section at the dashed line (b).

In the bar ETF above, a hot and a cold junction can be observed. Hot junctions are the ones that are adjacent to the heater and separated by a distance '*s*', and the junctions on the other side are cold junctions. Hot junctions define the crucial parameter *s*, since the heat signal is mostly received there, and the signal is minimal when it reaches the cold junction. The voltage output of the bar ETF, V_{ETF}, is obtained by connecting the aluminum/p+ diffusion resistor thermocouples on both sides of the heater in series. For the electrical model of the ETF, the p+ diffusion arms are modeled as series resistors mounted in an n-well with a parasitic junction capacitance. Hence, the electrical behavior of the thermopile resembles an RC filter.

While explaining the working principle of an ETF in the previous section, it is mentioned that the heat wave travels in a semi-spherical manner. However, by looking at the placement of the hot junctions in a bar ETF, the distance *s* is set as if the heat travels unidirectionally. Hence, the phase of the heat wave received at every hot junction would be different, creating inconsistency while summing up the thermocouple outputs. Redesigning the ETF to compensate for this, results in phase contour ETFs in Figure 1.4.

The newer design sets *s* as the radial distance between the heater and the hot junctions. Besides the adjustment to the thermophile alignment, other design changes have been made in the phase contour ETFs to improve their performance. For example, the length of the diffusion resistor arm of the thermocouple is set to maximize SNR [9] and the U-shaped heater design in Figure 1.2(b) is preferred for point-like behavior. These modifications result in better untrimmed accuracy (0.2℃ (3σ) [4]) and resolution compared to the previously proposed ETFs.

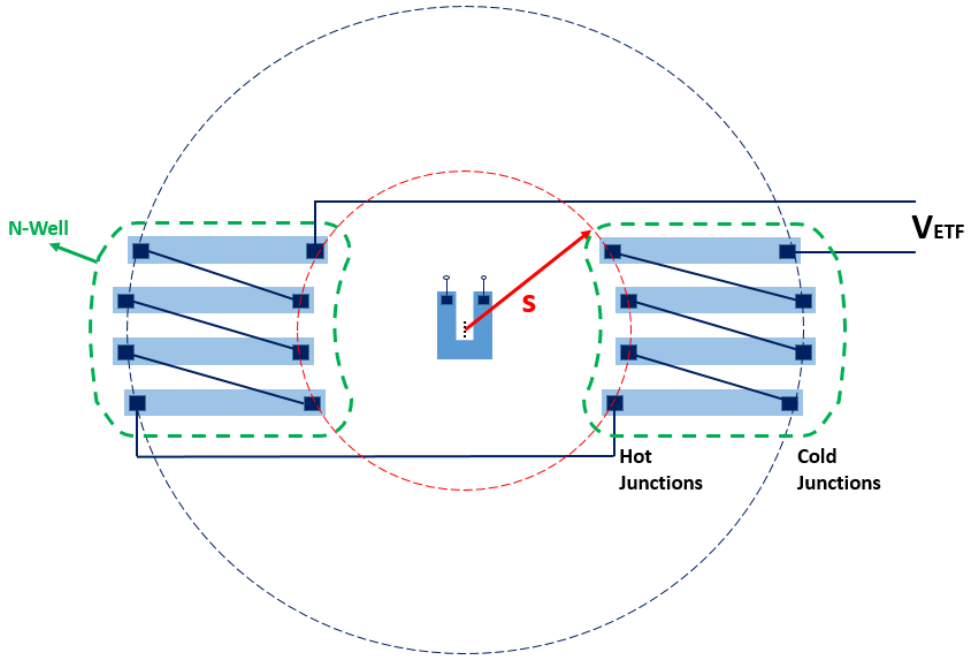


Figure 1.4: A phase contour ETF.

However, the heater in the phase contour ETF is only covered from the left and right sides, meaning that the thermopile does not fully receive the heat wave created. This degrades the resolution of the temperature sensor since some of the dissipated power is wasted. Hence, U. Sönmez et al. proposed another geometry for the ETF [10], as shown in Figure 1.5.

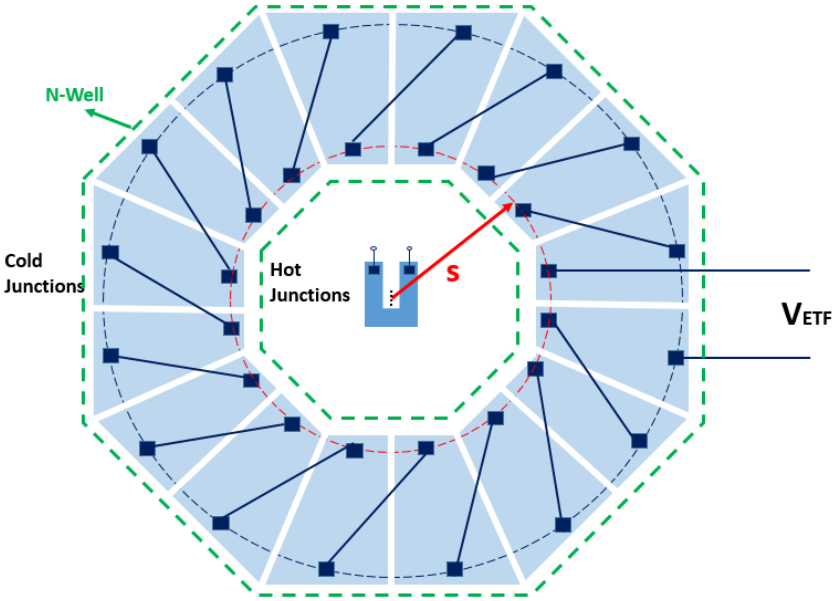


Figure 1.5: An octagonal ETF.

With the octagonal ETF design, the heater is now surrounded by the thermopile, using all the dissipated power to generate the voltage signal, V_{ETF}. The increased width of the thermopile arms reduces their resistance, hence, the introduced thermal noise decreases. On the other hand, their increased area also increases the parasitic junction capacitance mentioned before. This will decrease its intrinsic electrical bandwidth and affect the accuracy of the ETF as will be explained in detail in the following subsection.

In this thesis, octagonal ETFs are used. One of the goals of the thesis is to achieve better performance by further optimizing their design.

1.2.3 Aspects of ETF Performance

The main performance parameters of any temperature sensor are accuracy and energy efficiency. For thermal diffusivity (TD) temperature sensors, the ETF used is the main limiting factor on performance [5].

For the selected octagonal geometry of the ETF, there are still degrees of freedom with the selection of the radial distance *s*, driving frequency $f_{drive,}$ and heater power P_{heat}. Also, the process technology used for the implementation plays a role. The performance of the ETF will depend on these parameters.

1.2.3.1 Accuracy Limitations

To design an accurate sensor, it is important to investigate the various effects that can introduce spread in the measurement. Looking at Eq. 1.5, *s*, D_{Si} and f_{drive} directly affect the phase output, ϕ_{ETF}. Assuming D_{Si} is process independent and f_{drive} is sufficiently accurate, the variation in *s* will be the dominant error source. This variation is caused by lithographic misalignment in the ETF.

To estimate the temperature inaccuracy caused by the variation in *s*, the partial derivatives of Eq. 1.5 is taken as follows:

$$\frac{\delta\phi_{ETF}}{\phi_{ETF}} = \frac{\delta s}{s} = 0.9\frac{\delta T}{T} \tag{1.7}$$

From this relation, δT can be estimated for any process by assuming that the lithographic inaccuracy, δs, will be less than 10% of the minimum line width. The readout circuit is designed to introduce a minimal phase error, around 10% of $\delta\phi_{\mathrm{ETF}}$ in Eq. 1.7, by providing sufficient bandwidth.

Besides the effect of lithographic errors, the ETF has another accuracy limitation coming from the thermopile's electrical properties. The equivalent circuit model of an integrated thermopile is shown in Figure 1.6. In this circuit, every thermocouple in the thermopile is modeled by its lumped resistance $\mathrm{R_{tc}}$ and the distributed capacitance $\mathrm{C_{tc}}$ added to both ends of the resistor as $\mathrm{C_{tc}}/2$. $\mathrm{v_{tc}}$ represents the voltage generated by a single thermocouple due to the Seebeck effect.

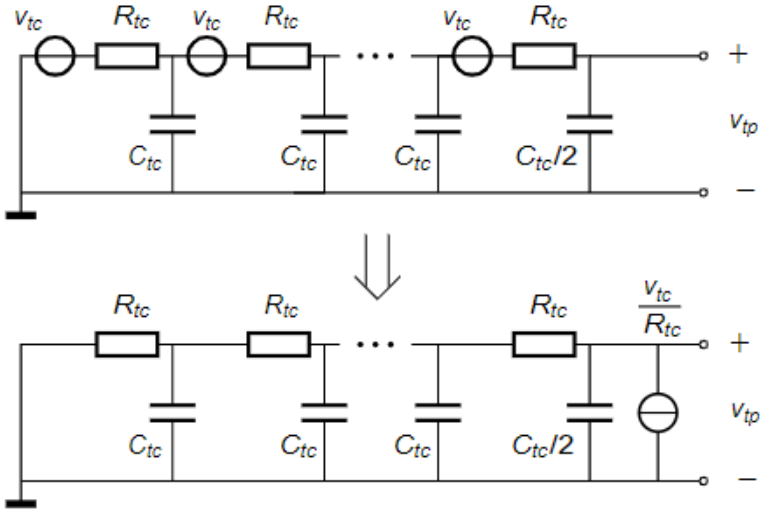


Figure 1.6: Equivalent circuit of an integrated thermophile [11].

For the ETF thermophile, $\mathrm{R_{tc}}$ is the resistance of the p+ diffusion layer arms and $\mathrm{C_{tc}}$ is the distributed capacitance coming from the junction formed between n-well and p+ resistors. With this model, the ETF will have a bandwidth determined by these characteristic properties, causing an intrinsic phase error at the driving frequency. As a result, the spread in this RC behavior will directly contribute to sensor inaccuracy.

1.2.3.2 Resolution Limitations

From Eq. 1.7, it is seen that the accuracy of the system improves as the distance *s* increases. But considering the octagonal ETF structure, increasing *s* results in a smaller output signal, $\mathrm{V_{ETF}}$, assuming a constant the heater power, $\mathrm{P_{heat}}$. For constant noise, the reduction of the signal amplitude directly reflects on the resolution of the sensor. $\mathrm{P_{heat}}$ can be increased to compensate for the loss, but this results in a significant increase in the overall power consumption of the temperature sensor since most of the power is dissipated in the heater. Hence, $\mathrm{P_{heat}}$ and *s* should be optimized to balance resolution, accuracy, and power consumption.

To gain a better understanding of the resolution in a TD temperature sensor, the simplified system in Figure 1.7 can be used.

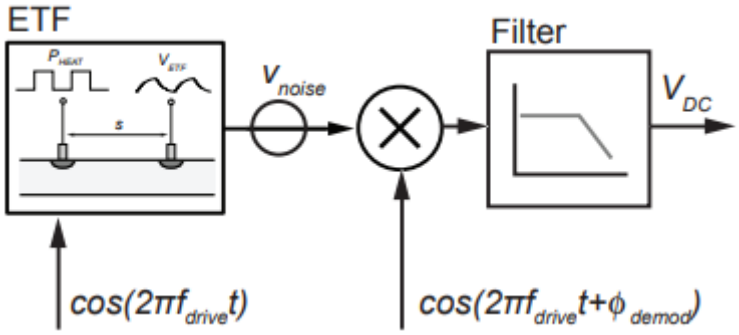


Figure 1.7: Simple ETF interface for resolution analysis [5].

In this system, the ETF is made out of a point heater and a point temperature sensor as in Figure 1.1. And it is driven by a square wave, dissipating average power $\mathrm{P_{heat}}$. The output of the ETF is then multiplied by a square signal which has a first harmonic of $\cos(2\pi f_{drive}t + \phi_{demod})$, creating a DC term proportional to $\cos(\phi_{ETF} - \phi_{demod})$ after multiplication. The multiplier output then passes through a low-pass filter with a bandwidth B.

The noise voltage, v_{noise}, in the model represents the ETF's thermal noise coming from the equivalent resistance of the thermopile seen in Figure 1.6. The power spectral density of this white noise is equal to $4kT(N * \mathrm{R_{tc}})$, where N is the number of thermocouples with resistances $\mathrm{R_{tc}}$. Combining these with the ETF output signal given in Eq. 1.4 results in the following resolution dependencies regarding *s* and $\mathrm{P_{heat}}$ [5]:

$$res \propto s\frac{\sqrt{4kT(N * R_{tc})B}}{P_{heat}} \tag{1.8}$$

Looking at Eq. 1.7 and 1.8 together, it can be seen that there is a tradeoff between resolution and accuracy when deciding *s*. However, in advanced processes, the more precise lithography should enable the use of small ETFs for higher resolution while still achieving sufficient accuracy. The different ETF designs in this project aim to experiment with this idea and observe how decreasing *s* affects the resolution and accuracy of TD temperature sensors.

1.2.4 The Readout Circuit

The ETFs form the front end of a TD temperature sensor. A readout circuit is necessary to process the ETF output without degrading its accuracy and resolution. As explained in subsection 1.2.1, the phase delay of the output signal, ϕ_{ETF}, is used to retrieve the temperature information in the sensor. Since the thermopile structure outputs a relatively small amplitude signal, the readout circuit should have low noise.

In some of the prior-art TD temperature sensors, the readout is based on temperature-to-frequency conversion [12], as illustrated in Figure 1.8. Here, the frequency-locked-loop (FLL) controls the driving frequency of the ETF heater. Since the ETF output is only a low-pass filtered version of the feedback signal, carrying the same frequency component, their multiplication performs phase detection. Then the multiplier's output has a DC component

proportional to $\cos(\phi_{ETF})$. Since the DC term at the input of the integrator is forced to be zero by the feedback loop, forcing ϕ_{ETF} to $90°$. In Eq. 1.5, knowing and controlling *s* and ϕ_{ETF} will give a frequency to temperature relation of $f_{drive} \propto 1/T^{1.8}$. Hence, the output frequency can be converted to temperature.

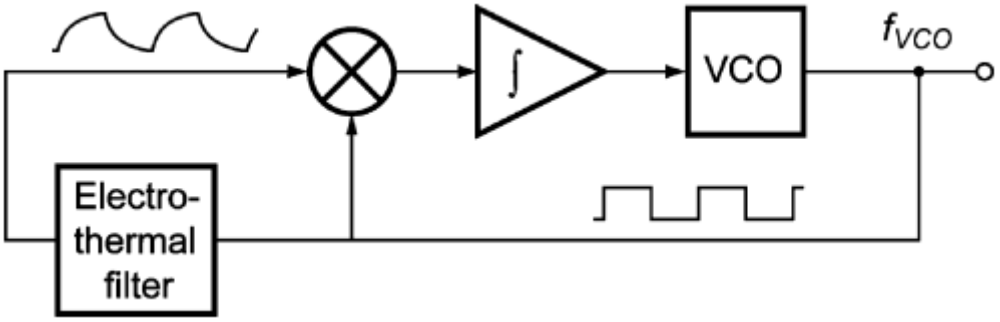


Figure 1.8: Block diagram of a temperature-to-frequency converter [8].

The disadvantage of the analog FLL in Figure 1.8 is that it requires a large integrating capacitor ($1\mu F$) that cannot be integrated on-chip, to provide desired loop bandwidth for low temperature-sensing resolution [8]. To mitigate the need for external passive elements, a frequency-domain delta-sigma modulator ($FD\Delta\Sigma M$) was proposed in [5]. The VCO in the FLL was replaced by a single-bit quantizer and the output bitstream was used to toggle f_{drive} between two reference frequencies. The bitstream average was then used to retrieve the temperature information. However, switching f_{drive} between the reference frequencies gave rise to the possibility of thermal inter-symbol-interference (ISI).

The substantially nonlinear frequency-temperature relation and the thermal ISI possibility in the previously mentioned method led to phase domain readouts. Since ϕ_{ETF} is proportional to $T^{0.9}$, it would be a better approach to obtain a phase output and convert it to temperature. This is done in [13] and the simplified block diagram can be seen in Figure 1.9.

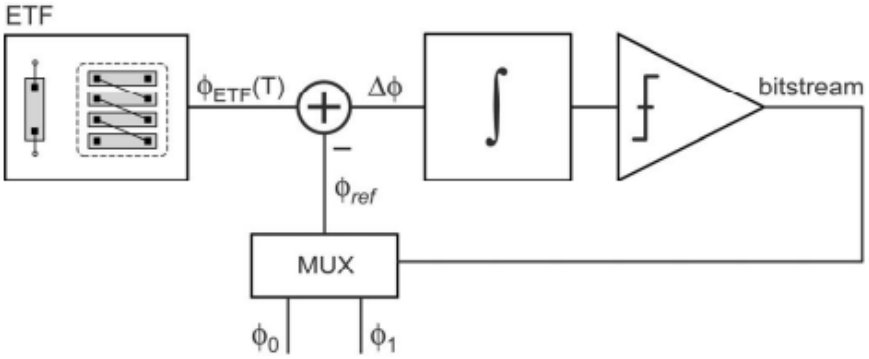


Figure 1.9: Block diagram of a phase-domain delta-sigma modulator [13].

In this design, the ETF is followed by a phase-domain delta-sigma modulator ($PD\Delta\Sigma M$). This enables a high-resolution readout which is essential for the TD temperature sensor. Here, the reference phase signals (ϕ_0, ϕ_1) with the same frequency as f_{drive}, are multiplied by the ETF output. This multiplication gives a DC term proportional to $\cos(\phi_{ETF} - \phi_{0,1})$. When (ϕ_0, ϕ_1)

are chosen to have $\cos(\phi_{ETF} - \phi_0)>0$ and $\cos(\phi_{ETF} - \phi_0)<0$, the bitstream toggles so that the average current flowing to the input of the integrator will approach zero. In the end, the bitstream average represents the weighted average of the reference phases and this is converted into ϕ_{ETF}.

In this thesis, the use of $PD\Delta\Sigma M$ readout circuits is preferred due to their near-linear phase-temperature relation and their digital output.

1.3 Organization of the thesis

The rest of the thesis is structured as follows. In chapter 2, the characterization of the new ETF designs in the 180nm process is presented. Furthermore, a multiplexing method is introduced to use a common readout circuit for the performance test of the new ETFs.

Chapter 3 presents the layout and characterization of the ETFs in the 65nm process. Then the implementation of the readout circuit for the temperature sensor is shown. Finally, the simulation results for the proposed design are illustrated.

Lastly, chapter 4 concludes the project and proposes improvements for future work.

2 TD Temperature Sensor in 180nm

In this chapter, the characteristics of ETF layouts with different heater/sensor spacings in 180nm CMOS are investigated. First, due to their unusual (octagonal) layout, the accuracy of the RC extraction tool (Calibre) is analyzed, as this will determine the accuracy of the estimated ETF bandwidth. Then, for an area-efficient implementation of the characterized ETFs, a method to multiplex different ETFs to a single readout circuit is introduced.

2.1 ETF Characterization

As explained in subsection 1.2.3.1. The thermopile of an ETF also behaves like an electrical RC network. It is necessary to simulate the resulting limitation on ETF bandwidth because this will contribute to the inaccuracy of the TD sensor.

The ETFs analyzed in this project have octagonal shapes. Hence, the p+ diffusion layer arms in the thermopile structure are not rectangular, unlike the Pcells of the other resistors provided in the process design kit (PDK). Therefore, the extraction results of Calibre are first checked to ensure that the ETF characterization is accurate.

2.1.1 Cadence extraction motive

The ETF designs are first laid out according to the design specifications. In this thesis, the preferred shape for the thermopile structure is the octagonal one described in the previous chapter. Such a structure is shown in Figure 2.1(a).

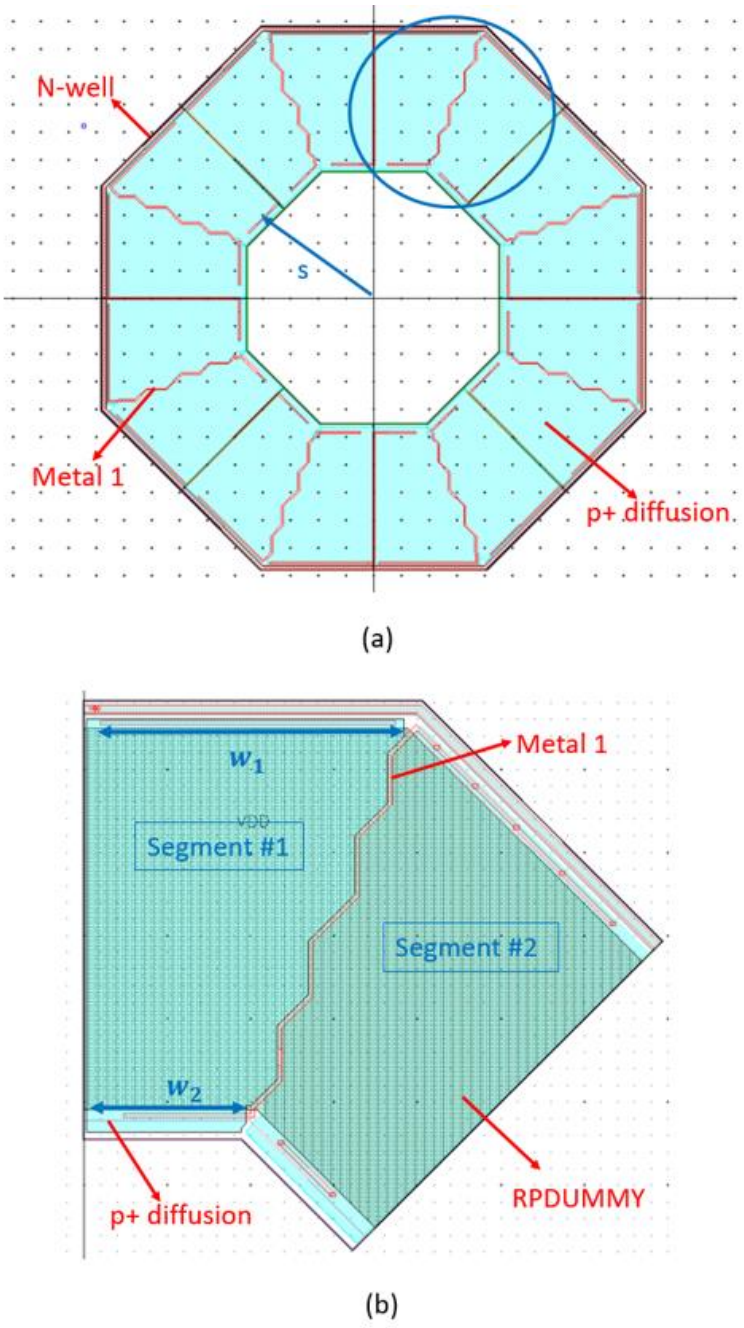


Figure 2.1: An octagonal thermopile layout (a) and the circled octant of the thermopile (b).

When zoomed in to the octant of the thermopile, as in Figure 2.1(b), the geometry of each thermocouple can be observed. Each segment in this figure represents the p+ diffusion arm of a thermocouple. They are shaped like trapezoids with one angled side.

To characterize the electrical bandwidth of an ETF, a schematic view must first be created from the layout. This is done by modeling the p+ diffusion arms as 3-terminal resistors. The third terminal is necessary to properly model the effect of the n-well in which the thermopile structure is implanted. The capacitance of the thermopile comes from this p+ to n-well junction. For the equivalent resistance of the thermopile, the resistances of each arm are summed up, since they are all connected in series.

For a resistor with a rectangular layout, the resistance calculated by Calibre is simply the sheet resistance of the used layer multiplied by the length-to-width ratio. The length and width of the resistor are determined by the RPDUMMY layer used in the layout. This layer can be seen in Figure 2.1(b) as the darker area covering most of the p+ diffusion layer. Since the contacts are placed on top of the diffusion layer, the area between the contacts determines the resistance. That is why the dummy layer is used, and the dimensions of the resistor are determined by the intersection between the dummy layer and the p+ diffusion layer. Then the resistor used in the schematic is given the length and width selected in the layout. Afterward, the LVS (Layout vs. Schematic) function is checked so that the layout matches the schematic. However, the thermocouple arms are trapezoidal, and they have angled sides. Hence, the extraction of the length and width values is not as straightforward as it would be for a rectangular area. Since the resistance of the arm is calculated with these values, the method used by Calibre to extract the dimensions should be understood and verified.

As an experiment, the L-shaped p+ diffusion resistor in Figure 2.2 was laid-out and the LVS report was examined for the extracted dimensions. The results showed that the width extracted by LVS is the average of the two different widths (W_1 and W_2). The extracted length is determined by dividing the RPDUMMY and p+ diffusion layer overlap area by the extracted width. In the end, the resistance is calculated by considering this layout as a rectangular area with these extracted width and length values.

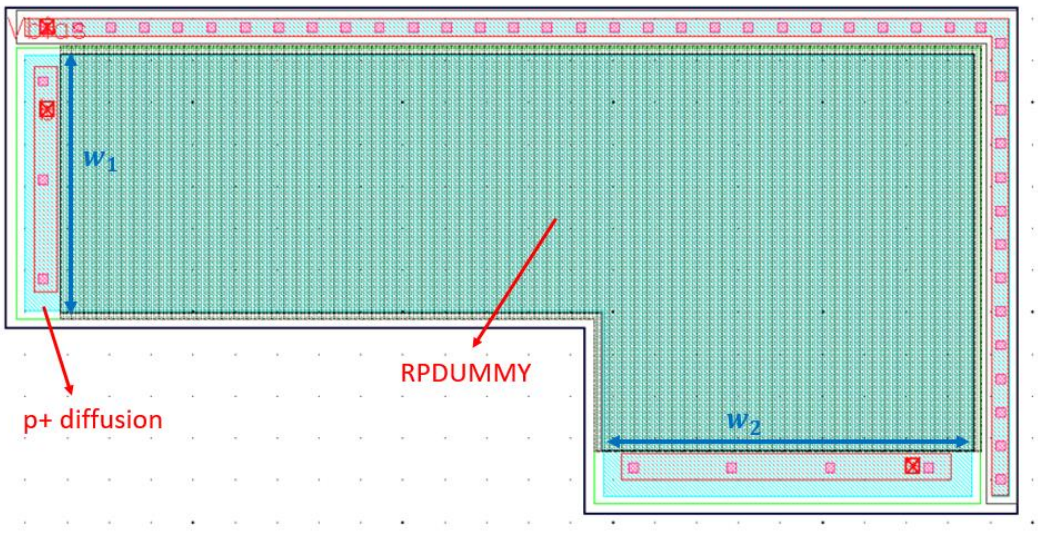


Figure 2.2: The test layout of an L-shaped resistor.

After observing the extraction pattern, the LVS was run for the thermopile octant in Figure 2.1(b). The dimensions extracted from the layout matched what was observed in the experiment. The extracted width for the first segment in Figure 2.1(b) was the average of w_1 and w_2, and the length was determined by dividing the area by the average width.

For the resistance calculation in Calibre, the obtained dimensions are put in a rectangular plate model. Hence, verifying if this approximation is accurate for the trapezoidal-shaped arm is also necessary. Therefore, the resistance of the arm was calculated by using the formula modeled for a trapezoidal conducting plate in Eq. 2.1 [14].

$$R = R_{sh}\left(\frac{l}{w_1 - w_2}\right) ln\left(\frac{w_1}{w_2}\right) \quad (2.1)$$

Where R_{sh} is the sheet resistance of the p+ diffusion layer, w_1 and w_2 are the different widths and l is the perpendicular distance between the two ends of the arm in Figure 2.1(b). The results for the hand-calculated and extracted resistances are presented in Table 2.1. From these results, it was concluded that the error in the approximation is negligible and that the Calibre resistance extraction can be trusted for the thermopile characterization.

To verify the extracted capacitance of the same segment in Figure 2.1(b), the 3-terminal resistor model provided by the TSMC model files in Figure 2.3 was compared by hand calculation. In the model, the p-n junction between the n-well (Body) and the diffusion layer is represented by distributed diodes. These reverse-biased diodes have capacitances that define the characteristics of the thermophile arms.

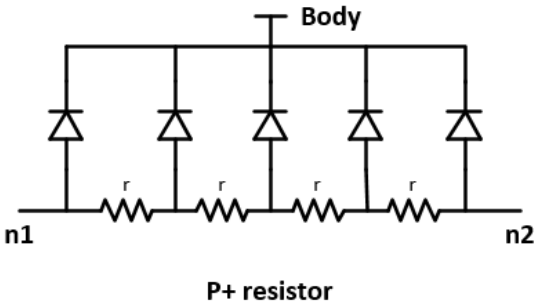


Figure 2.3: TSMC model for p+ diffusion resistor.

For the comparison, the reverse-biased junction capacitances of these diodes were retrieved from the dc operating point analysis. Then, they were summed up to obtain the total capacitance of one arm. The hand calculation was done by multiplying the trapezoidal segment area by the junction capacitance density provided by the model files of Cadence. The results are presented in Table 2.1.

	Hand calculations	Extraction
Resistance	231Ω	228Ω
Capacitance	270fF	277fF

Table 2.1: Extracted vs. hand-calculated electrical properties of Segment #1 in Figure 2.1(b)

Looking at the table above, it can be concluded that the rectangular area approximation done by Calibre can reliably extract the electrical properties of an octagonal ETF thermophile. Hence, the characterization of the ETFs would be accurate.

2.1.2 Octagonal ETFs in 180 nm

The ETFs characterized in this chapter aim to investigate the effects of the ETF geometry on sensor performance. Therefore, they are designed with three different heater-to-sensor distances: $6\mu m$, $12\mu m$, and $17\mu m$. As explained in the previous chapter, the temperature

information will be extracted from the phase component ϕ_{ETF}, by the given relation in Eq. 1.5. To enable the use of a single readout circuit, all the ETFs should be driven at a frequency that creates the same phase response over temperature. Therefore, the relation between s and f_{drive} is kept the same as the reference TD sensor in [15] ($s = 24\mu m$, $f_{drive} = 28.75kHz$). The resulting f_{drive} values for different ETF designs can be seen in Table 2.2.

s	24µm (reference)	17µm	12µm	6µm
f_{drive}	28.75kHz	57.3kHz	115kHz	460kHz

Table 2.2: Corresponding driving frequencies for ETF designs with different s values

The limited bandwidth of the ETFs corresponds to a phase error in the output, ϕ_{ETF}. The spread of this error will contribute to the inaccuracy of the TD sensor. To estimate the corresponding temperature error spread, the output phase sensitivity (6.25°C/º) of the reference TD sensor in [15] is used. By keeping the same relation between s and f_{drive} as the reference design, the same sensitivity can be used to convert the phase errors into temperature errors.

For the simulation, the differential version of the bottom circuit in Figure 1.6 is used. The simplified test bench can be seen in Figure 2.4. Every p+ diffusion arm is represented with a 3-terminal resistor having the extracted resistance and a portion of its junction capacitance on each side. Each ETF is octagonal, and every octagon has two p+ diffusion arms as previously shown in Figure 2.1(b). Hence, there are sixteen 3-terminal resistors in total. The third terminal of the resistors, the n-well biasing node, is connected to VDD=1.8V, and the signal dc level is set to VDD/2=0.9V. The test bench is run with an AC current source and the characterization is done by observing the magnitude and phase responses of V_{ETF}.

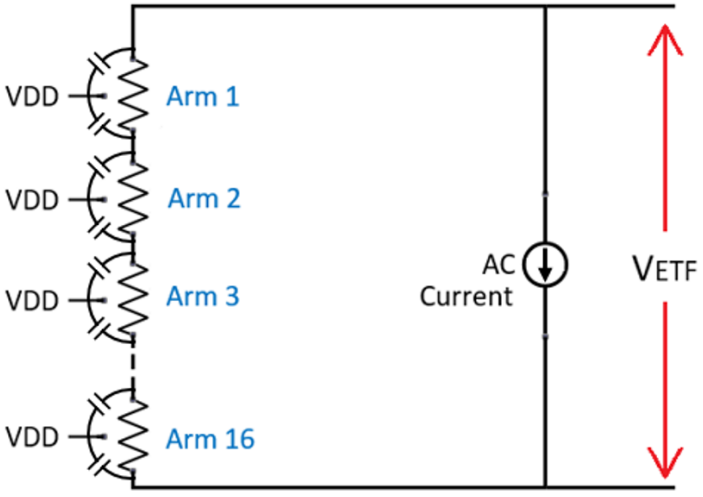


Figure 2.4: Simplified test bench for ETF characterization.

The ETFs in this chapter were laid out by colleagues in the Electronic Instrumentation group and only the characterizations were done as a part of this project. Hence, the individual layouts are not presented.

The magnitude responses of the four ETFs listed in Table 2.2 are plotted in Figure 2.5. Each ETF is named after its *s* distance, i.e., s24, s17, s12, and s6. The DC value represents the total resistance of the ETFs since the magnitude of the ac current source is 1A. The markers show the 3dB bandwidth of each design.

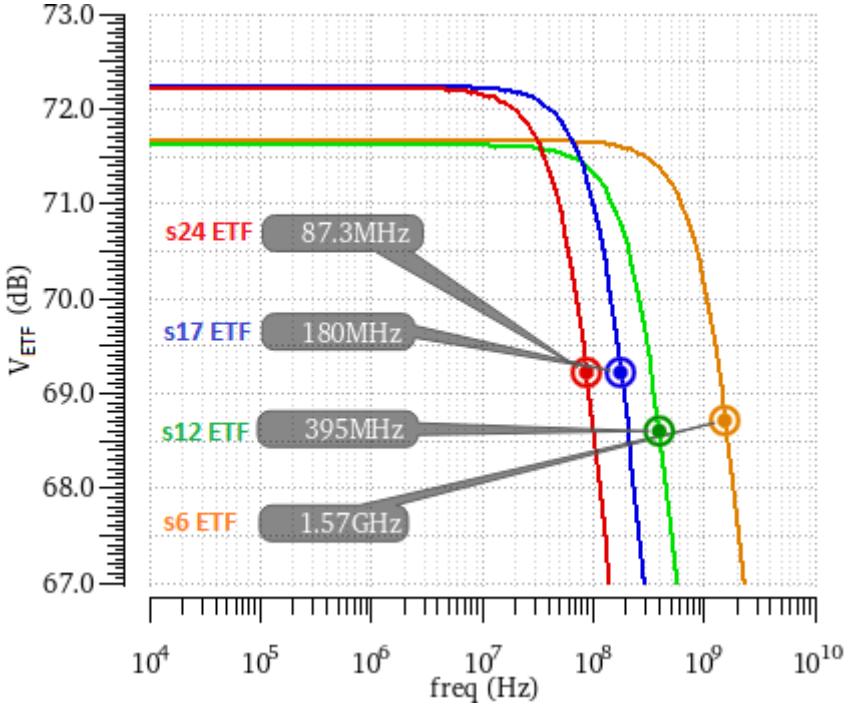


Figure 2.5: Magnitude response of V_ETF for all ETF designs.

The perpendicular distance between the two ends of the thermopile arms (its effective length) is set equal to the distance *s* for maximum SNR [5]. Hence, with reduced *s*, the length of the p+ diffusion arms also reduces. This means a proportional decrease in the effective width and length of the arms, resulting in no significant change in the resistance of the arm. And this is observed by looking at the magnitude response in Figure 2.5. The variation in the total resistance is less than 7% of the reference ETF.

When the effective width and length change proportional to *s*, the area, and consequently the inherent capacitance, of an arm change proportional to s^2. Knowing that the total resistance does not vary significantly, the 3dB bandwidth should change with respect to the capacitance, and thus, increase with smaller *s* values. From the plot in Figure 2.5, the expected change is observed. Taking s6 and s12 bandwidths as an example, the *s* value doubles from s6 to s12, and the bandwidth reduces to almost one-fourth (1.57GHz to 395MHz).

To observe the spread in the additional phases, the phase responses of the four ETFs are plotted over the corners in Figure 2.6. Every ETF is analyzed at the corresponding driving frequency listed previously in Table 2.2.

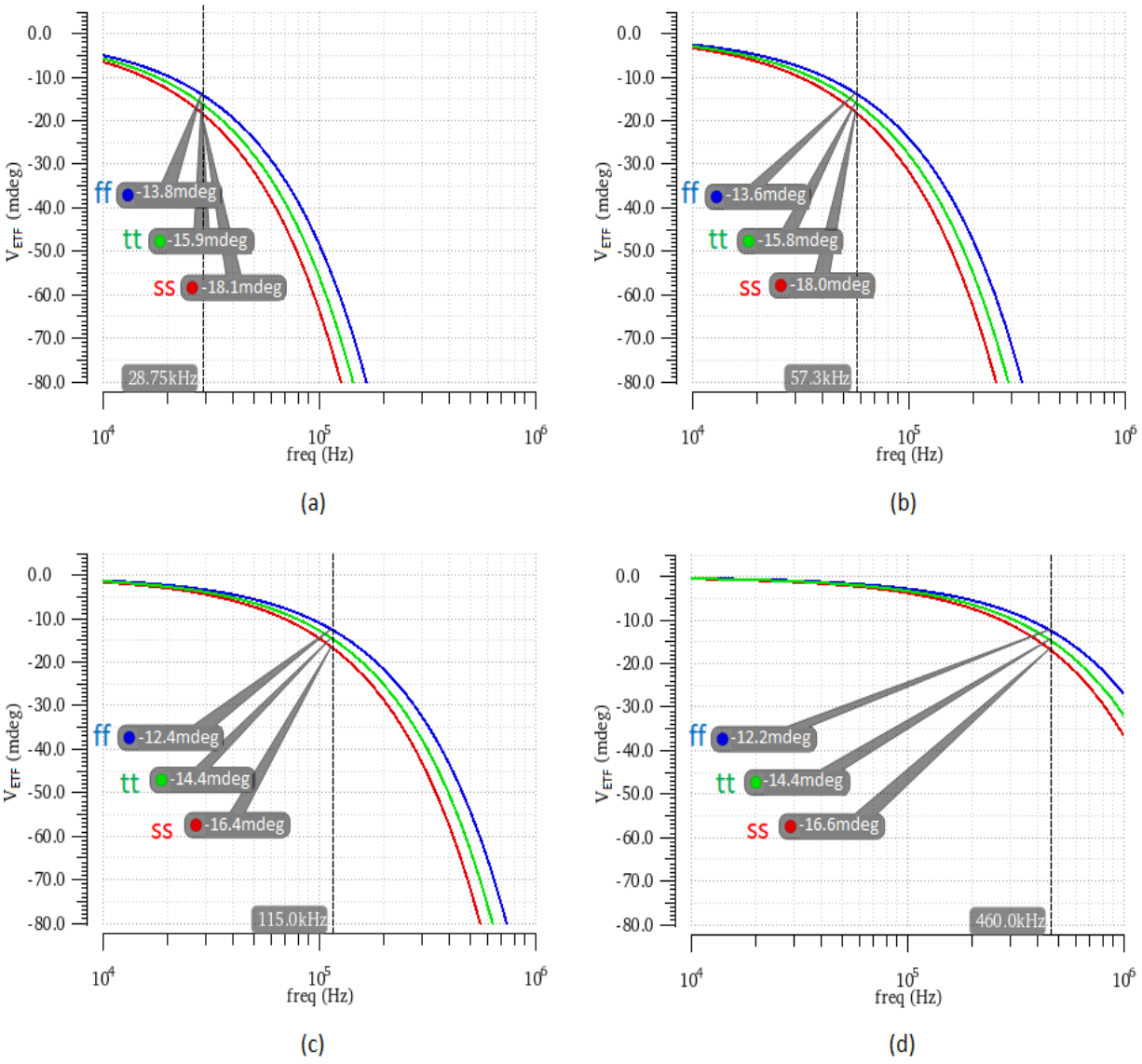


Figure 2.6: Phase responses over the corners for s24 (a), s17 (b), s12(c), and s6 (d).

By using the previously mentioned phase sensitivity of 6.25°C/º, the phase spread over the corners in Figure 2.6 is converted to temperature spread in Table 2.3.

	s24			s17			s12			s6		
Corners	ff	tt	ss	ff	tt	ss	ff	tt	ss	ff	tt	ss
Phase delay (mdeg)	13.8	15.9	18.1	13.6	15.8	18.0	12.4	14.4	16.4	12.2	14.4	16.6
Temperature spread over corners (℃)	±0.014°C			±0.014°C			±0.012°C			±0.014°C		

Table 2.3: Phase delays and corresponding temperature spreads of the four ETF designs.

Looking at the temperature spread over the corners in the table above, it can be concluded that the ultimate accuracy of the ETFs is limited to about ±0.014°C. However, in [15], the

measured 3σ inaccuracy of the reference s24 TD temperature sensor is 0.5°C. Hence, the accuracy of this sensor is probably not limited by the RC-limited bandwidth of the ETF.

2.2 Multiplexing 8 ETFs

Besides the octagonal ETFs introduced in the previous section, four other thermal-diffusivity-based sensing elements for temperature sensors were designed by colleagues in the Electronic Instrumentation group to investigate other aspects affecting the TD sensor performance besides *s*. Hence, there were 8 different temperature-sensing elements to be tested. To observe only the effect of the sensing element on the performance of the temperature sensor, all the front ends should have the same read out circuits.

For this purpose, the phase domain delta-sigma modulator (PDSDM) used in the reference TD sensor in the previous subsection was preferred. The circuit diagram of this sensor is shown in Figure 2.7.

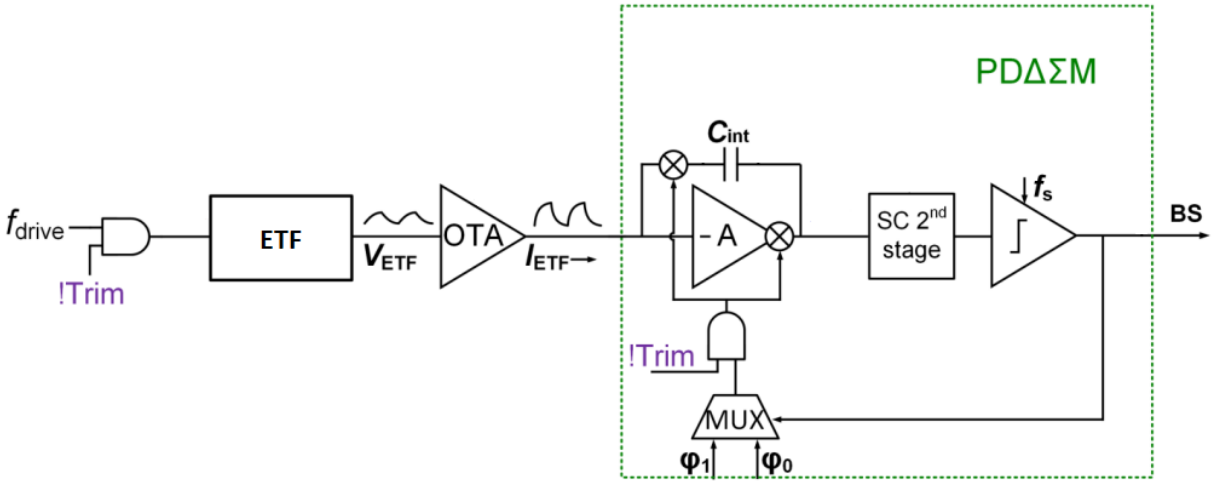


Figure 2.7: The reference TD sensor with the phase domain readout [15].

Implementing 8 sigma-delta modulators will require more area, which consequently, increases cost. Instead, the 8 ETFs can be multiplexed to the same readout circuit. The multiplexing node should be selected carefully, considering the phase error and thermal noise introduced by the switches. The former would affect the accuracy and the latter will degrade the resolution.

Since the output of the ETF will be at the mV level, it is first boosted by an OTA as seen in Figure 2.7. In [15], this OTA consisted of a telescopic amplifier, as shown in Fig. 2.8.

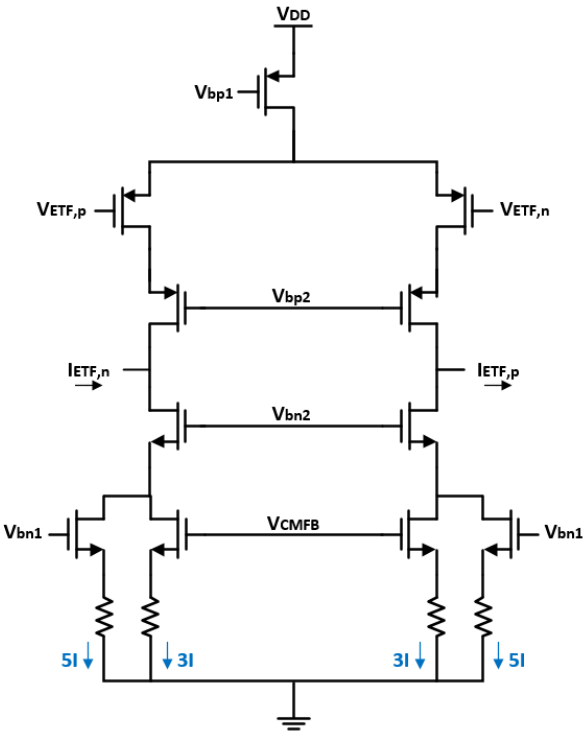


Figure 2.8: The telescopic OTA used in [15].

Three nodes of the OTA in Figure 2.8 were proposed for the multiplexing of the ETFs to the readout circuit. The first and most straightforward multiplexing node would be the input of the OTA. In this option, all of the ETF designs are connected to the gates of the input pair with switches, as presented in Figure 2.9

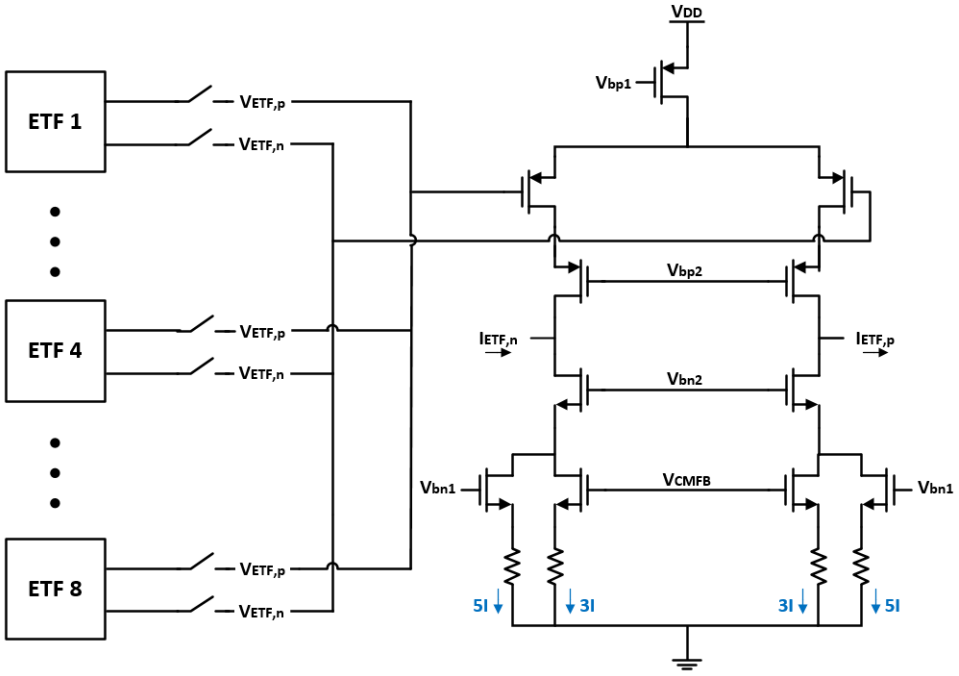


Figure 2.9: Multiplexed ETFs with a common readout circuit.

This is the most advantageous choice considering the chip area, however, the 8 switches connected to the input node of the OTA introduce parasitic capacitances. Since this is the ETF

output node, the switch parasitic capacitance is directly added to the intrinsic capacitance of the ETF, increasing the additional phase error mentioned in the previous section. Additionally, when the switches are sized to keep the parasitic capacitance lower, the on-resistance of the switches increases. This can result in an on-resistance that is comparable to the ETF resistance which is a few $k\Omega s$. Then the additional thermal noise of the switches becomes significant, degrading the resolution of the sensor.

The other two options are the internal nodes of the OTA, this requires some portion of the OTA to be replicated 8 times for each of the ETFs. The first multiplexing node in the OTA is the one between the PMOS input pair and the PMOS cascode transistor. For this option, the multiplexed element would consist of an ETF and the input pair of the telescopic OTA. The second option is the output node, right after the PMOS cascode transistors. For this, the multiplexed block would consist of an ETF, the input pair, and the PMOS cascodes. The aforementioned multiplexing elements with the necessary switches are presented in Figure 2.10.

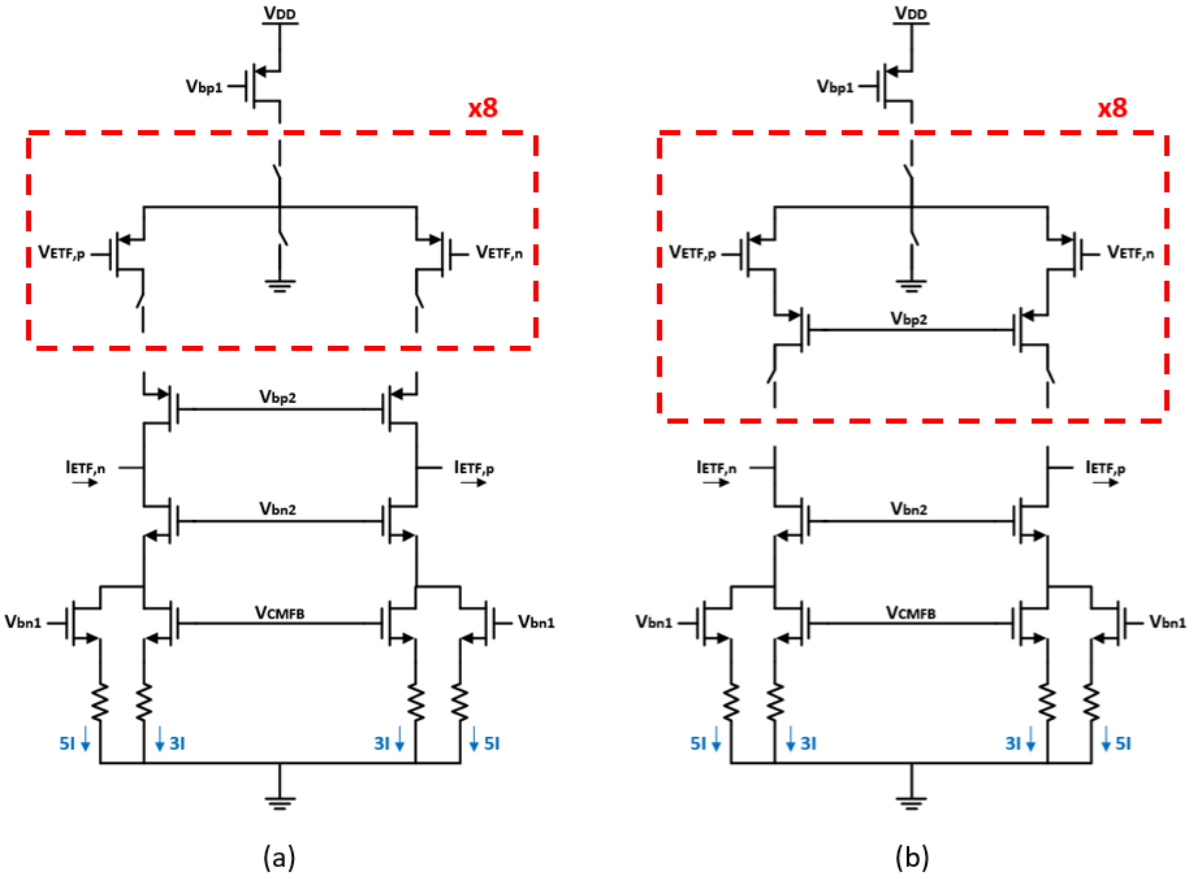


Figure 2.10: Multiplexed OTAs for Option 1 (a), and Option 2 (b).

The options in Figure 2.10, are both advantageous concerning the additional thermal noise compared to the multiplexing node at the input pair. Since the switches connected to the drains of the PMOS transistors in Figure 2.10 (a) and (b) are already at high resistance nodes, the on-resistance of the switches is not crucial. Hence, the switch sizes can be reduced to minimize parasitic capacitance. Due to the gate capacitance of the input pair, the output node

of the ETF is the dominant source of phase error. That is why both of the options presented in Figure 2.9 introduce less phase error to the system than multiplexing the ETFs at the input of the OTA. The only downside of choosing an internal node for the multiplexing is the increased area compared to choosing the input node. However, seeing as performance had priority over area reduction in this project, the decision should be made from the two options in Figure 2.10 (a) and (b).

The additional thermal noise for Options 1 and 2 is comparable. Furthermore, the additional phase error is not significantly less for one of the options. Hence, the choice is made based on the simplicity of the implementation. Multiplexed block in Option 1 has the ETF and the input pair of the OTA. The gate of the input pair is biased by the common mode level of V_{ETF} hence, no biasing is needed in the block. On the other hand, adding the PMOS cascodes to the multiplexed block in Option 2 requires additional biasing for the cascodes. This adds complexity and additional area. Moreover, the common mode voltage for the switches in Option 1 is close to VDD, whereas, in Option 2, it is closer to VDD/2. Hence, the switches in Option 1 can be implemented by PMOS transistors but more complex switches might be needed for Option 2. Therefore, Option 1 was selected to be used while multiplexing the 8 ETFs to the readout circuit in Figure 2.7.

The multiplexed block in Figure 2.10 (a) is presented in Figure 2.11. The block includes the input pair of the OTA and four switches for multiplexing. The connection nodes to the rest of the OTA are labeled as A, B, and C. Node A connects the input pair to the PMOS current source in Figure 2.10 (a), whereas nodes B and C are attached to the PMOS cascodes of the OTA. When DISABLE signal is high, the three PMOS switches turn off and the NMOS switch connected to the ground turns on. This means that the corresponding input pair along with the ETF is effectively disconnected from the OTA for a "DISABLE: HIGH", hence, the desired ETF design out of the 8 can be selected by grounding the DISABLE node.

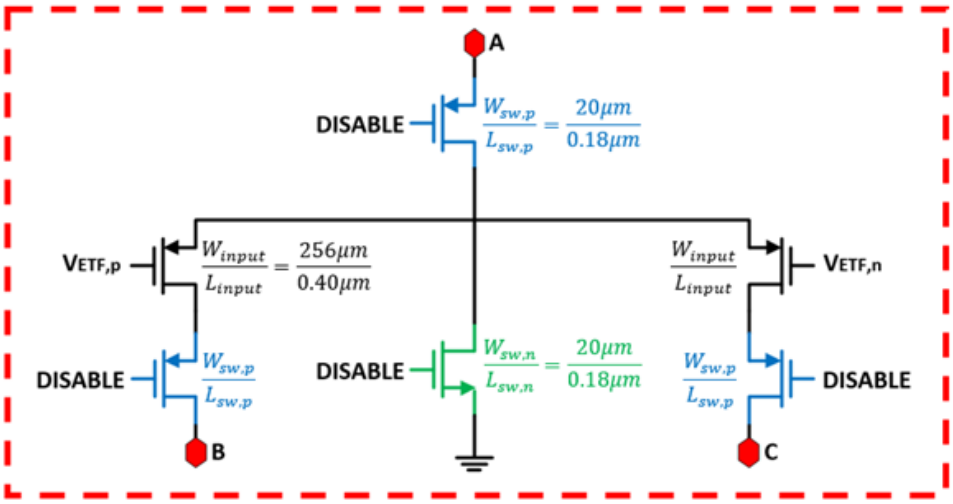


Figure 2.11: Multiplexed block of the OTA.

For the sizing of the switches, it was necessary to establish the tolerable amount of added phase error considering the aimed inaccuracy of the temperature sensor. The reference TD sensor in [15] achieves 0.5°C inaccuracy with a phase sensitivity of 6.25°C/º at the output.

Hence, 10% of this inaccuracy was decided to be a tolerable added temperature error. Using the sensitivity of the same sensor, 0.05°C of temperature error was converted to 0.008 º phase error. The test bench in Figure 2.12 was used to assess the performance after multiplexing the ETFs.

For the simulations, the same ETF design, s24, was connected to all the inputs. Only one of the input pairs was enabled and the transfer function of the OTA, its transconductance, was compared with the original circuit without the multiplexing switches. The test bench for the original circuit consisted only of the s24 ETF and the OTA with the same as the multiplexed circuit in Figure 2.12.

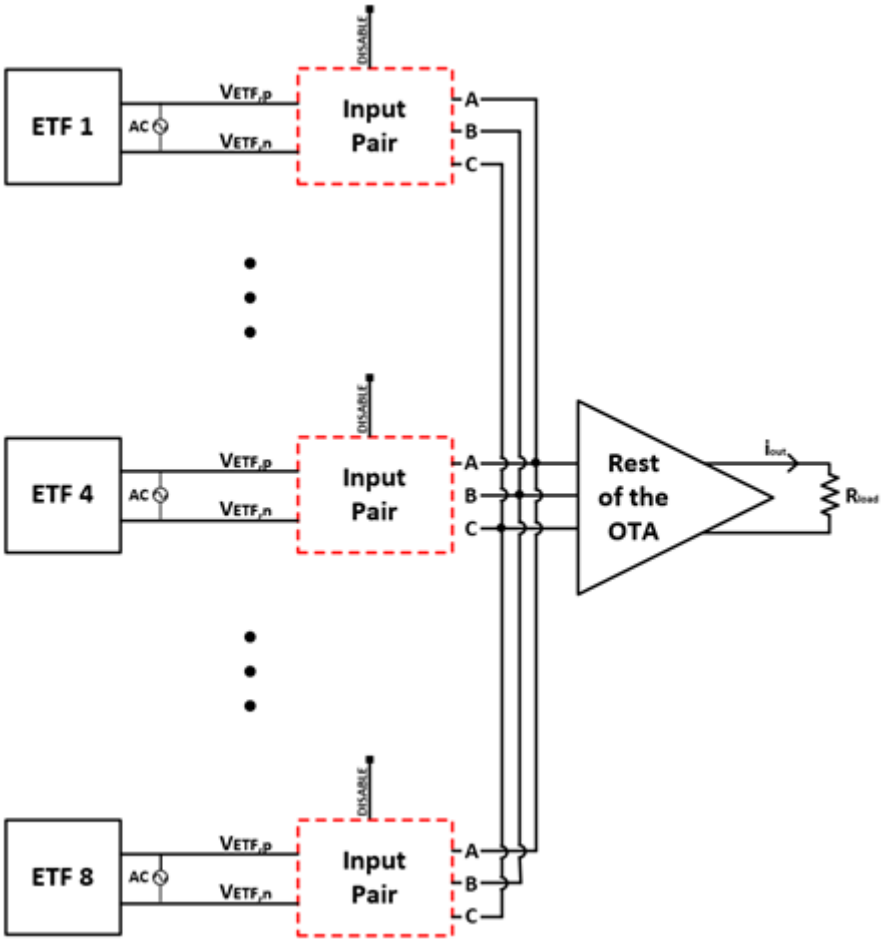


Figure 2.12: The simplified test bench for the multiplexed readout circuit.

The comparison was made regarding the phase responses of the OTA transconductances. The phase errors of s24 were compared in Figure 2.13.

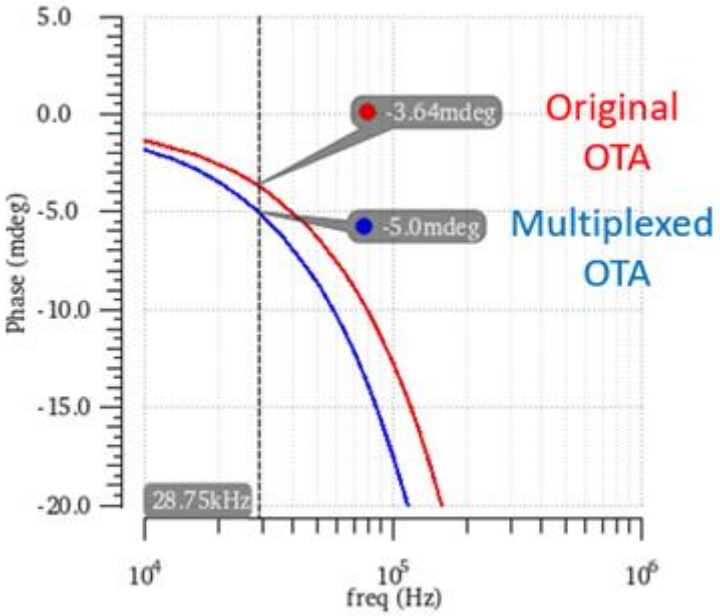


Figure 2.13: Phase responses of the original and the multiplexed OTA.

As seen in Figure 2.13, the additional phase after the multiplexing is 1.36mº (8.5m°C in temperature) at the driving frequency with the determined switch sizes in Figure 2.11. This is an absolute error, whereas the previously calculated tolerable phase error, 8mº, represents the spread of the additional phase error. Since the absolute error is already almost 6 times lower than the tolerable spread, it can be concluded that the proposed multiplexing scheme can be used for the testing of the 8 ETFs.

3 TD Temperature Sensor in 65nm

Another aspect affecting the performance of the ETFs is the CMOS technology. Scaling the ETF designs to more advanced CMOS processes promises better sensor accuracy [5]. Hence, in this chapter, some of the ETF designs and the readout circuits are scaled down to 65nm from the 180nm process.

3.1 ETF Layouts & Characterization

Two of the ETF designs characterized in the 180nm process in the previous chapter, s6, and s12, are scaled to a 65nm process to observe the effect of the improved lithography on the accuracy and resolution of TD temperature sensors.

Similar to what was done in Chapter 2, the ETFs have to be characterized to observe their intrinsic bandwidth and spread over the corners. However, due to the differences in the layout editors between the two processes, the layouts could not be transferred directly to the 65nm process. Hence, the ETFs had to be redrawn.

3.1.1 Thermopile Layouts and Characterization

As thoroughly explained in the previous chapter, the intrinsic bandwidth of an ETF is limited by the RC behavior of its thermopile. Therefore, first, the thermopile layouts of s6 and s12 ETFs are presented in Figures 3.1 and 3.2 and then the ETFs are characterized.

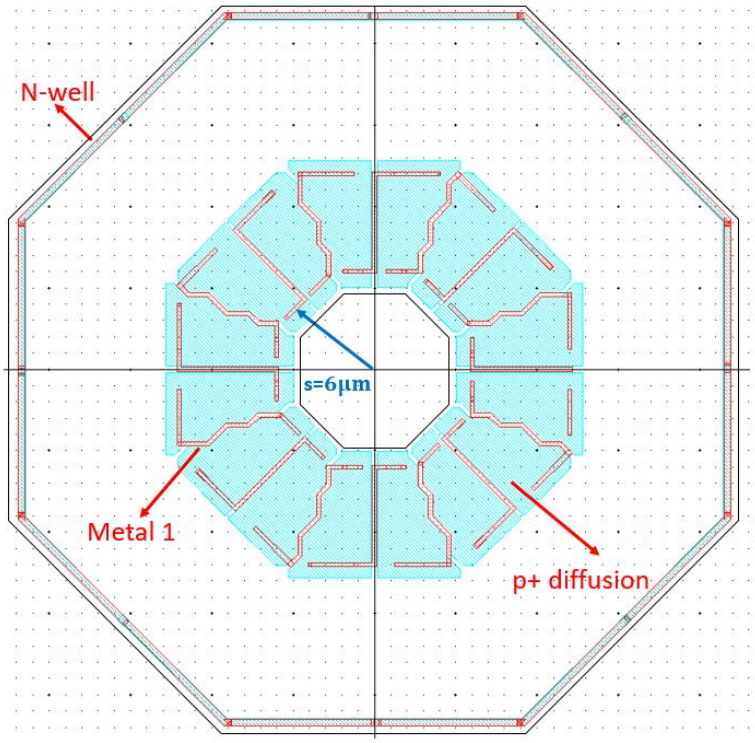


Figure 3.1: s6 thermopile layout.

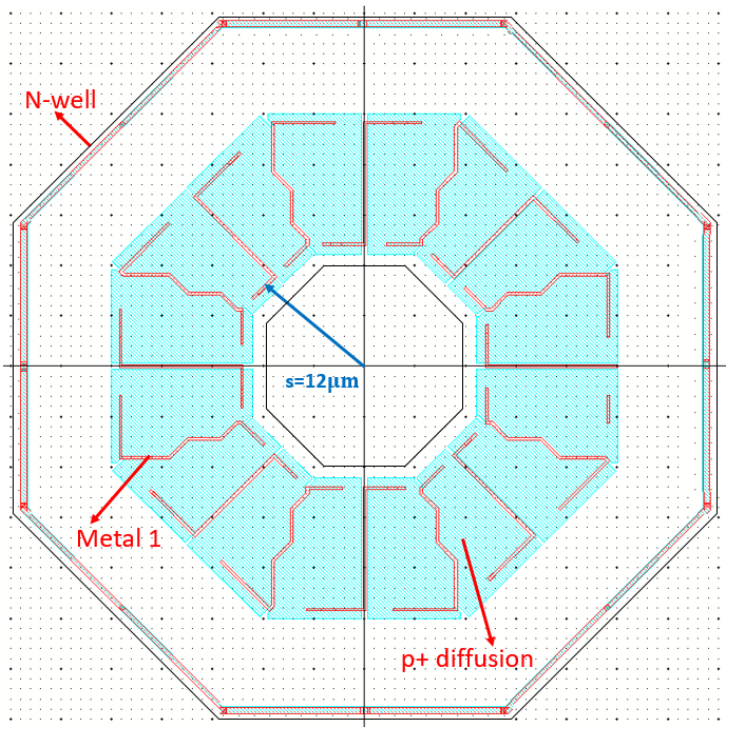


Figure 3.2: s12 thermopile layout.

For readability, only 3 layers of the thermopile layouts are shown in Figures 3.1 and 3.2: n-well, metal 1, and p+ diffusion. s6 and s12 thermopile designs are both kept the same as the ones in 180nm that are characterized in Chapter 2. Furthermore, since D_{Si} is a process-independent parameter, the relations between *s* and f_{drive} presented in Table 2.2 remain the same. Hence, the f_{drive} values used for the s6 and s12 ETFs in Table 2.2 are again used during the characterization in this section.

The same test bench (Figure 2.4) is also used for the characterization. The only difference is the VDD voltage level which decreases to 1.2V from 1.8V. This modification is necessary due to technology node change. Therefore, the common mode voltage on the signal path is arranged to 0.6V to maintain VDD/2 reverse biasing on the p+ diffusion/n-well junction. Then the magnitude and phase responses of V_{ETF} are observed for characterization.

The magnitude responses of the two ETFs are plotted in Figure 3.3. The DC value of V_{ETF} represents the total resistance of the ETFs since the magnitude of the ac current source is set to 1A. The markers show the 3dB bandwidth of each design.

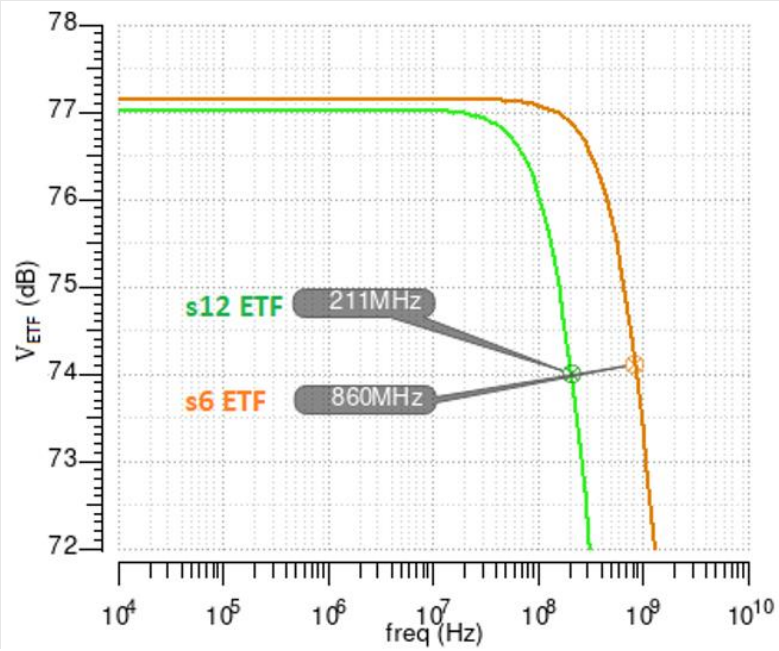


Figure 3.3: Magnitude response of V_{ETF} for the two ETF designs.

In the magnitude responses plotted in Figure 3.3, the total resistances of s6 and s12 are almost the same (0.1dB difference), which is expected for the reasons explained in Chapter 2. Moreover, the bandwidth should scale inversely with s^2 from the findings in Chapter 2 and this is observed when the bandwidths of s6 and s12 are compared from the magnitude plot. From s6 to s12, *s* doubles and the intrinsic bandwidth reduces to almost a quarter.

By looking at Figures 2.6 and 3.3, the differences in the magnitude responses between 180nm and 65nm processes can be observed. For the convenience of comparison, the total resistances and intrinsic bandwidths of each ETF are retrieved from the plots and presented in Table 3.1.

	Total Resistance (dB)		**Intrinsic Bandwidth (f_{-3dB}, MHz)**	
	180nm	65nm	180nm	65nm
s6	71.8	77.1	1570	860
s12	71.7	77.0	395	211

Table 3.1: Magnitude response comparison between the 65nm and 180nm processes.

Firstly, looking at the total resistance values in Table 3.1, there is a 5.3dB difference between the technologies for both s6 and s12 ETFs. This amount in dB corresponds to a 1.8 times increase in the total resistance of each thermopile. Even though the thermopile designs are the same, the sheet resistance of the p+ diffusion layer in the 65nm process is around 1.8 times higher than the one in 180nm. Hence, this increase in the total resistance is expected. Secondly, s12 and s6 ETF intrinsic bandwidths are reduced by 1.87 and 1.83 times, respectively. The bandwidth is inversely proportional to the total resistance and the junction

capacitance. Since the decrease in the bandwidths is almost the same as the increase in the total resistances, it can be concluded that the junction capacitance does not differ significantly between the two processes.

As explained in the previous chapters, the intrinsic bandwidth of the ETF causes an additional phase error in ϕ_{ETF}. And the spread in the additional phase at f_{drive} contributes to the sensor's inaccuracy. Hence, the phase responses of the two ETFs are plotted over the corners in Figure 3.4.

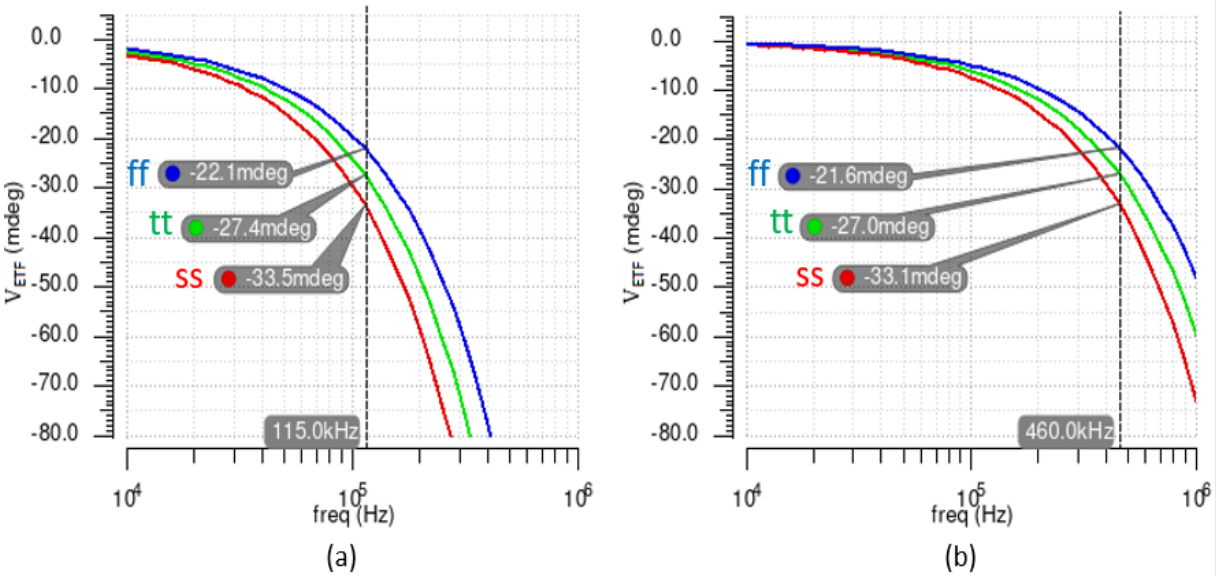


Figure 3.4: Phase responses over the corners for s12 (a) and s6 (b).

For compatibility, the output phase sensitivity (6.25°C/º) of the reference TD sensor in [15] is used to estimate the corresponding temperature error spread and the results are presented in Table 3.2.

	s12			s6		
Corners	ff	tt	ss	ff	tt	ss
Phase delay (mdeg)	22.1	27.4	33.5	21.6	27.0	33.1
Temperature spread over corners (℃)	±0.038°C			±0.038°C		

Table 3.2: Phase delays and corresponding temperature spreads of the ETF designs.

Looking at the spread of the temperature errors over the corners in the table above, it can be concluded that the ultimate accuracy of the ETFs is limited to about ±0.038°C due to its intrinsic bandwidth. Whereas, the ultimate accuracy for the 180nm process is ±0.015°C as calculated in Chapter 2. However, the increased inaccuracy due to the spread in the intrinsic bandwidth should not be detrimental since it is found in Chapter 2 that the main accuracy limitation comes from the lithographic misalignment and is significantly higher than the inaccuracy numbers stated above.

3.1.2 Heater Design & Layout

The U-shaped heater introduced in Chapter 1 is used for all the ETF designs in the 180nm process. The same shape is maintained for the ETFs in the 65nm process. However, the increase in the sheet resistance from the 180nm to 65nm process also applies to the heater's n+ diffusion layer. Furthermore, the supply voltage reduces to 1.2V as mentioned previously. Then looking at Eq. 3.1, the heater should be resized to maintain $\mathrm{P_{heat}}$ similar to the TD sensor in 180nm. The equation includes a 0.5 coefficient since the heater signal is a square wave switching between VDD and ground.

$$P_{heat} = \frac{1}{2} * \frac{V_{DD}^2}{R_{heater}} \tag{3.1}$$

Considering the previous TD sensors, $\mathrm{P_{heat}}$ was decided to be around 2.5mW. Using this value and VDD=1.2V in Eq. 3.1, R_{heater} was calculated to be 288Ω. The heater designed with these specifications is presented in Figure 3.5.

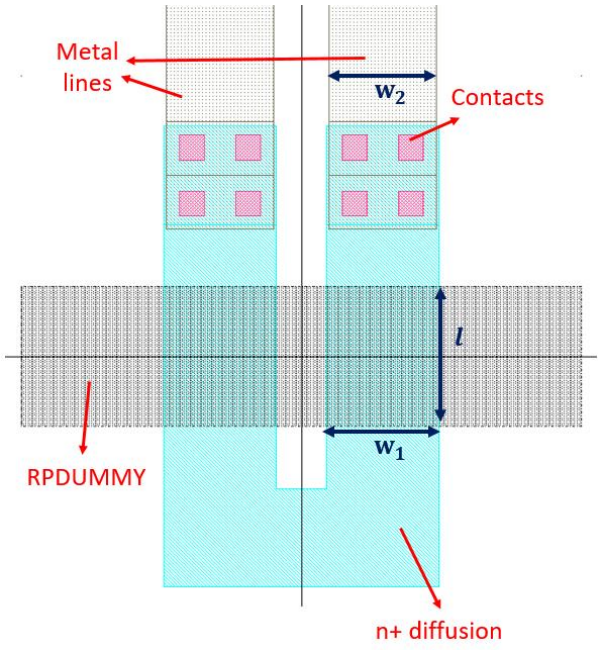


Figure 3.5: Heater design for the ETFs in 65nm process.

The resistance of the heater in Figure 3.5 is calculated using the intersection area of RPDUMMY and n+ diffusion layers. Since the aim is to minimize the heater area for a point-heater approximation, minimum resistor width of $0.4\mu m$ was used as w_1. The length "l" was selected as $0.5\mu m$ considering the sheet resistance of the n+ diffusion layer to obtain 260Ω from the intersection area. The 28Ω margin was left considering the remaining areas outside the RPDUMMY layer.

The number of contacts had to be decided based on the average current that would flow through the heater. From Ohm's law, knowing R_{heater} and VDD, the average current was calculated as 2.1mA. Then, the 65nm process documentation was examined to determine the number of contacts that can handle this average current. The 2x2 contact array shown in

Figure 3.5 was selected because the maximum current it allows, 2.4mA, was higher than the expected average current.

The last decision was the width of the metal line that would carry the heater signal, labeled as w_2 in Figure 3.5. Again, considering the calculated average current, w_2 was chosen as $0.38\mu m$ which would allow 2.7mA as the maximum current according to the 65nm process documentation.

3.1.3 ETF Shielding

The heater is placed at the center of the octagonal ETF as shown in Figure 3.6. Hence, the heater signal passes above the thermopile structure. Since the amplitude of V_{ETF} is only a few mVs, any coupling between the heater and the output signal lines would be detrimental for V_{ETF}. Therefore, either the heater lines or the thermopile outputs should be shielded. The n-well bias, Vcm, and V_{ETF} seen in Figure 3.6 are all drawn on the same metal layer, M1, whereas another metal layer is used for the heater signal along with the shielding lines.

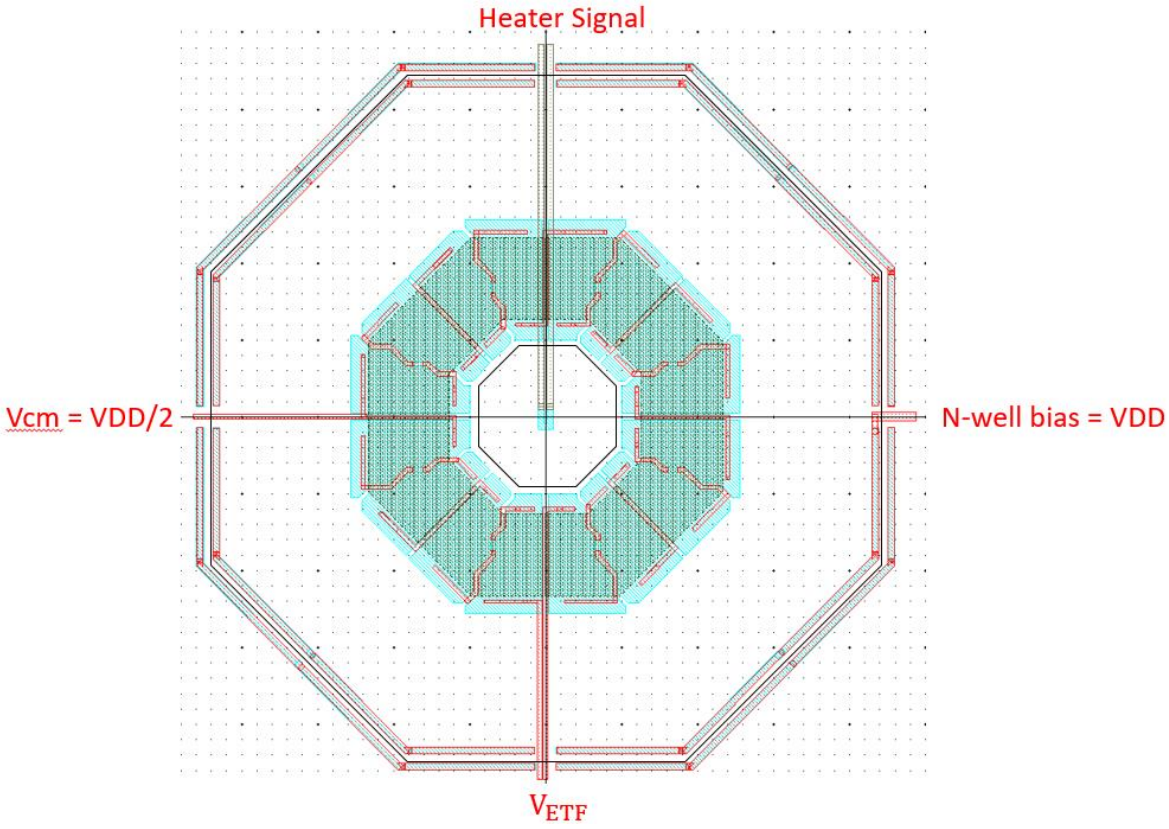


Figure 3.6: An ETF structure with signal lines.

The first option that was also used in the previous TD sensors in 180nm is shielding the heater. This is done by placing the heater signal line in between two metal traces that are connected to the ground. This way, the voltage level changes in the heater signal would not be affecting the thermopile output signal. The layers used for the shielding are presented in Figure 3.7.

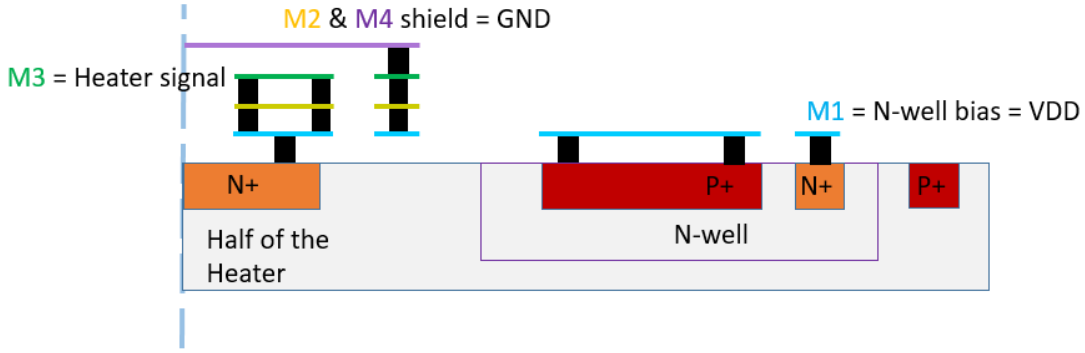


Figure 3.7: The cross-section at the horizontal centerline (right half).

Since the M1 layer is used for the n-well bias, Vcm, and V_{ETF}, the bottom metal trace for the shielding is selected as the M2 layer. Then, the M3 layer is used to carry the heater signal and the shielding is finalized by using the M4 layer as the top metal trace. M2 and M4 traces are connected to the ground. The layout of the heater shielding is presented in Figure 3.8.

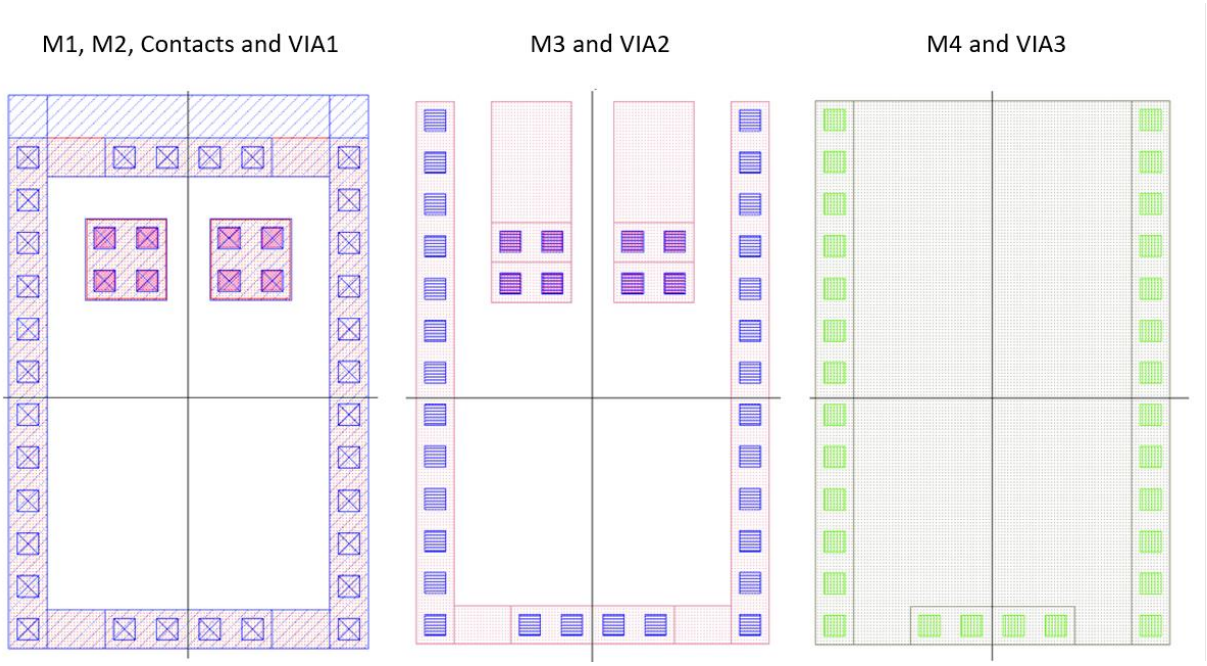


Figure 3.8: The metal layers and contact/vias used for the heater shielding.

The second option is to shield the thermopile instead of the heater. Since there is no metal layer available under the diffusion layer, the shielding is done by covering the p+ diffusion thermopile with a metal layer that is connected to the ground. The cross-section of this option is presented in Figure 3.9.

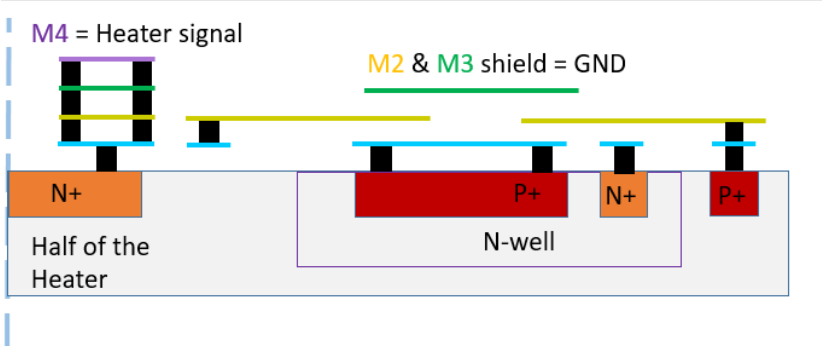


Figure 3.9: The cross-section at the horizontal centerline (right half).

In layout rules, each metal layer has a maximum width that must be followed. The radius of an ETF is several times the maximum allowed width. Therefore, two different metal layers, M2 and M3, are used together to shield the thermopile. And the heater signal is carried on an M4 trace. The layout of the thermopile shielding is presented in Figure 3.10.

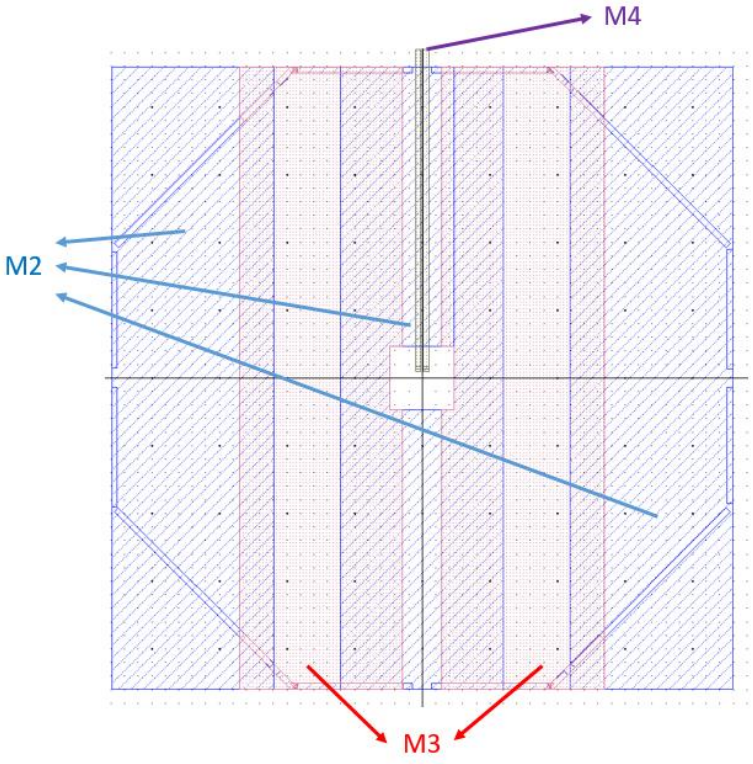


Figure 3.10: The metal layers used for thermopile shielding.

Comparing the two shielding options, Option 1 offers to shield the heater signal from both the top and bottom sides, whereas, in Option 2, the thermopile is only shielded on top. However, covering the thermopile enables better isolation for V_{ETF} considering any other possible interaction besides the heater signal. The downside of Option 2 is the additional RC delay due to the parasitic capacitance coming from the added metal layers. However, after running simulations with the added metal layers of M2 and M3, and looking at the intrinsic bandwidth of the ETFs, it was seen that the decrease in the intrinsic bandwidth is not significant (<10%). Furthermore, looking at the measurement results of s6 and s12 ETFs in 180nm that were prepared by a colleague in the Electronic Instrumentation group, shielding of the thermopile

was suggested to obtain better results. Therefore, Option 2 was selected for shielding s6 and s12 ETFs in the 65nm process. The final layouts including the shielded thermopile and the open heater for s6 and s12 ETFs can be seen in Figures 3.11 and 3.12.

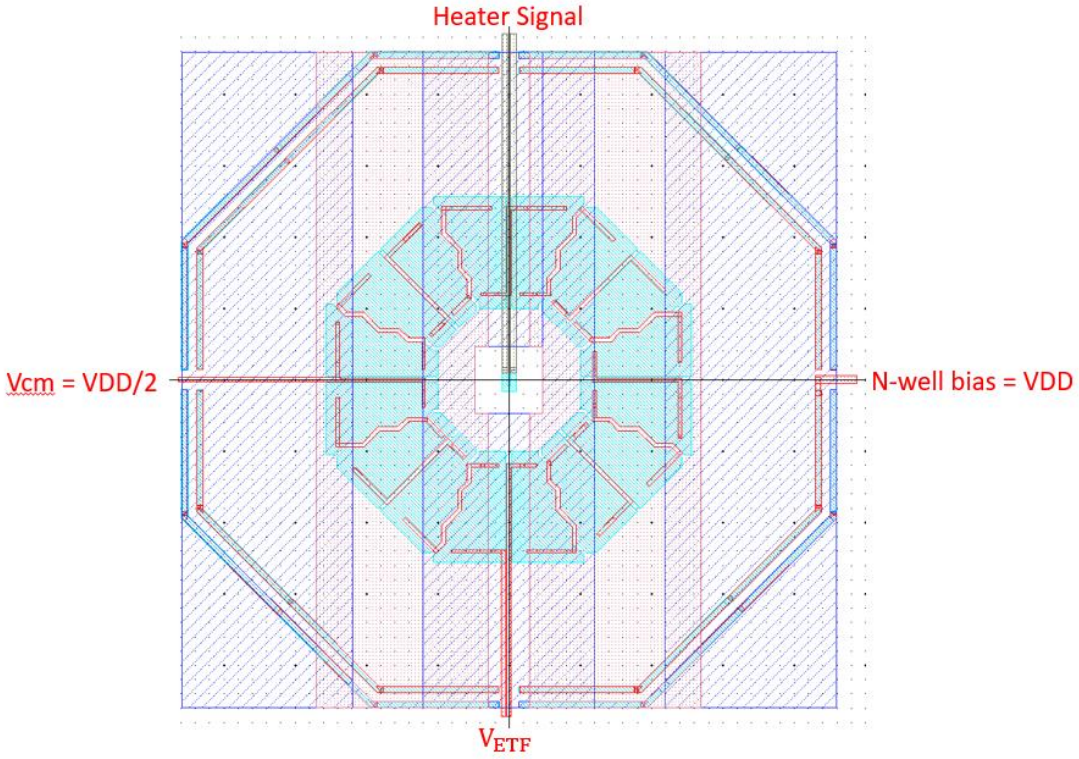


Figure 3.11: The shielded s6 ETF.

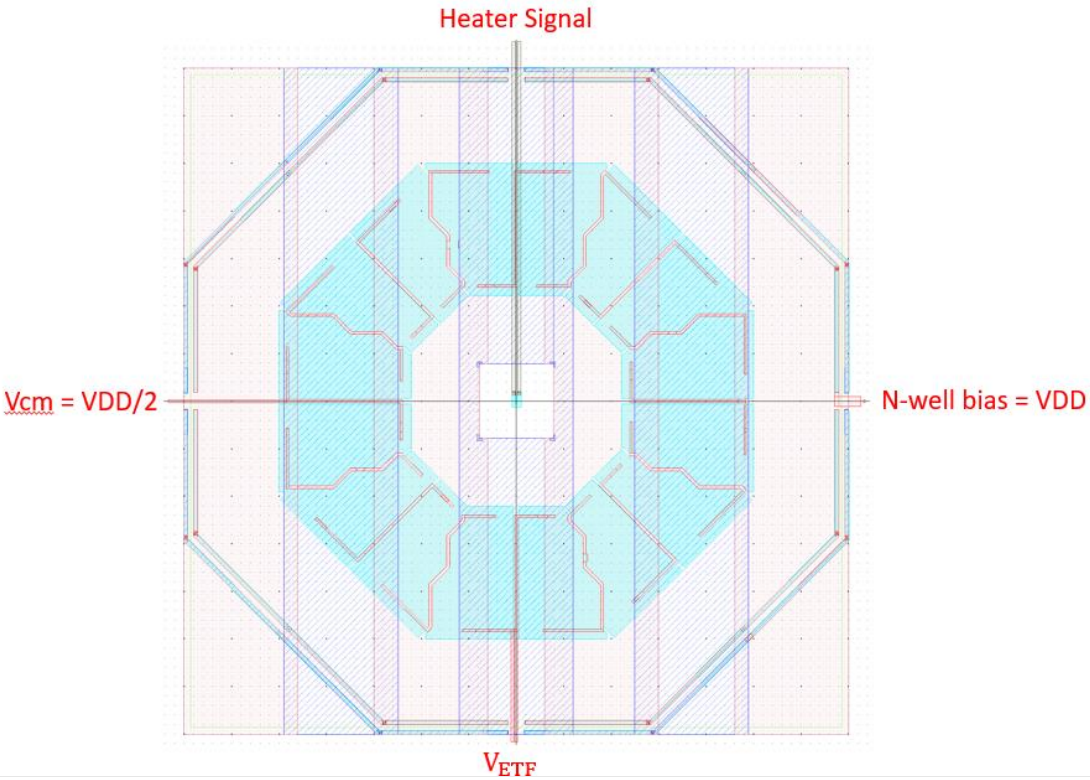


Figure 3.12: The shielded s12 ETF.

Figures 3.6 and 3.10 present the layouts of s6 ETF for simplicity. All the shielding layers are kept the same for s12 ETF and the only difference is the additional M3 shielding layers on both sides as seen in Figure 3.12. This is due to the aforementioned maximum width of the metal layers and s12 being wider than s6. Therefore, these M3 layers are added to fully cover the s12 ETF.

3.2 Phase Domain Delta-Sigma Modulator

In Chapter 1, the readout circuits that are used for the ETF-based temperature sensors were discussed. In the end, $PD\Delta\Sigma M$ is decided to be the best candidate for ETF readout due to its high-resolution capability and phase-to-digital conversion.

3.2.1 Design Considerations and Overview

For the reference s24 TD sensor in [15], the readout circuit is a second-order $PD\Sigma\Delta M$ shown in Figure 2.7. To suppress the quantization noise, sampling frequency, f_s, is set equal to f_{drive} which is $28.75kHz$ for s24. However, for s6 and s12, f_{drive} increases to $460kHz$ and $115kHz$, respectively. Since $f_s = f_{drive}$, the $PD\Delta\Sigma Ms$ for s6 and s12 will have higher f_s, consequently, higher oversampling ratios (OSRs). Therefore, a first-order $PD\Delta\Sigma M$ could offer sufficient quantization noise suppression for the sensor resolution to be dominated by ETFs' thermal noise.

To decide on the order of the modulator and set specifications for the $PD\Delta\Sigma M$, the inaccuracy caused by the front-end, the ETF, should be established. The accuracy of the sensor would be limited by the lithographic misalignment in the ETF as explained previously. Hence, the temperature errors due to the lithography errors are estimated by Eq. 1.7 and presented in Table 3.3.

	s12	s6
Temperature error (3σ)	0.18℃	0.36℃
Phase error	29mdeg	58mdeg

Table 3.3: Temperature inaccuracies and the corresponding phase errors due to lithography error.

While using Eq. 1.7, the lithographic inaccuracy, δs, is assumed to be 10% of the minimum line width of the technology, 6.5nm, and T is selected as room temperature, 300K. The corresponding phase errors are calculated by using the output phase sensitivity (6.25°C/º) of the reference TD sensor in [15].

A high-resolution sensor is designed to have around 10 times better resolution than its inaccuracy. Therefore, the resolution for the s12 sensor should be around 0.018℃ and for the s6, it should be around 0.036℃. The phase range of the reference sensor corresponds to a 300℃ temperature range, [15]. Considering the desired temperature resolutions for the sensors and taking 300℃ as the full range, the resolution of the $PD\Delta\Sigma M$ should be 13 bits for the s6 and 14 bits for the s12.

For higher energy efficiency, a 10dB higher SQNR is targeted so that the overall resolution is limited by thermal noise, which corresponds to an additional 1.5 bits approximately. Therefore, the minimum OSRs required for a first-order DSM can be calculated as follows:

$$\begin{aligned} OSR_{s6} &\approx 2^{13+1.5} = 2^{14.5} = 23170 \\ OSR_{s12} &\approx 2^{14+1.5} = 2^{15.5} = 46340 \end{aligned} \tag{3.2}$$

To decide if a first-order $PD\Delta\Sigma M$ could provide the minimum OSRs, the conversion times, $\mathrm{T_{conv}}$, for the modulators should be estimated. In Eq. 1.8, the resolution dependencies regarding the ETF parameters are presented. The only parameter concerning the readout circuit in this relation is B, the noise bandwidth. For a $PD\Delta\Sigma M$, B has the following relation with the $\mathrm{T_{conv}}$:

$$B = \frac{1}{2T_{conv}} \tag{3.3}$$

Replacing B in Eq. 1.8 with the relation in Eq. 3.3 gives the following resolution dependencies:

$$res \propto \frac{s}{P_{heat}} \sqrt{\frac{4kT(N * R_{tc})}{2T_{conv}}} \tag{3.4}$$

Since the sensitivity of the reference s24 sensor in the 180nm process is assumed to be the same for the sensors in the 65nm process and all the values in Eq. 3.4 are known for the reference sensor, the necessary conversion time for s6 and s12 can be estimated by scaling the reference values.

For simplicity, this is done in two steps. First, the s24 sensor resolution in the 180nm process is scaled for the 65nm process considering R_{tc} has increased 1.8 times due to the increase in the sheet resistance. Also, the heater power has been reduced to 2.5mW from 3.6mW. The conversion time and *s* are kept the same. Hence, the resolution scaled up by 1.93. The scaled resolution is shown in Table 3.4 with the other known parameters.

	180nm	65nm
s	$24\mu m$	$24\mu m$
Heater Power	3.6mW	2.5mW
Conversion Time	1s	1s
Resolution	18mK	35mK

Table 3.4: Resolution scaling from the 180nm to the 65nm process.

The second step is to estimate the necessary conversion time for the s6 and s12 sensors to have the desired resolutions (0.036℃ and 0.018℃) in 65nm. While characterizing the ETFs in Chapter 2 and the first section of this chapter, it is observed and explained why the total

resistance of the thermopile does not differ significantly with changing s. And the same heater is used for both ETFs, meaning the sensors will have the same heater power. Therefore, by using Eq. 3.4, the conversion times are calculated and presented in Table 3.5.

	s24	s12	s6
s	$24\mu m$	$12\mu m$	$6\mu m$
Heater Power	2.5mW	2.5mW	2.5mW
Conversion Time	1s	~1s	~0.06s
Resolution	35mK	18mK	36mK

Table 3.5: Conversion time scaling for the s6 and s12 sensors in 65nm.

After estimating the conversion times for the desired resolutions, the achievable OSRs with a first-order $PD\Delta\Sigma M$ can be calculated as follows:

$$\begin{aligned} OSR_{s6} &= f_s * T_{conv} = 460k * 0.06 = 27600 \\ OSR_{s12} &= f_s * T_{conv} = 115k * 1 = 115000 \end{aligned} \tag{3.5}$$

By comparing the results in Eq. 3.5 and 3.2, due to higher OSR, it can be concluded that the first-order $PD\Delta\Sigma Ms$ as their readout circuits is enough to suppress quantization noise much more than 10dB below the ETFs' thermal noise for both the s6 and s12 sensors. The architecture of the first-order $PD\Delta\Sigma M$ that would be used for the s6 and s12 sensors is presented in Figure 3.13.

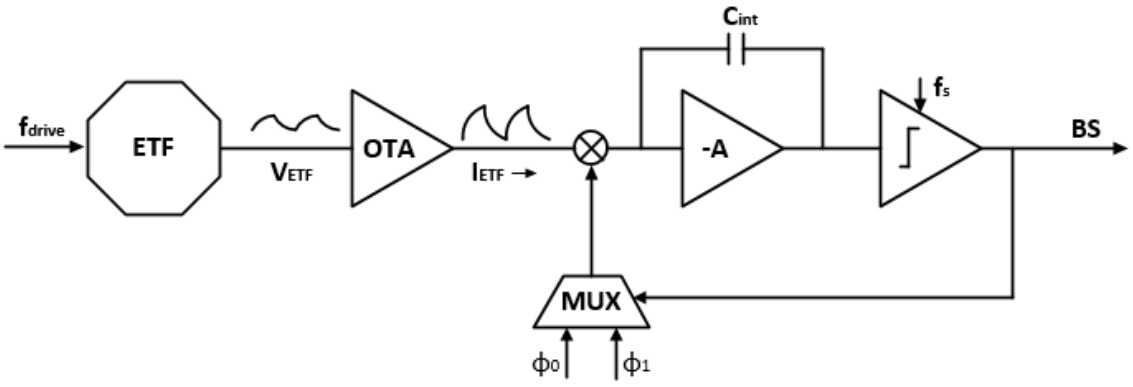


Figure 3.13: An ETF-based temperature sensor with a first-order PDΔΣM.

The conceptual functioning of an ETF-based temperature sensor with a $PD\Delta\Sigma M$ is explained in detail in Subsection 1.2.4. Figure 3.13 solely introduces the chosen integrator topology which is a Gm-OTA-C.

After deciding on the order of the modulator and the architecture, the multiplexing scheme utilized for the OTA in Chapter 2 is applied for the s6 and s12 ETFs in the 65nm process as presented in Figure 3.14. Besides the multiplexing of the ETFs, two different integrating capacitors are used to obtain the same voltage amplitude at the integrator output for both of

the ETFs. Therefore, two switches are added to the left of the capacitors, and according to the enabled ETF, the corresponding capacitor switch would be turned ON while the other one remains OFF.

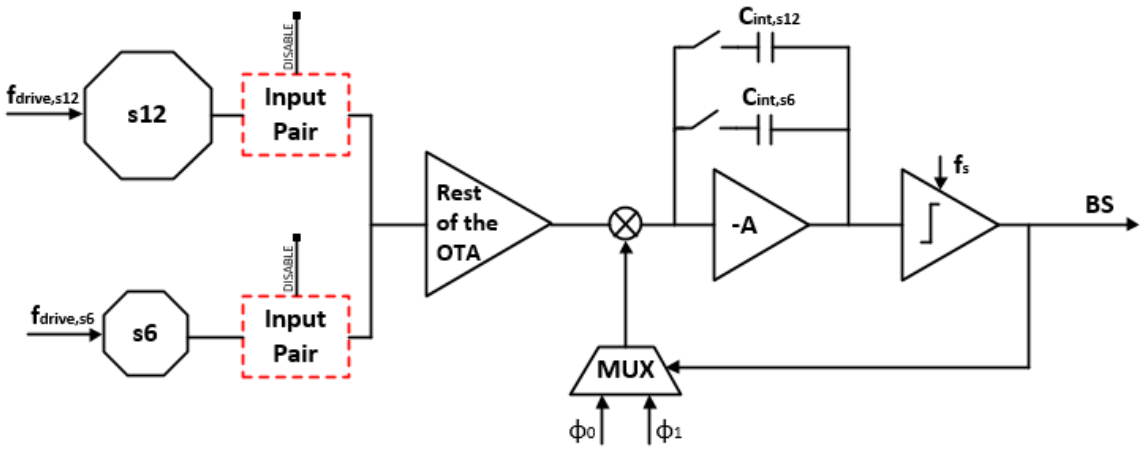


Figure 3.14: The block diagram of the multiplexed TD temperature sensor in the 65nm process.

3.2.2 Circuit Implementation

This subsection will present the circuit implementations of the blocks in Figure 3.14. The first block after the ETFs is the transconductor of the integrator. Then comes the demodulator controlled by the output bitstream. This is followed by an OTA with capacitive feedback as the remaining part of the integrator. The last block is the comparator which produces the output bitstream.

3.2.2.1 Transconductor and demodulator

The simplest choice for the transconductor would be a resistor connected to a virtual ground of the integrator. However, as previously mentioned, V_{ETF} has few mVs amplitude, making the ETF output a sensitive node. Therefore, using an OTA rather than a resistor would prevent the loading on the ETF and isolate the ETF output from the rest of the circuit without affecting the linearity.

The telescopic cascode amplifier presented in Figure 3.15 is chosen as the OTA architecture. For a VDD=1.2V, a telescopic amplifier might not have enough output swing to maintain all the transistors in the saturation region, hence, a folded cascode could be a better option, which may require more current. However, in this system, the output of the OTA is applied to the virtual ground of the 1st integrator, so the voltage headroom is not a problem. Therefore, the telescopic cascode architecture is chosen for less power consumption.

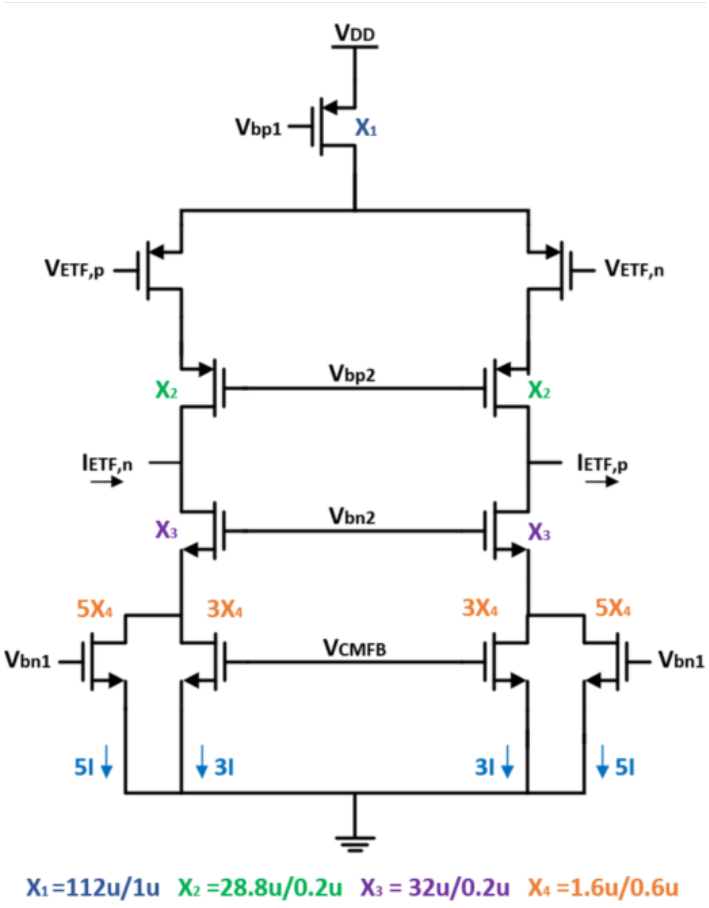


Figure 3.15: Implementation of the transconductor.

As presented in the block diagram in Figure 3.14, the s6 and s12 ETFs are multiplexed to a single readout circuit. This is done previously in Chapter 2 for the TD sensors in the 180nm process. The transconductor used in the $PD\Delta\Sigma M$ of the 65nm process TD sensor is almost the same OTA that is used in 180nm process sensors in Chapter 2. Therefore, the same multiplexing scheme is applied for the 65nm TD sensor as presented in Figure 3.16.

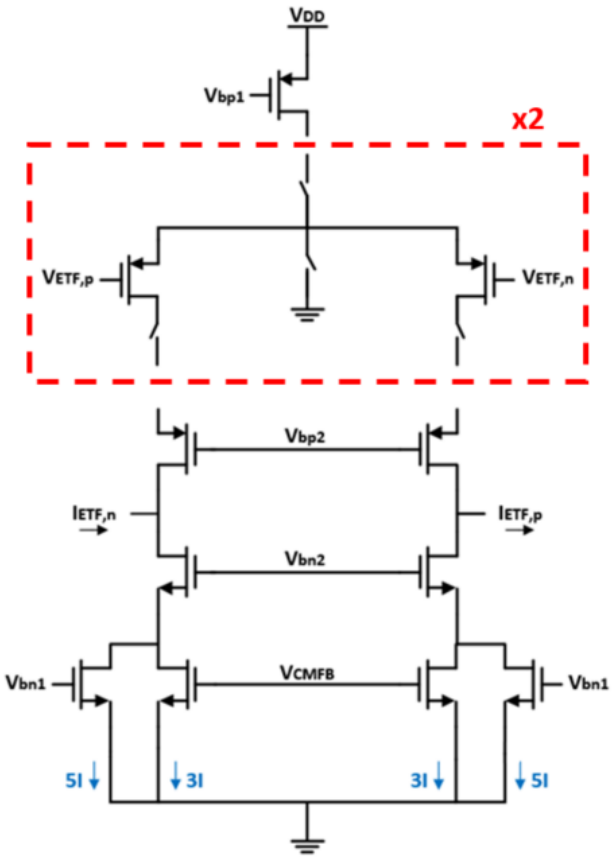


Figure 3.16: Multiplexed OTA.

The input pairs used in Figure 3.16 are not identical unlike the pairs multiplexed in Chapter 2. Since this TD sensor has only 2 ETFs to be multiplexed and they are both characterized previously, the input pairs can be customized accordingly. This customization is based on the ETF properties presented in Table 3.6.

		s6	s12
f_{drive}		460kHz	115kHz
R_{ETF} (Equivalent resistance)		7.2kΩ	7.1kΩ
Expected temperature error	Due to lithography errors (3σ)	0.36°C	0.18°C
	Due to the intrinsic BW of the ETFs	0.17°C	0.17°C
Corresponding phase error	Due to lithography errors (3σ)	58mdeg	29mdeg
	Due to the intrinsic BW of the ETFs	27mdeg	27.4mdeg

Table 3.6: Front-end properties.

The main design considerations for the OTA are the introduced noise and the added phase error at f_{drive}. Since the OTA is selected to be a telescopic amplifier, with proper sizing, the dominating noise source would be the input pair of the OTA. For the added phase error, the OTA output is a low-impedance node as it is driving a virtual ground, thus, the BW of the OTA is relatively high. That is why, the main addition to the phase error would be due to the gate capacitance of the input pair at the ETF output node, decreasing the intrinsic BW of the ETF. Therefore, for both the noise and the phase error addition, the input pair of the OTA must be properly sized.

The added noise power budget for the input pair was decided to be half of the thermal noise power of the ETF at f_{drive} as shown in Eq. 3.6.

$$\frac{1}{2} v_{n,th,\,ETF}^2 = v_{n,th,diff.pair}^2 + v_{n,1/f}^2 \tag{3.6}$$

The main noise contributors of the input pair are 1/f and thermal noise. They were targeted to be equal at f_{drive} as presented in Eq. 3.7.

$$\frac{1}{4} v_{n,th,\,ETF}^2 = v_{n,th,diff.pair}^2 = v_{n,1/f}^2 \tag{3.7}$$

Putting the respective thermal noise power formulas in Eq. 3.7 gives:

$$\frac{1}{4} 4kTR_{ETF} = 4kT\gamma \frac{1}{gm} \tag{3.8}$$

Taking $\gamma = 1$ and knowing R_{ETF}s from Table 3.6, the minimum values for the gm of the input pairs can be calculated by Eq. 3.8. The 1/f noise corner frequency is determined according to the targeted noise power in Eq. 3.7. Since the ETF thermal noise will be dominating at f_{drive} being 4 times higher than the 1/f noise, the corner frequency should be $f_{drive}/4$ since the noise power is inversely proportional to the frequency. The calculated gm values and corner frequencies are presented in Table 3.7.

	s6	s12
gm (per device)	1.12mS	1.13mS
f_c (Corner frequency)	115kHz	28.75kHz

Table 3.7: Design considerations for the input pairs regarding noise.

The phase errors caused by the intrinsic BW of the ETFs in Table 3.6 are retrieved from Figure 3.4 as the tt corner phase values, and, converted to temperature errors by using the reference sensitivity value of 6.25°C/º. Therefore, they represent absolute errors. The 3σ values can be estimated by taking 10% of these absolute errors. When this is done, the expected temperature errors for s6 and s12 due to the BW limitation are around 0.017°C. Compared to the expected error due to lithography, this value becomes insignificant. Hence, the readout

circuit is designed considering the phase errors caused by the intrinsic BWs so that the dominant source of inaccuracy would remain as lithographic misalignment.

As previously mentioned, the most significant addition to the phase error would happen at the connection node of the ETF and the OTA due to the gate capacitance of the input pair. The design consideration for the input pair is to introduce the same order of magnitude phase error as the intrinsic BW of the ETF does. Therefore, from the values in Table 3.6, the added phase error by the gate capacitance should be around 27mdeg. Since the OTA will be connected to the ETF output, this error would directly add to the phase error due to the intrinsic BWs. Hence, the targeted phase error at the connection node would be around 54mdeg. This could be converted to a BW value by scaling the BW values in Figure 3.3 by using the relation in Eq. 3.9.

$$BW \propto \frac{1}{Phase\ error_{@f_{drive}}} \tag{3.9}$$

The estimated BW values at the input of the OTA (connection node with the ETF) are presented in Table 3.8.

	s6	s12
BW	430MHz	106MHz
Corresponding phase error	54mdeg	54.4mdeg

Table 3.8:Design considerations for the input pairs regarding the accuracy.

The input pairs were sized to meet the design considerations specified in Tables 3.7 and 3.8 with the dimensions presented in Figure 3.17. Then the switches were sized to introduce minimum additional phase error similar to what was done in the multiplexed TD sensor in Chapter 2.

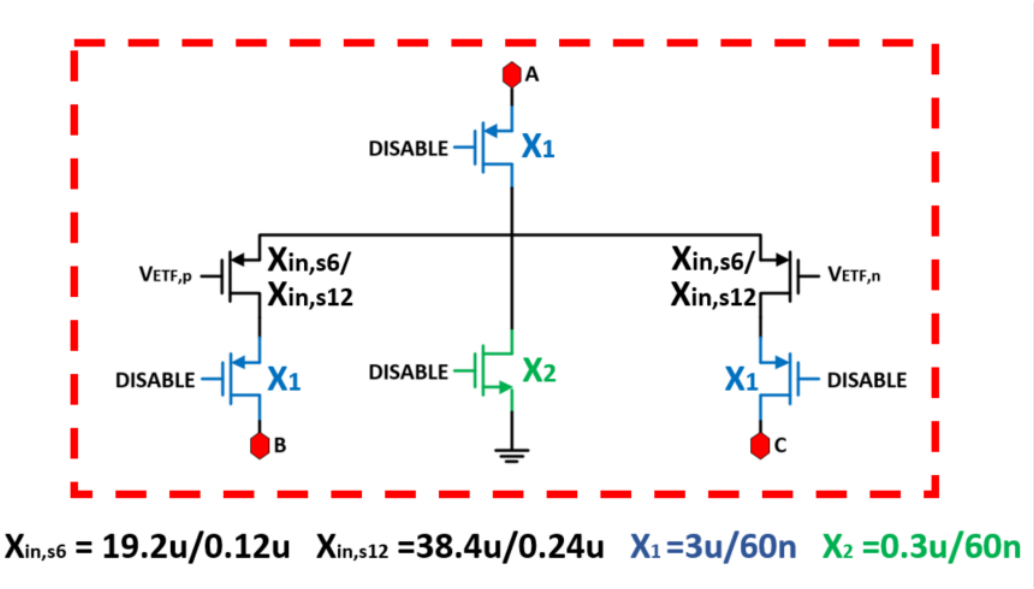


Figure 3.17: The multiplexed part of the OTA.

The achieved gm, f_c and input BW values for the multiplexed input pairs in Figure 3.17 were obtained by connecting an ideal current source to node A and ideal voltage sources providing enough overdrive voltages to nodes B and C. The current was set to the same value, $130\mu A$, for both of the input pairs considering they will be connected to the same current source via node A. The results are presented in Table 3.9.

	s6	s12
gm (per device)	1.20mS	1.25mS
f_c (Corner frequency)	≈115kHz	≈28.75kHz
BW	550MHz	142MHz
Corresponding phase error	45mdeg	43mdeg

Table 3.9: Obtained results for the input pairs.

The results in Table 3.9 show that all the specifications are met and the added phase errors due to the gate capacitance are almost half of what was expected.

For the rest of the OTA, the main considerations are the added noise by the NMOS current sources and the phase error addition due to the OTA BW. The added noise power at f_{drive} from the rest of the OTA is targeted to be half of the input pairs' contribution as shown in Eq. 3.10.

$$\frac{1}{4}\, v_{n,th,\,ETF}^2 = \frac{1}{2} v_{n,input\ pair}^2 = v_{n,rest}^2 \tag{3.10}$$

It is mentioned before that the BW of the OTA would be considerably larger than the BW at the input of the OTA. Therefore, the added phase error at the driving frequency is estimated to be lower than the contribution from the gate capacitances. Since the input pairs introduced almost half of their budget, the remaining phase error budget is targeted for the rest of the OTA. The BW of the OTA would be almost the same for both input pairs considering they are multiplexed to the same block. Hence, the BW is estimated using the s6 ETF budget because of its higher f_{drive}. The design considerations for the whole OTA, including the input pairs, are presented in Table 3.10.

	s6	s12
Noise power	$0.75\ v_{n,th,\,ETF}^2$	$0.75\ v_{n,th,\,ETF}^2$
BW	3.35GHz	3.35GHz
Corresponding phase error	10mdeg	2.5mdeg

Table 3.10: Design considerations for the OTA with different input pairs.

When the rest of the OTA was sized as shown in Figure 3.15, the results in Table 3.10 are obtained.

	s6	s12
gm (per device)	1.13mS	1.14mS
Noise power	$0.6\ v_{n,th,\ ETF}^2$	$0.9\ v_{n,th,\ ETF}^2$
BW	2.8GHz	2.3GHz
Corresponding phase error	11mdeg	3.6mdeg

Table 3.11: Achieved results with the OTA

The BW, and consequently phase error, requirements are reached with the OTA design. The BWs of the OTAs with different input pairs do not match perfectly due to the variation in the transistor lengths, affecting the overall BW. The gm values decrease compared to the results in Table 3.9 since the previous values are obtained by using ideal sources for the biasing. With the overdrive voltages and the biasing current in the OTA, the gm values reduce while still meeting the requirements set in Table 3.7. While estimating the total noise coming from the rest of the OTA, the flicker noise contribution was overlooked in Table 3.10. Since the NMOS current sources are shared and f_{drive} for s6 is 4 times higher than it is for s12, 1/f noise power from these devices is 4 times higher in s12's OTA compared to s6's. Therefore, the resulting noise power is higher than the estimations.

The transconductance frequency responses of the OTA with both input pairs over the corners are presented in Figures 3.18 and 3.19.

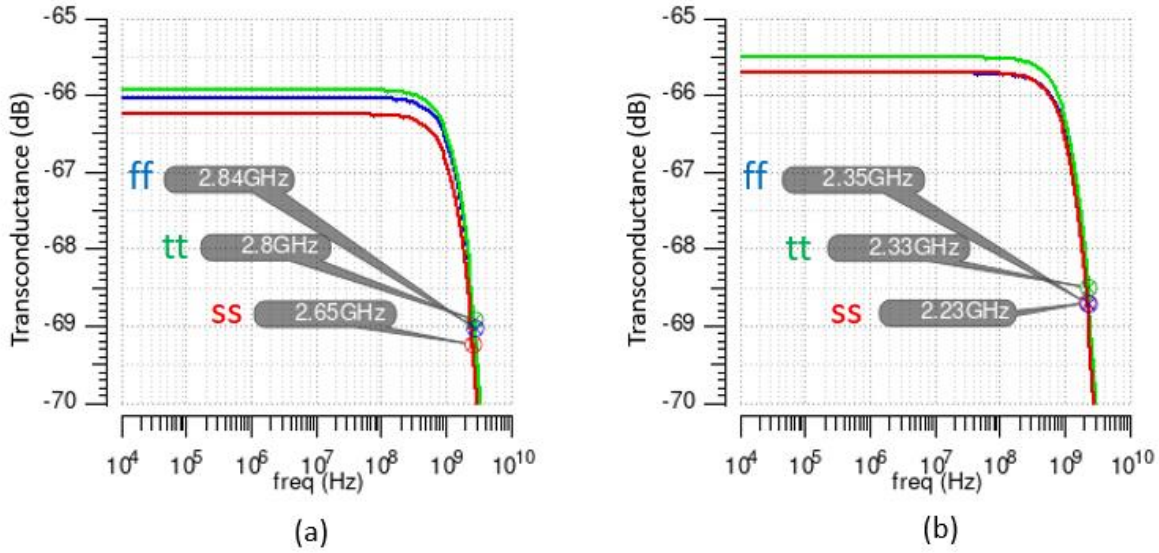


Figure 3.18: Magnitude responses of the OTA transconductance over the corners for s6 (a) and s12 (b).

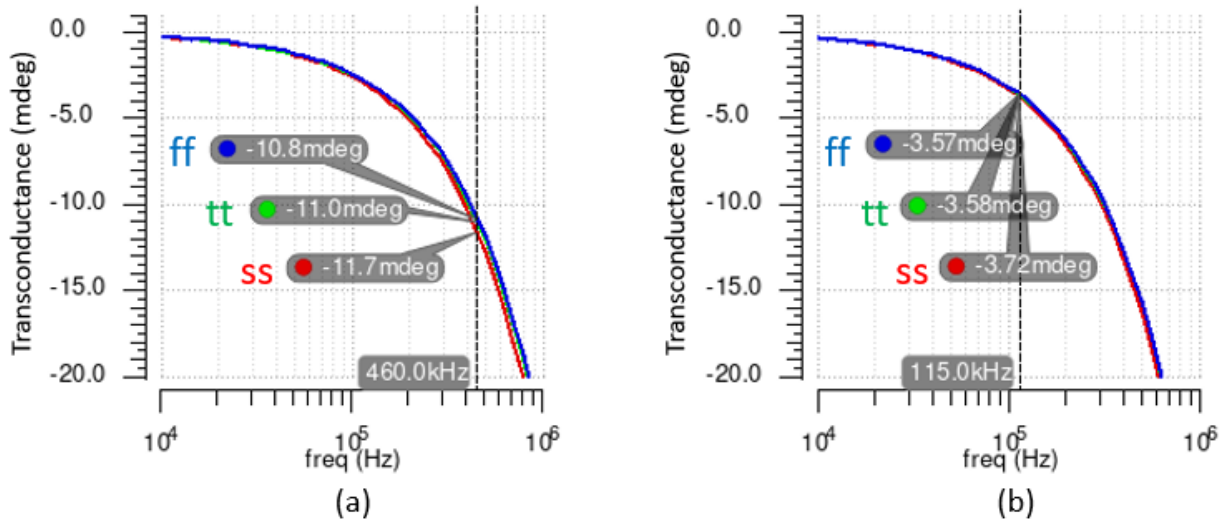


Figure 3.19: Frequency responses of the OTA transconductance over the corners for s6 (a) and s12 (b).

The BW and phase spread seen in Figures 3.18 and 3.19 validate that the OTA with different input pairs would function as required over the corners.

The OTA draws $172\mu A$ current including the biasing and CMFB circuits. Compared to the heater's current average, 2.1mA, the power consumption of the OTA stands significantly lower.

With the OTA, V_{ETF} is converted to I_{ETF} and this current signal is then multiplied by the phase references in the demodulator seen in Figure 3.14. The demodulator is a chopper whose switches are controlled by the multiplexer output that toggles between phase reference signals according to the output bitstream. For the single-bit quantizer, i.e. comparator, used in the first-order $PD\Delta\Sigma M$ in this TD sensor, there are two phase reference signals. These signals have the same frequency as f_{drive} with phases ϕ_0 and ϕ_1. The implementation of the demodulator is presented in Figure 3.20.

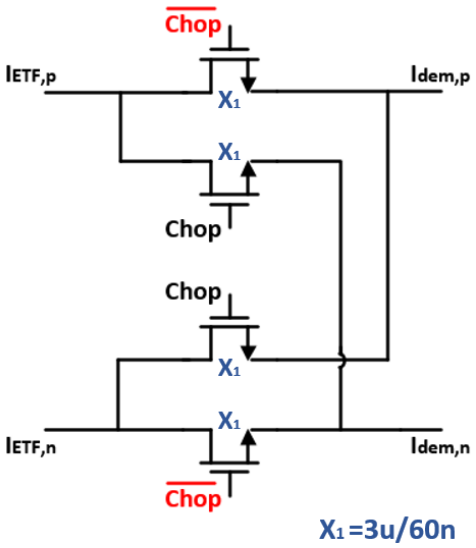


Figure 3.20: Demodulator implementation.

The switches are selected to be NMOS transistors since the output common mode of the OTA would be slightly lower than VDD/2 and the demodulator is followed by a virtual ground. Therefore, NMOS switches could be easily implemented. The sizes shown in Figure 3.20 are optimized for the minimum additional phase error at the driving frequency and their contribution is insignificant considering the previously mentioned accuracy limitations.

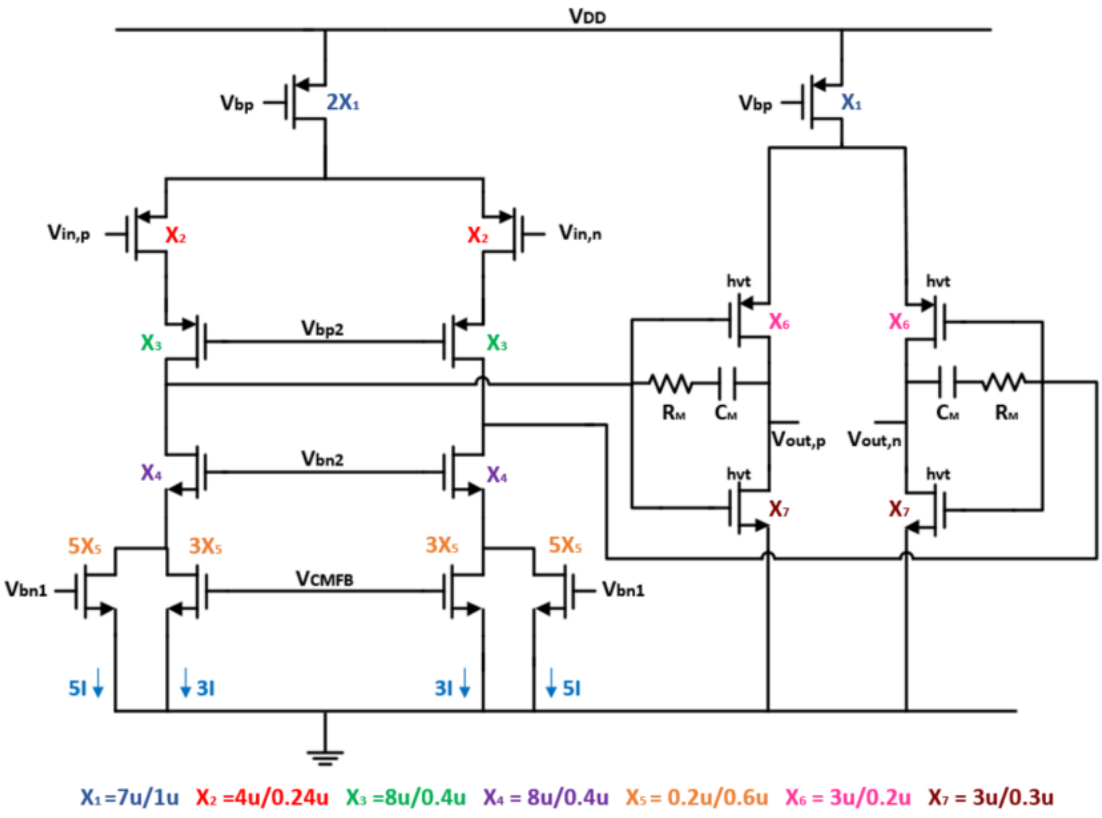
ϕ_0 and ϕ_1 are chosen to have $\cos(\phi_{ETF} - \phi_0)$>0 and $\cos(\phi_{ETF} - \phi_1)$<0 so that when the bitstream toggles, the average current flowing to the input of the integrator will approach zero. When the range of ϕ_{ETF} is retrieved from the reference TD sensor in [15] as 25°-65°, the following values for the phase references are chosen:

$$\phi_0 = 112.5°$$
$$\phi_1 = 157.5° \tag{3.11}$$

These phase references are chosen since the frequency divisions of 2^N are generally preferred on the chips. Therefore, the references are obtained by combining 22.5°, 45°, and 90° according to the cosine relations.

3.2.2.2 Integrator

An active integrator is used to integrate the demodulated current. This is preferred to create a low-impedance virtual ground at the transconductor output with a minimal signal swing. The OTA designed for the integrator has two stages with Miller compensation, as presented in Figure 3.21.



X1 =7u/1u X2 =4u/0.24u X3 =8u/0.4u X4 = 8u/0.4u X5 = 0.2u/0.6u X6 = 3u/0.2u X7 = 3u/0.3u

Figure 3.21: Integrator OTA.

A two-stage design is implemented to achieve a DC gain over 80dB. This gain specification is obtained by system simulations using a voltage-controlled-voltage source instead of the amplifier in the $PD\Delta\Sigma M$ and reducing its gain until the desired quantization noise suppression cannot be reached. Miller compensation with a nulling resistor is used to ensure the stability of the two-stage design ($C_M = 250f, R_M = 5.5k\Omega$).

The voltage gain frequency response of the amplifier over the corners is presented in Figure 3.22.

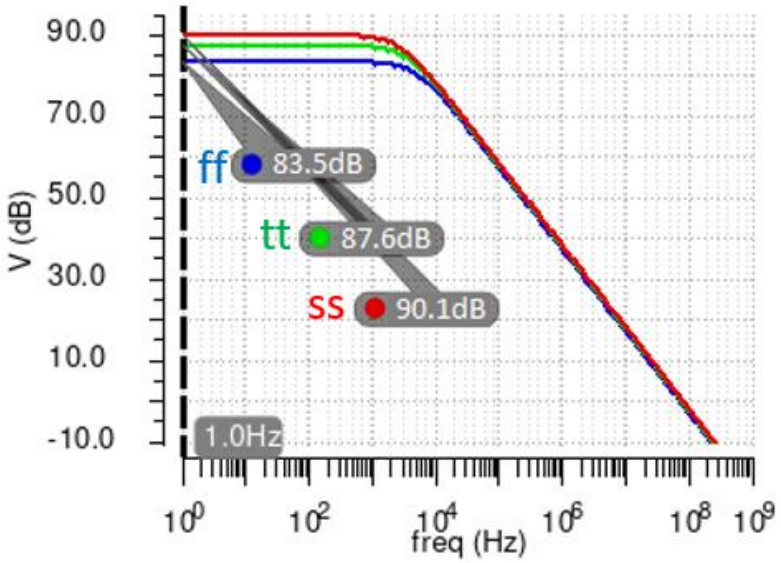


Figure 3.22: The voltage gain over the corners.

Even in the fast corner, the amplifier provides 83.5dB voltage gain, higher than the targeted value. The OTA draws around $44\mu A$ including the biasing and CMFB blocks. This corresponds to a quarter of the transconductor OTA's power consumption.

The integrating capacitors are sized considering the signal swing at the output of the integrator, i.e. the input of the comparator. $300mV_{pp}$ is targeted for the signal amplitude considering the voltage headroom at the output of the integrator and the comparator design. The voltage swing is determined by the following equation [5]:

$$V_{swing_{pp}} = V_{ETF_{pp}} \frac{8}{\pi^2} cos(\phi_1 - \phi_0) \frac{g_m}{C_{int} f_s} \tag{3.12}$$

Where gm is the transconductance of the transconductor OTA and C_{int} is the integrating capacitor. From Eq. 1.4, it is known that V_{ETF} is inversely proportional to s. Therefore, $V_{ETF_{s12}}$ is half of $V_{ETF_{s6}}$. The $f_{s_{12}}$ is a quarter of f_{s_6} and both of the ETFs have almost the same gm value. Putting all the relations together, the integrating capacitor of s12 should be double that of s6.

The integrating capacitor for s6 is calculated to be around 5pF, hence, 10pF is used for s12. MIM capacitors are selected for the realization since they offer good matching and linearity. The utilized layers and the sizing of the capacitors are adjusted for minimal parasitics that would be loading the integrator. Due to the usage of different capacitors, switches should be

utilized to select the corresponding capacitor for the selected ETF. The switch implementation is presented in Figure 3.23.

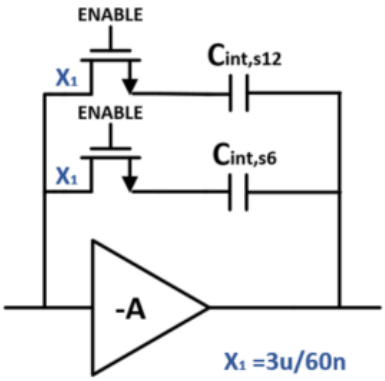


Figure 3.23: The integrator with adjustable capacitors.

The switches are located before the capacitors to benefit from the virtual ground of the integrator to introduce less parasitic capacitance.

3.2.2.3 Comparator

The integrator output is sampled by a single-bit quantizer. This is realized by the latched comparator shown in Figure 3.24.

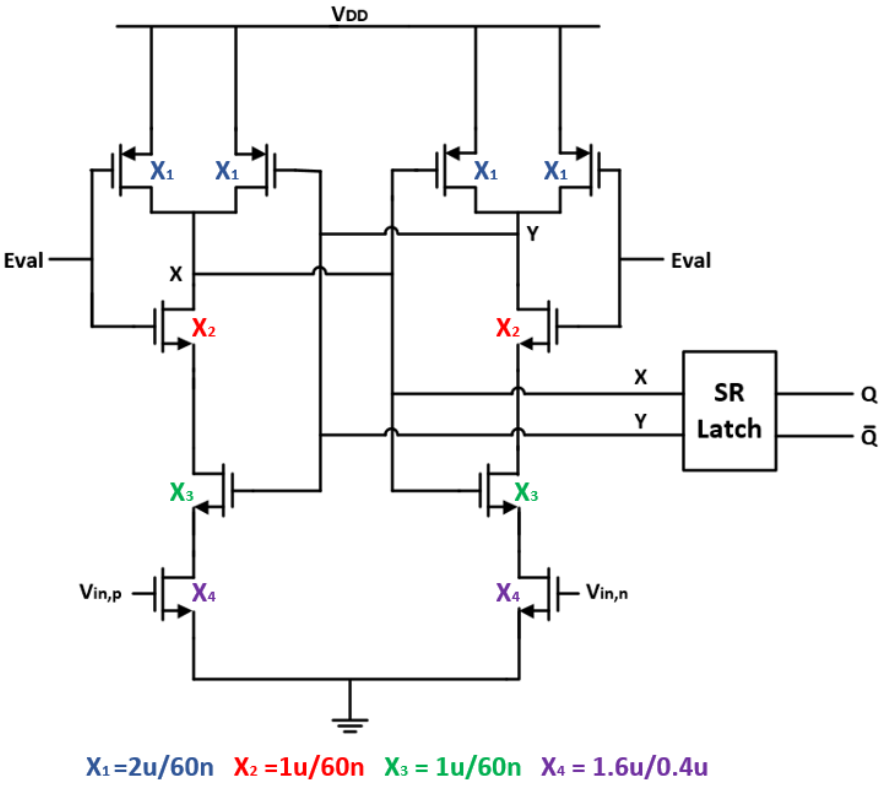


Figure 3.24: Implementation of the comparator.

When Eval is low, the latch input nodes X and Y are high and the latch is reset. At the rising edge of Eval, for the case of $V_{in,p} > V_{in,n}$, node X voltage starts decreasing and with the positive feedback formed by back-to-back inverters, it rapidly changes to low. The opposite

rapid change happens at node Y and the node becomes high. Then a digital output corresponding to the polarity of the differential input signal is generated at the output of the SR latch. The SR latch structure is shown in Figure 3.25.

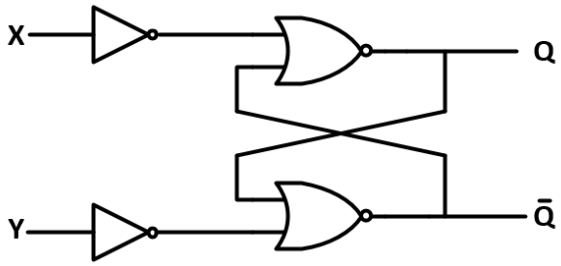


Figure 3.25: SR latch block.

For the SR latch, two inverters and two NOR gates from the TSMCN65 logic gates library are used. While the NOR gates are kept at the minimum size given by the library, the inverters are re-sized to adjust the threshold voltage. At the switching moments of Eval, the voltages at nodes X and Y are exposed to sudden changes. The sizing of the inverters ensures that these changes are always neglected by the choice of the threshold voltage.

3.3 Simulation Results

To obtain an output that can be used for the accuracy validation of the designed blocks, a decimation filter was needed after the $PD\Delta\Sigma M$ to filter the out-of-band quantization noise as shown in Figure 3.26. Since the sensor uses a first-order $PD\Delta\Sigma M$, the decimation filter was realized by a simple sinc filter or counter.

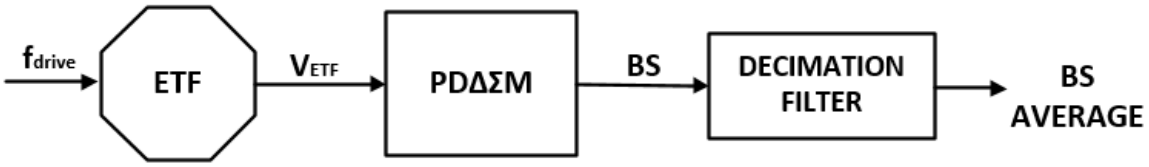


Figure 3.26: Block diagram of the system.

For simulation purposes, V_{ETF} signals were obtained by placing a current source between the differential output nodes of the ETF as shown in Figure 3.27.

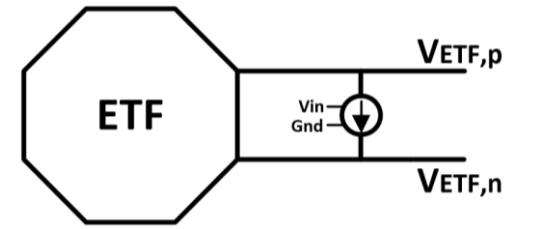


Figure 3.27: Front-end realization.

The source used in Figure 3.27 is a voltage-controlled current source. This was done to introduce ϕ_{ETF} to the test bench which is the main input to the $PD\Delta\Sigma M$. Voltage V_{in} that carries ϕ_{ETF} information was generated using an RC filter shown in Figure 3.28.

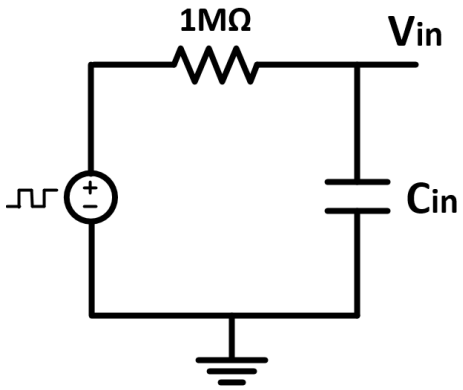


Figure 3.28: The RC filter to introduce ϕ_{ETF}.

Any desired input phase could be adjusted by changing the C_{in} value in Figure 3.28. The amplitude of V_{ETF} is also an important parameter to be adjusted by setting the gain of the voltage-controlled-current-source. Considering the *s* and P_{heat} relations given by Eq. 1.4, the desired V_{ETF} amplitudes were scaled from the measurement results of s24 sensor in [15] as follows:

	s24	s12	s6
s	$24\mu m$	$12\mu m$	$6\mu m$
Heater Power	3.6mW	2.5mW	2.5mW
V_{ETF}	$\sim 0.9mV_{pp}$	$\sim 1.2mV_{pp}$	$\sim 2.4mV_{pp}$

Table 3.12: Expected ETF output voltages.

In order to observe the behavior of the readout circuit, 3 different ϕ_{ETF} were used as inputs during the simulations. The chosen input phases are as follows:

$$\begin{aligned} \phi_{\mathrm{ETF},1} &= 29° \\ \phi_{\mathrm{ETF},2} &= 39° \\ \phi_{\mathrm{ETF},3} &= 52° \end{aligned} \tag{3.13}$$

Firstly, a test bench was created where each ETF had its own $PD\Delta\Sigma M$, with the $PD\Delta\Sigma M$ made up of ideal blocks. Later, these ideal blocks are replaced with transistor-level implementations, as explained in section 3.2 one by one, following the signal path order. Lastly, the switches required to multiplex the ETFs were added. After the addition of each implemented block, the decimated BS average was recorded and the difference from the ideal test bench BS average was calculated. The difference in the BS average was then transformed into temperature error by using the sensitivity observed from the measurement results in [15].

For simplicity, the temperature errors after the addition of each block are not presented. The main comparisons made with the ideal test bench are after the addition of the transconductor

OTA and the integrator OTA. The presented results following these steps are after the addition of the comparator, the demodulator, and TSMC C_{int} capacitors together. For the final results, the two sensors, s6 and s12, are multiplexed and the C_{int} switches are added. The obtained temperature errors are presented in Figure 3.29.

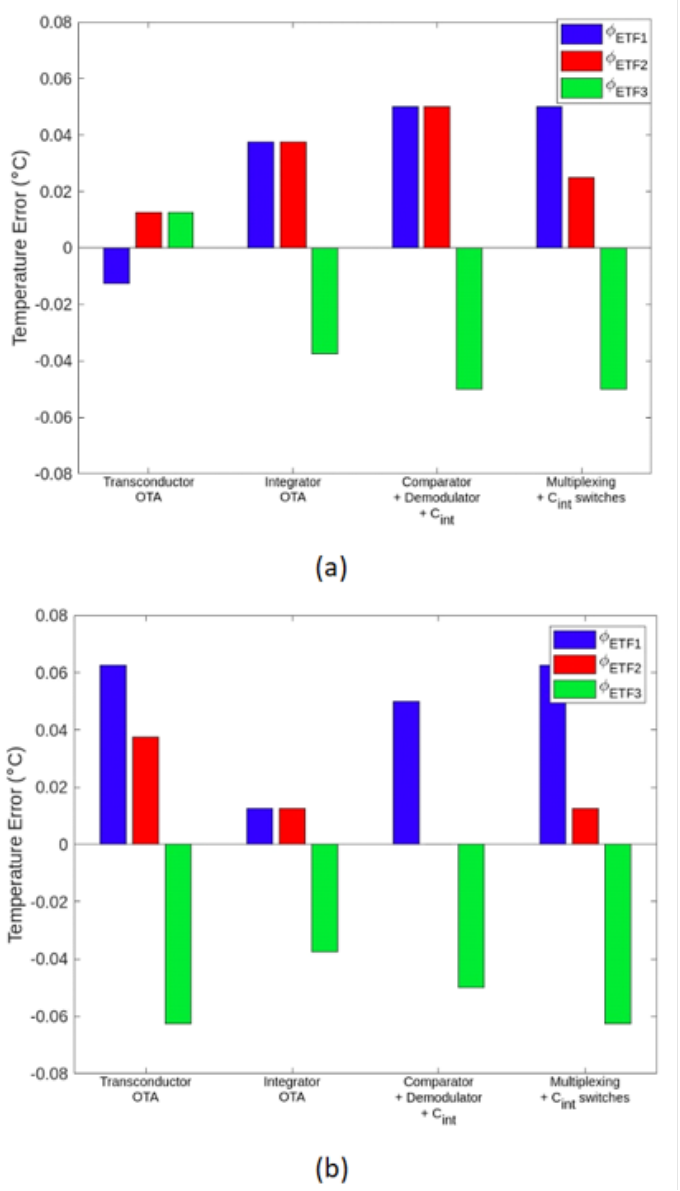


Figure 3.29: Temperature errors after the addition of the implemented blocks for s6 (a) and s12 (b).

The same simulations were done for the 3 different input phases in Eq. 3.13. The DC offset over the different inputs was removed from the BS averages after each step, and the corresponding temperature error was calculated. The accuracy of these results after each step may also be limited due to the tolerances of the cadence simulator like maximum time step and reltol etc.

Looking at the final results after the multiplexing of the two sensors, the readout introduces $\pm$ 0.05℃ for the s6 and $\pm$ 0.06℃ for the s12 sensor. These are absolute errors and since the DC offset over the 3 inputs is removed, the errors are less than the temperature errors caused by the intrinsic BW of the ETFs presented in Table 3.6. Considering the expected 3σ

temperature errors due to lithographic misalignment presented in Table 3.3, the readout errors are insignificant.

The output FFTs are plotted to observe the noise floor changes after the block level implementations and multiplexing the two ETFs to a common readout. Furthermore, the quantization noise suppression level is verified from the FFTs by comparing the simulation results including and excluding the transient noise. For simplicity, the FFT results of only one of the input phases, ϕ_{ETF2}, are shown. For plotting the FFTs, 2 conversion cycles are taken with the OSR values calculated in Eq. 3.5 and a Hanning window is used.

Firstly, the output FFT of the test bench with the ideal readout components is plotted together with the multiplexed sensor's output FFT while transient noise is included for both. The second comparison is made with the multiplexed sensor's output FFT with- and without the transient noise to observe the quantization noise suppression. In Figure 3.30, the ideal vs implemented readout comparisons are presented.

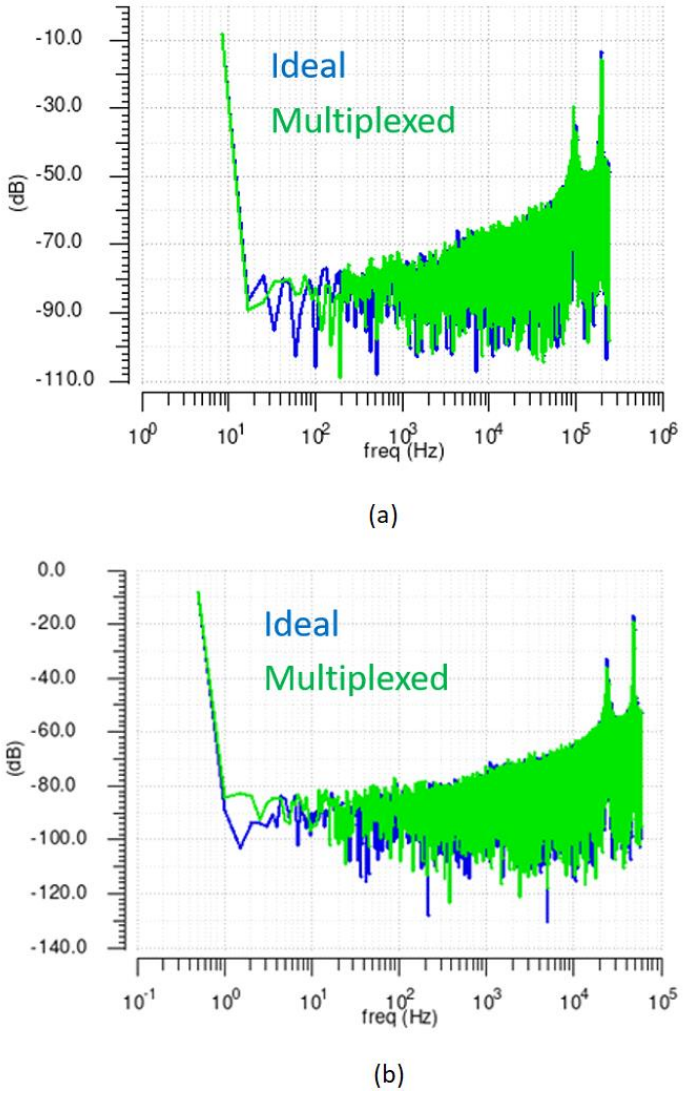


Figure 3.30: Output FFTs of the ideal readout vs implemented readout with multiplexing for s6(a) and s12(b).

The multiplexed readout FFTs for s6 and s12 ETFs match the readouts created using only ideal elements. This shows that the thermal noise floor after the addition of $PD\Delta\Sigma M$ block does not

change significantly, concluding that the ETF remains the dominant noise source. Furthermore, at higher frequencies, the noise shaping with 20dB/dec slope is observed in the FFTs which is expected for a first-order $\Delta\Sigma M$.

For the verification of the quantization noise suppression, the simulated FFTs with and without transient noise are presented in Figure 3.31.

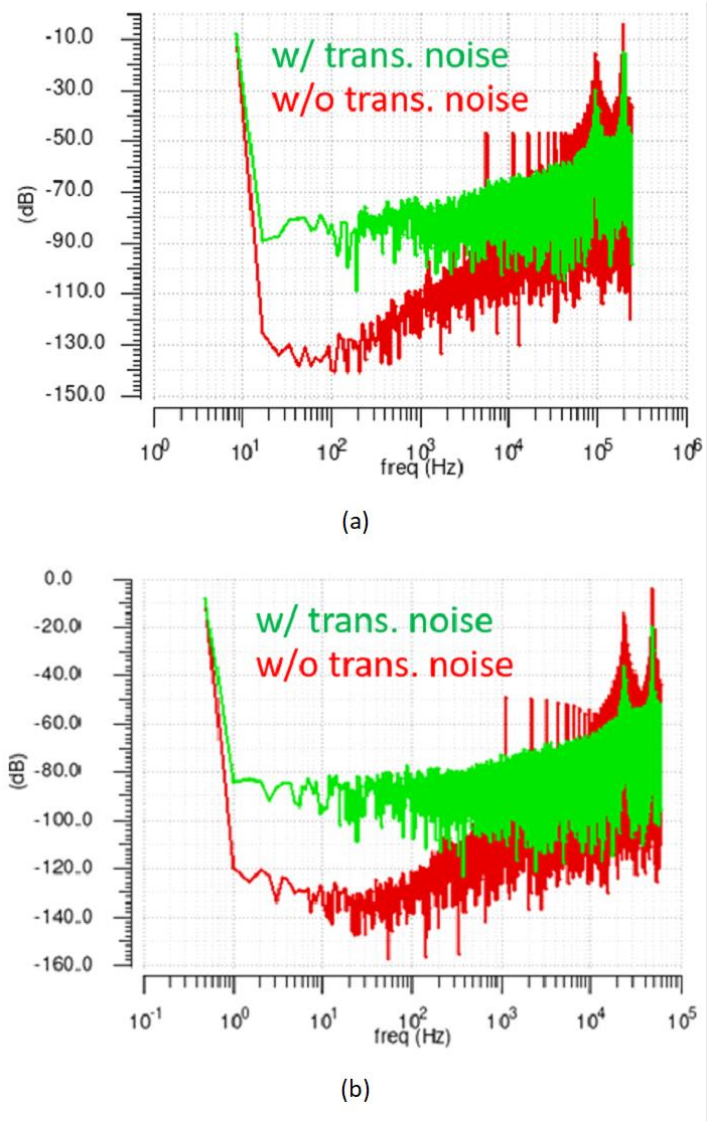


Figure 3.31: Output FFTs of the sensor with and without transient noise for s6(a) and s12(b).

The targeted in-band quantization noise suppression was 10dB below the ETF's thermal noise floor in the design considerations. Furthermore, it was found that with the calculated OSR values, the suppression should be even more than 10dB. This is observed in the FFTs presented in Figure 3.31. The quantization noise suppression is more than 20dB compared to the thermal noise for both s6 and s12 sensors.

Lastly, the current consumption and the power dissipation of the TD sensor blocks at 27℃ can be found in Table 3.13. The percentages demonstrate that the power consumption of the sensor is dominated by the heater power as targeted.

	Consumed current (mA)	Power (mW) (VDD=1.2V)	Distribution (%)
Heater	2.10	2.52	91
Transconductor OTA	0.17	0.20	7
Integrator OTA	0.04	0.05	2
Total	2.31	2.77	100

Table 3.13: Current consumption and power dissipation of the sensor components.

4 Conclusion and Future Work

4.1 Conclusion

This thesis investigates two aspects that affect ETF-based temperature sensor performance: the distance *s* and the design technology node. Firstly, four ETFs with different '*s*' distances are characterized and a multiplexing scheme for the measurement of multiple TD sensing elements is designed for a lower cost and time-efficient tape-out. The multiplexing scheme should limit neither the energy efficiency nor the accuracy, which must be verified by measurement in the future. Following this, two of the previously mentioned ETF designs are scaled from the 180nm to the 65nm process to observe the improvement in the accuracy of the TD sensors due to the better lithographic alignment. A first-order $PD\Delta\Sigma M$ is designed and verified for the 65nm sensor readout and a previously designed multiplexing scheme is used for a common readout. To properly evaluate the accuracy and resolution of the designed TD sensors, measurement results are necessary. However, other sources of error will first need to be addressed using the error reduction techniques explained below and left as future work.

4.2 Future Work

4.2.1 Error reduction methods

The TD temperature sensor in the 65nm process designed and simulated in Chapter 2 does not include any mechanisms for error reduction. In this section, the error sources in the readout circuit will be analyzed and error reduction techniques will be proposed for future implementations.

4.2.1.1 Transconductor offset

The offset of the telescopic OTA will create an error current, i_{error}, at the output of the transconductor stage. Considering that the amplitude of V_{ETF} is only a few mV, i_{error} would cause a significant error in ϕ_{ETF}. Fortunately, the demodulator chopper modulates i_{error} to AC, removing the DC error. However, the modulated i_{error} causes a voltage ripple on C_{int} with an amplitude equal to [5]:

$$V_{ripple} = \frac{i_{error}}{2f_{drive}C_{int}} \tag{4.1}$$

The offset must be suppressed to avoid clipping at the integrator output due to this ripple voltage. This could be done by auto-zeroing the OTA periodically as in [5]. A more advanced method proposed in [15] offers robustness at high temperatures that the previous method lacks due to capacitor and switch leakage. In this method, the OTA is digitally trimmed offering better suppression while increasing the complexity of implementation. The latter technique

could be a better option for the TD sensor in the 65nm process since leakage becomes more significant as the technology node reduces.

4.2.1.2 Charge injection mismatch

The charge injection mismatch in the demodulator is another source of error in the demodulated current. The mismatch between the demodulator switches will cause charge injection into the integrating capacitors. The offset current associated with this mechanism is given by [5]:

$$I_{OS} = 2f_{drive}\Delta Q_{inj} \tag{4.2}$$

I_{OS} for the s24 sensors used in [5] and [15] was significant, thus, dynamic offset reduction techniques were utilized. The multiplexed TD sensor would certainly be affected by this offset current considering f_{drive}values used in this sensor are relatively high, 115kHz and 460kHz, compared to the aforementioned s24 sensors. Therefore, the same error reduction method used in s24 sensors can be implemented for the multiplexed TD sensor in the 65nm process. In the prior work, two low-frequency choppers are placed around the demodulator as seen in Figure 4.1.

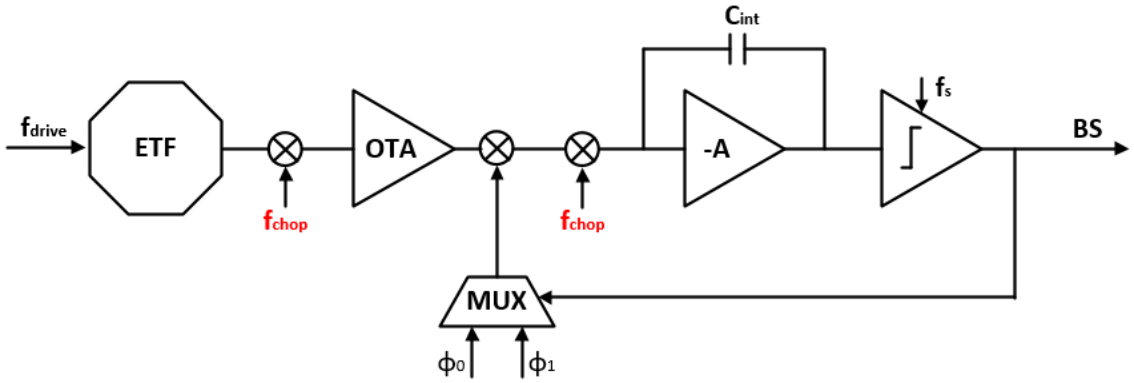


Figure 4.1: Low-frequency chopping for charge injection mismatch.

With these choppers, the charge injection mismatch will be converted to AC and filtered out by C_{int} and the decimation filter following the BS output. These chopper switches will also introduce charge injection mismatch, however, they can be operated once or twice per conversion, making f_{chop} a significantly lower frequency compared to f_{drive}, resulting in negligible error.

4.2.1.3 Integrator OTA 1/f noise and offset

The TD sensor resolution is targeted to be limited by the ETF's thermal noise. Therefore, the integrated 1/f noise of the integrator OTA should be analyzed. The following analysis is done for the s6 readout:

$$Noise\ BW = \frac{1}{2T_{conv}} \tag{4.3}$$

The noise BW for the s6 readout is calculated as 8.34Hz by using Eq. 4.3. When the input-referred noise power spectral density of the integrator OTA in Figure 4.2 is integrated from 0.01m to 8.34Hz, the corresponding noise power is $V_n^2 = 4.5 * 10^{-9} V^2$.

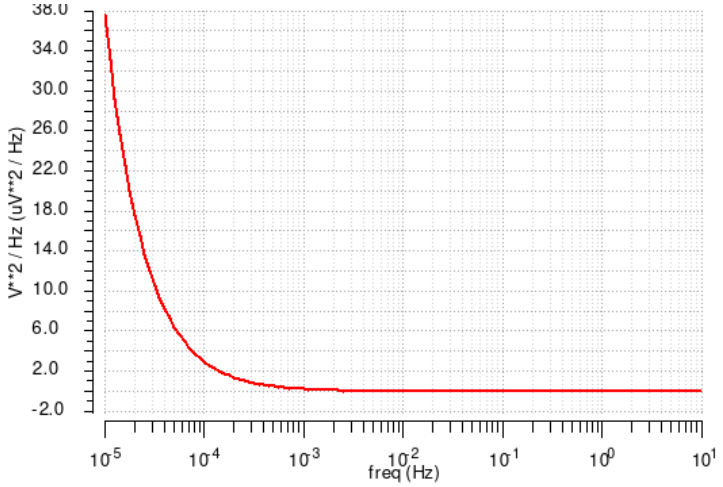


Figure 4.2: Input-referred noise power spectral density of the integrator OTA.

The input referred 1/f noise rms voltage of the integrator OTA will create a current due to the output resistance of the transconductor stage. When the rms noise voltage, $V_{1/f,rms} = 67\mu V$, is divided by $R_{out,gm}$, the resulting rms current becomes $I_{1/f,rms} = 105pA$. For comparison, the rms current corresponding to the ETF's thermal noise at the transconductor output node can be calculated by the following equation:

$$I_{ETF,n,rms} = \sqrt{4kTR_{ETF} * BW * \frac{\pi}{2}} * gm_{OTA} \tag{4.4}$$

From Eq. 4.4, $I_{ETF,n,rms} = 20.4pA$. For the TD sensor resolution to be limited by the ETF thermal noise, $I_{ETF,n,rms}$ should be significantly higher than $I_{1/f,rms}$. However, looking at the results, it is seen that the 1/f noise contribution of the integrator OTA is higher than the ETF's thermal noise. Therefore, the integrator OTA should be chopped to reduce the 1/f noise corner frequency and mitigate its effect. Chopping would also suppress the DC error current caused by the OTA offset. The location of the choppers is shown in Figure 4.3.

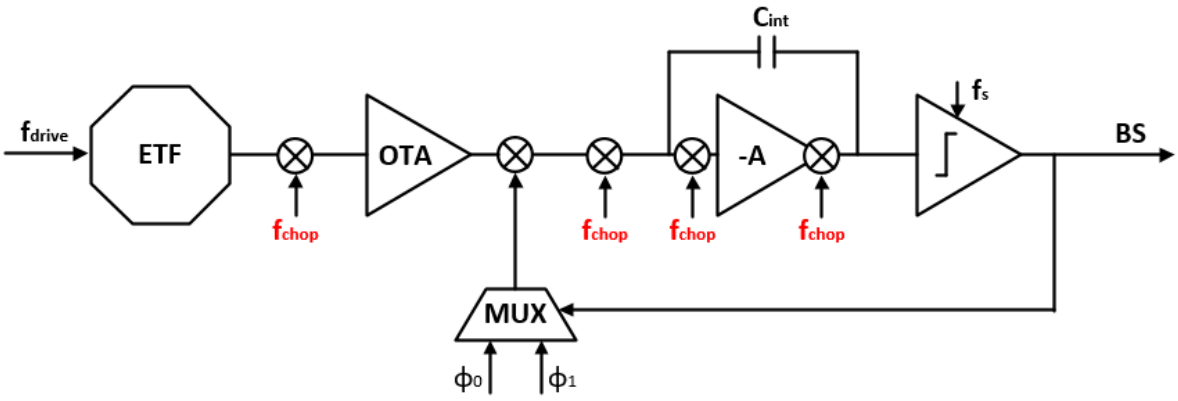


Figure 4.3: Integrator OTA choppers.

The integrator OTA has two stages as shown in Figure 3.20. Hence, there are two possible placements for the output chopper as presented in Figure 4.4.

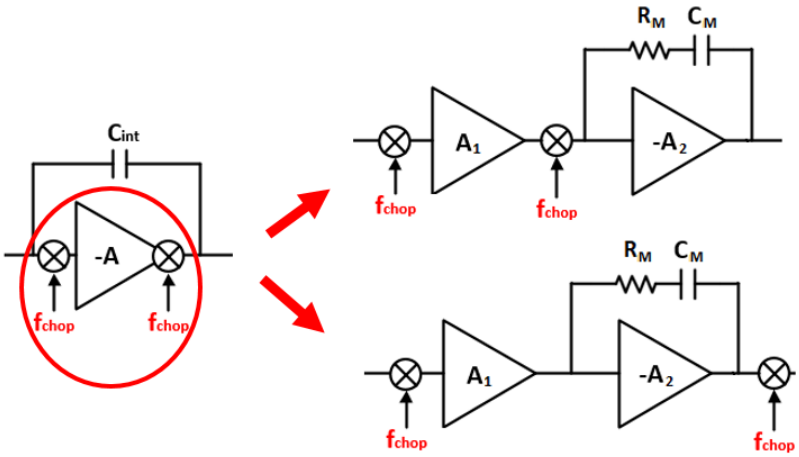


Figure 4.4: Two options for the output chopper location.

Placing the output chopper after the second stage would modulate the flicker noise coming from both stages but significantly reduce the DC gain of the first stage due to the miller compensation capacitor CM. Instead, the output chopper can be placed after the first stage and the flicker noise coming from the second stage would still be suppressed by the gain of the first stage. Therefore, placing the output chopper between the two stages should be preferred.

For simplicity, the same low-frequency f_{chop} in Figure 4.1 can be used for the integrator OTA choppers. The minimum chopping frequency can be determined by detecting the 1/f noise corner of the OTA when it is referred to the ETF's output node. The simulated noise power spectral density at the ETF output is shown in Figure 4.5.

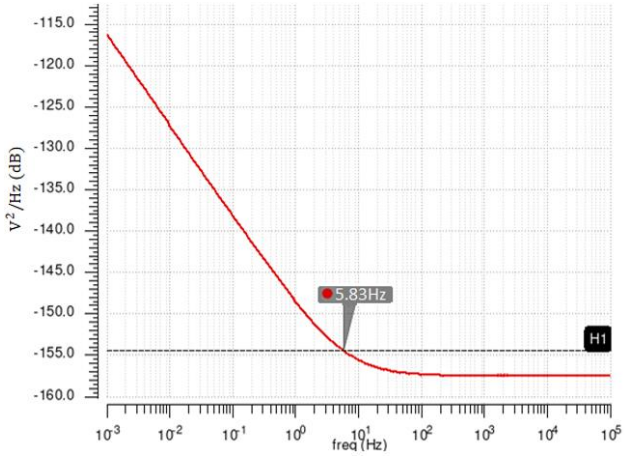


Figure 4.5: Integrator OTA's referred noise power spectral density.

The 1/f noise corner is around 6Hz from Figure 4.5. For s6, the noise BW is calculated previously as 8.34 Hz. Since T_{conv} for s12 is significantly higher than s6, the limiting minimum frequency would be decided by s6 noise BW. Therefore, the minimum chopping frequency should be around 15Hz. For the upper limit, the 3dB BW of the voltage gain in Figure 3.21,

3.5kHz, is taken so that the gain loss would be negligible. Hence, low-frequency f_{chop} could be chosen from the range 15-3.5kHz.

If there would be integer f_{chop} periods per conversion, the associated low-frequency tones will be placed at the notch frequencies of the decimation filter. Hence, they will not deteriorate the $PD\Delta\Sigma M$'s resolution. Therefore, this should be considered while choosing f_{chop}.

The chopping implementation shown in Figure 4.3 can be simplified if the same f_{chop} is used for all the low-frequency choppers. Firstly, ETF output is a sensitive node, thus, the chopper at the input of the transconductor stage can be moved to the input of the ETF, i.e. the f_{drive} signal polarity can be reversed. Secondly, the choppers at the virtual ground can be merged into a single chopper in the OTA's feedback path. This is shown in Figure 4.6:

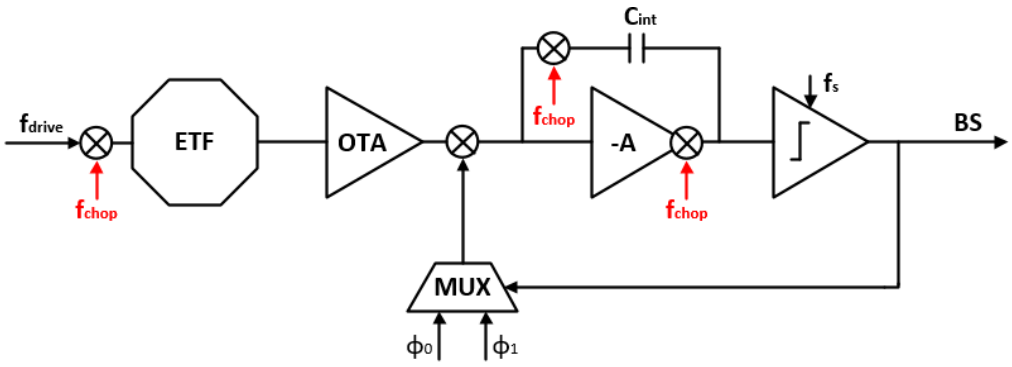


Figure 4.6: System-level chopping implementation.

4.2.1.4 Comparator offset

The quantization noise suppression target corresponded to an additional 1.5bits to the desired sensor resolution as shown in Eq. 3.2. Considering the same suppression levels for the comparator offset, the tolerable V_{OS} at the output of the ETFs can be calculated with the following equation:

$$V_{OS,max} = \frac{V_{ETF}}{2^{res+1.5bits}} \tag{4.5}$$

With V_{ETF} values estimated in Table 3.12 and desired resolution values determined in Chapter 3, $V_{OS,max,s12} = 18nV$ and $V_{OS,max,s16} = 72nV$. When V_{OS} is referred to the transconductor output as a current, $I_{OS,s6} = 40pA$ and $I_{OS,s12} = 10pA$.

The comparator offset used in the TD sensor is simulated to be 10.4mV. This offset will be noise-shaped by the $\Delta\Sigma M$. After a conversion of N samples, the DC error current $I_{OS,comp}$ at the demodulator output due to the comparator offset is given by:

$$I_{OS,comp} = \frac{V_{OS,comp} C_{int}}{N t_s} \tag{4.6}$$

With the corresponding values for s6 and s12 given in Chapter 3, $I_{OS,\,comp,s6} \approx 1pA$ and $I_{OS,\,comp,s12} \approx 0.13pA$. Since the calculated offset currents for both ETF readouts are significantly smaller than the aforementioned tolerable values, the comparator offset does not need to be suppressed.

5 References

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