Circuit Design for a Wireless ECG Device

Wireless Electrocardiogram (WiECG)

Bachelor thesis

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Delft University of Technology

TU Delft

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by

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TU Delft

Abstract

WiECG aims to create a prototype device which enable ambulance personnel to perform a 12-lead ECG without wires connecting the patient to the monitor. The proposed solution consists of a transmitter and a receiver device. The transmitter transmits the measured signals, the receiver sends the measured signals to the monitor, which shows the measured signals.

This thesis describes the design and implementation process for the hardware. This concerns the amplification and filtering of the signals produced by the heart of the patient as well as the reconstruction and attenuation at the output of the receiver module. These processes should be done for 9 signals. Furthermore, component selection, design decisions and the process of implementing this analog signal processing on a printed circuit board is described including the interfaces with the modules used by the other subgroups of this thesis.

The prototype built during this project was able to filter the 9 signals and send it from transmitter to receiver while only adding 1.572 μV RMS noise to the output ECG signal.

Preface

This thesis was completed in cooperation with two other groups, Protocol: Stefan Loen, Geert Custers and Digital Signal Processing: Keyvan Khalili, Sebastian Speekenbrink. Under the supervisement of Prof. Dr. Ir. W.A. Serdijn. As the group worked together in almost all cases, documenting the work in a logical flow was quite the challenge. **We therefore recommend to read the theses in the following order: Protocol [1], Digital Signal Processing [2] and Hardware.**

We would like to thank our supervisor Wouter Serdijn for providing invaluable insights and great starting points, Asli Boru and Francesc Varkevisser for the great feedback and of course the other members of the WiECG group for their hard work in completing the project. Furthermore we also would like to thank Martin Schumacher and Ton Slats for facilitating and aiding in the assembly and our family and friends for the support they have given throughout our bachelor degree.

P.J. Wiersma & R.G. van Krieken
Delft, June 2022

Contents

Nomenclature

Abbreviations

Abbreviation	Definition
ECG	Electrocardiogram
I2C	Inter-integrated circuit
WiFi	Name for international standard IEEE 802.11
PoR	Program of Requirements
PROT	Protocol Subgroup
DSP	Digital Signal Processing Subgroup
HW	Hardware Subgroup
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
DRL	Drive Right Leg
CMRR	Common Mode Rejection Ratio
EMI	ElectroMagnetic Interference
PCB	Printed Circuit Board
LDO	Low Drop-Out
IC	Integrated Circuit
HPF	High-Pass Filter
LPF	Low-Pass Filter
SMD	Surface-Mount Device
AHA	American Heart Association

1 Introduction

This thesis was written in collaboration with 6 people. The project was divided in three subgroups, each delivering their own thesis. For this reason some parts in this thesis will mimic those of other groups (e.g. General Introduction, problem statement, proposed solution and state of the art). To preserve the logical flow of the design the order of reading should be as follows: Protocols [1], Digital Signal Processing [2] and Hardware.

1.1. The WiECG Project

In the Netherlands alone, 1.3 million ambulance rides are made each year . Of these 1.3 million rides 76 % are urgent [3]. After interviewing Jim van Akkeren (Operational Head Witte Kruis Ambulance Zorg Den Haag) and Mirthe Ruijgrok (Ambulance operator) it was concluded that in 90% cases an ECG is connected to the patient being transported. An ECG is used in many cases to exclude a heart related problem as the treatment of such should happen as fast as possible. Furthermore ECGs are used when any form of anaesthesia or medicine is administered, to monitor the patients reaction.

As the deployment of an ECG requires wires, problems arise for the ambulance personnel in applying them. The Wireless ElectroCardioGram project aims to replace these wires with a wireless solution.

1.1.1. Basics of ECG

An ECG is a visualization of the muscle contraptions produced by a heart. This is done by measuring the vector projection of the hearts electrical field on the chest of a patient. Which in turn is done using electrodes located on the body of the patient, the potentials which cause these contraptions produced by the heart are registered and visualized on a monitor.

There are two main ECG variations health workers employ [4]. One with 4 electrodes and one with 6 additional ones. The first configuration are called the extremity electrodes, which can give a general electrical overview of the heart functions. In the second configuration 6 other electrodes are added: the chest electrodes. These give more detailed information of the heart on which diagnoses can be made [5]. With these signals 12 signatures in total can be obtained.

1.1.2. Problem statement

As shown before, the usage of ECGs by ambulance personnel is crucial to ensure the well being of the patients. ECGs currently applied by usage of electrodes attached to the chest of the patient. For regular, non emergency use, only the extremity electrodes are used. In emergency situations a full 12 lead (10 electrodes/wires) configuration is used. Currently these electrodes consist out of stickers connected to wires which are connected to a heart monitor. According to the interviewed ambulance personnel, the wires are very annoying to work with in emergency situations. The wires get tangled, dirty and in the way of the ambulance personnel as it obstructs the cabin.

1.1.3. Proposed Solution

The proposed solution is a device where the same monitor can be used as before, but where the cables have been replaced by a pair of wireless devices. The transmitter device has 10 electrodes which have to be applied to the patient like before, requiring no extra actions for the operator. The receiver side can be plugged in to the monitor, also requiring no extra actions. This plug n' play system can be used with any ECG monitor as long as the connector for that monitor is available. To make sure that the devices transmit and receive the right signal and not that of another pair, they can be paired easily by having the transmitter and receiver tap each other. This solution solves the problems mentioned in Chapter 1.1.2 in the following way:

- The short cables tend to tangle up way less compared to the longer ones.
- Because the transmitter device is located near the patient and the receiver lies next to the ECG monitor, no cables are suspended through the ambulance, greatly improving on the comfort/workflow of the operator.

To achieve this goal, a self proposed electrical engineering bachelor graduation project was submitted to Delft University of Technology. This project will be executed with 6 others, and be split up into three parts (as can also be seen in Figure 1.1):

- Protocol (PROT)
  The group that deals with the wireless transmission of the ECG data
- Digital Signal Processing (DSP
  The group that process the signal digitally and forwards it to the wireless module
- Hardware (HW)
  The group that prepares the measured signals for digital conversion and facilitates the aforementioned groups in creating a prototype device.

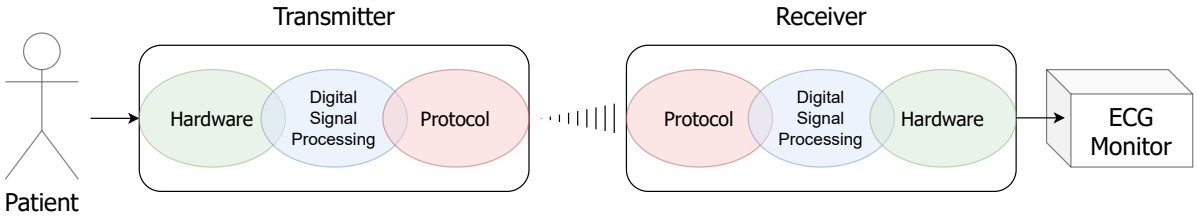


Figure 1.1: Brief overview of the solution, and the aforementioned seperation of tasks

1.1.4. State Of The Art

Currently wireless heart monitoring (via ECG)is mainly used in several markets; medical and consumer. Consumer wireless ECG systems (e.g. KardiaMobile 6L™[6]) are usually limited to 6 leads, or only one in case of wearable devices (e.g. *Apple Watch™, Galaxy Watch™*), which output the data to a smartphone or display. Furthermore, the sensors and workflow used to obtain the ECG differ majorly from those medical personnel uses. (No stickers but hand**held**/wearable sensor device).

The medical market is home to devices which are purpose-made for health monitoring on a diagnostic or treatment level. Currently, the Lifepak 15™[7] is in use in many ambulances to monitor the vitals of the patient. This device is part of a production line which is 12 years old and is still in use - in Dutch ambulances - due to the others[1] not being reliable (slow to start up, breakable or plainly not working. The connections to the monitor of these currently used monitors are wired however, leading to the aforementioned problems.

There are however medical wireless monitoring systems on the market that remove the wires between patient and monitor. Some examples are the ZOLL Heart Failure Management System (HFMS)™[9] and the Corpuls3™[10]. However, the HFMS focusses on detection of heartattacks in a non emergency setting

[1]Jim van Akkeren stated that since 2017 the Philips Tempus ALS™[8] monitor was in use. But most ambulance regions stopped usage due to reliability complaints

and the corpuls3 simply has a detachable wireless display (the relatively bulky defibrilator/patient box of around 3 kg has to be close to the patient). None of the devices researched focused on removing the medium of the signal like the proposed solution.

1.2. Subgroup Hardware

The hardware subgroup concerns itself with the realisation of a prototype device which has to be delivered within 10 weeks. It should deliver a device which is able to employ the measures and designs found by the other subgroups whilst keeping in mind power consumption, size and price. The components selected were chosen in close collaboration with the other groups.

Additionally, the hardware group is responsible for preparing the analog signal for the digital domain and the power infrastructure of the device.

1.2.1. The ECG signal

An ECG is a visualization of the muscle contraptions produced by a heart. Using electrodes located on the body of the patient, the potentials which cause these contraptions produced by the heart are registered and visualized on a monitor.

As the amplitudes of the potentials are relatively small (highest peak in the order of $\pm 0.5 - 3mV$ [5], they are easily polluted by the environment. Therefore, measuring these signals becomes non-trivial. The two main interfering signals components are:

- Baseline wandering: Movement of the body of the patient (e.g. breathing) that introduces a low frequency signal which a large amplitude relative to the heart potentials ([11], Ch. 6.5)
- Power Line noise: 50Hz AC interference caused by the AC net. Increases with cable length, and number of devices in close proximity. [12]
- Cellular / other RF communications EMI: Phones emit a strong electromagnetic signal when calling, this can get caught on the ECG leads or device. [13]

In our situation a 10 electrode ECG probe is used to measure 9 signals. These signals are combined to create 12 different signatures of the heart. The basic principle is that differential voltages (with respect to the Wilson central terminal; a virtual ground based on the probes on the left foot, left hand and right hand) are measured.

1.2.2. State of the art ECG circuits

Current iterations of ECG circuits (e.g. [14] [15] show a few common ideas:

- The ECG signal is a differential signal, an instrumentation amplifier is needed
- There is a high pass filer in place to get rid of the baseline wander
- There is a low pass filter in place to prepare the signal for digitalization (Anti-Aliasing)
- To get rid of large common mode interference a *right leg drive* circuit is made
- The signal is amplified to a value within the analog to digital converters (ADC) recommended operation range

None of these circuits however mention any form of wireless transmission of ECG data.

2

Program of requirements

Here the most important requirements are listed. Throughout the report, these requirements will get referenced to ensure that the design choices that were made have value for the end result of this project. The design described in this report and the reports of the other subgroups will attempt to completely fulfill the following list:

- **G1:** The device must not employ wires from patient to monitor.
- **G2:** The device must allow the user to perform a 12 lead ECG.
- **G3:** The device must be safe for the patient
- **G4:** The data handled by the device must be safeguarded
- **G5:** The device must not induce a delay of more than 5 seconds to the workflow of the user compared to a regular ECG wire.
- **G6:** The signal transferred by the device must be indistinguishable by the eye from the signal transferred by a regular ECG wire.
- **G7:** The device must have a battery life of 2 hours.
- **G8:** The device must not be bigger than 10cm x 20cm x 5cm (a smartphone-device)
- **G9:** The device must be lighter than 500 gram
- **G10:** A prototype device must be functional within 10 weeks from the start of the project.
- **G11:** The prototype must not cost more than 500 euros.

From this list, the following requirements were specified which specifically apply to the hardware part of this project.

- **G1H:** Two prototypes need to be made, receiver and transmitter
- **G2H:** The prototype must process 9 signals
- **G6H.a:** The added noise should be lower than the quantization error
- **G6H.b:** The signal should add minimal group delay
- **G6H.c:** The signal should remove baseline wandering
- **G6H.d:** The signal should remove all frequencies above 250 Hz (sample frequency)
- **G7H:** Choose batteries that allow the complete system to run for 2 hours
- **G10H.a:** Prototype must be hand solderable
- **G10H.b:** Prototype must be built from (In stock) off the shelf components
- **G10H.c:** Testing and programming overhead must be included on the design
- **G10H.d:** Prototype design and manufacturing should not bottleneck progress of other groups
- **G11H:** Prototype must be built from commonly used components.

On top of this list, some requirements come from the other subgroups, but apply to the hardware part. These requirements are listed here:

- **G6D.a:** An input signal must be sampled at 500 Hz
- **G6D.b:** An input signal must be sampled at 16 bits resolution
- **GD.a:** An input signal must be in the range of 0V to +3.3V

2.1. Reliability

One of the most important design goals of the final product is reliability. State of the art ECG monitor designs have seen minimal adoption because they aren't reliable enough. I.e., when the device is powered on, there is uncertainty if the device will function correctly. This problem is further substantiated in the introduction of the report.

Therefore, to differentiate our final product from other existing solutions, throughout the project there is an emphasis on reliability. The product must always work, and any failing conditions must be analysed and handled appropriately. However, this requirement cannot be reasonably tested within the 10 week time frame that is allocated to the BAP. Hence, it is not included in the list of requirements. Regardless, reliability is an important design principle throughout the project.

3

System Overview

The proposed solution in the introduction subsection 1.1.3 can, in accordance to the Programme of requirements (PoR), be further specified as shown in figure 3.1. This also depicts a high-level overview of the contributions of each subgroup. In section 3.1 and 3.2, brief descriptions will be given of how the different parts of the transmitter and receiver attempt to fulfill the requirements given in Chapter 2. Finally, in section 3.3, the complete system is shown where the detailed overviews are connected to the detailed overviews of other subgroups.

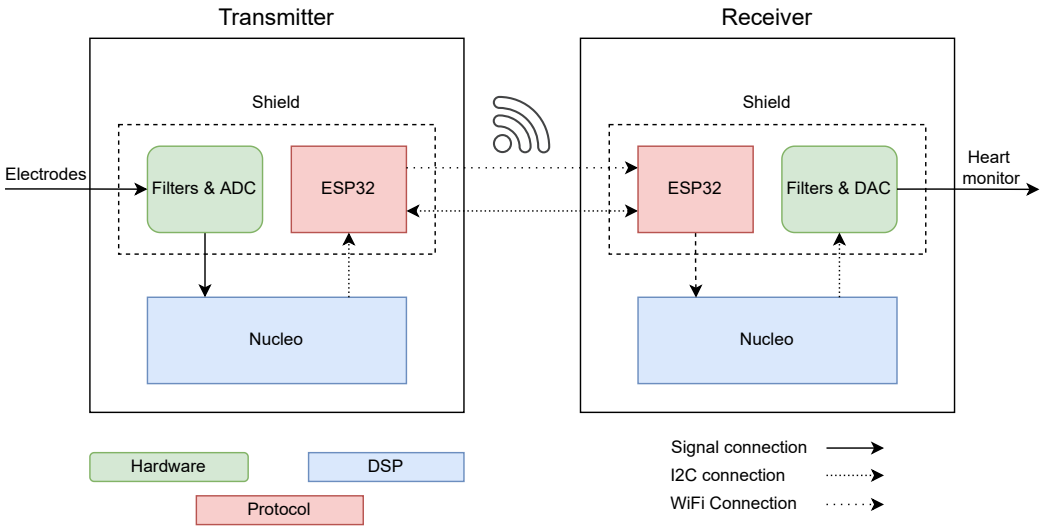


Figure 3.1: Block diagram of the general overview of the solution

3.1. Transmitter overview

As shown in Figure 3.2, the transmitter module transforms the signals coming from the electrodes on the patient to the Nucleo board. The instrumentation amplifier amplifies the signal from the electrode, such that less noise is added by the parts following the amplifier. Together with the offset circuit, the signals are transformed to the correct range such that requirement **GD.a** is fulfilled. The High- and Low-pass filters filter the signal in such a way that **G6H.b**, **G6H.c**, and **G6H.d** are fulfilled. The ADC takes the signal from the analog domain to the digital domain such that the DSP subgroup can do further operations.

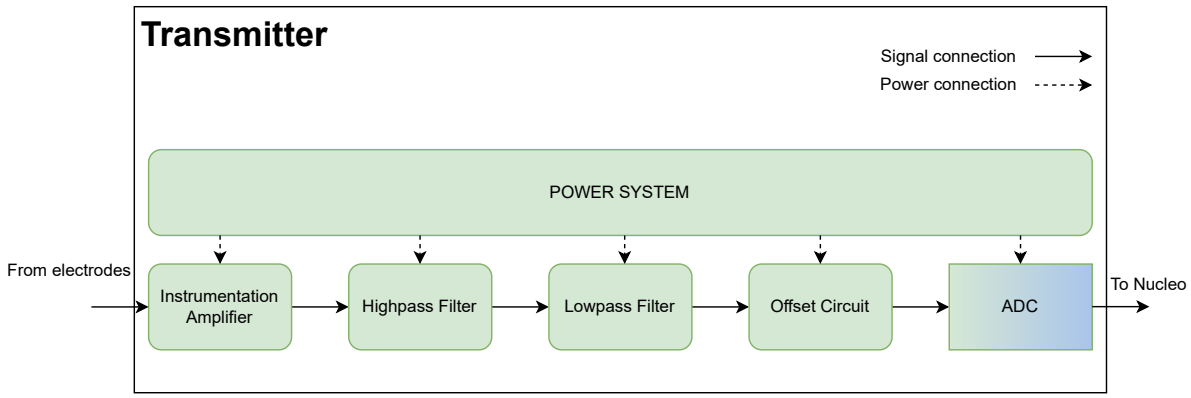


Figure 3.2: Block diagram of the proposed transmitter solution

The Power system block in Figure 3.2 consists out of batteries and voltage regulators. Although the power system is not the main focus of this project for the hardware subgroup, the design is briefly discussed in Chapter 5.

3.2. Receiver overview

As shown in Figure 3.3, the receiver module transforms the signals coming from the DSP subgroup to the heart monitor. To provide the heart monitor operator with a signals that (according to requirement **G6**) are indistinguishable from the original heart signal, some operations have to be done: The DC offset that is created due to the output range of the DAC is removed by a high-pass filter. Following this, the low-pass filter removes the high frequency noise that is introduced by the DAC (Requirement **G6H.d**). Last but not least, the signal is attenuated to the level of the original level.

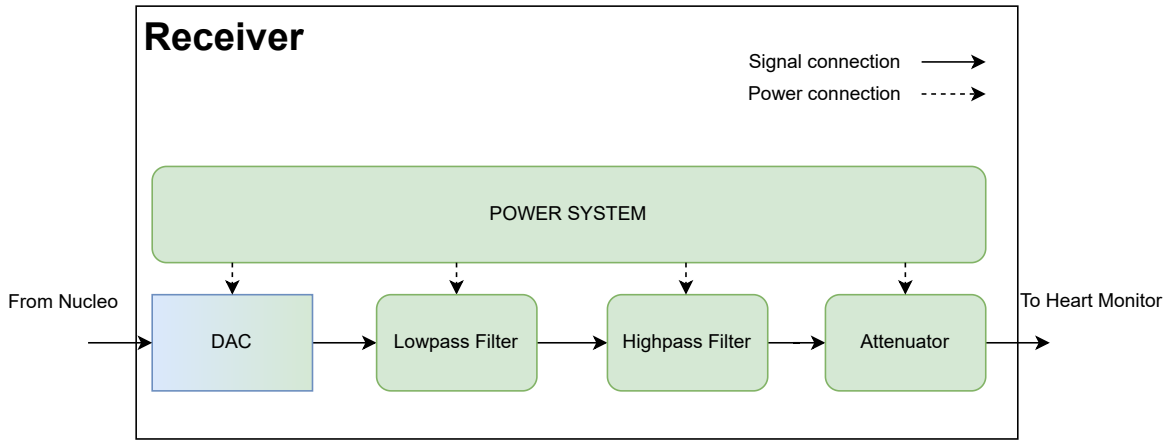


Figure 3.3: Block diagram of the proposed receiver solution

While there is a possibility that the receiver can be powered through the supply of the heart monitor or the ambulance itself, it is assumed that this is not the case and that the module has to provide it's own power. Therefore, the power system block is the same as for the transmitter.

3.3. Complete overview

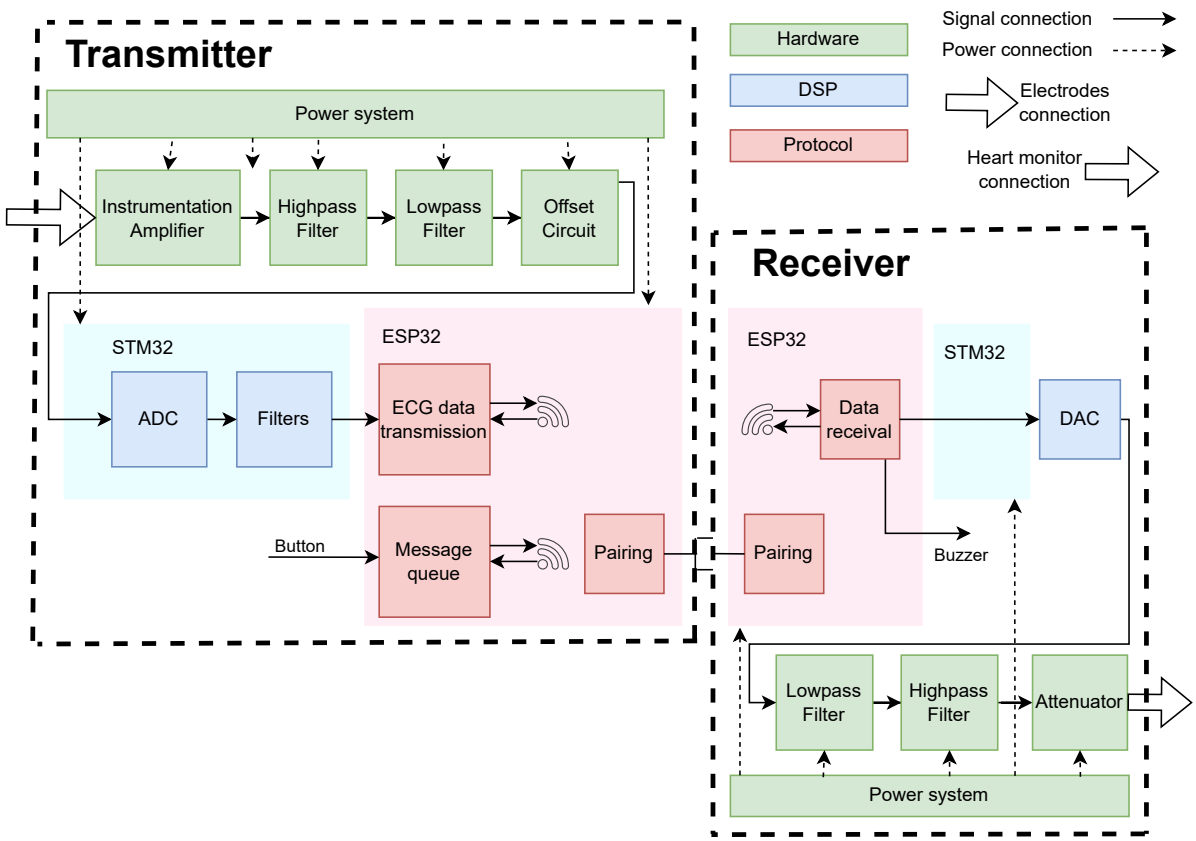


Figure 3.4: Detailed block diagram of the proposed solution including all subgroups

4

Design

This chapter will discuss the design process of the prototype circuit. It will share design choices, component choices and a general train of thought used for the creation of the prototype. The chapter will explain the design from the input signal all the way through the system to the output. This means the transmitter will be explained first followed by the receiver using the diagrams shown in Figure 3.2 Figure 3.3. There are nine signals to be transmitted which all use the same circuit topology in different channels.

4.1. Transmitter

The transmitter is the device that measures, filters, digitizes and transmits the signal. Nine signals need to be transmitted in total. All nine channels have identical circuitry.

4.1.1. Instrumentation Amplifier

As the ECG signal is a differential one, some sort of voltage summing must be implemented. Furthermore, the signal measured from the electrodes is a very weak one. To avoid adding a lot of component noise it should be amplified as soon as possible (**G6H.a**). The signal will also be polluted by power line interference, which due to the nature of the measurement, is common mode. Additionally the wire impedance is unknown which can lead to unwanted loading.

To solve these problems the first stage of the circuit should be an instrumentation amplifier. This device can measure differential signals, reject common mode errors with its high Common Mode Rejection Ratio, ensure good signal transfer due to high input resistance (CMRR) and amplify the signal to a level where added component noise is less of an concern.

The instrumentation amplifier which was chosen was the low noise, low power and High CMRR INA821 [16]. This instrumentation amplifier has the following desirable properties:

- High Gain 1-10000
- High CMRR (132 dB at a gain of 100, 140-150 dB at a gain of 1000, both from 0-60Hz)
- Low input noise (7nV per $\sqrt{\text{Hz}}$)
- Low output noise (65nV per $\sqrt{\text{Hz}}$)
- Datasheet specifies that this is to be used in applications such as ECGs and Surgical equipment
- Detailed Spice model available

As the signal strength is $0.3 - 3$ mV peak to peak and the ADC works at $0 - 3.3$V a gain of 1000 was chosen.

General Purpose Amplifiers

As it was expected that the circuit would use more amplifiers for filters/buffers the general purpose TL072 amplifier[17] was selected. This was done for the following reasons:

- As the signal was amplified already, noise added would be less of an concern
- The availability of the TL072 is very high
- Detailed Spice model available
- 4-in-1 packages are available to save PCB space (TL074)

4.1.2. On the Right Leg Drive (RLD)

A right leg drive circuit is a circuit that increases the CMRR of a system by actively driving the common mode error back into the body. This effectively subtracts the error by placing a negative voltage on the patients body [18]. The usage of such a circuit was considered but eventually it was decided not to implement it. Mainly because of three reasons:

- It was assumed that the CMRR of the INA821 (140-150dB) is high enough for the removal of the common mode.
- The main use case for a RLD is to filter out EMI (mainly powerline and fluorescent lighting [18]). It was assumed that the use case for this device is inside of an ambulance, which works from DC batteries and has LED lighting. Additionally, if there would be powerline noise it is assumed its magnitude small enough to not saturate the amplifier.
- **G2** and **G10**, The process of injecting current unto a patient is one which carries a lot of safety concerns. These needed to be addressed with extra safety measures which would be difficult to execute in the given timeframe.

4.1.3. Filters

When the signal gets amplified it still needs to get filtered. According to **G6D.b-d** the signal needs to get filtered such that the sample rate of 500Hz does not lead to aliasing. As a very large amount of the power spectral density (PSD) is within the first 100Hz [2], a Low Pass filter (LPF) with its f_{3dB} at 250Hz should suffice. This filter will also lead to less white noise, as the signal will be bandlimited. (as noise is spectrum wide)

Furthermore, the filter also suffers from baseline wandering, an added artifact caused my movement of the chest. To circumvent this a High Pass Filter (HPF) should be implemented. The f_{3dB} frequency was chosen to be 0.05Hz as higher would lead to wrong classification of signatures [19] and it being in accordance with the AHA (American Heart Association) recommended standard [20].

There are many filter topologies available for the bandpass filter. When selecting one, it is important to consider the added component noise (i.e. amount of components) and the performance (phase and groupdelay, rolloff, corner frequencies).

Filter types

Three filter types were considered: Butterworth, Bessel and Chebyshev. The pros and cons are listed in Table 4.1

Table 4.1: Table highlighting pros and cons of considered filter types

Filter type	Pros	Cons
Bessel	Very favorable phase characteristics	Many filter stages & slow rolloff
Butterworth	Flat passband, no ripple in passband	Medium phase characteristic
Chebyshev	Very sharp rolloff, Less filter stages	Non linear delay, ripple in passband

One of the most important factors is that the waveform should remain intact. (**G6H**) Phase, or its derivative group delay, and a flat frequency response in the passband are the most important characteristics as these distort the signal. An other important aspect is the amount of filter stages, as it increases the amount of components needed and thus price, size and added noise.

For the aforementioned reasons the **Butterworth** filter was chosen.

Filter Topologies
The implementation of the filters can be done by usage of filter topologies. There were three topologies considered for the circuit: Passive, Multiple feedback and Sallen Key. Multiple filters were evaluated (via LTSpice simulation) on LPF and HPF performance, group delay, number of components and noise characteristics. At the end of this subsection a cost matrix will be given with the final choice.
Noise will be evaluated last. (on the chosen topology). The reason for this is that mostly the component values (e.g. resistance) lead to higher noise. These values can however be tweaked by changing the capacitance (or possibly, inductance) and lowering the resistance (whilst keeping the same corner frequencies).

Passive Filter
Passive filters are filters consisting out of resistive and reactive components. These filters do not need to be powered by an external source. Using the LC-filter design tool as found in [21] a topology using passive components was created. The corner frequencies of this bandpass filter were specified at 0.05 Hz and 250 Hz, and the order was specified to three (third order HPF + third order LPF). This led to a very unrealistic filter. Shunt coils were needed with values ranging into the 80-300H, which would clearly violate PoR point **G8, G9 & G11** due to the weight, dimensions and price. This topology will therefore not be evaluated any further.

Multiple feedback 6th order

One form of a filter topology is the multiple feedback configuration. It gains this name due to the fact that the amplifier exerts negative feedback via two (therefore multiple) branches. The topology is inverting meaning that the output is inverted which could complicate the design. As most higher order filters require cascading, the transfer function will be showed along with how the corner frequency relates to the component values. A multiple feedback filter topology can be seen in Figure 4.1.

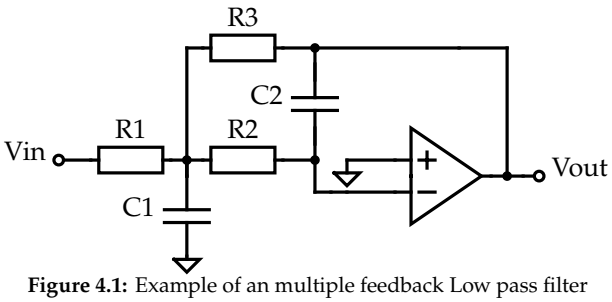


Figure 4.1: Example of an multiple feedback Low pass filter

The transfer function of a second order low-pass multiple feedback stage (analysis of high-pass stage will be omitted) can be seen in Equation 4.1[22]

$$H_1(s) = \frac{-\frac{1}{C_1 C_2 R_1 R_2}}{s^2 + s\frac{1}{C_1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) + \frac{1}{C_1 C_2 R_2 R_3}} \tag{4.1}$$

From this, the corner frequency can be obtained. This is can be seen in Equation 4.2

$$f_c = \frac{1}{2\pi\sqrt{R_2 R_3 C_1 C_2}} \tag{4.2}$$

Two multiple feedback configurations were made: one sixth order and one eighth order. The Sixth order multiple feedback bandpass filter is shown in Figure 4.2.

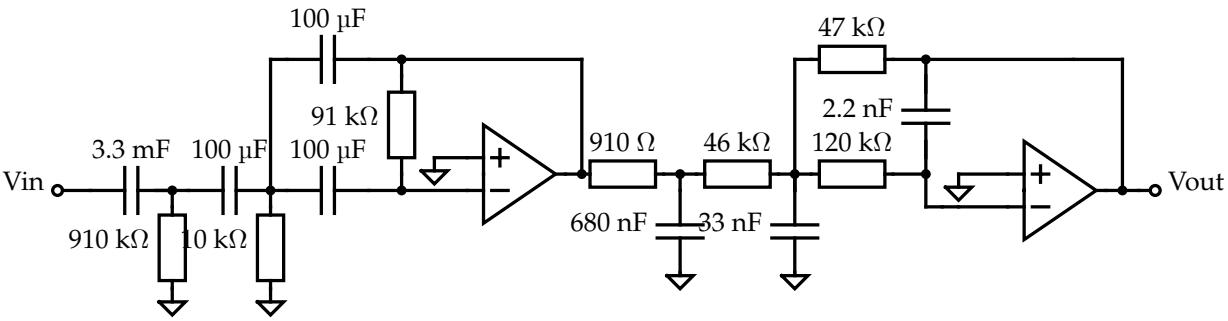


Figure 4.2: Sixth order Multiple Feedback bandpass configuration

In essence this design is a combination of two cascaded second order multiple feedback filters, cascaded with an RC filter ($H_2(s), f_{3dB} = \frac{1}{2\pi RC}$) in front of it. The component values were calculated by multiplying the transferfunctions of the aforementioned stages ($H_1(s)H_2(s)$). Then the corner frequencies of the LPF and HPF stage (which are made up out of the component values) were optimized such that the total LPF and HPF stage corner frequency would be 0.05Hz and 250Hz, respectively.

Figure 4.2 was implemented into an LTSpice model for further analysis on filter performance and group delay.

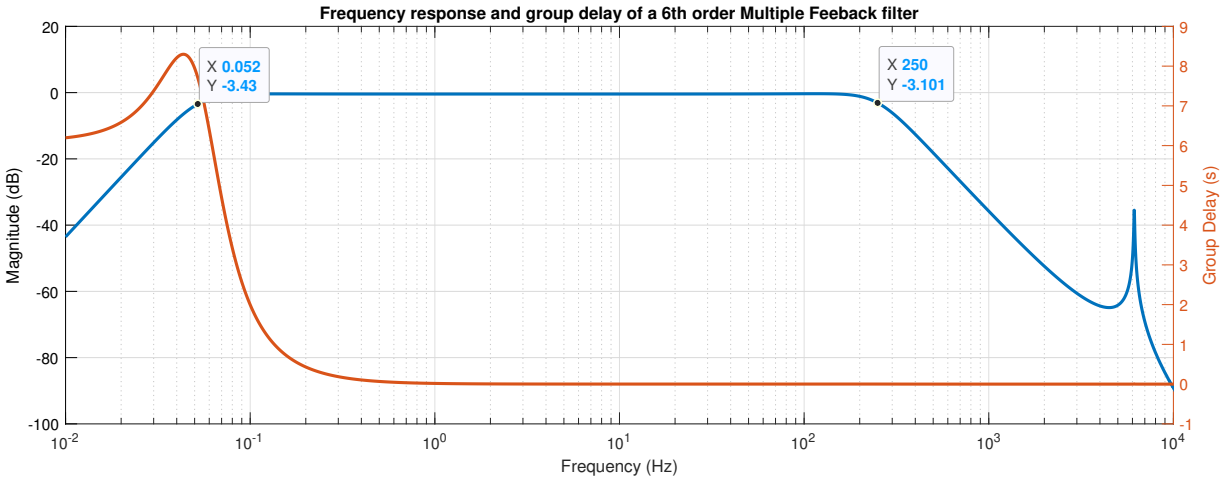


Figure 4.3: Frequency response of a Multiple Feedback 6th order bandpass filter

From Figure 4.3, one can see that the desired filter requirements have been met by this filter topology: A group delay which does not act after 0.05Hz, correct passband bandwith and rolloff[1] of -60dB/dec. However, of this topology the output is inverted and the configuration uses 16 components.

Multiple feedback 8th order

To obtain a stronger rolloff, multiple second order multiple feedback filters can be cascaded after each other (HPF-HPF-LPF-LPF). This will however lead to the following problem: the corner frequencies will shift (if identical corner frequencies are used). To circumvent this issue, one should take a look at the Q factors of the (individual second stage) filter stages such that compensation occurs at the corner frequency. When this Q factor is calculated, the calculation tool [22] can determine the component values as it only works up to third order filters.

[1]The high frequency spike is an artefact of the HPF, which has a resonance at very high frequencies

A butterworth filter can mathematically be characterized by the following [23]:

- It is an all pole realization
- The poles ($\theta_{1,2,3}$) lay on a halfcircle in the left complex half plane
- The angles between the poles are equal
- Even order butterworth filters can be considered as biquad

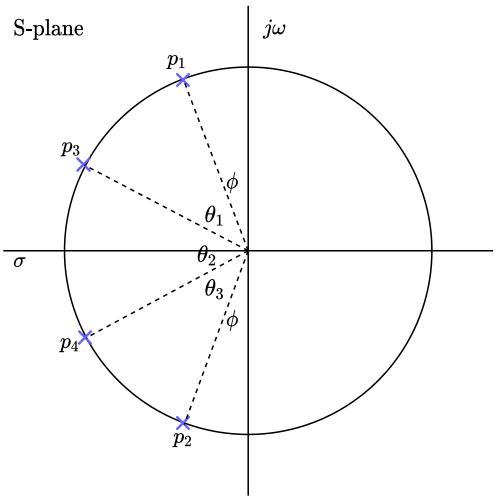


Figure 4.4: Normalized ($\omega_c = \sqrt{\sigma^2 + (j\omega^2)} = 1$) Butterworth poles in the S Plane on the unit circle

The poles of a normalized fourth order Butterworths filter can be seen in Figure 4.4. To find the needed poles p_{1-4} the sine and cosine of the angles need to be taken ($p = \cos(90° + \phi + \theta_1) + j\sin(90° + \phi + \theta_1)$ etc.). In this case those are $\theta_{1,2,3} = 45°, \phi = 22.5°$. The transferfunction of this 4th order filter seen in Equation 4.3. The Q factor is defined as $Q = \frac{\omega_c}{2\Re\mathfrak{e}(p)}$ [23]. And as the poles are complex conjugates one can say that $p_1 + p_2 = 2\Re\mathfrak{e}(p)$ one can conclude that the needed quality factors are $Q_1 = \frac{1}{p_1 + p_2} = 1.30652734$ and $Q_2 = \frac{1}{p_3 + p_4} = 0.54119612$, as the frequency $\omega_c = 1$ due to the normalization.

$$\begin{aligned} H &= \frac{1}{(s+p_1)(s+p_2)(s+p_3)(s+p_4)} \\ &= \frac{1}{(s^2 + s(p_1+p_2) + p_1p_2)(s^2 + s(p_3+p_4) + p_3p_4)} \\ &= \frac{1}{(s^2 + 0.765367s + 1)(s^2 + 1.847759s + 1)} \end{aligned} \tag{4.3}$$

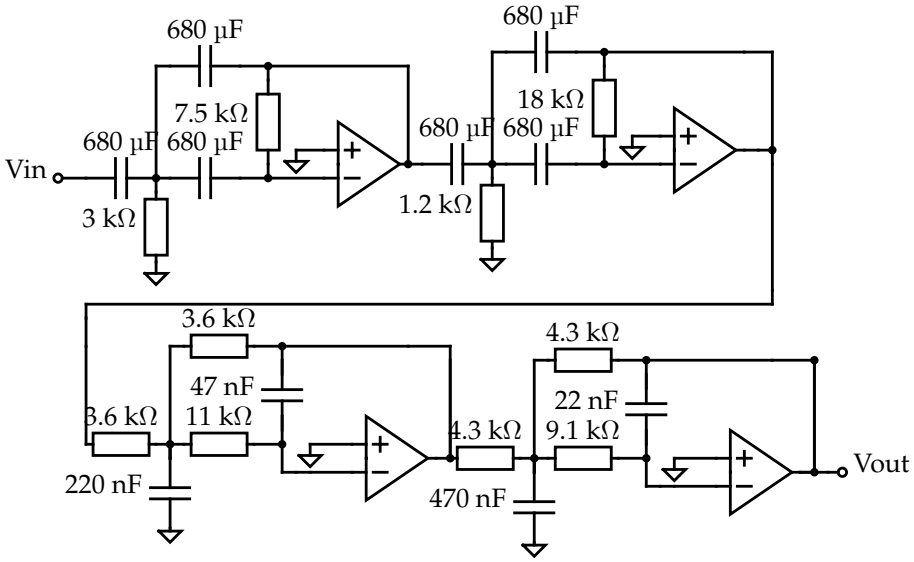


Figure 4.5: Eigth order Multiple Feedback bandpass configuration

The quality factors were entered into the calculation tool, which by frequency transform, gave the component values for the HPF-HPF-LPF-LPF stages of the filter as shown in Figure 4.5.

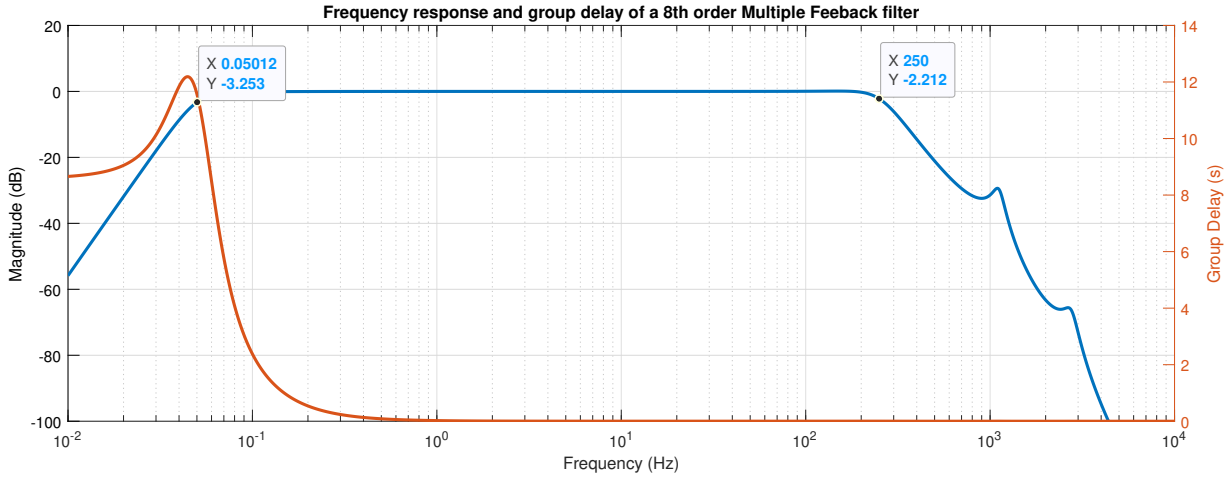


Figure 4.6: Frequency response of a Multiple feedback 8th order bandpass filter

This filter was also simulated in LTSpice, which led to the results as shown in Figure 4.6. Whilst the high-pass corner frequency suffices, the low-pass corner frequency is off. It is expected that there are two reasons for this: The calculation tool uses component values which exist on the market and the effect of the peaks from the double high-pass filter. The group delay is very good, much like that of Figure 4.3. This configuration however, uses 24 components and outputs inverted signal.

Sallen Key 6th order

Another filter topology which was looked into was the Sallen Key configuration (Figure 4.7). This too, is a topology using active components to mimic inductances in filtering circuits. Unlike most other amplifier configuration it employs positive feedback. It does however show some weaknesses in the stopband at higher frequencies (due to capacitance C2). In this subsection the topology will also be cascaded in two ways: sixth order and eight order bandpass (HPF-HPF-LPF-LPF).

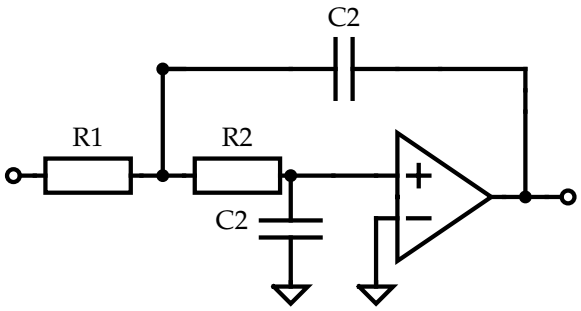


Figure 4.7: Example of an Sallen Key low pass filter

The transfer function of a second order low-pass Sallen Key filter can be seen in Equation 4.4 [22]

$$H(s) = \frac{\frac{1}{R_1 C_1 R_2 C_2}}{s^2 + s\left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_2}\right) + \frac{1}{R_1 C_1 R_2 C_2}} \tag{4.4}$$

From this the corner frequency can be deduced which is shown in Equation 4.5

$$f_c = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}} \tag{4.5}$$

The second order filters were cascaded with a simple first order shunt/series capacitance which, using the same calculation tool as before, led to the configuration as shown in Figure 4.8.

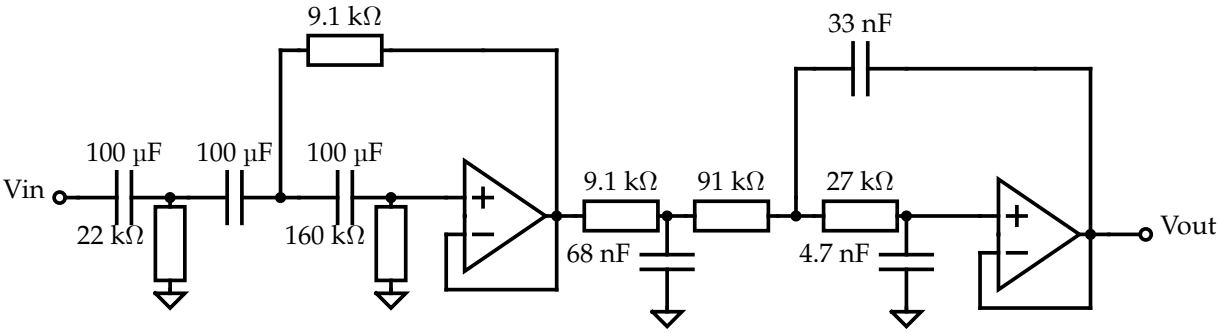


Figure 4.8: Sixth order Sallen Key bandpass configuration

The circuit was evaluated in LTSpice which led to the frequency response as shown in Figure 4.9. The magnitude response is smooth in the pass-band, shows good rolloff (-60dB/dec) and the group delay only starts to be in effect at less then 0.05 Hz. The corner frequency of the low-pass filter deviates from the specified, most likely due to the fact that the calculation tool rounds component values to standardized ones. This configuration uses only 14 components.

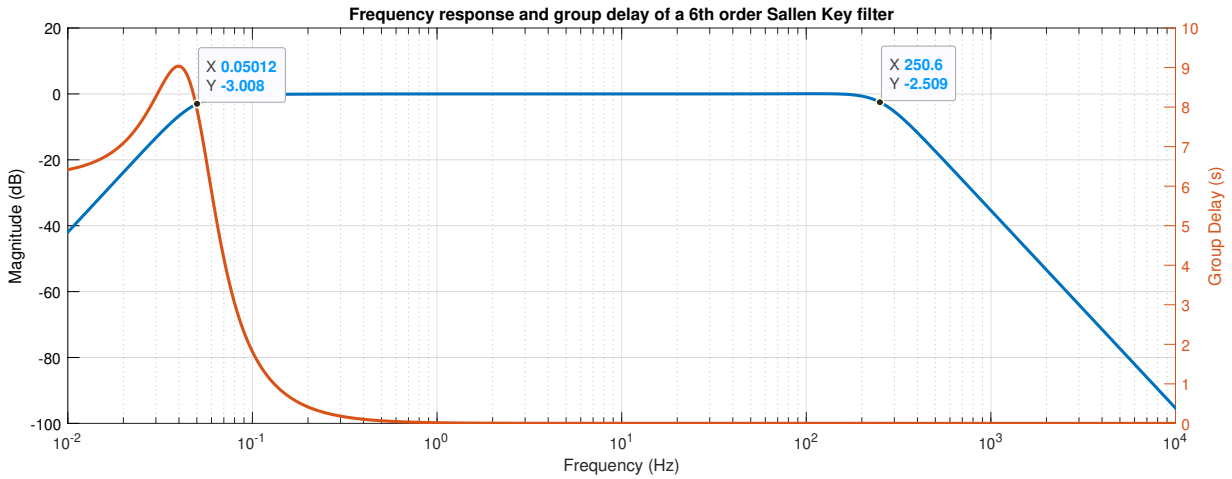


Figure 4.9: Frequency response of a Sallen Key 6th order bandpass filter

Sallen Key 8th order

To obtain a stronger rolloff, much like the eighth order multiple feedback topology, multiple second order Sallen Key stages were cascaded. The same procedure was used to obtain the quality factors and the topology as seen in Figure 4.10 was created.

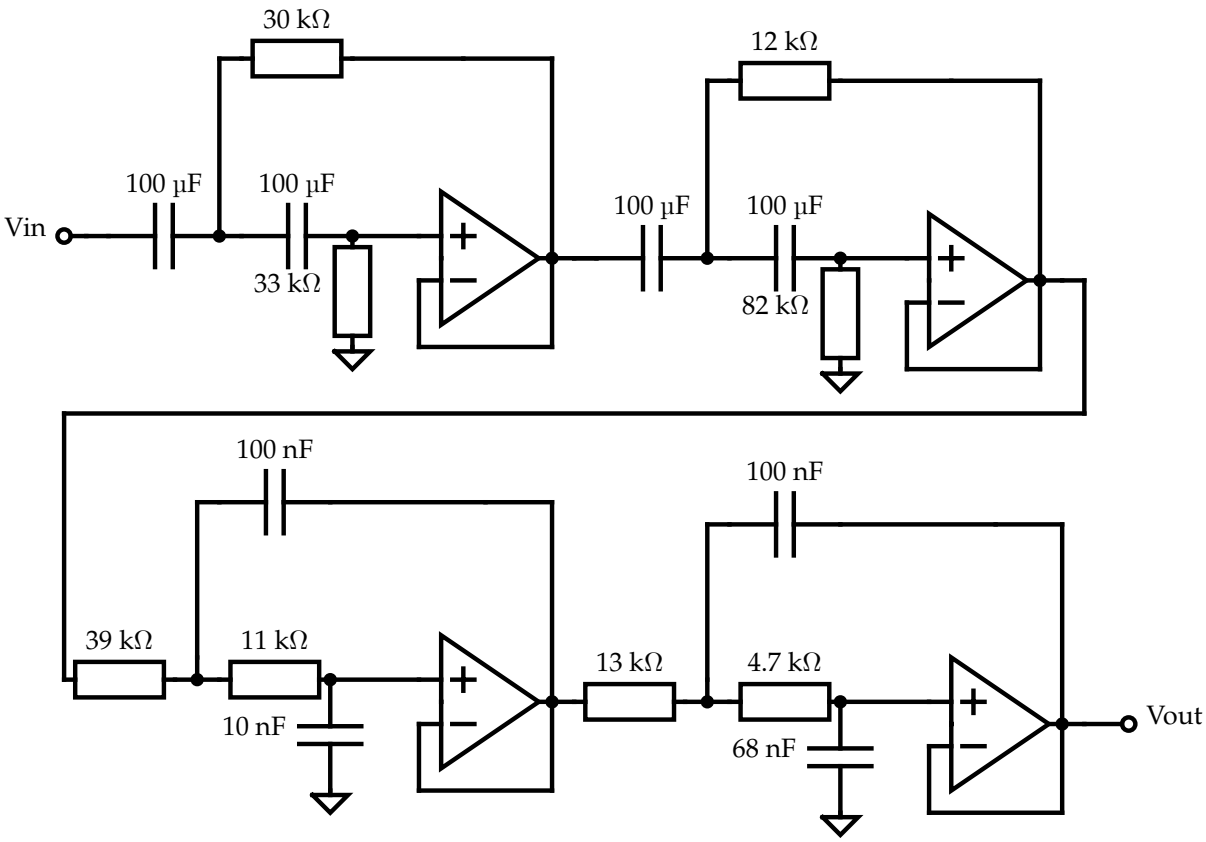


Figure 4.10: Eigth order Sallen Key bandpass configuration

This circuit was simulated in LTSpice, leading to the results as shown in Figure 4.11

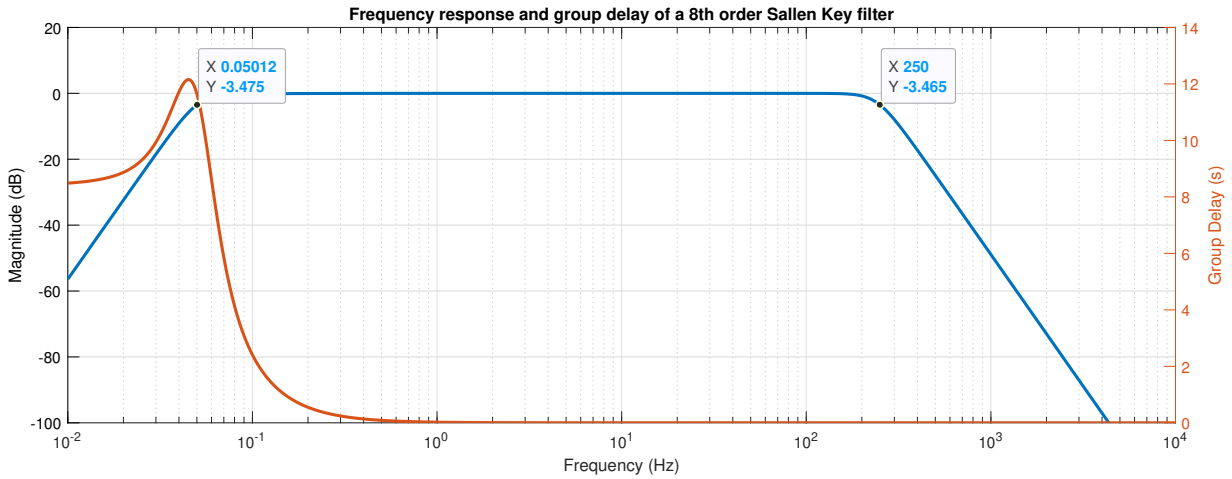


Figure 4.11: Frequency response of a Sallen Key 8th order bandpass filter

A good flat response can be seen in the passband of the filter, it shows the correct corner frequencies and the group delay only acts at frequencies less than 0.05Hz. The topology however uses a lot of components; 20.

Cost analysis

To select the correct filtering topology all obtained simulation results were bundled in the cost matrix shown in Table 4.2.

Table 4.2: Cost analysis matrix

	6th order MF	8th order MF	6th order SK	8th order SK
LPF performance	-	-	+	++
HPF performance	++	++	++	++
Group delay	++	++	+	++
# of components	16	24	12	20
Other	Inverted output	Inverted output	N/A	N/A

One can therefore conclude that the Sallen Key topology fits best for the project. Smooth correct rolloffs, good group delays and less components needed than an multiple feedback topology.

Filter order
The filter rolloff is determined by the order. It shows how fast the signal attenuates towards the stopband. Increasing the order of the filter does imply using more components. As the prototype needs to process 9 signals from the body, a difference of order means an extra 72 needed components. To check whether the extra rolloff is needed for signal shape preservation, a sample heartbeat [24] (ANSI/AAMI test reference ECG signals) was ran through both circuits and compared to each other. The results can be seen in Figure 4.12.

As one can see, very little difference is seen when comparing the waveform of the sixth and eighth order Sallen key filters. (Furthermore, the difference between reference and filtered signals was not distinguishable by eye by any of the group members). In the view of reducing space, (assembling)time, weight and noise the sixth order Sallen Key configuration was selected as the main filter topology.

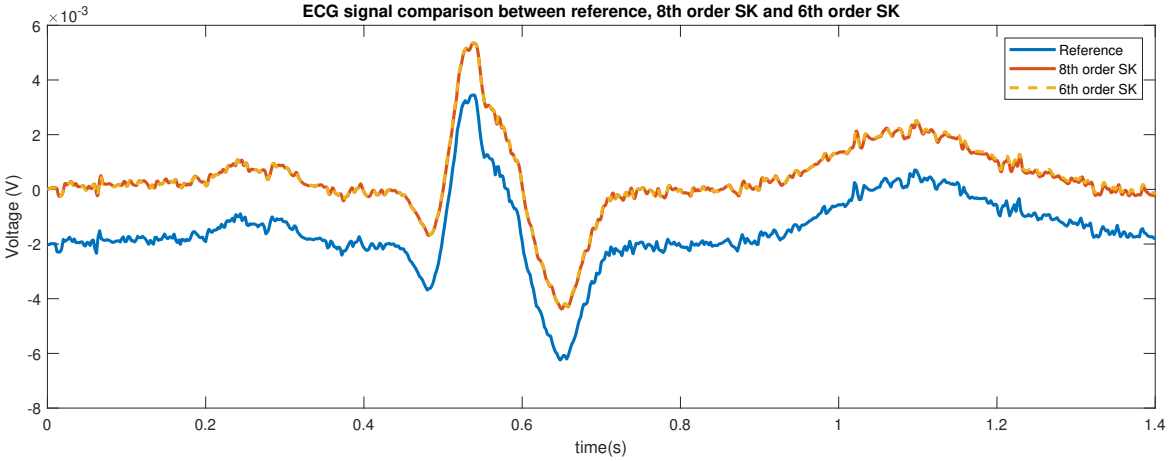


Figure 4.12: Comparisons of filter effects on the shape of the ECG waveform

4.1.4. Offset

Before the signal can get measured by the Analog to Digital Converter (ADC), it needs to get through one more stage. As the ADC has a maximum operating voltage of -0.3 to 3.3V, the signal needs to be placed at a higher potential (as ECG signals can get negative). In addition, protection for extensive negative voltages from the ECG signal must be built in. This led to the equivalent circuit as shown in Figure 4.13 where C_{ADC} is the internal capacitance of the sample and hold circuit of the Nucleo [25].

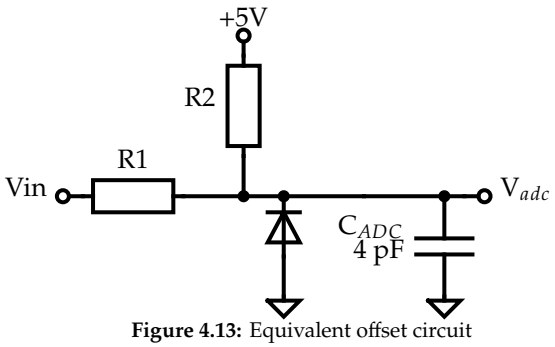


Figure 4.13: Equivalent offset circuit

The circuit works as follows:

1. 300 mV (no DC offset) signal enters the circuit (0.3mV × 1000)
2. An offset of $\frac{R1}{R2+R1} * 5$ is added to the signal [2]
3. Should the signal be too negative (operating voltage ADC is -0.3 to 3.3V), it is discharged through the shunt diode.
4. The signal charges the internal capacitance of the ADC

To ensure the ADC can take a good value (and reduce noise) low values should be chosen for $R1$, $R2$. To give an offset of 1.66V the resistances $R1 = 5k\Omega$ and $R2 = 10k\Omega$ were chosen.

4.1.5. Noise and Power simulations

To simulate the added noise at the output of the circuit on the signal, an LTSpice noise analysis was done on the entire circuit. To complete PoR goal G6H.a the added noise should be less than the quantization noise. The ADC is 16-bit and has an voltage range of 0-3.3V. This leads to a noise ceiling of $\epsilon_{max} = \frac{N_{voltage}}{2^{N_{bits}} - 1} = \frac{3.3}{2^{16} - 1} = 50.35\mu$V. For this SPICE models of the INA821 and TL072 were used. The noise spectrum of the circuit can be seen in Figure A.1. (The "entire circuit" is one channel as shown in Figure B.1) Of this data the total RMS noise was calculated via LTSpice. This amounted to be $V_{rms} = 15.74\mu$V over the entire signal, which is lower than the quantization noise ϵ_{max} of the system.

The power consumption was also simulated by checking the output current of the ±5V supply rail. It amounted to $\tilde{1}$0mA for a single filter channel.

[2] When testing the prototype this configuration proved to be not as resilient as originally hoped, more on this in subsection 7.2.3

4.2. Receiver

The receiver component is less complex compared to the transmitter. It receives the signal from a DAC, reconstructs it with a reconstruction filter, removes the DC component and attenuates it to the original level.

4.2.1. Reconstruction filter

To remove the digital artifacts out of the signal, a reconstruction filter was needed. To check what filter order was best three configurations have been tested: A simple shunt capacitor and a second/third order Sallen Key filter. The test was done by quantizing a heartbeat signal with the onboard LTSpice ADC/DAC component. This component has an infinite resolution but for the purposes of testing reconstruction rate this is irrelevant (The signal is sampled at 500Hz). The signals then went through the reconstruction filter stage which led to the results seen in Figure 4.14.

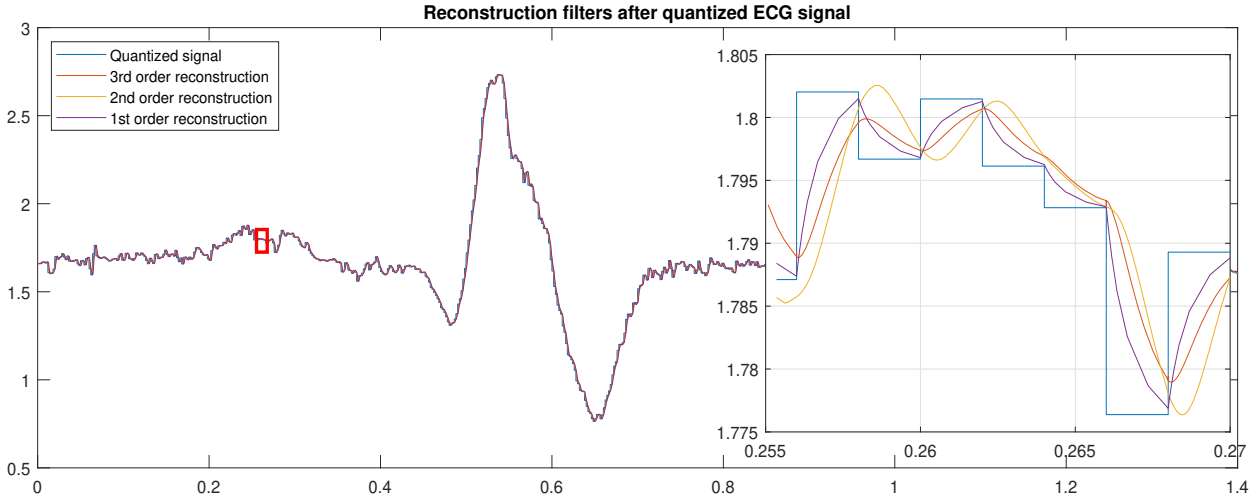


Figure 4.14: The reconstructed signal from three configurations, Red square is magnified

From this figure it can be concluded that the third order Sallen Key configuration leads to the least amount of distortive traces (RC discharge curves) of the reconstruction.

The output ECG signal should be freed of the DC offset introduced at 7.2.3. To do this a High pass filter (shunt capacitor) with a corner frequency of 0.05 Hz was implemented with component values R = 500$k\Omega$ and C = 5 μF.

4.2.2. Attenuation

As the circuit is plugged into another heart monitor, the signal needs to be attenuated again. This should be done with care, as the attenuated signal is very sensitive to noise added by output resistances. As the project became more and more time constrained it was decided to place a 5kΩ trim potentiometer in a voltage divider with a 1kΩ resistance (This resistance was later shorted to allow for more attenuation). This way the attenuation could be set at the optimal point and assembly could start as soon as possible.

4.2.3. Noise and power calculations

To calculate the added noise on the output of the circuit (one channel as shown in Figure B.4), the same noise simulation was done in Ltspice as the receiver. It led to the results as shown in Figure A.2. Of this data the total RMS noise was again calculated via LTSpice. This amounted to be V_{rms} = 1.572μV over the entire signal. The added output noise is again lower than the quantization noise ϵ_{max} of the system.

The power consumption was measured the same way as that of the transmitter, the output current of the 5v rail voltage source was measured. This amounted to a current draw of 9.72 mA.

5

Prototype

To test the complete system (i.e. Amplification, attenuation, filtering, voltage level offset, and the interfaces with the Nucleo board and the ESP32 module), and fulfill requirement **G1H.a**, prototypes were developed of both the transmitter module and the receiver module. The design choices specific to the prototype as well as the process and results will be described in this chapter.

5.1. Design considerations

According to Requirement **G10H.d**, the design of the prototype shouldn't interfere with the progress of the other subgroups. This was accomplished by choosing development platforms (microcontrollers of interest on development boards) that can be used independently of each other. However, for the final prototype of this project, these development platforms must be integrated with each other.

5.1.1. Size

Due to the large size of the STM32 Nucleo development board which is used by the DSP subgroup, and to fulfill Requirement **G8**, the size of this development board was kept as a guideline for maximum dimensions of the prototype, such that when placed stacked on top of eachother, the size would only increase in depth, rather than in width and height.

5.1.2. Placement

To accommodate for the development platforms that were mentioned in section 5.1, several restrictions were put on the PCB design because of their physical dimensions. Because of the small magnitude of the voltages measured on the patients body, short traces are preferred as they decrease the amount of parasitic capacitance, resistance and inductance. Additionally, because the edge of the PCB is a

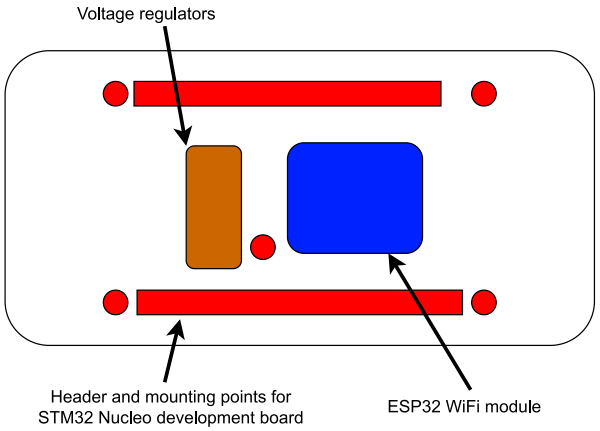


Figure 5.1: Placement restrictions due to development boards used by other subgroups

logical position for the electrodes, the edge is the most appropriate position to place the filtering circuits mentioned in subsection 4.1.3.
The STM32 Nucleo development board[2] contains headers which allow peripheral devices to be connected. These were connected to the prototype PCB. The ESP32[1] has to communicate with the STM32 Nucleo development board through the mentioned headers. Therefore, placing the ESP32 right next to the headers was chosen as a suitable location. In Figure 5.1, the restrictions are visualized.

5.1.3. Testability

To fulfill **G10H.c**, several measures were taken:

- **Oscilloscope test points** were placed at the outputs of the filtering circuits on the receiver side to allow for easy testing
- **ESP32 Programming Header** was installed on the PCB to allow for debugging while the PCB is in use
- **Variable resistors** were installed to allow modifications while testing to see if the circuit performs as expected
- **Placing all parts on one side** allows the tester to easily access all parts with a probe or multimeter

5.1.4. Manufacturability

As mentioned in subsection 5.1.2, smaller traces are preferred when working with sensitive signals. Additionally, smaller parts are also preferred as parasitics also decrease with part size. However, to make a prototype that is still manufacturable in 10 weeks (Requirement **G10**), parts were chosen that are commonly used and available (Requirement **G10H.b** and **G11H**), and as small as possible while still solderable by hand (Requirement **G10H.a**).

Placing all components on a single side of the PCB not only increases the testability of the prototypes, but also increases manufacturability, because tools such as a PCB hot plate or a reflow oven can be used to solder the components.

5.1.5. Power

Batteries
Because the power consumption of the components used by the DSP and Protocol subgroups was not known prior to designing the power circuitry, the battery sizing was done after power measurements were done on each subgroup. From the measurements, the following figures were acquired:

Filtering circuitry: 90mA
STM32 Nucleo Development board: 230mA
ESP32: 140mA
Linear voltage regulators: 25mA
Total: 485mA

Using this as a guideline and adding a margin of 10%, 4x 9V batteries with 550mAh of capacity each connected with 2x in series and 2x in parallel provide the right voltage and power requirements to comply with Requirement **G7**. In Figure 5.2, the lay-out of the main components are visualized.

Voltage regulators
In a wireless system, efficiency is key to using small batteries. To bring the voltage of the batteries to a constant level that is suitable for the electronics, voltage regulators are used. The three types of voltage regulators that were considered are linear voltage regulators, low drop-out regulators and switching regulators. Switching regulators have the benefit that they are more efficient than linear voltage regulators and low-dropout regulators. However, switching voltage regulators also introduce switching noise, which needs to be attenuated to avoid this noise from showing up in the measured signals. This requires additional components, which add complexity to the circuit. As the voltage regulation was not the focus of this project, LDOs were used for both the positive and for the negative rail. These regulators were sized to allow for a large margin of current consumption because at the moment of designing, the requirements for power were not known.

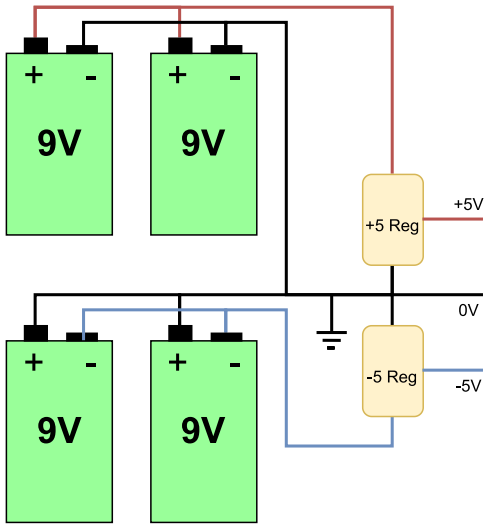


Figure 5.2: Power circuit used for the prototypes

Selected components:
XC6902N501PR-G [26] $V_{in} = -2.4V \rightarrow -16V$, $V_{out} = -5V$, $200mA$ LDO voltage regulator
NCP1117ST50T3G [27] $V_{in} = 3.5V \rightarrow 20V$, $V_{out} = 5V$, $1A$ LDO voltage regulator

5.1.6. Additional measures

Power planes
To further improve the performance of the filter circuits, power planes were used. These fill up all remaining PCB surfaces that are not occupied by traces and components. Due to their large surface, resistance is greatly reduced which improves the stability of the supply voltages at the IC pins. Due to the PCB being a 2-layer PCB, only power planes were used for +5V and 0V.

To improve the stability of the supply voltages for the analog circuits, separate voltage regulators were used, such that the analog circuits and digital circuits are separated. This works because the switching of digital signals creates variations on the supply voltages [28].

Bypass capacitors
When more than 1 digital IC are connected to the same power rail, the digital IC will cause small disturbances in the rail which can result in disturbances in the other components. This effect was reduced by installing bypass capacitors with a value of 0.1uF. This generally is a good value for most applications [29].

Selected component:
CC1206KKX7R0BB104 [30] SMD Multilayer Ceramic Capacitor, 0.1 µF, 100V, ±10%

Traces
Traces were sized according to two groups. Power lines and data/signal lines. As only -5V is applied using traces (instead of a power plane), only the -5V rail will be considered for the power group. Using $R = \rho \cdot \frac{l}{A}$, where $\rho = 1.72 \cdot 10^{-8} \frac{\Omega}{m}$, the resistivity of copper at room temperature, the following trace resistances are calculated:

Table 5.1: Expected max trace resistances and their effect. Trace thickness is 350μm. Current for the -5V rail was estimated as simulated current draw of all filtering circuits combined. Current for the signals was estimated as maximum voltage divided by minimum resistance.

	Width [mm]	Trace length [mm]	Trace impedance [Ω]	Current [mA]	Voltage drop
-5V rail	0.5	133	0.13	100	13mV
Signal	0.3	10	0.016	0.0055	88nV

Although 13mV seems like a large drop, considering that requirement **G6D.b** is that the resolution should be <15uV, there is no effect on the analog signals if the voltage drop is constant. The concern is the maximum "ripple" on the supply that is caused by the trace resistance on the rail. From the simulation can be derived that although there is a noticeable voltage supply ripple of several micro-volts, the signal is not distorted. The bypass capacitors of $0.1\mu F$ that are installed next to every IC will not reduce this amount, as the cut-off frequency of the LPF that consists of the trace resistance and the by-pass capacitor is:

$$F_{-3dB} = \frac{1}{2\pi \cdot RC} = 12Mhz$$

which is far larger than the frequency components of the supply deviations which are in the range of the signal data; 0.05Hz to 250Hz. From this, it is concluded that the voltage drops will not affect the signal and therefore, requirement **G6D.b** is still fulfilled.

5.2. Process

5.2.1. Schematic

Using the design considerations, the complete schematics were drawn. Following this, the PCBs were designed using Autodesk EAGLE PCBs design software.

5.2.2. Component selection

Components were chosen as described in subsection 5.1.4. From these requirements the following packages were chosen:

- Resistors: 0805 package
- Capacitors: 1206 package
- ICs: SOIC and TSSOP where SOIC is not available

where the package sizes are imperial.

5.2.3. PCB

As can be seen in Figure 5.3, the component density was kept as high as possible to minimize the trace length and therefore parasitic resistances.

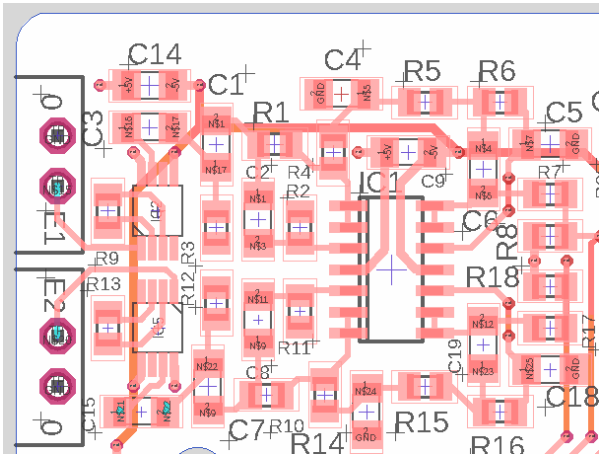
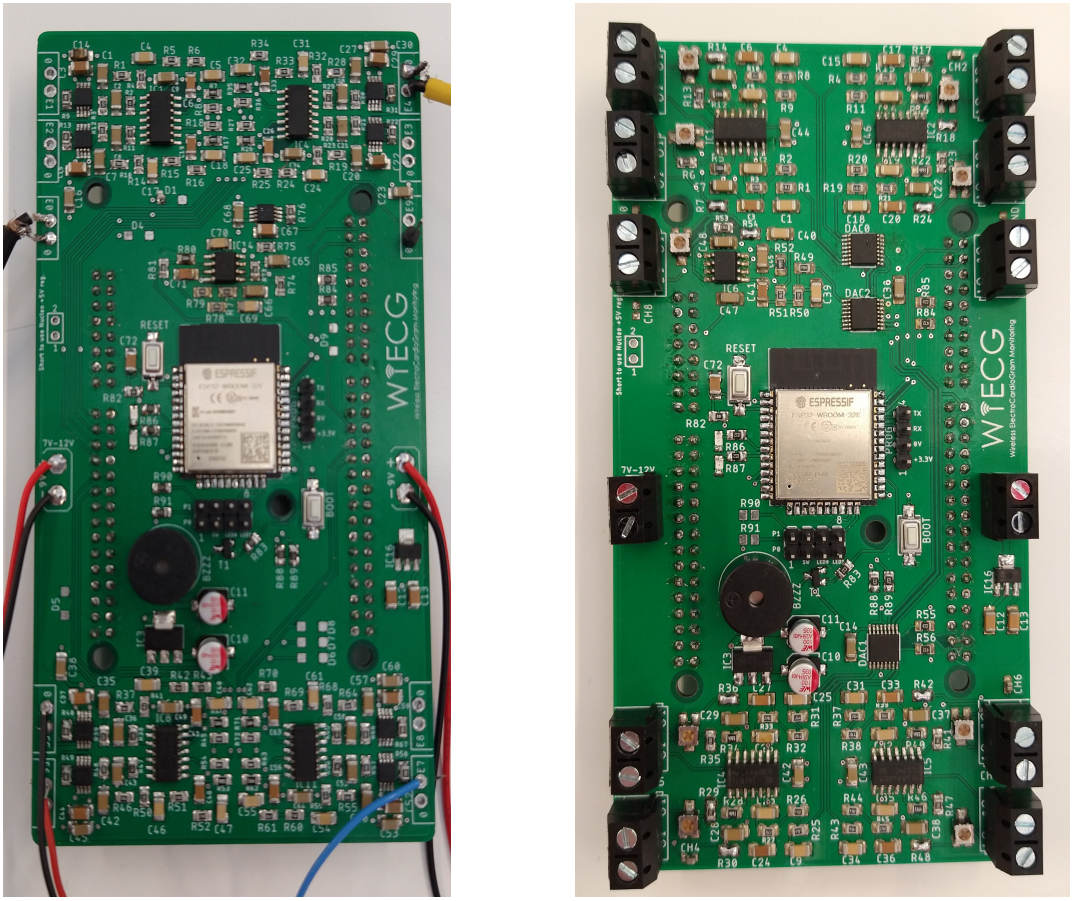


Figure 5.3: Filtering sections of 2 out of 9 channels

5.2.4. Soldering

While all of the components are solderable by hand, a stencil was used to improve the quality of the soldering. While the stencil was placed on the empty PCB, solder paste was applied (almost) perfectly on the pads of the components and nowhere else. Components were placed on the solder paste using tweezers. The components were soldered using a Weller hot plate WHP3000. Some components had to be retouched using soldering irons, tweezers, blood, sweat, and tears.

5.3. Results



(a) Transmitter **(b)** Receiver

Figure 5.4: Prototype PCBs

The total weight (Inluding the 9V batteries), is approximately 300g.

With the dimensions: 133mm x 70mm x 30mm, requirements **G8** and **G9** are satisfied.

5.4. Cost

Table 5.2: Estimated cost for 1 prototype

	Transmitter	Receiver
Components	€100	€90
PCB	€1,20	€1,20
Nucleo	€30	€30
Shipping	€60	€60
Total	€191,2	€181,2

In Table 5.2, estimations of the cost of the prototypes are given. The shipping cost could be lowered if there was no time contraint. From this table can be concluded that **G11** has been fulfilled.

5.5. Possible improvements

Because time was limited due to requirement **G10**, there are too many factors too take into account when only 1 iteration is possible.

- As mentioned, power planes are used to reduce the resistance of supply paths. Due to the large amount of components, the plane on the side of the PCB where the components are is not very uniform. (especially in between the filtering circuits) This could be avoided by using 4-layer PCBs. This way, because all components are on a single side of the PCB, solid power planes would be available for -5V, 0V, and +5V.
- While designing, the hardware guidelines for the ESP32 module were not followed leading to the following issue: The 0V power plane extends underneath the antenna. This can cause interference of the transmitted signals, reducing signal strength [31]. Making sure that the area underneath the antenna is clear (e.g. by placing the ESP32 on the edge of the PCB) would prevent this from happening.
- While soldering electrodes and their shielding is an easy solution to attach the electrodes to the PCB, purpose made (screw)terminals for co-axial cables would make manufacturing easier and more robust. The robustness in the current system is low because of the metal-fatigue wearing out the exposed copper near the PCB.
- As voltage drops are a big risk for this sensitive application, wider traces and a thicker copper layer would further reduce the impedances of the traces and therefore improve the stability of the supply rails and decrease the distortion on the signal paths.
- Ideally, a different type of battery cell would be used which has the right capacity (instead of multiple cells parallel) and with a rechargeable chemistry such as Li-Po or Li-Ion. The main down-side is that there will always be multiple cells necessary, as Li-Po cells have a nominal voltage of 3.7V. Furthermore, these would also require a battery management system which prevents under- and overcharging. Example parts for such an improvement are: 6x Melasta LP803048 Li-Po cells [32] and a 6 cell balancing circuit with under- and overvoltage protection.
- To counteract the effects of bad conductivity of the electrode probes, the gain of the instrumentation amplifier could be made variable. This can be employed using a potentiometer or an active feedback network. This should ensure that the circuit always amplifies the signal to a certain range. Avoiding under-amplification or clipping of the signal.
- In this project safety has faded to the background in the design. It is however a critical aspect of electrical devices, especially devices related to health. To improve the safety of this design, the following measures could be taken:
  - Install fuses such that a short would not destroy the circuitry or the power source
  - Make sure that batteries can be plugged in / make contact, in only one orientation. While 9V batteries do have only one orientation that they can be plugged in, accidentally touching the terminal in reverse could damage the circuitry and/or the batteries.

6

Measurements

After the prototype was assembled, the following measurement set-up was used to verify the performance of the filtering circuits. Tools used: Function generator: Tektronix AFG3021B, oscilloscope: Tektronix TDS2022B. Network analyzer: SR770 FFT network analyzer.

6.1. Transmitter

6.1.1. Amplification

The amount of amplification done by the instrumentation amplifier was measured by applying a $13mV_{pp}$ sine at a frequency of 100Hz to the input of the instrumentation amplifier.

The resulting amplitude of the sine at the output of the instrumentation amplifier is:

$$V_{out} = 9.60V$$

Therefore the amplification factor is:

$$A = \frac{V_{out}}{V_{in}} = 738.5$$

When a 7mVpp signal is applied to the input, at the ADC, 3.3V is measured, resulting in a total amplification (including offset attenuation) of 446x.

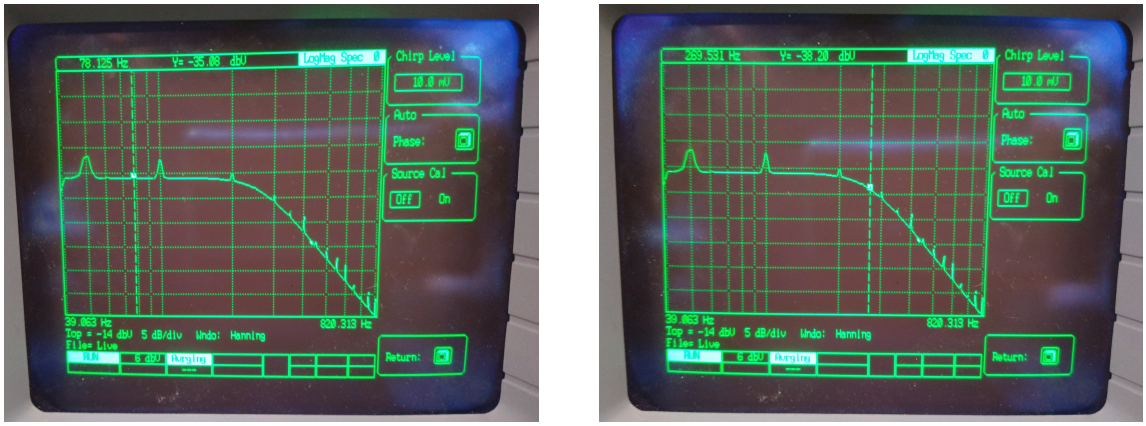
6.1.2. Filters

Methods

The function generator was connected to the input of the instrumentation amplifier on the PCB. The function generator was applying a sine waveform with an amplitude of 10mV. This was attenuated using a voltage divider to reduce the amplitude to 1mV. The frequency was swept within the bandwidth of which measurement points were taken. The results are shown in Figure 6.3 and Figure 6.5

Additionally, a network analyzer was connected to the circuit which used a chirp signal to measure the frequency response. These results can be seen in Figure 6.1a and Figure 6.1b.

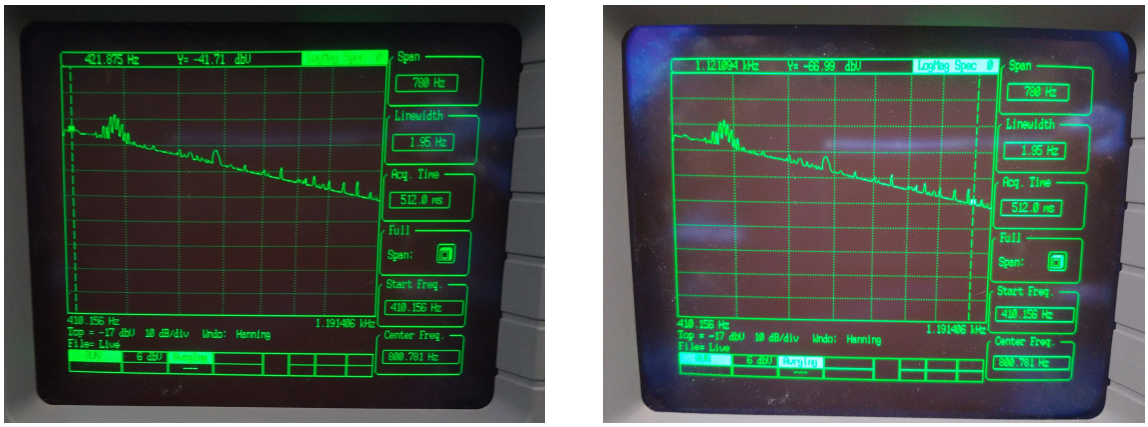
Results



(a) Roll-off curve of the low-pass filter. Marker at pass-band

(b) Roll-off curve of the low-pass filter. Marker at -3dB point

Figure 6.1: LPF roll-off curve shown with markers at different points



(a) Roll-off curve zoomed in at stop band. Marker at point A

(b) Roll-off curve zoomed in at stop band. Marker at point B

Figure 6.2: LPF roll-off curve zoomed in at the stop-band with markers at different points. As a source for the network analyzer, a 10mV chirp was used

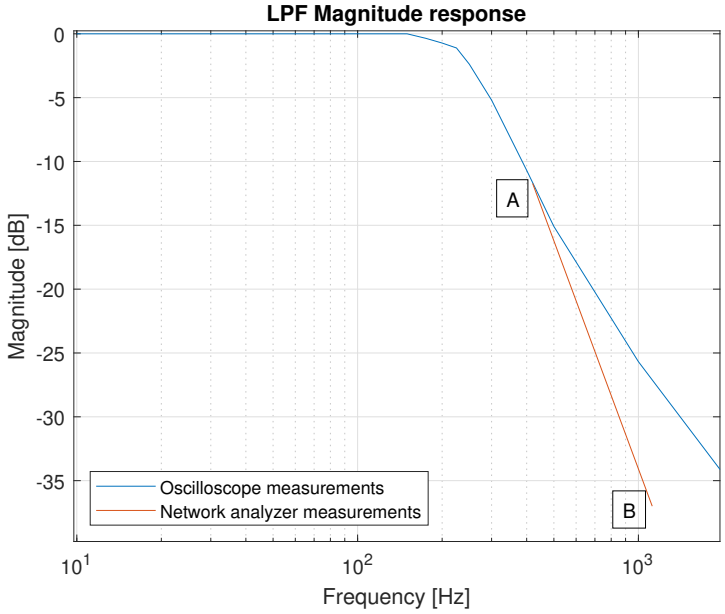


Figure 6.3: Filter response of the 6th-order Sallen-Key low-pass filter. Point A and B come from Figure 6.2a and Figure 6.2b and are off-set with 30dB to account for the magnitude of the LPF in the pass-band

Using the coordinates of points A and B: $A = \begin{bmatrix} 420Hz \\ -11.72dB \end{bmatrix}$, $B = \begin{bmatrix} 1120Hz \\ -37.00dB \end{bmatrix}$. Extrapolating this results in a estimated roll-off rate of 64dB/decade.

Figure 6.4: Filter response of the 6th-order Sallen-Key high-pass filter measured using a network analyzer and as a source: 10mV chirp

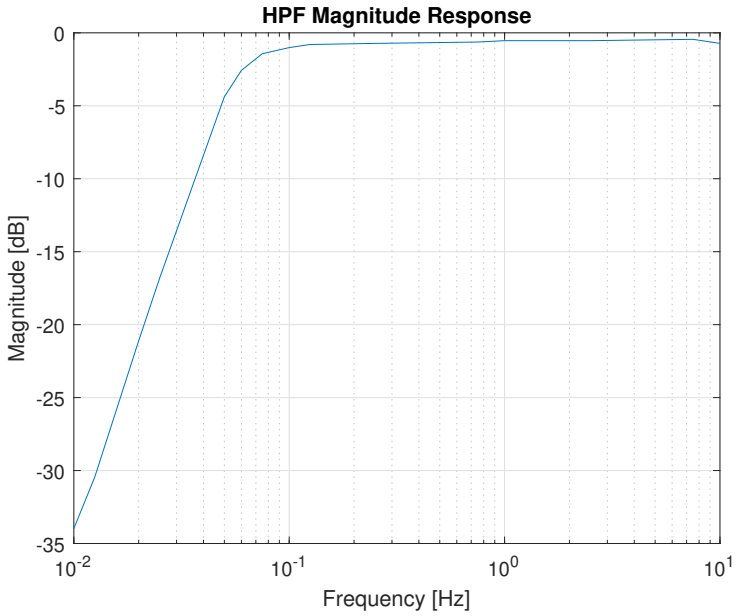


Figure 6.5: Filter response of the 6th-order Sallen-Key high-pass filter

Extrapolating the line in the pass-band shown in Figure 6.5 results in an estimated roll-off rate of 45dB/decade.

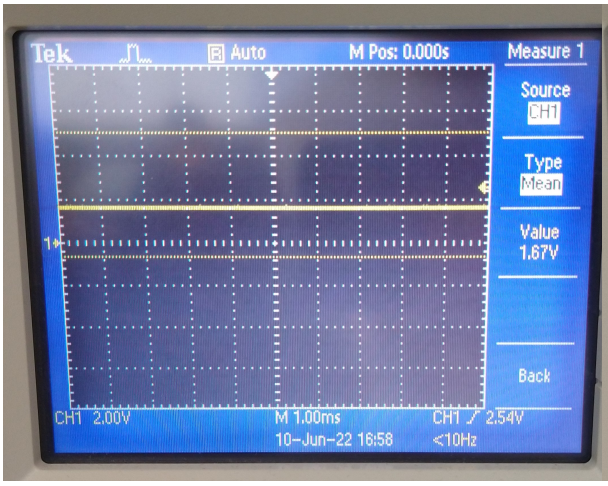
6.1.3. Offset circuit

To measure the offset circuit, 0V was applied to the electrode.

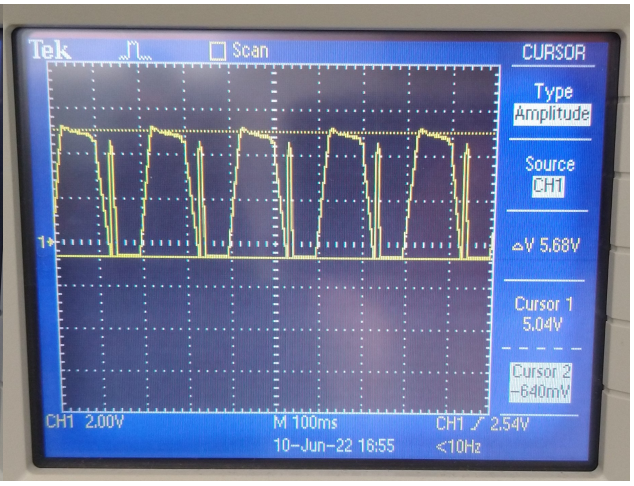
Resulting amplitude at the output of the filtering circuit:

$$V_{offset} = 1.67V$$

The maximum and minimum voltage that can be reached at the output of the offset circuit are: Maximum voltage of 5.0V. Minimum voltage of -0.64V.



(a) Offset when 0V is applied to the electrode



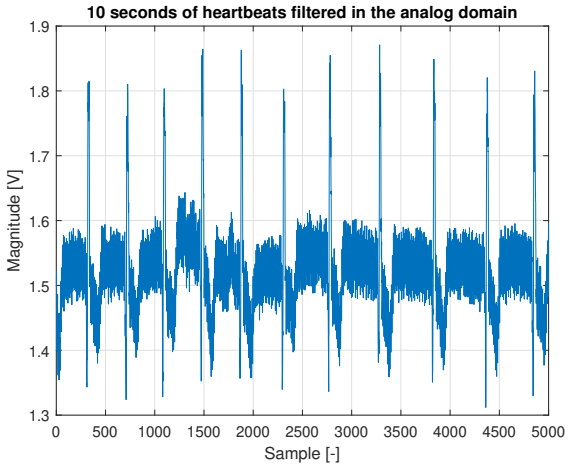
(b) Max. and min. amplitude when a sine of 5Hz 18mVpp is applied

6.1.4. Heartbeat

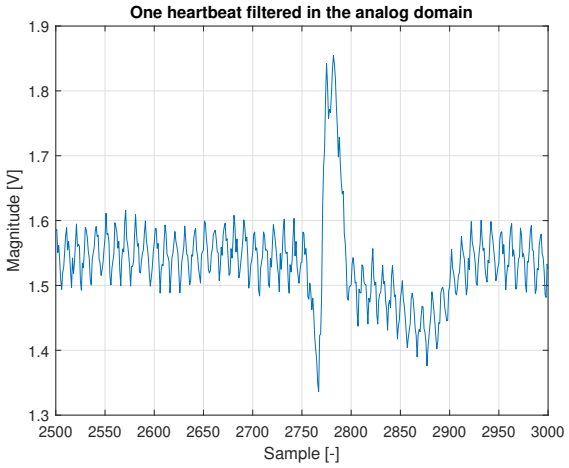
Methods

Ceracarta Top Trace electrodes [33] were applied to a patient. These were connected to the Transmitter PCB using electrode cables (From a Corpuls [34] heart monitor). The positions of the two electrodes whose differential was measured are known as V2 (directly on top of the heart), and the right leg (Ground).[1]

Results



(a) 10 seconds of heartbeats measured by the ADC of the Nucleo development board sampled at 500Hz



(b) A single heartbeat measured by the ADC of the Nucleo development board sampled at 500Hz

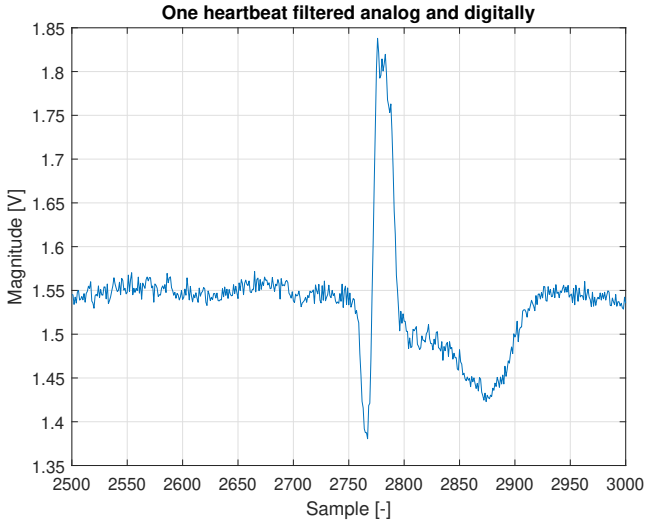


Figure 6.8: A single heartbeat filtered in both the analog and in the digital domain

6.2. Receiver

The low-pass filter in the receiver is identical to the one in the transmitter module. Because of this and because of the complexity of measuring the roll-off at the output of a DAC, no extra measurement is shown.

[1] Usually V2 is measured against the Wilson Central Terminal instead of ground. This results in a differing waveform.

6.2.1. Attenuation circuit

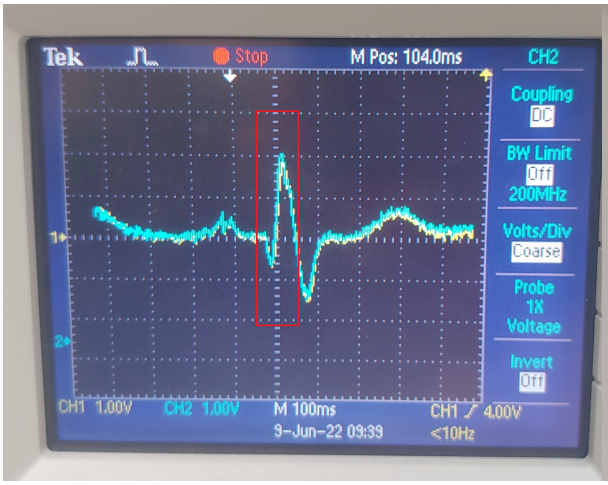
The attenuation is a simple voltage divider with selectable attenuation using a trimmer resistor to a range of : 5x to ∞(i.e. connected to ground). Therefore, no additional measurement was done.

6.2.2. Heartbeat

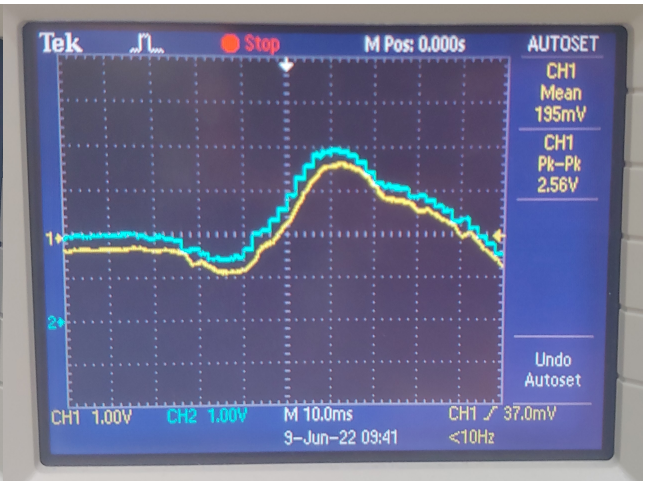
Methods

A regular heartbeat signal was transmitted to one of the DACs. The resulting waveform was measured directly at the output of the DAC (i.e. quantized), and also at the output of the filter stages.

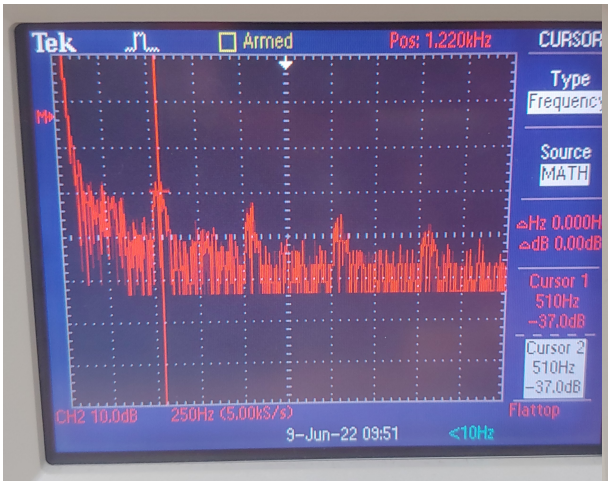
Results



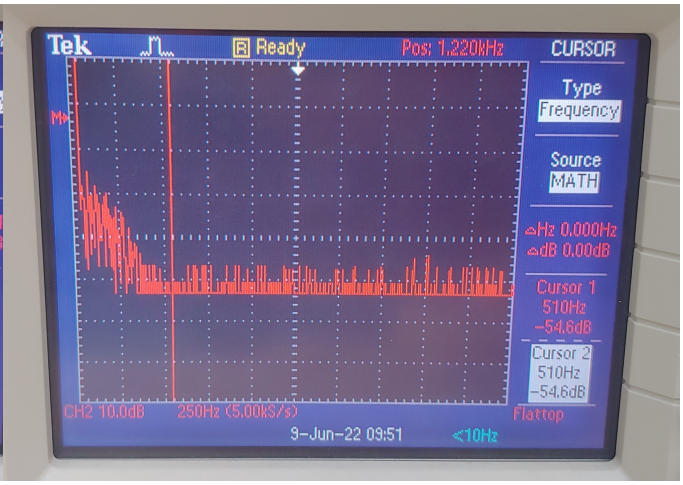
(a) Heartbeat before and after the filter stages



(b) Heartbeat before and after the filter stages, zoomed in



(a) FFT of the heartbeat signal from the DAC



(b) FFT of the heartbeat signal after filtering

The reason why the waveform is not shown after attenuation (by 500x) is that the amplitude of the heartbeat becomes so small, that the noise introduced by the lead of the oscilloscope greatly exceeds the expected heartbeat, making the heartbeat unrecognisable.

7 Discussion

In this chapter, a discussion is given on the reliability of the system, and the accuracy of the acquired results.

7.1. Reliability

While reliability is a crucial point while developing a medical device, delivering a functional prototype is the main goal during this project. In this section, a description will be given on how this product can be designed for reliability.

A medical product can be designed for reliability using the following 5 paradigms [35]:

1. Spend significant effort on requirement analysis
2. Critical failure is not an option for medical devices
3. Measure reliability in terms of total lifecycle cost
4. Do not just design for reliability, design for durability
5. Design for prognostics to minimize suprise failures

Requirement analysis As medical grade electronics have relative high requirement standards compared to other branches, a thorough analysis should be done. The following requirements would be applicable to set-up for the device described in this thesis not considering the efficiency of manufacturing:

- Functional requirements
- FDA standards and compliance requirements
- Reliability requirements (The chance of failure given a usage period length)
- Durability requirements
- Environmental requirements (Temperature, humidity and altitude)
- Handling requirements (vibrations, shocks, packaging materials)
- Installation requirements (Mistake-proofing)
- UI requirements to ensure ease of use, alerts and robustness against human mistakes
- Maintainability/Serviceability requirements, to make sure the repair and testing time are adequate
- Output/Input requirements

Failure analysis When peoples lives are at stake, a critical failure is not acceptable. Therefore, a FMEA (Failure Modes and Effects Analysis) is a useful tool to identify all failure scenarios. To each of the blocks, a probability should be determined such that the magnitude of the concerns is quantified.

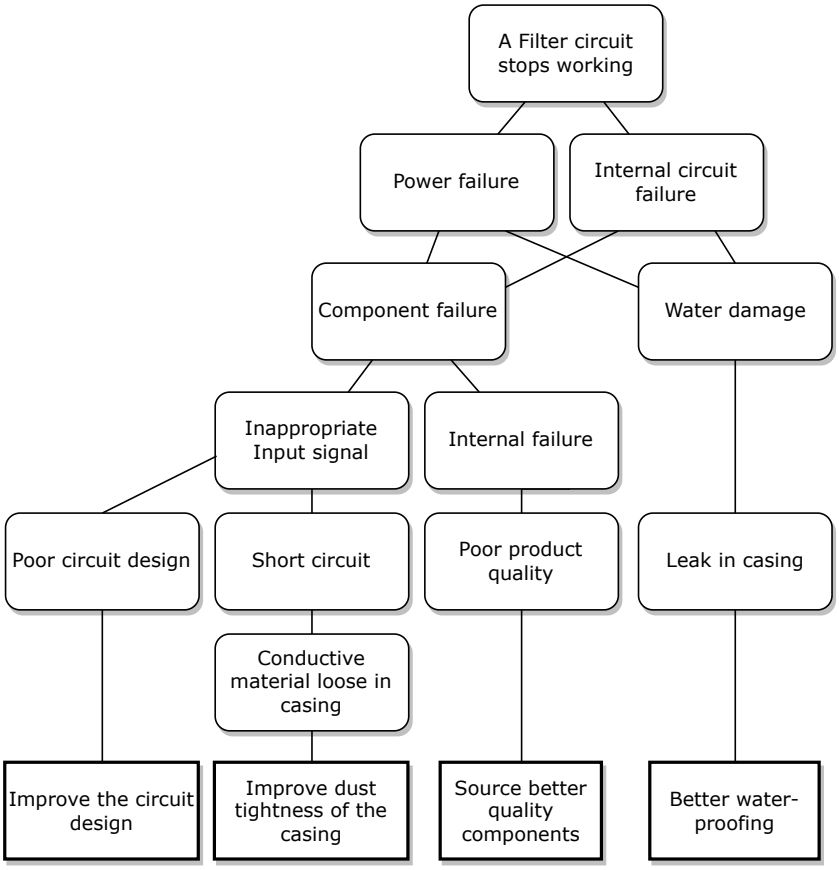


Figure 7.1: Potential FMEA of the filtering circuits

Reliability in terms of cost Although a more materialistic approach, minimizing the cost of a product over the whole lifetime instead of the physical cost is a great way to improve reliability. This is the case because more reliable products have a higher value. In the product described in this report; a higher quality voltage regulator (i.e. more reliable) might increase the cost of the product, but in the long term, loss of a customer due to a failing product would be a greater cost. Therefore, care should be taken when selecting components. They should be chosen such that the physical cost of components is considered less and instead effort is put on minimizing the total expenses due to the chosen component.

Design for durability In [35], two methods are described for designing for durability: Stress/Fatigue testing and safety margins. As there are no moving parts in the prototypes, stress and fatigue testing are not valuable for this project. However, safety margins can be considered for each component on the PCB including the PCB itself. In this project component ratings were chosen such that the applied voltage/current and dissipated power did not exceed them. However, to design for durability, component ratings should be at least twice what is required, such that there is a safety margin of >100%.

Design for prognostics In case the methods above can not prevent a failure, a useful feature is to inform the user that the device is about to fail. In a future version of the product in this report, Power On Startup Tests (POSTs) and periodic Built-In Self Tests (BISTs) should be implemented. A Power On Startup Test could consist of applying voltages (e.h. impulse response) at the input of the filters and checking if the response is as expected. As the electrode cables catch EM noise, periodically, the noise could be measured to identify if the cables are behaving properly.

Following these guidelines, the product is not merely functional, but a medical grade product worthy of monitoring peoples health in life and death situations.

7.2. Accuracy of the designed circuits

7.2.1. Amplification

The amplification was chosen such that a 10mVpp input signal would be amplified to 10Vpp. Therefore components were chosen such that a gain of 1000x was achieved. Meanwhile, the 738x amplification mentioned in the results is has a clear deviation from the theoretical amplification of 989x. The cause of this is unclear. Guidelines mentioned in the datasheet [16] were followed. The only difference is that a 0.1uF bypass capacitor was installed between +5V and -5V, while the datasheet suggests that 2 bypass capacitors should be installed. One between -5V and 0V, one between 0V and 5V. However, that this is the cause for a 25% discrepancy is unlikely. The installation of trimming resistors would have allowed easy modifications such that a perfect 1000x amplification could be achieved.

7.2.2. Filtering

Low-pass filter

Measuring the magnitude response of the low-pass filter posed several problems. The first of which is that measurements done using the oscilloscope (by plotting points) become less accurate as magnitude decreases. The sine amplitude measured is barely distinguishable from the noise caught by the oscilloscope leads (which was confirmed by disconnecting the probe and measuring the noise on the oscilloscope). This makes this type of oscilloscope not suitable for measuring such a response. Because of this, a network analyzer was used, which is accurate at high frequencies and low magnitudes. The only downside is that it is not a spectrum analyzer. This causes the magnitude to be much lower than would be expected, approximately 30dB lower. This is due to the fact that the network analyzer expects a network to move with the chirp source. Because this is not the case in our circuit, power is dispersed over the whole span of the window, resulting in much lower magnitudes at specific frequency points. Using a combination of these tools, as shown in Figure 6.3, an expected slope of around 60dB/decade was achieved. The slight deviation could be due to measurement error. More points would have resulted in a more accurate estimation.

The -3dB point is accurate at 270Hz as shown in Figure 6.1b.

High-pass filter

Measuring the magnitude response of the low-pass filter was even more difficult because neither of the tools were able to measure accurately the magnitude of frequencies at mHz range, as can be seen in Figure 6.4. Furthermore, each test of span and range had an acquisition time of up to 5min. Although Figure 6.5 shows a beautiful roll-off curve, the extrapolated slope results in a roll-off of 45dB, which is theoretically impossible, as there are 3 capacitors in the filtering circuit, each contributing 20dB.

The -3dB point is accurate, being at approximately 50mHz. Deviations here are probably caused by component tolerance (The capacitors used have a tolerance of 10%).

7.2.3. Offset circuit

In the results can be seen that the output voltage of the offset circuit can exceed 3.3V, up to 5V. This is due to a design error. As the STM32 Nucleo development board contains input protection against higher voltage, it can not cause harm. However, due to this error, peaks above 3.3V (After main amplification stage) will be clipped to 1.66V. This should have been designed to convert peaks of up to 5V to an amplitude of up to 1.66V. In a future prototype, the offset resistor should be equal in value and not greater than $50k\Omega$ (to charge the ADCs sample-and-hold capacitor quick enough), and pull-up the signal to 3.3V instead of 5.

While the peaks have an error when converted, the 0V signal point is exactly offset by 1.67V, as expected.

8

Conclusion and Recommendations

8.1. Conclusion

This thesis described the design process of a prototype which is able to amplify, filter, digitize, receive, reconstruct and attenuate the signal. Additionally, the design of the power infrastructure, ESP32/Nucleo overhead and PCB layout where thoroughly discussed in line with the PoR.

In total two prototypes which were able to measure and reconstruct heart signals have been delivered in the given timespan: the transmitter and receiver. (**G1H**, **G10H.a-d**) The device processes 9 signals (**G2H**) by measuring it with a high CMRR instrumentation amplifier and employing filters. The HPF filter was measured to have a cornerfrequency of 50mHz, which ensures baseline wandering and DC components are removed (**G6H.c**). The LPF filter has a corner frequency of 270 Hz, which is higher than the required 250Hz. (**G6H.d**) However, the attenuation is -60dB/dec which results in quick attenuation. There were no visual differences seen (by the group members) between reference ECG and filtered ECG signals, implying that the signal is distortion free (**G6**).

The filters were designed to add very low amounts of group delay within the operating frequencies (**G6H.b**) and the added noise was calculated to be 1.572 and 15.74 μV RMS of the receiver and transmitter respectively. Both below the quantization noise floor of 50.35 μV. (**G6H.a**,**G6D.ab**)

The offset circuit and attenuation circuit were designed to place the ECG signal voltage within the operating range of the ADCs and heart monitor input. (**GD.a**). The total current draw amounted to 485mA, so four 9V 550mAh batteries were added to ensure completion of (**G7**)

The prototypes weight amounted to be approximately 300g (with batteries) with dimensions of 133mm x 70mm x 30mm, satisfying (**G8**) and (**G9**). The total price of the prototypes amounted to €372.4 (**G11**) as commonly used components were used. (**G11H**).

8.2. Recommendations

Due to time limitations only one iteration of the prototype design was possible. This meant that for further iterations of the prototypes improvements could be made. As the PCB/Prototype (design process) improvements have already been listed in section 5.5 and section 7.1 this section will discuss how the results could be verified in a better way.

Program of Requirement point (G6)
As the correctness of the waveforms has only been checked by (untrained) group members, claiming that there was no signal distortion can not be said with full confidence. To ensure that the waveform outputted by the system is correct medical personnel should evaluate the results. The group proposes that, for further validation, a query should be done to validate the correctness of the results.

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A

Figures

A.1. Noise spectra of Transmitter and Receiver

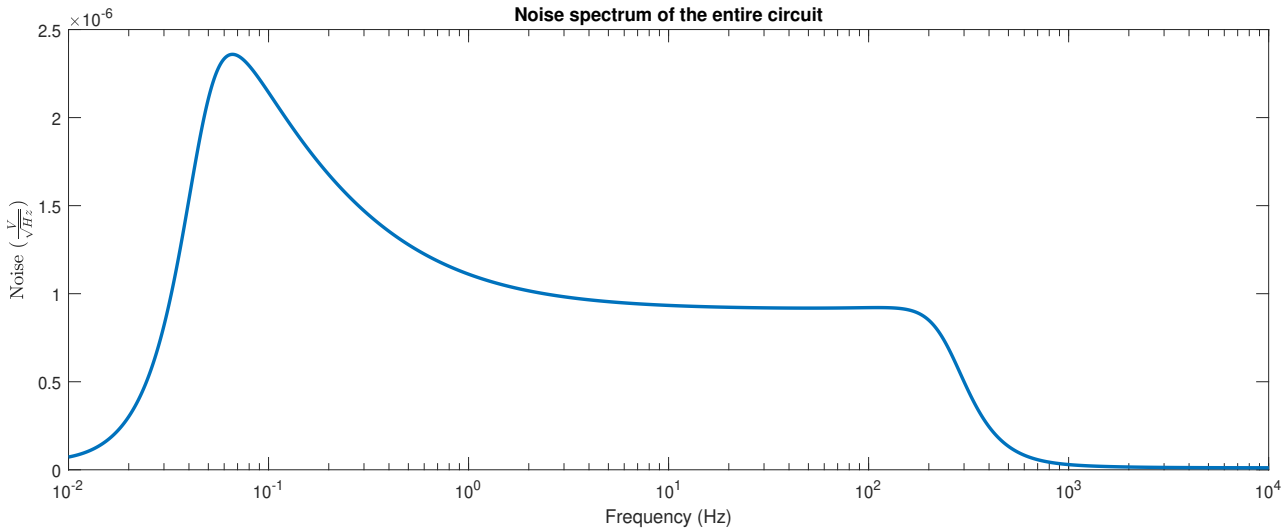

Figure A.1: Noise spectrum of the entire transmitter circuit

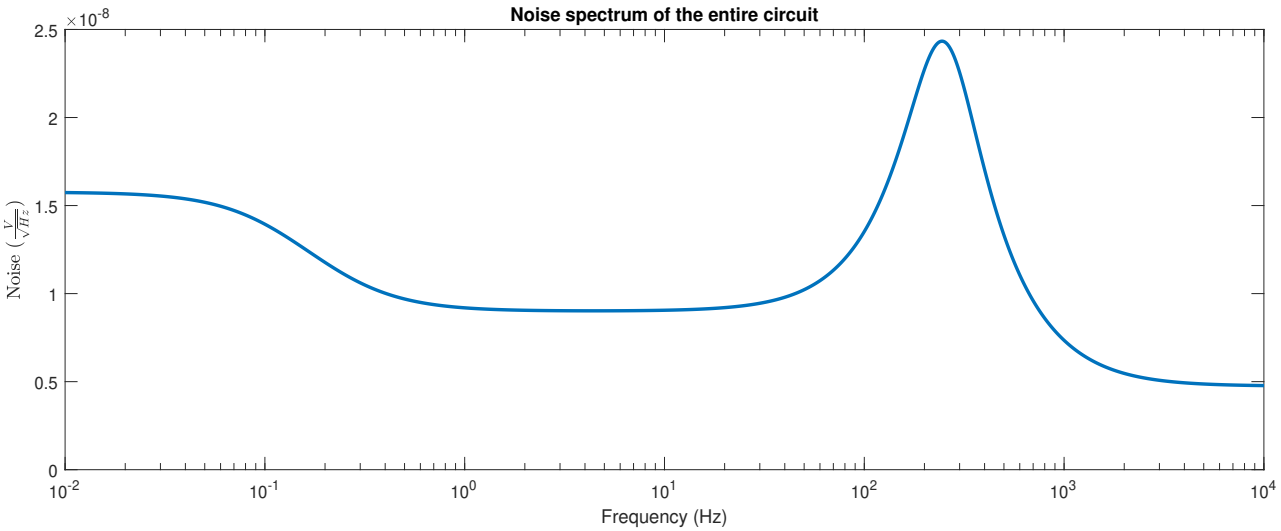

Figure A.2: The noise spectrum of the entire receiver circuit

B

Parts and Schematics

B.1. Transmitter

Part	Value	Part	Value
BOOT	6X3X2.5SWITCHA2	IC13	INA821
BZZZ	F/QMBIII	IC14	TL072D
E0	TPPAD1-13	IC15	INA821
E1	TPPAD1-13	IC16	XC6902N501PR-G
E2	TPPAD1-13	LED1	
E3	TPPAD1-13	LED2	
E4	TPPAD1-13	PROG	
E5	TPPAD1-13	RESET	6X3X2.5SWITCHA2
E6	TPPAD1-13	SV1	
E7	TPPAD1-13	SV2	
E8	TPPAD1-13	SV3	
E9	TPPAD1-13	SV4	
G1	AB9V	SV6	
G2	AB9V	T1	
IC1	TL074D	TP2	TPPAD1-13
IC2	INA821	TP4	TPPAD1-13
IC3	NCP1117TRS	TP6	TPPAD1-13
IC4	TL074D	TP8	TPPAD1-13
IC5	INA821	TP10	TPPAD1-13
IC6	INA821	TP12	TPPAD1-13
IC7	INA821	TP14	TPPAD1-13
IC8	TL074D	TP16	TPPAD1-13
IC9	INA821	TP18	TPPAD1-13
IC10	INA821	TP20	TPPAD1-13
IC11	TL074D	U$2	ESP32-WROOM
IC12	INA821	X1	TSW-101-07-G-D

Table B.1: Transmitter components

Part	Value	Part	Value
R1	9.1k	R47	
R2	160k	R48	
R3	22k	R49	
R4	9.1k	R50	
R5	91k	R51	
R6	27k	R52	
R7	500k	R53	500k
R8	1M	R54	1M
R9	232	R55	
R10		R56	
R11		R57	
R12		R58	
R13		R59	
R14		R60	
R15		R61	
R16		R62	500k
R17	500k	R63	1M
R18	1M	R64	
R19		R65	
R20		R66	
R21		R67	
R22		R68	
R23		R69	
R24		R70	
R25		R71	500k
R26	500k	R72	1M
R27	1M	R73	
R28		R74	
R29		R75	
R30		R76	
R31		R77	
R32		R78	
R33		R79	
R34		R80	500k
R35	500k	R81	1M
R36	1M	R82	10k
R37		R83	1k
R38		R84	4.7k
R39		R85	4.7k
R40		R86	1k
R41		R87	1k
R42		R88	1k
R43		R89	1k
R44	500k	R90	4.7k
R45	1M	R91	4.7k
R46			

Part	Value	Part	Value
C1	100u	C47	
C2	100u	C48	
C3	100u	C49	100n
C4	68n	C50	
C5	4.7n	C51	
C6	33n	C52	
C7		C53	100n
C8		C54	
C9	100n	C55	
C10	10u	C56	
C11	10u	C57	
C12	1u	C58	
C13	1u	C59	
C14	100n	C60	100n
C15		C61	
C16	100n	C62	
C17		C63	
C18		C64	100n
C19		C65	
C20		C66	
C21		C67	
C22		C68	100n
C23	100n	C69	
C24		C70	
C25		C71	
C26		C72	1u
C27			
C28			
C29			
C30	100n		
C31			
C32			
C33			
C34	100n		
C35			
C36			
C37			
C38	100n		
C39			
C40			
C41			
C42			
C43			
C44			
C45	100n		
C46			

Table B.2: Transmitter components: Resistors and Capacitors

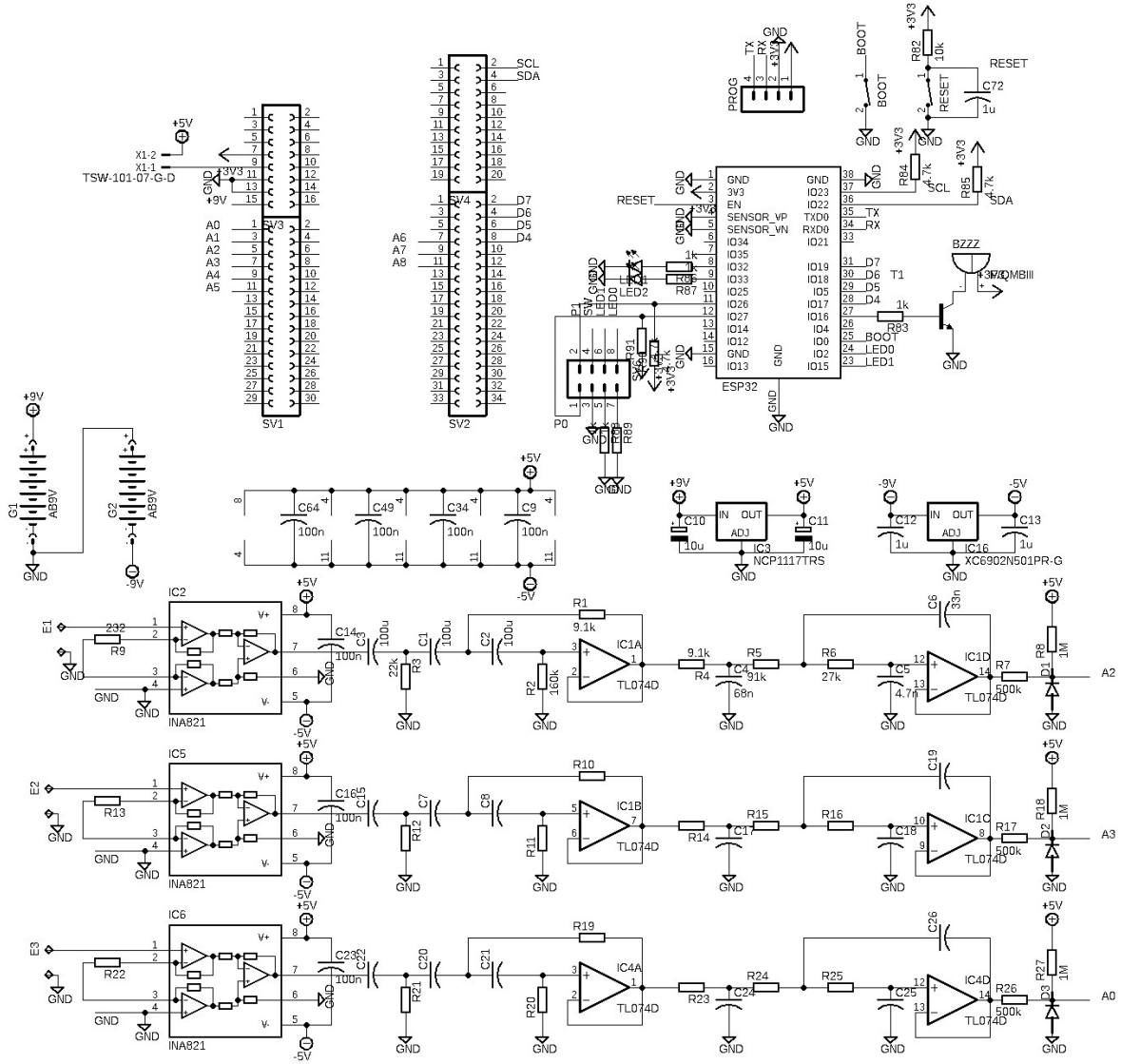

Figure B.1: Schematic of the transmitter prototype: Sheet 1

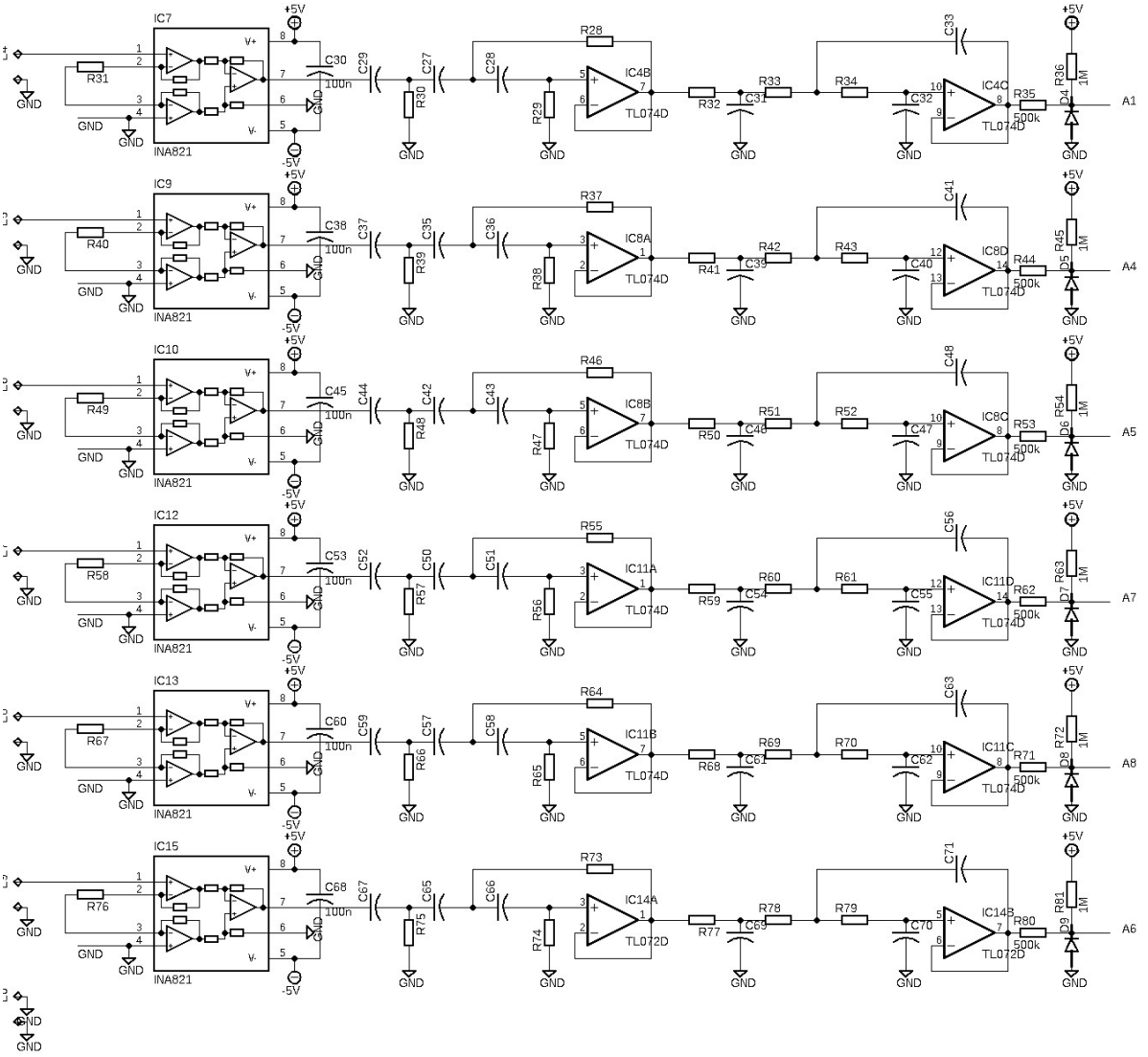

Figure B.2: Schematic of the transmitter prototype: Sheet 2

B.2. Receiver

Part	Value	Part	Value
R1		R47	
R2		R48	
R3		R49	
R4		R50	
R5		R51	
R6		R52	
R7		R53	
R8		R54	
R9		R82	10k
R10		R83	1k
R11		R84	4.7k
R12		R85	4.7k
R13		R86	1k
R14		R87	1k
R15		R88	1k
R16		R89	1k
R17		R90	4.7k
R18		R91	4.7k
R19		C1	
R20		C2	
R21		C3	
R22		C4	
R23		C5	
R24		C6	
R25		C7	
R26		C8	
R27		C9	
R28		C10	10u
R29		C11	10u
R30		C12	1u
R31		C13	1u
R32		C14	100n
R33		C15	
R34		C16	
R35		C17	
R36		C18	
R37		C19	
R38		C20	
R39		C21	
R40		C22	
R41		C23	
R42		C24	
R43		C25	
R44		C26	
R45		C27	
R46		C28	

Part	Value	Part	Value
C29		T1	NPN Transistror
C30		U$2	ESP32-WROOM
C31		U$5	TRIMMER
C32		U$6	TRIMMER
C33		U$7	TRIMMER
C34		U$8	TRIMMER
C35		U$9	TRIMMER
C36		U$10	TRIMMER
C37		U$11	TRIMMER
C38		U$12	TRIMMER
C39		U$13	TRIMMER
C40		X1	TSW-101-07-G-D
C41		X2	Screw Header
C42	100n	X3	Screw Header
C43	100n	X4	Screw Header
C44	100n	X5	Screw Header
C45		X6	Screw Header
C46	100n	X7	Screw Header
C47		X8	Screw Header
C48	100n	X9	Screw Header
C72	1u	X10	Screw Header
CH0	Testpoint	X11	Screw Header
CH1	Testpoint		
CH2	Testpoint		
CH3	Testpoint		
CH4	Testpoint		
CH5	Testpoint		
CH6	Testpoint		
CH7	Testpoint		
CH8	Testpoint		
DAC0	DAC8574		
DAC1	DAC8574		
DAC2	DAC8574		
G1	9-V BATTERY CLIP		
G2	9-V BATTERY CLIP		
GND	Testpoint		
IC1	TL074D		
IC2	TL074D		
IC3	NCP1117TRS		
IC4	TL074D		
RESET	SMD Switch		
SV1	FEMALE HEADER		
SV2	FEMALE HEADER		
SV3	FEMALE HEADER		
SV4	FEMALE HEADER		
SV6	FEMALE HEADER		

Table B.3: Receiver components

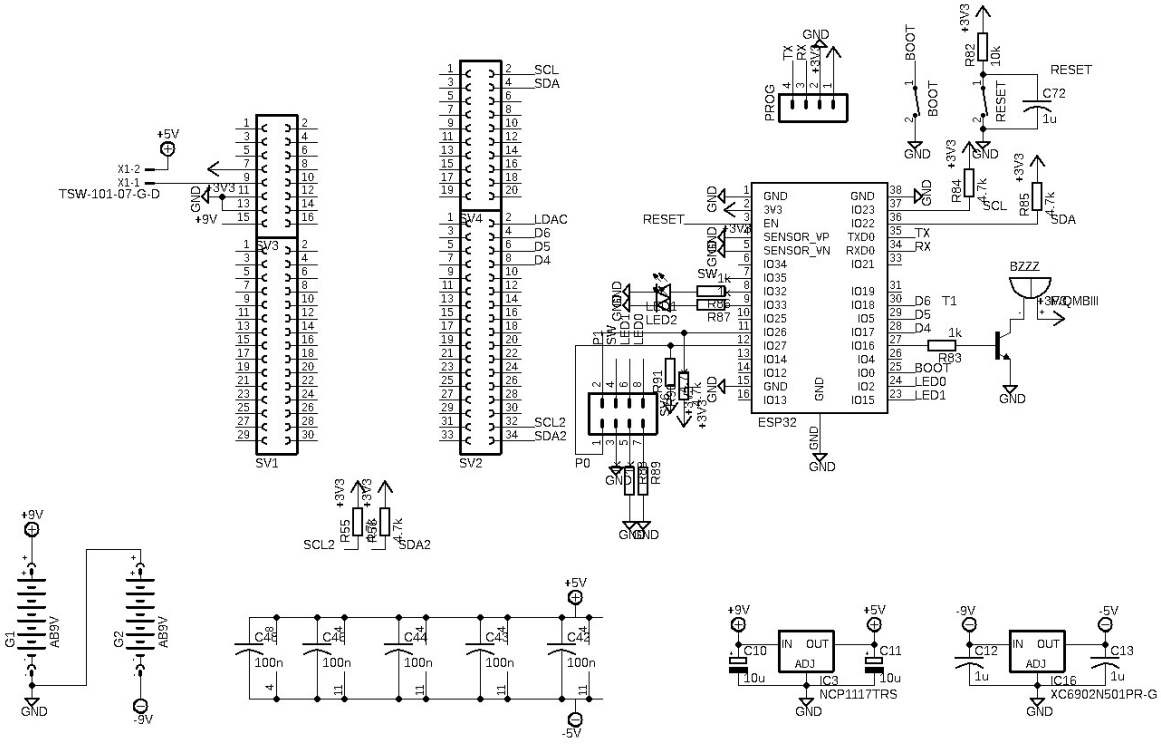

Figure B.3: Schematic of the receiver prototype: Sheet 1

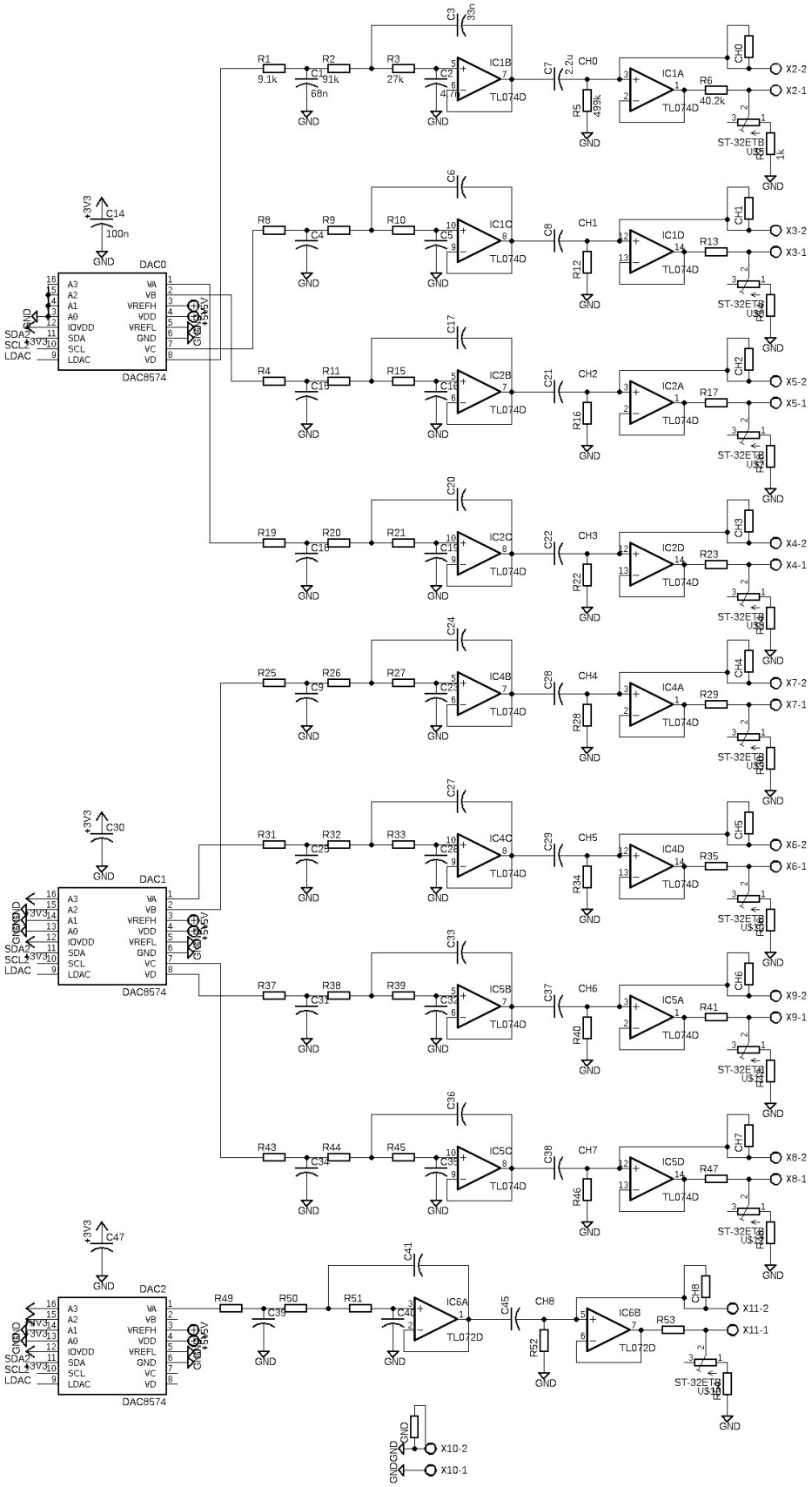

Figure B.4: Schematic of the receiver prototype: Sheet 2