A NEW INPUT-PARALLEL-OUTPUT-SERIES THREE-PHASE HYBRID RECTIFIER FOR HEAVY-DUTY ELECTRIC VEHICLE CHARGERS

by

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ABSTRACT

The range anxiety and relatively long charging time issues of electric vehicles (EVs) have boosted the development of fast charging technology. With charging light EVs being the main focus in the past decade, a trend of promoting the charging infrastructures dedicated to heavy-duty EVs (HDEVs) such as E-trucks, and E-buses has emerged to further the electrification of global transportation. Accordingly, the market is calling for advantageous architectures and circuit topologies specialized in the fast charging of HDEVs. For the charging of HDEVs, the power rating of chargers can reach an ultra-high power level (>1 MW) to ensure a charging time comparable to the refueling time of internal combustion engine (ICE) vehicles. At this power rating, the conventional full power processing (FPP) AC-DC plus DC-DC two-stage architecture has limited space for improvement in terms of the efficiency and effective cost of the charger circuits.

This thesis proposes a solution to the HDEV fast charger topologies. Firstly, the state-of-the-art EV fast charging technology, concepts of the hybrid rectifier, and partial power processing (PPP), which could be beneficial in advancing the charging architecture are reviewed. A new unidirectional Input-Parallel-Output-Series (IPOS) three-phase hybrid rectifier topology is proposed and analyzed. The IPOS topology is advantageous at ultra-high power rating to interface the next-generation heavy-duty EV batteries which require a high and wide output voltage range of 800~1500 V with available 600/1200V commercial semiconductors. Besides, the proposed topology is efficient, cost-effective, and scalable with the grid input current harmonic components in compliance with the IEEE-519 standard. The benefits of the IPOS topology are supported by circuit derivation, control strategy, analytical modelling, simulation, and experimental verification.

***Index terms*—** fast charging, hybrid rectifier, partial power processing, power factor correction, AC–DC converter

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INTRODUCTION

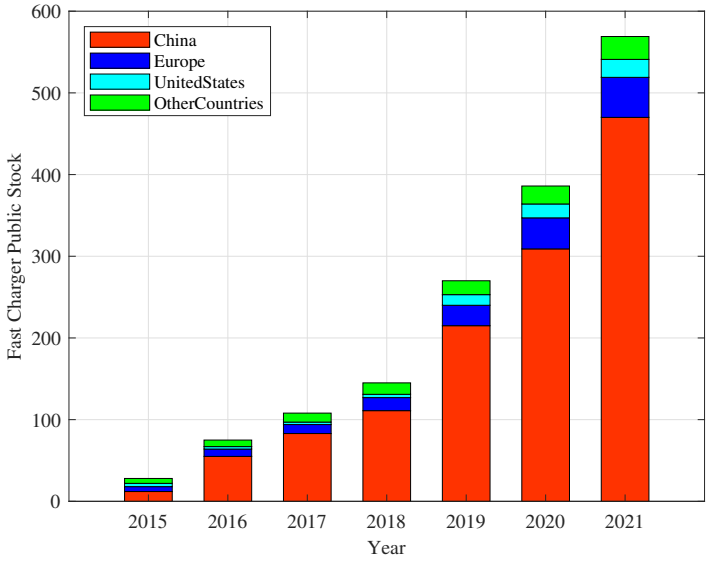

Figure 1.1: Fast publicly available chargers 2015-2021 [1]

1.1. BACKGROUND AND MOTIVATION

1.1.1. BACKGROUND

The Electrification of transport is making tremendous progress as a powerful solution to the global warming issue. With the continuing decline in the average price of EV batteries and the increase in the charging infrastructures, the EV market thrives with nearly 10% of global car sales being electric in 2021, four times the market share in 2019 [1]. As the price of EV batteries continues to decline to $110/kWh (one-tenth of that in 2010), and the average capacity continues to increase, the relatively high cost and the range anxiety issues of EVs have been mitigated.

At present, the relatively long charging time and the insufficiency of charging infrastructures have become the main obstacles to the electrifying transport, which stimulates a significant market growth in the EV fast charging technology (cf. [Fig. 1.1]).

In the past decade, the priority has been placed on the electrification and related technology of light-duty electric vehicles (LDEVs). Heavy-duty electric vehicles (HDEVs) such as electric trucks accounted for only 0.3% of global truck sales in 2021, which needs to reach around 10% by 2030 according to the IEA Announced

Pledges Scenario (APS) [1]. A trend of electrifying heavy-duty vehicles and developing ultra-fast chargers has emerged for the next phase of the global electrifying transport. Because of the increasing market demand, various research projects were initiated and are going well underway. In 2018, CharIN initiated the "Megawatt Charging System" (MCS) project to investigate the possible solutions and standards for charging E-trucks and E-buses [6]. In 2020, CHAdeMO has released the ultra-high-power protocol "CHAdeMO 3.0 ChaoJi", enabling a charging power rating up to 900 kW [7]. In the application of charging batteries of HDEVs, the power rating of the chargers can reach an ultra-high level (>1 MW) to ensure the charging time is comparable to the refuelling time of an internal combustion engine (ICE) vehicle. It is evident that the charging power rating will continue to increase in the near future, welcoming more up-to-date protocols, charging architectures, and suitable power electronic circuits.

1.1.2. MOTIVATION

This thesis is dedicated to proposing a highly efficient and cost-effective power electronic circuit topology applying the concepts of the hybrid rectifier and partial power processing which can be benefiting in the applications of ultra-high-power EV chargers.

Much research effort has been spent on improving the efficiency, power density, and the effective cost of the power conversion stages of fast chargers. The Full Power Processing (FPP) AC-DC plus DC-DC two-stage conversion has become a standardized solution to the charger topology (cf. [Fig. 1.2]). The AC-DC stage regulates the AC current to a close-to-sinusoidal current waveform with a unity power factor and supplies a DC power to the controlled DC bus. The cascaded DC-DC stage delivers a regulated output voltage to interface the battery. In the application of fast chargers (> 50 kW) interfacing the next-generation HDEV batteries, the average output voltage of the two-stage FPP topology can exceed 1200 V to reduce the average output current, and thus the size of the charging cable. Consequently, certain semiconductor components with higher reverse blocking voltage ratings, e.g. 1700 V, and current ratings of hundreds of Amperes in the circuits are required. The 1700 V semiconductors are typically more expensive and less available than 1200 V semiconductors, imposing constraints on the design space. Furthermore, passive components with a full power rating in both stages are required in the FPP topology, which further limits the efficiency, effective cost, and power density of the conversion stage.

Concepts of partial power processing and hybrid rectifier are appealing in addressing the above-mentioned issues. Converters that process only a fraction of

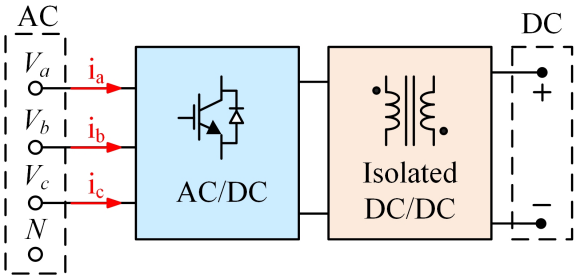

Figure 1.2: Classic two-stage EV charger circuit topology

the total power with the rest of the power processed by a close-to-unity efficient secondary path, are addressed as Partial Power Processing (PPP) converters. Accordingly, the PPP contributes to higher overall system efficiency and power density compared to a Full Power Processing (FPP) converter [4]. The hybrid rectifier is a parallel/serial connection of two or more rectifier stages. Hybrid rectifiers innately incorporate the PPP characteristic by processing the majority of the active power through a more efficient line-commuted rectifier, and the minority of active power through a less efficient self-commuted Pulse-Width Modulation (PWM) rectifier which is able to compensate for the reactive power, offering a higher system efficiency.

1.2. RESEARCH OBJECTIVES

The research objectives of this thesis are listed as follows.

- Review the state-of-the-art status of DC-type fast charger technology and beneficial concepts such as partial power processing and hybrid rectifier;
- Propose an advantageous power electronic topology which is suitable for ultra-high-power HDEV chargers;
- Benchmark and simulate the proposed topology;
- Experimentally verify the EV charger topology concept.

The contribution of this thesis is the proposal of a new Input-Parallel-Output-Series (IPOS) three-phase hybrid rectifier topology in Chpt. 3. The serial connection of the DC-links enables the hybrid rectifier system to deliver a wide total output voltage range of 800~1500 V. It is worth noting that semiconductors with

higher voltage rating, e.g. 1700 V, can be avoided in the proposed topology because of the serial connection, bringing more design choices and a lower cost on semiconductors. Employing the concepts of partial power processing and hybrid rectifier, the proposed topology is highly efficient, cost-effective, and able to deliver an ultra-high power with a wide output voltage range in compliance with the IEEE-519 standards, which is supported by analytical modelling.

The thesis outline is as follows. The background, motivation, and the research objectives of this thesis are introduced in Chapter 1. The literature reviews on the EV fast charging technology, partial power processing (PPP), and hybrid rectifier are presented in Chapter 2. The derivation of the proposed input-parallel-output-series (IPOS) hybrid rectifier topology and the topology selection, accompanied by theoretical analysis, the control strategy, the current modulation technique, and the design of converter parameters are introduced in Chapter 3. The simulation and analytical modelling results that demonstrate the system efficiencies under various load conditions are presented in Chapter 4. The experimental verification of the current modulation technique applied in the IPOS topology is presented in Chapter 5. The prime of this paper and the future work are concluded in Chapter 6.

2

LITERATURE REVIEW

2.1. INTRODUCTION

With the aim of deriving an advantageous topology for DC-type fast EV chargers, it is essential to study the requirements and specifications of the state-of-the-art DC-type chargers. With the knowledge of related standards, the research can then be further developed with more advanced concepts such as partial power processing and hybrid rectifier, which are potential in improving the efficiency, power density, and effective cost of the power conversion stage. It is also important to obtain an explicit understanding of their mechanisms through a systematic literature review.

A literature review is carried out to summarize the basic and prime knowledge of the concepts mentioned above, focusing on the topology-level analysis. This chapter is divided into three sections, where the fast charging technology, partial power processing, and hybrid rectifier are studied. A new IPOS hybrid rectifier topology concept suitable for ultra-high-power chargers is proposed in light of the knowledge acquired.

2.2. EV FAST CHARGING TECHNOLOGY

The rapid growth of the electric vehicle market has stimulated the development of the DC-type fast charging technology and its infrastructures. To address the range anxiety and long charging time issues, the capacity of the EV batteries is increased. The power rating of EV chargers also rises to ensure a comparable charging time. Because of the weight/volume restrictions on the EVs, fast chargers with high power ratings (> 50 kW) are hence located outside the vehicles, named the off-board charger. The number of publications related to fast and ultra-fast charging technology, and related applications have seen an average annual growth rate of approximately 25% in the past decade [1, 7].

With an abundance of research on chargers for light EVs, researchers are gradually placing more attention on the electrification of heavy-duty vehicles such as buses, trucks, and ships and their charging infrastructures [6]. The capacity of heavy-duty EV batteries is 300-800 kWh, which would require chargers with an ultra-high-power (> 1 MW) rating for a reasonable charging time. These ultra-fast chargers need to supply large currents (typically hundreds of Amperes), which generates considerable losses and heat. Consequently, charging cables with increased size and complexity to handle the heat dissipation is required. To deliver the same amount of power, the output voltage of the fast chargers is typically high (800-1200 V). At present, the typically rated voltages of the LDEV battery packs are around 350-400 V and those of the HDEV batteries are 800 V.

The rated voltage and capacity of the EV batteries will continue to increase in the future. Optimizations and new charger architectures able to safely and efficiently deliver high output voltage and power to various load conditions are of great research interest.

This section reviews the fast charging technology for both light and heavy-duty EVs. Firstly the definitions, protocols, and standards of EV fast chargers are introduced. Then typical charger architectures and topologies are analyzed. Finally, present issues and associated requirements on the fast charger topologies are discussed.

2.2.1. STANDARDS OF FAST CHARGING

The EV fast charger denotes the off-board DC-type charger which delivers a DC current (up to 600 A), a DC-link voltage (up to 1.5 kV), and thus high peak power (> 50 kW) to the EV battery under the control of the battery management system (BMS) [7]. Because of the high power rating and isolation requirements, fast chargers are typically bulky and located outside the vehicle, compared to the on-board AC level 1 (1.9 kW) and level 2 (19.2 kW) chargers. The unit of the power rating of the chargers is kilowatt as the unit of the battery capacity expressed in kilowatt-hours. The E-rate denotes the rate of power able to fully charge the battery in one hour. For fast and ultra-fast chargers, the E-rates can achieve (6-10 E), which can fully charge the EV battery within 10 minutes. Fast charging is typically applied to charge the state-of-charge (SoC) of the battery to 80% of its nominal capacity and then switched to normal/slow charging with a lower power rating to charge the rest of the SoC. This is to avoid the overcharging and rapid degradation of the battery life caused by high charging rates, i.e., 6-10 E. Standards on off-board DC-type fast chargers are shown in Table. 2.1.

Table 2.1: Fast charger types [3]

Charger Type	CCS Type1	CCS Type2	CHAdeMO	GB/T	ChaoJi	Tesla
Issued Year	2014	2013	2009	2013	2020	2012
V_{max} (V)	600	900	1000	750	1500	500
I_{max} (A)	400	400	400	250	600	631
P_{max} (kW)	200	350	400	185	900	250
Communication	PLC	PLC	CAN	CAN	CAN	CAN
V2G	No	NO	Yes	NO	Yes	NO

Isolation Requirements According to IEC 61851-23 and IEEE 2030.1.1 standards, galvanic isolation is required to prevent failure in the AC grid or the DC-Bus to interfere with one another [7, 8]. The galvanic isolation can be implemented on either the front-end grid side by a lower-frequency transformer ([cf. Fig. 2.1(a)] and/or the back-end DC side by an isolated DC-DC converter ([cf. Fig. 2.1(b)]. Moreover, if a charger has multiple output ports, the output ports shall be isolated from the non-charging side to prevent failure in one port to interfere with the other ports. Therefore, in applications of ultra-high-power DC-type chargers, if the isolation is provided on the AC side, an isolated DC-DC converter is not necessary since typically the fast charger has only one output port considering its power rating.

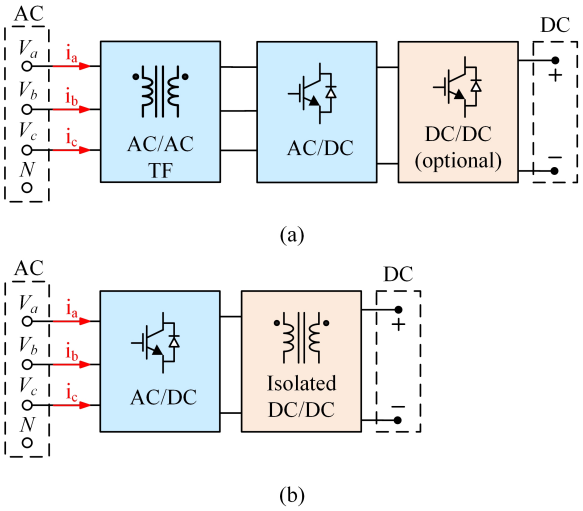

Figure 2.1: Isolation topologies: (a) Isolation on the AC front-end. (b) Isolation on the DC back-end

2.2.2. ARCHITECTURES AND TOPOLOGIES

CHARGING STATION ARCHITECTURES

The distribution network of a charging station including chargers, energy storage systems (ESSs), and renewable energy sources (RESs) is shown in Fig. 2.2 and 2.3. Considering the high power demand of chargers, the charging station is usually connected to a medium voltage (MV) distribution network via a line-frequency MV/LV step-down transformer to avoid overloading the grid. The galvanic isolation between the charger circuits and the grid is also provided by the transformer

in compliance with IEC 61851-23 std [3].

There are two types of distribution networks, i.e., the AC and DC distribution network. The AC distribution network ([cf. Fig. 2.2]) is dominant in industrial applications because of the well-established standards and mature AC-DC/DC-AC converter topologies. On the other hand, the AC network has more power conversion stages than the DC distribution because the ESSs, RESs, and EV batteries have individual DC-AC/AC-DC converters connected to the AC distribution bus, resulting in lower system efficiency and higher complexity [3].

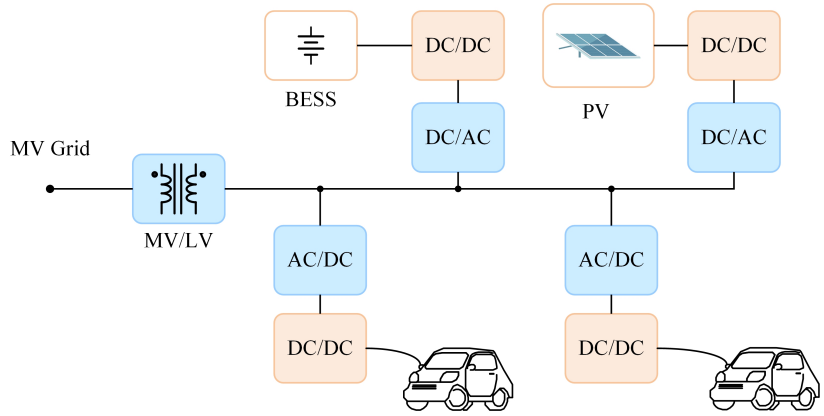

Figure 2.2: AC distribution network

The DC network deploys a central AC-DC converter to create a DC bus, where only a DC-DC stage is required to interface RESs, ESSs, and EV batteries, ensuing in fewer conversion stages and thus higher system efficiency ([cf. Fig. 2.3]). Conversely, the standards, metering, and protection schemes are not well-established [3]. Therefore, it is more complex to deploy bidirectional chargers in the DC network because of the non-standardized protection scheme [9].

The power conversion stage of chargers consists of a front-end AC-DC stage and a back-end DC-DC stage. To increase the total power rating, a method adopted by manufacturers is connecting multiple modules with lower power ratings in parallel, e.g., the Tesla supercharger which is composed of 12 modules [3].

FRONT-END AC-DC CONVERTER TOPOLOGIES

The front-end AC-DC stage is implemented by PWM rectifiers capable of current shaping and DC-link voltage regulation, as shown in Fig. 2.4. The power factor correction (PFC) rectifier plus the passive filter at the grid side allow the rectifier

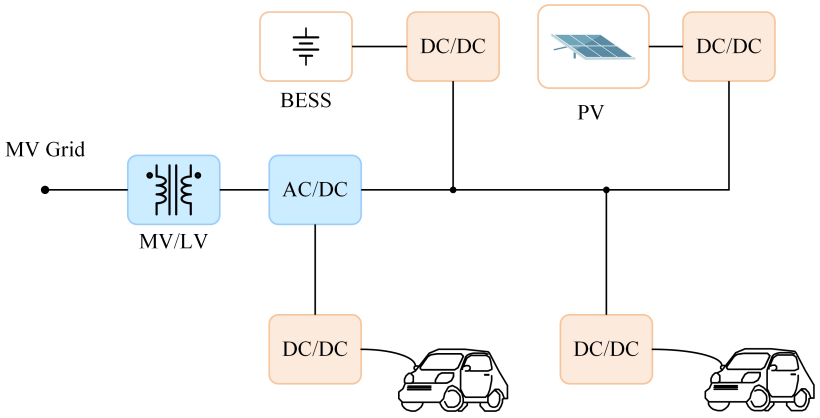

Figure 2.3: DC distribution network

to deliver a close-to-sinusoidal grid input current and a unity power factor. These PFC rectifiers can be classified into Boost-type ($V_{pn} > \sqrt{2}V_{ll,rms}$) or Buck-type ($V_{pn} < \sqrt{\frac{3}{2}}V_{ll,rms}$) rectifiers based on the relationship between the amplitude of line-to-line voltage and DC-link voltages [10]. The Buck-type rectifiers are mostly applied to interface the batteries of LDEVs [11]. Based on the number of voltage levels a rectifier can supply at the grid input side, the rectifiers can be classified into multi-level converters. Here, only Three-Level converters (3LCs) and Two-Level converters (2LCs) are considered. Based on the power flow, these rectifiers can be classified into bidirectional or unidirectional rectifiers.

Table 2.2: Comparison of front-end AC-DC topologies [3]

Converter	Switches/Diodes	V_o Level	Power Flow	PF Range	Control
T-type	6/6	3L	Uni.	Limited	Medium
NPC	12/6	3L	Bi.	Wide	Medium
PWM	6/0	2L	Bi.	Wide	Low
Buck-type	6/6	3L	Uni.	Limited	Low
Delta-switch	6/6	2L	Uni.	Limited	Medium

The comparison of these AC-DC converter topologies is shown in Table. 2.2. It can be concluded that all four topologies are able to achieve a unity power factor and a grid current with low THD_i. 3LCs such as the T-type converter and the three-Level Neutral Point Clamped Converter (NPC) enable certain semiconductors with lower voltage ratings, which leads to lower semiconductor losses and higher system efficiency, and power density compared to the 2LCs for the same specifications [12, 13]. When operated at full/high loads and low switching fre-

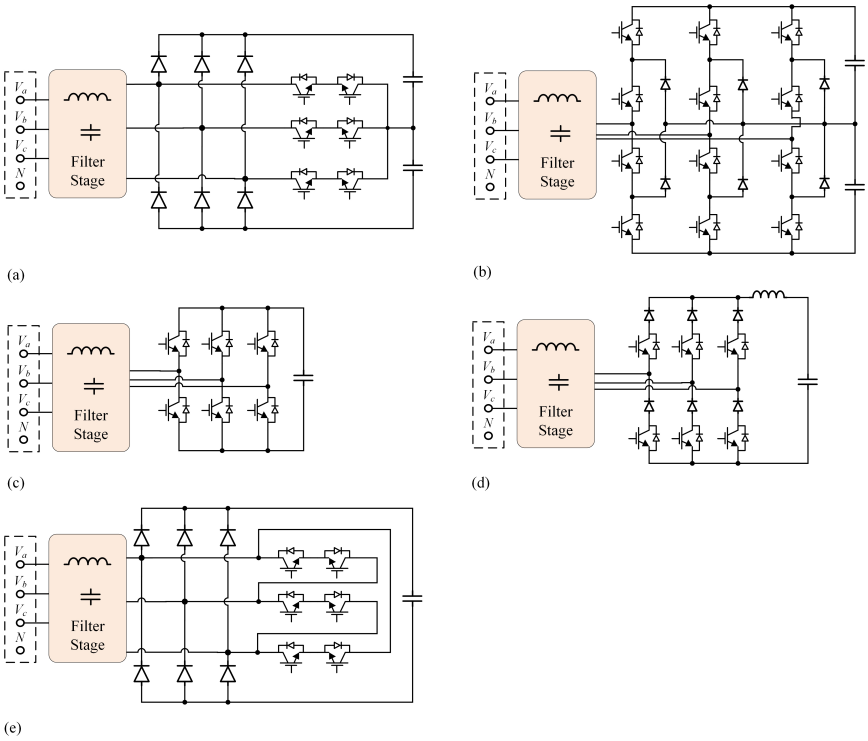

Figure 2.4: AC-DC topologies: (a) Unidirectional T-type rectifier. (b) NPC rectifier. (c) 6-switch PWM rectifier. (d) Buck-type rectifier. (e) Unidirectional Delta-type rectifier

quency (< 12 kHz), the T-type topology has higher efficiency than that of 3LNPC. Whereas, at light loads and high switching frequency (> 12 kHz), the 3LPNC has higher efficiency and power density than the T-type rectifier. For the application of high-power unidirectional HDEV chargers, the T-type rectifier is preferable because the high output voltage requires a Boost-type rectifier with a low switching frequency to ensure low semiconductor losses.

BACK-END DC-DC CONVERTER TOPOLOGIES

The back-end DC-DC stage is implemented by isolated/non-isolated DC-DC converters with regulated DC output voltage to interface the battery. Isolated DC-DC converters can provide galvanic isolation between the battery and the charging system, which is mandatory if the charger has multiple output ports according to IEEE 2030.1.1^{TM} std. As isolated converters add another insurance to the protection of the battery, they are favored by most manufacturers compared to non-isolated converters. The DC-DC converters can be classified into isolated and

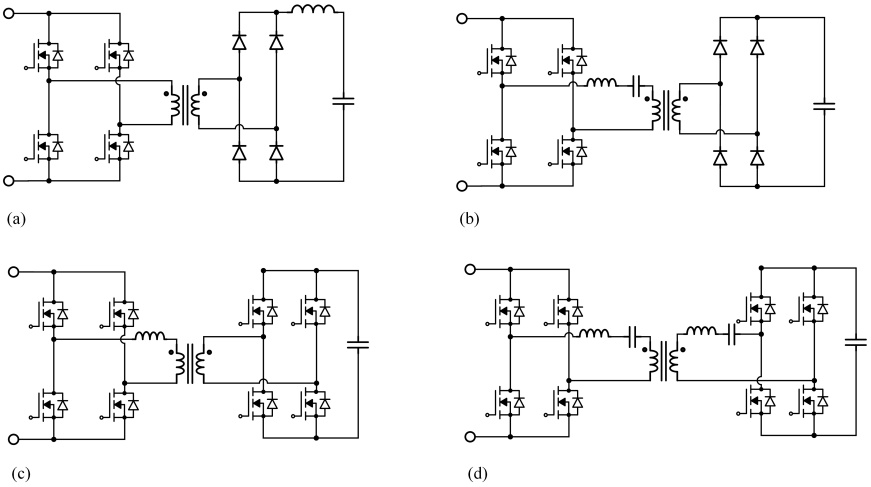

Figure 2.5: Isolated DC-DC topologies: (a) PSFB converter. (b) CLC converter. (c) DAB converter. (d) CLLC converter.

non-isolated converters, which are shown in Fig. 2.5 and 2.6.

Isolated DC-DC Converters The phase-shift full-bridge (PSFB) converter is desirable for its simple control strategy and zero-voltage switching (ZVS) turn-on features [14]. Moreover, the appropriate transformer turns ratio and PWM scheme enables the converter to deliver a wide output voltage range [15]. However, compared to a dual active bridge converter (DAB), the diode bridge on the secondary side leads to higher conduction losses and the resonance between the leakage inductance of the transformer and the parasitic capacitance of the primary side semiconductor switches results in higher turn-off switching losses. Snubber circuits can be deployed to prevent the voltage overshoot and ringing at turn-offs to protect the semiconductor switches, compromising the system efficiency [16].

The LLC resonant converter can also achieve ZVS switching, exhibiting very high peak efficiency when operated around the resonant frequency [3]. The LLC converter is sensitive to the load variations. A premise for the high-efficiency operation is a narrow output voltage range limited by the design of the resonant tank. Considering a wide output range that requires altering the switching frequency, the LLC converter can operate in a region where ZVS is not available and the efficiency is compromised. The LLC converter needs to be equipped with extra hardware and modulation efforts to achieve high-efficiency operation in a wider output voltage range [17].

The DAB converter enables features such as ZVS and a wide output voltage range. Applied with a phase-shifted control similar to the PSFB converter, the DAB converter can achieve high efficiency, power density, and bidirectional power flow. However, the ZVS operation may not hold under light load conditions, resulting in high switching losses. This can be improved by implementing dual-phase shift (DPS) or triple-phase shift (TPS) modulation as introduced in [18]. Compared to a PSFB converter, the conduction losses on the secondary side are lower since the on-resistance of active semiconductor switches is typically smaller than that of the diodes at the same rating [19].

The CLLC converter can be treated as a symmetrical version of the LLC converter, allowing the bidirectional power flow. Similar to an LLC converter, ZVS operation can be applied and the maximum efficiency operating point appears at the resonant frequency. The converter's efficiency is compromised at a wide voltage gain range and load conditions where the ZVS operation is not feasible. Compared to an LLC converter, the resonant capacitors are downsized because they are implemented on both sides of the transformer. Compared to the DAB converter, the leakage inductance required for the resonance is smaller. Main semiconductor losses are the conduction losses because of the high RMS current through the switches [20]. The comparison between the CLLC converter and the DAB has been carried out in [18, 20] with opposing conclusions. In fact, both converters can be designed to achieve high peak efficiency and power density. The topology selection is more dependent on the voltage gain and power range.

Non-Isolated DC-DC Converters The non-isolated DC-DC converters can be implemented if the galvanic isolation is provided at the front-end AC side with a line-frequency transformer. Commonly used non-isolated DC-DC topologies are shown in Fig. 2.6. These topologies are derivations of the Boost converter which are simple to control, featuring bidirectional power flow and reduction of current ripple. To reduce the current stress on the semiconductors and the size of the magnetic components, a modification to interleave the boost converter can be applied with more control and hardware efforts. The three-level boost converter can also be applied to reduce the output current ripple and voltage stress on the semiconductor components ([cf. Fig. 2.6(b)]). However, phase synchronization or an integrated inductor is required to eliminate the circulating current when the converter is interleaved [3].

The comparison of DC-DC converters is listed in Table. 2.3. The application scenario of fast chargers is to charge a vehicle in a short period of time instead of drawing energy from the battery. And the protocols and economical mode of the

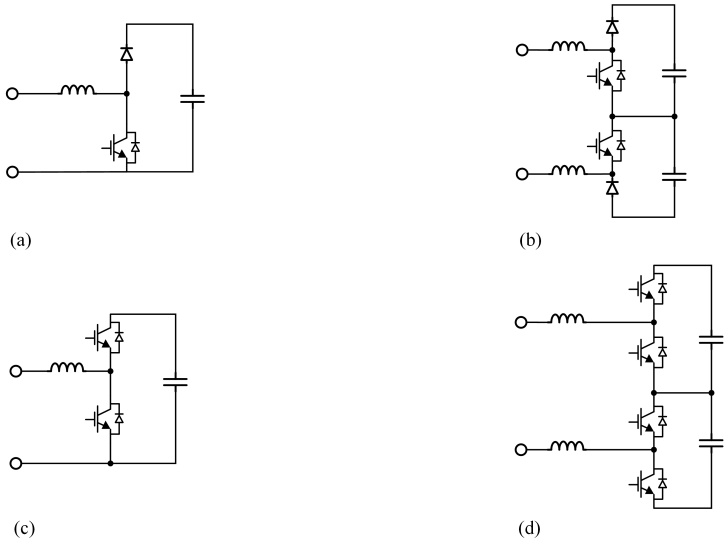

Figure 2.6: Non-isolated DC-DC topologies: (a) Unidirectional Boost converter. (b) Unidirectional Boost converter (3-level). (c) Bidirectional Boost converter. (d) Unidirectional Boost converter (3-level).

V2G function are not yet mature. Thus, unidirectional power flow is sufficient. The DAB converter can be applied where the trade-off between efficiency and cost is prone to the former. Various load conditions and voltage range issues rule out the LLC converter. It can be concluded that for fast chargers which require high efficiency over a wide output voltage range, the PSFB converter is a preferable option for the DC-DC converter stage.

Table 2.3: Comparison of back-end DC-DC converters

Converter	Switches/Diodes	Isolation	Power flow	V_o range	Control
PSFB	4/4	Yes	Uni.	Wide	Low
LLC	4/4	Yes	Uni.	Limited	Medium
DAB	8/0	Yes	Bi.	Wide	High
CLLC	8/0	Yes	Bi.	Limited	Medium
Boost	2/0(1/1)	No	Bi./Uni.	Limited	Low
3L Boost	4/0(2/2)	No	Bi./Uni.	Limited	Low

2.3. PARTIAL POWER PROCESSING

An intriguing approach to improve the efficiency, power density, and effective cost of the power conversion stages is to apply partial power processing (PPP) converters. PPP converters denote converters that process only a fraction of the total power with the rest of the power processed by a close-to-unity efficient secondary path ([cf. Fig. 2.7]). Accordingly, the PPP configuration leads to higher system efficiency and power density compared to Full Power Processing (FPP) converters [4]. This is because the FPP converters have to be rated for full power rating, imposing constraints on the design space for improvements in the above aspects, especially when a wide voltage gain range is required. The PPP scheme is widely applied in DC-DC converters in applications of battery chargers, BESS, and photovoltaic (PV) systems [2]. For the DC-DC stage in EV charger applications, a PPP PSFB converter is implemented and compared with its FPP version in [21] and a PPP DAB converter is implemented in [22] with the conclusion that both PPP converters can achieve reduced ratings and improved system efficiency.

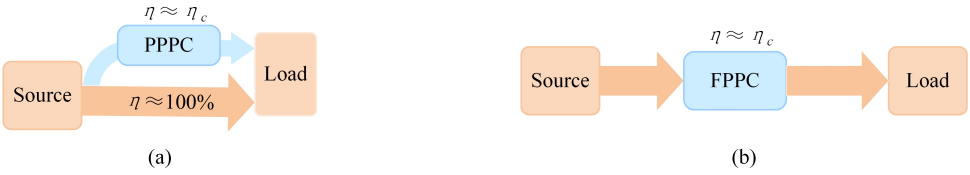

Figure 2.7: PPP power flow: (a) PPP power flow. (b) FPP power flow.

By connecting the source, converter, and the load in an input-parallel-output-series (IPOS) ([cf. Fig. 2.8(a)]) or input-series-output-parallel (ISOP) ([cf. Fig. 2.8(b)]) manner, only a part of the power needs to be processed by the converter [2]. In both configurations, the output of the converter can be rated for only the differential voltage of the source and the load [4], as shown in the following equation,

$$k_p = \frac{P_{PP}}{P_{sys}} = \frac{V_o \cdot I_S}{V_S \cdot I_S} = \frac{V_L - V_S}{V_S} \tag{2.1}$$

where k_p is the partial power sharing ratio of the PPP converter. P_{PP} is the partial power processed by the PPP. P_{sys} is the power processed by the whole system. V_o is the output voltage of the PPP converter. V_S is the voltage of the source. I_S is the current of the source.

On the other hand, the PPP configurations introduce a few drawbacks. Firstly, the PPP configurations can only be applied to isolated converters and non-isolated

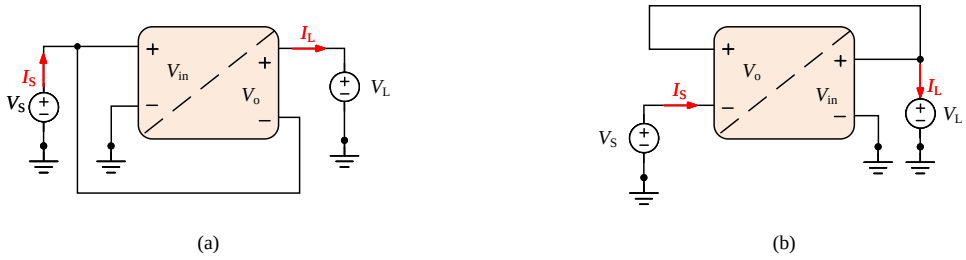

Figure 2.8: PPP configurations: (a) IPOS configuration. (b) ISOP configuration.

DC-DC converters without an internal ground connection, as shown in Fig. 2.9. For example, the Boost converter cannot be configured as a PPP converter because the ground at the input and the output ports are connected, thereby causing a short-circuit at the input source. Secondly, the PPP configurations nullify the galvanic isolation between the source and the load of isolated DC-DC converter topologies [4]. In applications where galvanic isolation is not mandatory, the PPP configurations can then be deployed to achieve higher efficiency, power density, and lower cost compared to the FPP configuration.

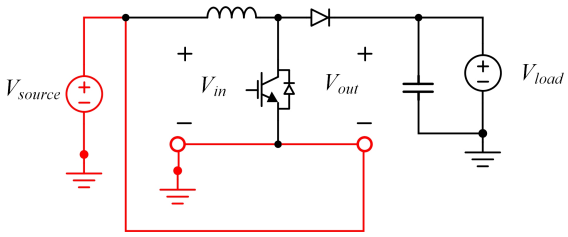

Figure 2.9: PPP Boost (short circuit) [2]

Comparison Between Two PPP Configurations The mathematical relationship between the system efficiency η_{sys}, the partial power processed P_{PP} and the power sharing ratio k_p, PPP converter efficiency η_c under different power flow directions and configurations of PPP are shown in Table. 2.4. The comparison is well elaborated in [4]. The authors in [4] summarized that the ISOP converter, regardless of the power flow direction, can process more power than an FPP converter under certain relationships of the partial power ratio and the converter efficiency, losing the advantages of a PPP converter. Whereas the IPOS converter, regardless of the power flow direction and the relationship between the converter efficiency and the power-sharing ratio, always processes less power than an FPP converter with higher system efficiency. Therefore, the IPOS configuration is the

Table 2.4: Efficiency and partial power processed in conventional PPP configurations [4]

Configuration	η_{sys}	P_{PP}
IPOS source to load	$\frac{\eta_c \cdot (1+k_p)}{\eta_c + k_p}$	$\frac{k_p}{k_p+\eta_c}$
IPOS load to source	$\frac{1+k_p \cdot \eta_c}{1+\eta_p}$	$\frac{k_p}{k_p+1}$
ISOP source to load	$\frac{(1+k_p)\cdot\eta_c - k_p}{\eta_c}$	$\frac{k_p}{\eta_c}$
ISOP load to source	$\frac{1}{1+k_p\cdot(1-\eta_c)}$	$\frac{k_p}{1+k_p-k_p\cdot\eta_c}$

preferable solution to a DC-DC PPP converter.

The essence of the PPP scheme is allowing the converter to deliver only a fraction of the total output voltage and power by the series connection. This idea is especially valuable in the application of HDEV chargers since the output voltage of which is typically high (800-1200 V). A new topology derived from the conventional IPOS configuration is applied in the hybrid rectifier topology with the benefits of reduced voltage and current ratings of semiconductor components and filter size, which will be presented in Chpt 3.

2.4. HYBRID RECTIFIER

The Hybrid rectifier denotes the series or parallel connection of a line-commutated rectifier and a self-commutated rectifier [5]. The circuitry connection enables the power to be shared by two rectifier stages ([cf. Fig. 2.7]). Therefore, each converter stage in the hybrid system is innately a PPP converter with improved efficiency and power density [23]. Applied with appropriate current modulation schemes, rectifier stages can coordinate to shape the AC current and regulate the DC-link voltage [24]. Hybrid rectifier systems are able to embrace the merits of both rectifiers which are highly efficient, cost-effective, and able to provide a close-to-unity power factor and a close-to-sinusoidal grid current. General requirements [10] placed on three-phase PFC rectifier systems apply to the hybrid rectifier systems, which are

- Sinusoidal grid input current in compliance with IEC 61000-3-2/4, IEEE-519 THD_i requirements;
- Ohmic fundamental mains behavior (PF>0.99);
- Regulated output voltage;

- Handling of a grid phase failure.

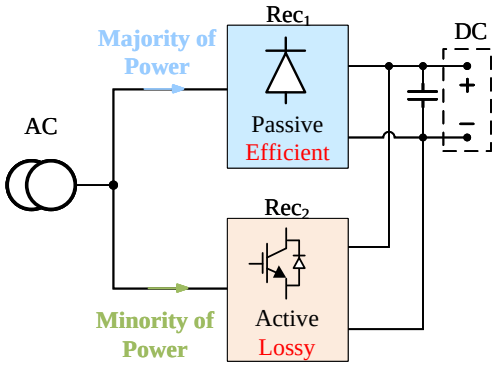

Figure 2.10: Hybrid rectifier power flow

Line-Commutated Rectifiers The line-commutated rectifiers (passive rectifiers) are rectifiers of which the commutation process of the switching components depends on the AC power line. Those rectifier systems are simple, compact, relatively inexpensive, highly efficient, and robust. Conversely, these rectifiers inject significant current harmonics into the grid, which does not comply with the IEEE-519 standards on the total distortion demand (TDD) and the individual harmonic amplitude [5]. Passive filters can be implemented to smooth the current on both the AC side and the DC side ([cf. Fig. 2.11]). A typical line-commutated rectifier consists of a passive three-phase diode bridge with an optional DC-DC stage in series ([cf. Fig. 2.12]). Without the DC-DC stage, the output voltage and the inductor current are not controllable. The output voltage is dependent on the grid input voltage amplitude and the load condition. Oppositely, a diode bridge cascaded with a DC-DC stage, e.g., a Boost converter stage, enables the controllability of the DC-link voltage and the grid current under various load conditions. Each phase leg of the diode bridge is forward-biased with the current conducted in an interval of 120° in half of the grid cycle. Because the phase current of the diode bridge does not conduct in full cycle, the grid current imposed by a three-phase diode bridge plus a DC-DC stage cannot achieve a sinusoidal shape. Extra circuit and control efforts are required to meet the current harmonic requirements.

Self-Commutated Rectifiers The self-commutated rectifiers denote rectifiers of which the commutation process of the switching components is dependent on

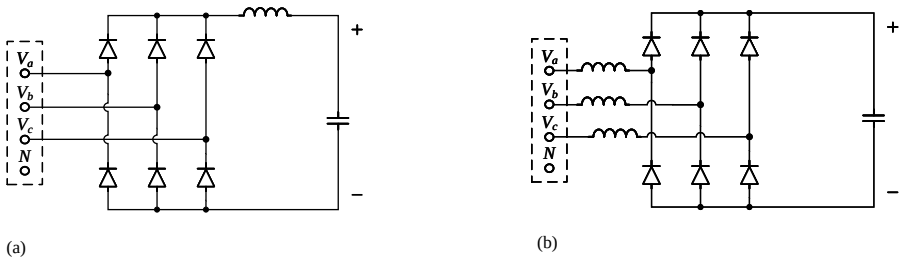

Figure 2.11: Line-commutated rectifiers: (a) Filter inductor on the DC side. (b) Filter inductor on the AC side.

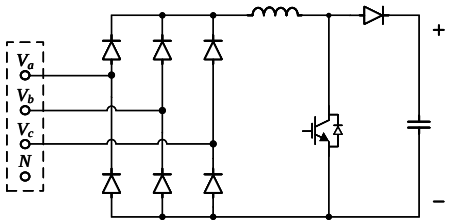

Figure 2.12: Boost PFC rectifier

the command of active switches, e.g., Vienna rectifier, Delta-switch rectifier, 6-switch PWM rectifier ([cf. Fig. 2.4]), which are introduced in Section. 2.2. Applied with appropriate control schemes, these rectifier systems are able to provide full power factor correction functionality. A close-to-unity power factor and a grid input current with harmonic component complying with the IEEE-519 standard can be achieved [24]. On the other hand, the self-commutated rectifiers are more expensive, less reliable, and less efficient compared to the line-commutated rectifiers [5].

Hybrid Rectifier Power Flow It is essential to analyze the power-sharing mechanism to obtain an explicit understanding of the hybrid rectifier. The more-efficient line-commutated rectifier is controlled to process the majority of the active power while the less-efficient self-commutated rectifier processes the minority of the active power ([cf. Fig. 2.13]). The high-order current harmonic components presented in the grid input currents and the generated reactive power due to the line-commutated rectifier are compensated by the self-commutated rectifier. At the AC front-end, the grid current shared by two stages is added up to a sinusoidal shape in compliance with the current harmonics standard e.g., IEEE-519. In addition, two rectifier stages can be operated at different switching

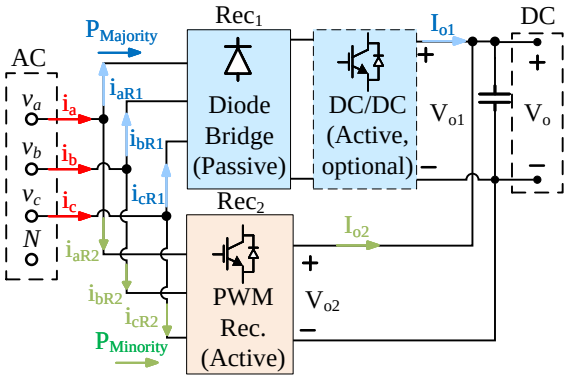

Figure 2.13: Hybrid rectifier power flow (IPOP)

frequencies. To minimize the switching losses of the line-commutated rectifier, it is operated at a relatively low switching frequency (< 10 kHz). Whereas the self-commutated rectifier is operated at a higher switching frequency to ensure the grid current shaping and improve the power density [5].

Hybrid Rectifier Topologies The hybrid rectifier can be regarded as a black box of two rectifier stages in series or parallel connection. An advantageous combination of line-commutated and self-commutated rectifiers is required to possess the features of the high efficiency and reliability of the passive rectifier and the power factor correction of the active rectifier. Typical hybrid rectifier topologies with grid current and DC-link voltage regulation are shown in Fig. 2.14. Based on their characteristics, these systems can be classified into unidirectional ([cf. Fig. 2.14(b), (c), (d), (e), (f)])/bidirectional ([cf. Fig. 2.14(a)]), three-phase ([cf. Fig. 2.14(a), (b), (c), (d)])/modular hybrid rectifiers ([cf. Fig. 2.14(e), (f)]) [25].

A visualized summary of the selected hybrid rectifier topologies on each rectifier stage, semiconductors, and the corresponding THD_i in 23 publications [26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48] on hybrid rectifier systems are shown in Fig. 2.15 and 2.16. It can be concluded that the for the line-commutated rectifier, the passive diode bridge plus a boost rectifier is preferable for its regulated output voltage and current controllability. IGBTs are preferred because they are typically cheaper compared to MOSFETs under system specifications in industrial applications. Hybrid rectifier systems with three-phase active rectifier topologies such as the T-type rectifier and the Delta-switch rectifier can all achieve low THD_i of grid input current. Modular topologies such as the single-phase SEPIC converter and the Boost converter can

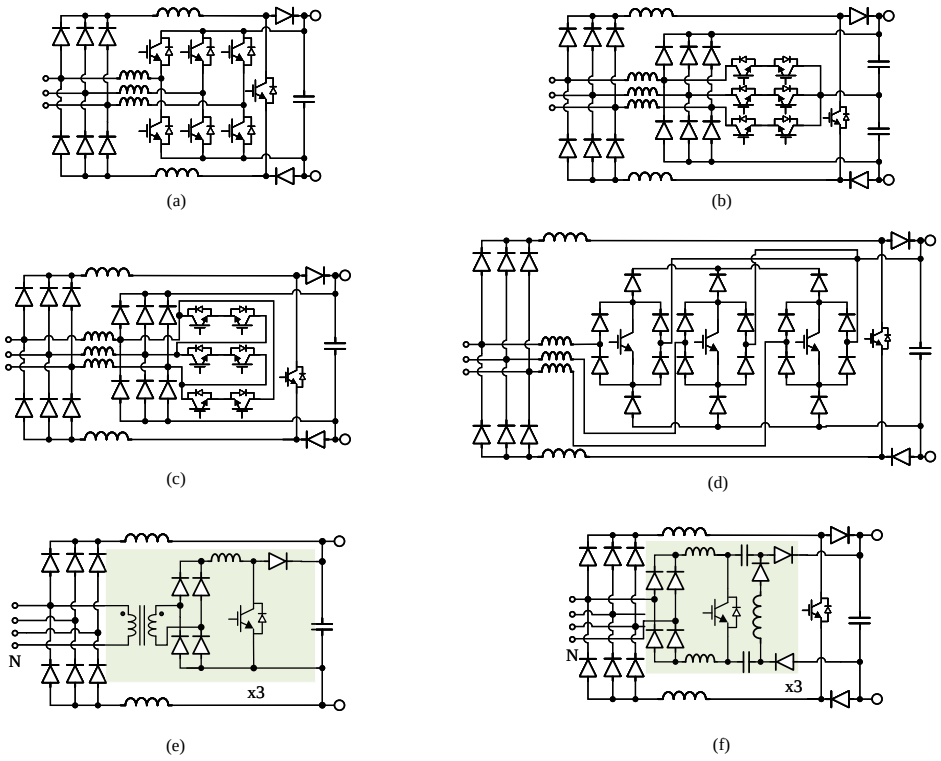

Figure 2.14: Hybrid rectifier topologies: (a) Rec. 1: Boost PFC, Rec. 2: PWM rectifier. (b) Rec. 1: Boost PFC, Rec. 2: T-type rectifier. (c) Rec. 1: Boost PFC, Rec. 2: Delta-switch rectifier. (d) Rec. 1: Boost PFC, Rec. 2: Vienna rectifier. (e) Rec. 1: Passive diode bridge, Rec. 2: Modular single-phase Boost PFC. (f) Passive diode bridge, Rec. 2: Modular single-phase SEPIC converter.

also achieve low THD_i. However, three-phase rectifier systems are more compact compared to modular rectifier systems.

2.4.1. ACTIVE POWER FACTOR CORRECTION (PFC)

The active power factor correction (PFC) aims to improve the grid power quality and reduce the losses caused by reactive power. The active PFC is achieved by the current and voltage feedback control to obtain a close-to-sinusoidal grid current waveform and a regulated DC-link voltage. A classic PFC control scheme for three-phase Boost PFC rectifier is shown in Fig. 2.17. The DC-link voltage is sensed and compared with a reference value to generate an error signal which will be fed to a voltage controller to generate a transconductance. Multiplied by a reference signal v_ref, which can be set as the reference of the desirable cur-

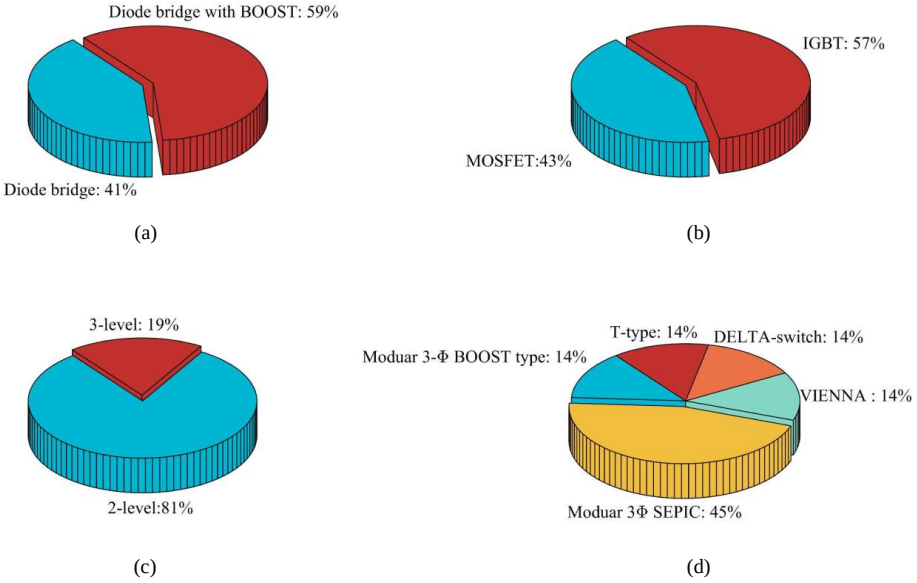

Figure 2.15: Review of hybrid rectifier topologies selection: (a) Line-commutated rectifier selection. (b) Semiconductor technology. (c) Output voltage level of selected self-commutated rectifiers. (d) Self-commutated rectifier selection.

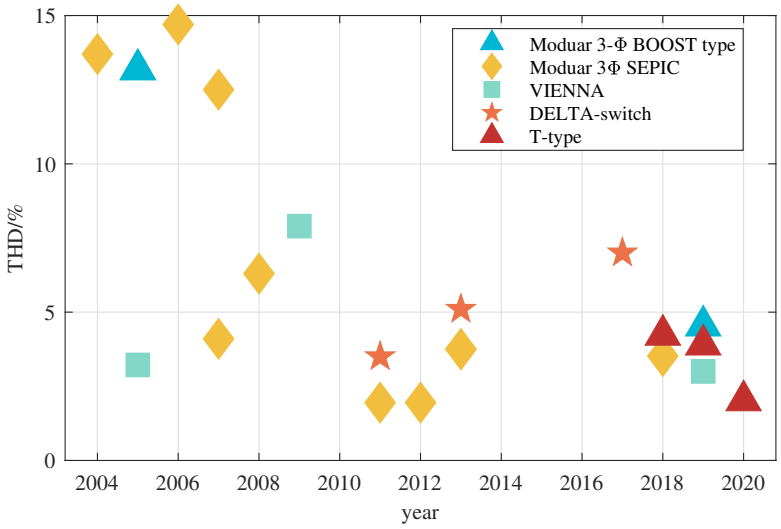

Figure 2.16: THD_i achieved in hybrid rectifier publications

rent waveform, the current reference signal i_{ref} is generated and fed to a current controller. The PWM modulator generates switching commands and the inductor and AC current waveform can be imposed to a desirable shape. This control scheme is derived from that of the single-phase PFC rectifier [49].

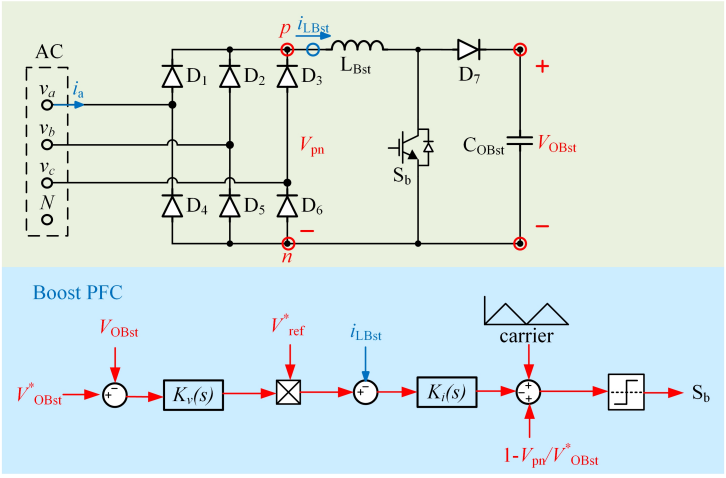

Figure 2.17: Boost PFC rectifier control

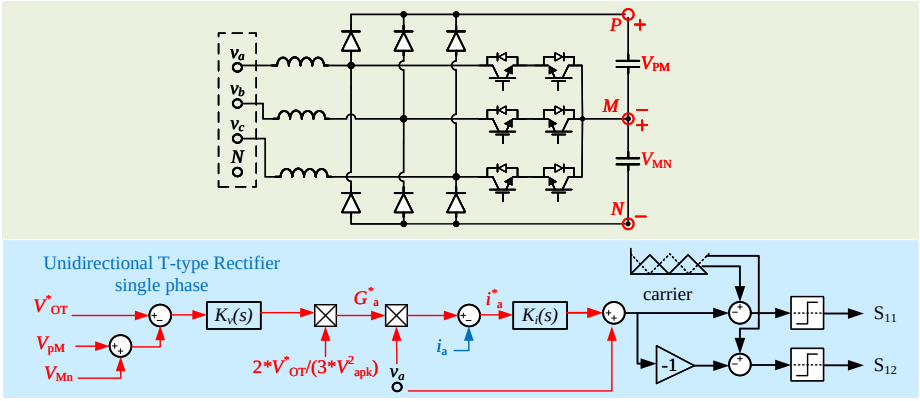

Figure 2.18: T-type PWM PFC control

Active three-phase PWM rectifiers with full PFC can also be implemented with this type of control on each phase leg ([cf. Fig. 2.18]). For the unidirectional T-type rectifier, the bidirectional switches are commanded such that the power can be delivered in both the positive and negative semi-cycles of the line phase voltage. The voltage reference signal is given by the waveform of the phase voltage v_a as a reference to generate a sinusoidal current waveform i_a. The phase current

waveform is imposed to follow the sensed phase line voltage waveform with zero phase shift, achieving a unity power factor. The three phases can be controlled independently with this SPWM strategy.

This PWM control strategy is widely applied in PFC rectifier systems for its simplicity and capability of handling phase-loss conditions [12]. Space vector modulation (SVPWM) based control, on the other hand, is not beneficial in phase loss operation and is more complex with more mathematical descriptions. PFC can also be achieved by passive filtering, but the filtering cannot provide a regulated output voltage.

3

PROPOSED HYBRID RECTIFIER TOPOLOGY

3.1. TOPOLOGY DERIVATION

As discussed in Chpt. 2.3, the high power rating leads to high voltage and current in the charging circuits of HDEV. Therefore, the conventional 2-stage topology is less desirable for its limited space for improvement in terms of system efficiency, cost, and power density. The topology selection of the AC-DC power conversion stage will be in the scope of the hybrid rectifier systems. The derivation of the proposed topology, which applies concepts of the hybrid rectifier and partial power processing, is presented will be this section. The topology selection of the hybrid rectifier system should be based on the application. Firstly, features of HDEV Charger circuits are introduced to select suitable rectifier topologies.

- Scalable and can be paralleled to process ultra high power (> 1 MW);
- Capable of delivering a relatively high and wide output voltage (800-1500 V) to interface the next-generation HDEV batteries;
- Unidirectional power flow;
- Active PFC which provides a close-to-unity power factor (PF) and a close-to-sinusoidal grid current in compliance with, e.g., IEEE-519 standard;
- Highly efficient and cost-effective;
- Handling of a phase loss condition.

Firstly, the possibility of implementing a conventional IPOP hybrid rectifier for the charging circuit is considered. Since the required output voltage range is higher than the peak value of the three-phase line-to-line voltage ($V_{\mathrm{ll,pk}}$, 564 V for EU standard), Boost-type PFC rectifiers with DC-link voltage controllability for both rectifier stages are required. A combination of a three-phase Boost PFC rectifier and a unidirectional T-type rectifier is preferred for their well-established design and PFC control scheme. The grid current is shared by two rectifier stages to achieve lower current stress on the semiconductor components (cf. [Fig. 3.1(a)]). The power processed by the two rectifier stages are defined as (P_{o1}, P_{o2}) respectively. The power shared on each rectifier stage of the IPOP topology is determined by the proportion of its average output current (I_{o1} and I_{o2}) in the total output current (I_{o}). The power-sharing ratio on the self-commuted rectifier for the IPOP hybrid rectifier is defined as $\alpha_{\mathrm{parallel}}$, as shown in Eq. 3.6-3.10. α is an important property because it is closely related to the system efficiency and the grid current $\mathrm{THD_i}$.

$$P_{\mathrm{o}} = P_{\mathrm{o1}} + P_{\mathrm{o2}} \tag{3.1}$$

$$P_{\mathrm{o1}} > P_{\mathrm{o2}} \tag{3.2}$$

$$\eta_{\mathrm{R1}} > \eta_{\mathrm{R2}} \tag{3.3}$$

$$\eta_{\mathrm{sys2}} = \frac{P_{\mathrm{o1}} \cdot \eta_{\mathrm{R1}} + P_{\mathrm{o2}} \cdot \eta_{\mathrm{R2}} \cdot \eta_{\mathrm{DC/DC}}}{P_{\mathrm{in}}} > \tag{3.4}$$

$$\eta_{\mathrm{sys1}} = \frac{P_{\mathrm{o1}} \cdot \eta_{\mathrm{R1}} \cdot \eta_{\mathrm{DC/DC}} + P_{\mathrm{o2}} \cdot \eta_{\mathrm{R2}}}{P_{\mathrm{in}}} \tag{3.5}$$

$$V_{\mathrm{o}} = V_{\mathrm{o1}} = V_{\mathrm{o2}} \tag{3.6}$$

$$\alpha_{\mathrm{parallel}} = \frac{P_{\mathrm{o2}}}{P_{\mathrm{o}}} = \frac{V_{\mathrm{o2}} I_{\mathrm{o2}}}{V_{\mathrm{o}} I_{\mathrm{o}}} \tag{3.7}$$

$$= \frac{V_{\mathrm{o}} I_{\mathrm{o2}}}{V_{\mathrm{o}} I_{\mathrm{o2}}} = \frac{I_{\mathrm{o2}}}{I_{\mathrm{o}}} \tag{3.8}$$

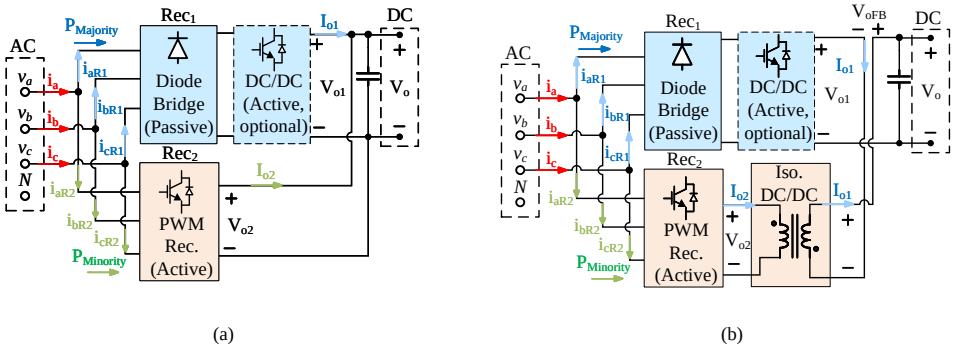

Figure 3.1: IPOS and IPOP hybrid rectifier configuration: (a) IPOP. (b) IPOS.

In the IPOP topology, the DC-link voltage of each rectifier stage is equal to the total output voltage due to the parallel connection. Thus, a high output voltage (> 1200 V) will require an upscale of voltage ratings of certain semiconductors from 1200/650 V to 1700/1200 V in the AC-DC/DC-DC stage to safely handle the voltage stress. Consequently, the design space is limited by a higher cost and fewer available component options in the required power/voltage range. The system efficiency will also be compromised because of the high voltage stress on the components.

This issue brings to the essence of this paper, which is to modify the parallel connection of the DC-link in the IPOP topology to a serial connection (cf. [Fig.

3.1(b)]). This idea is inspired by the advantages of the series connection which leads to a partial output voltage of the converter in the PPP configurations presented in Chpt. 2.3. In this new IPOS topology, the total output voltage V_o is the addition of the DC-link voltage of rectifier 1 V_{o1} and the DC-link voltage of the isolated DC-DC converter V_{oFB}. The power-sharing of each stage is determined by the proportion of the DC-link voltage in the total DC-link voltage as Eq. 3.9. The DC-link voltage of the PWM rectifier V_{o2} does not influence the power-sharing and can be kept constant. In this case, the DC-link voltage of each rectifier stage is only a fraction of the total output voltage. With appropriate sharing of the output voltage, upgrading the semiconductor components to a higher voltage rating can be avoided. It is worth noting that the output current of Rec. 1 I_{o1} is fed to the load via the secondary side of the high-frequency transformer. According to Kirchhoff's law, the average output current of Rec.1 is equal to that of the isolated converter, and the total DC output current I_o. α_{series} addresses the power-sharing ratio on the PWM Rec. 2 plus the isolated DC-DC converter path in the IPOS topology. By regulating the DC-link voltages V_{o1} and V_{oFB}, the power shared on each stage can be changed accordingly.

$$I_o = I_{o1} = I_{oFB} \tag{3.9}$$

$$\begin{aligned} \alpha_{series} &= \frac{P_{o2}}{P_o} \approx \frac{P_{oFB}}{P_o} = \frac{I_{oFB} V_{oFB}}{I_o V_o} \\ &= \frac{I_o V_{oFB}}{I_o V_o} = \frac{V_{oFB}}{V_o} = \frac{V_{oFB}}{V_{o1} + V_{oFB}} \end{aligned} \tag{3.10}$$

The IPOS circuit topology is depicted in Fig. 3.2. Note that the serial connection of the IPOS topology brings a circulating current issue which requires an isolated DC-DC converter to provide galvanic isolation between two rectifier stages (cf. [Fig. 3.3]). Without the isolation stage, the output current of the Rec. 1 will bypass the load and flow back to the grid via the diode bridge of Rec. 2, resulting in a malfunctioning state of the system. The isolated DC-DC converter should be selected based on the comparison of the DC-DC topologies in Table. 2.3 and the following considerations.

- An isolated DC-DC converter with low complexity is preferable since the control and integration of the hybrid rectifier system are already complicated;
- A wide voltage gain range. Since the total output voltage is the addition of those of the Rec. 1 and the DC-DC stage, a wide output voltage range will

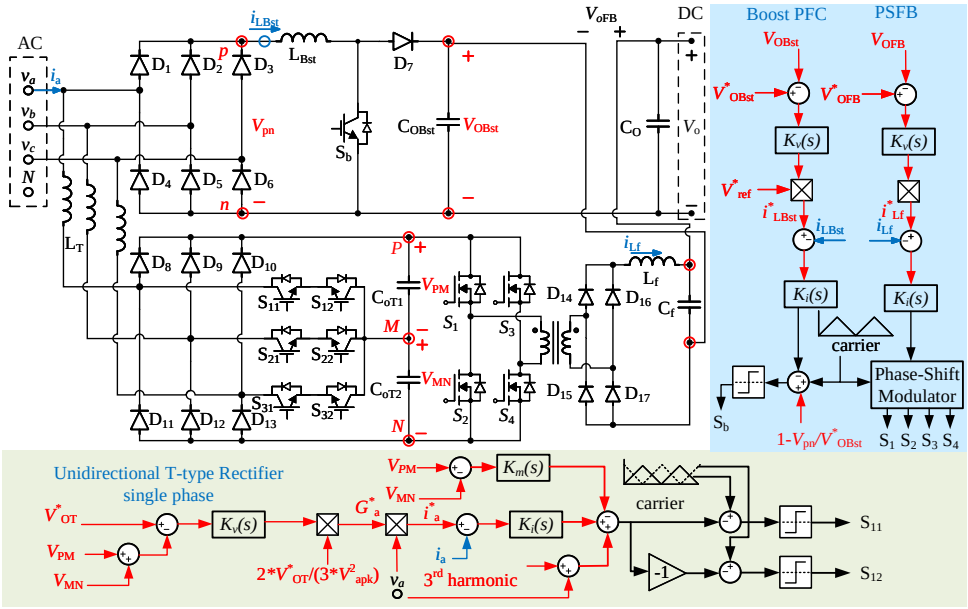

Figure 3.2: Proposed hybrid rectifier topology and the control scheme

extend the total output voltage range. Also, the power-sharing of the IPOS hybrid rectifier system is determined by the output voltage share of Rec. 1 and the DC-DC stage, a wide output voltage range can guarantee a wide power-sharing ratio to handle various load conditions;

- The active PFC of the hybrid rectifier system should not be hindered by the DC-DC stage.
- Unidirectional power flow.

Simple isolated DC-DC converters such as the flyback and the forward converter suffer from bulky magnetic components, relatively low efficiency, and high component voltage stress in high-power applications and thus are ruled out. The LLC and CLLC converters are ruled out because of their limited output voltage range (184 V- 540 V). The DAB converter is ruled out because only unidirectional power flow is required, the active switches on the secondary contribute to more cost. Finally, a PSFB is selected because it satisfies all the above-mentioned requirements. The PSFB can be placed after Rec. 1 or Rec. 2 to provide the isolation. A simple derivation explains that cascading it with the less efficient Rec. 2 which processes the minority of the active power will lead to higher system efficiency.

It is worth noting that the isolated DC-DC converter does not provide galvanic

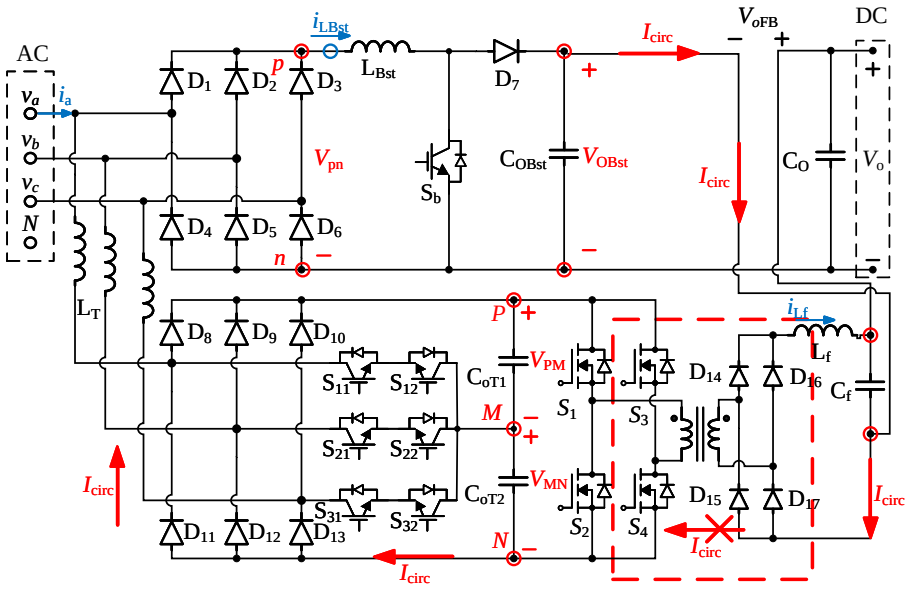

Figure 3.3: Circulating current in the IPOS hybrid rectifier topology

isolation between the AC source and the DC load. This is because the series connection provides a direct path for the output current of Rec. 1 on the secondary side of the isolated converter. Therefore, the isolation between the source and the load needs to be implemented by a line-frequency transformer at the AC front-end as shown in Fig. 2.1(a). As introduced in Chpt. 2.2, a step-down line-frequency transformer (MV/LV) is required in both charging architectures (cf. [Fig. 2.2 and 2.3]) and it already provides galvanic isolation. Another concern is that the AC-AC stage will become another source of power losses. However, the efficiency of the line-frequency transformer is typically beyond 99%, which contributes to insignificant losses in the system [50]. With the isolation provided by the transformer, the IPOS hybrid rectifier can be implemented to interface the batteries.

3.2. CONTROL STRATEGY

A few modifications are required to apply the control strategy proposed in [5] for the IPOS hybrid rectifier topology. The control scheme should be adapted with the following considerations.

- The total output voltage should be controllable in a wide range;
- The DC-link voltage of each converter stage should be controlled separately to achieve a desirable power-sharing ratio;
- The control of the added PFSB converter should not hinder the PFC operation of two rectifiers.

3.2.1. ACTIVE PFC CONTROL

A typical feedback control with PWM is implemented to regulate the DC-link voltage and grid current of the IPOS hybrid rectifier, which is depicted in Fig. 3.2. The Boost PFC rectifier, the T-type rectifier, and the isolated DC-DC stage are controlled separately.

Voltage Control Loop The DC-link voltage of each stage needs to be controlled separately since its proportion in the total output voltage, i.e., the power sharing ratio, determines the power processed by each stage. The voltage feedback control loop for each stage is identical. Firstly, the DC-link voltage is sensed and the error between the sensed voltage and its reference value is fed to a PI compensator $K_{\mathrm{v}}(s)$. Since the two selected rectifiers are Boost-type PFC rectifiers, their DC-link voltages are supposed to be larger than the peak value of the three-phase line-to-line voltage ($V_{\mathrm{DC}} > V_{\mathrm{ll,pk}}$) to ensure the controllability. The DC-link voltage of the Boost PFC is set to be $(1-\alpha)\cdot V_{\mathrm{o}}$ with a maximum value of 960 (1200×0.8) V, constrained by the maximum blocking voltage of the 1200 V semiconductor. The DC-link voltage of the T-type rectifier is set to a constant 650 V regardless of the power-sharing. The rest of the active power is processed by the T-type rectifier and the PSFB path with the DC-link voltage of the PSFB set to be $\alpha \cdot V_{\mathrm{o}}$. By altering the DC-link voltage reference value of the Boost PFC rectifier and the PSFB, a desirable power-sharing ratio can be achieved. Moreover, the total output voltage, which is the addition of the DC-link voltage of the Boost PFC rectifier and the PSFB converter, can achieve a high and wide range.

Current Control Loop The active PFC operation which shapes the input current of both rectifier stages is achieved by the inner current feedback control loop. For the Boost PFC rectifier, the output of the voltage compensator is multiplied with a voltage reference signal v^*_{ref} obtained from fragments of the grid voltage to generate the current reference i^*_{LBst} ([cf. Fig. 3.4 and Table. 3.1]) [5]. The reference current waveform which can be derived by sensing the line voltage effectively utilizes the hardware resources of both rectifier stages. The voltage reference is the desirable waveform of the inductor current. The inductor current i_{LBst} is then sensed and compared to i^*_{LBst}, with the error sent to the current

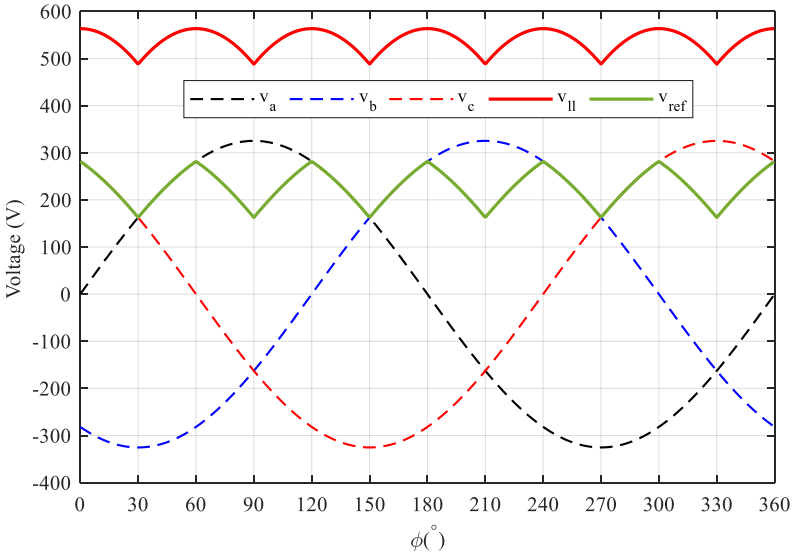

Figure 3.4: Boost inductor reference signal

compensator $K_i(s)$. The output of $K_i(s)$ is added by a feedforward signal, which is the preset duty-cycle derived from the voltage gain of a Boost converter regarding the six-pulse output voltage of the three-phase diode bridge as the input, and a reference DC-link voltage as the output. Finally, the output is sent to a PWM modulator, generating the gate signal of the Boost switch. Applying this type of control, the inductor current and the input current of the passive diode bridge can be imposed.

Table 3.1: Generation of current reference signal [5]

Interval	v_{ref}	Interval	v_{ref}	Interval	v_{ref}
0°-30°	v_a	120°-150°	v_b	240°-270°	v_c
30°-60°	$-v_b$	150°-180°	$-v_c$	270°-300°	$-v_a$
60°-90°	$-v_c$	180°-210°	$-v_a$	300°-330°	$-v_b$
90°-120°	v_a	210°-240°	v_b	330°-360°	v_c

The current control loop of a single phase of the T-type rectifier is depicted in Fig. 3.2. The control of the three-phase T-type rectifier are three duplicates of the single-phase SPWM control. The configuration of the modulator is shown in Fig. 3.5. The modulation signal V_{mod} can be treated as constant since the switch-

ing frequency is much higher than the line frequency. Similar to the Boost PFC control, the output of the voltage compensator $K_v(s)$ is multiplied by a gain to derive the line frequency transconductance G_a^*, which is then multiplied by the sensed sinusoidal grid voltage v_a to generate a sinusoidal line current reference signal i_a^*. The sensed grid current i_a is compared to the reference current and the error is sent to a current compensator $K_i(s)$. The output of $K_i(s)$ is then superimposed on a feedforward grid voltage signal v_a which presets the duty cycle of the SPWM operation [5]. Incorporating a voltage balance control of the two DC-link capacitor voltages V_{PM} and V_{MN} through another compensator $K_m(s)$, the gate signals are generated to control the bidirectional switches. This control scheme enables the T-type rectifier to generate a phase current waveform in compensation for the imposed current on the passive three-phase diode bridge to form a sinusoidal grid current ([cf. Fig. 3.6(c)]).

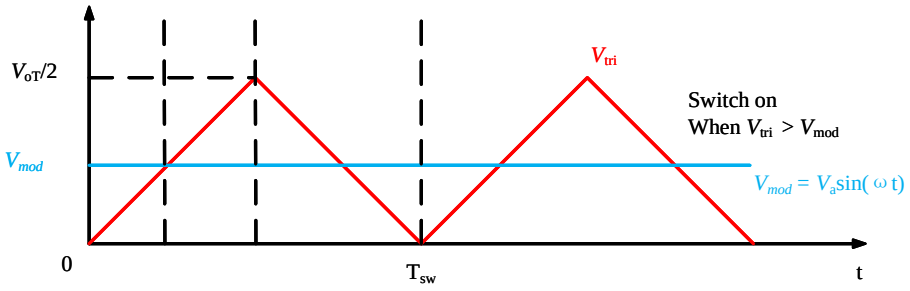

Figure 3.5: Carrier-based PWM

3.2.2. CONTROL OF THE ISOLATED DC-DC CONVERTER

To achieve a desirable total output voltage range (800-1500 V) and power-sharing ratio, the DC-link voltage of the PSFB converter needs to be controlled. The maximum DC-link voltage of the Boost PFC rectifier stage is 960 V (1200 × 0.8), which is the maximum blocking voltage of the 1200 V semiconductor devices. At this point, the total voltage of the system is 1247 V (960/0.77) considering the maximum power-sharing ratio. If higher total output voltages are required, the differential voltage has to be provided by the PSFB stage alone since further increasing the DC-link voltage of the Boost stage might damage the semiconductor devices. Therefore, for the output voltage range beyond 1247 V, the PSFB converter is responsible for the voltage increment.

A typical phase-shifted modulator is implemented to command the switches of the PSFB converter. The input voltage of the PSFB stage is the output voltage of the T-type rectifier. The voltage gain of the PSFB is determined by the phase

shift between the switches on the leading leg and the lagging leg. A voltage feedback control is implemented to ensure a desirable DC-link voltage. Peak-current mode control is implemented by a P compensator to limit the peak current of i_{Lf} on the secondary side filter inductor L_{f}. The duty cycle of the leading switches is set to be 50% as in a classic phase-shift control. A dead time is implemented to prevent the simultaneous conduction of the switches on the same bridge leg. Moreover, the ZVS takes place in the dead times, which is achieved by the resonance of the parasitic capacitance of the MOSFETs and the leakage inductance of the transformer [51, 52, 53].

3.2.3. CONSTRAINTS OF THE UNIDIRECTIONAL POWER FLOW

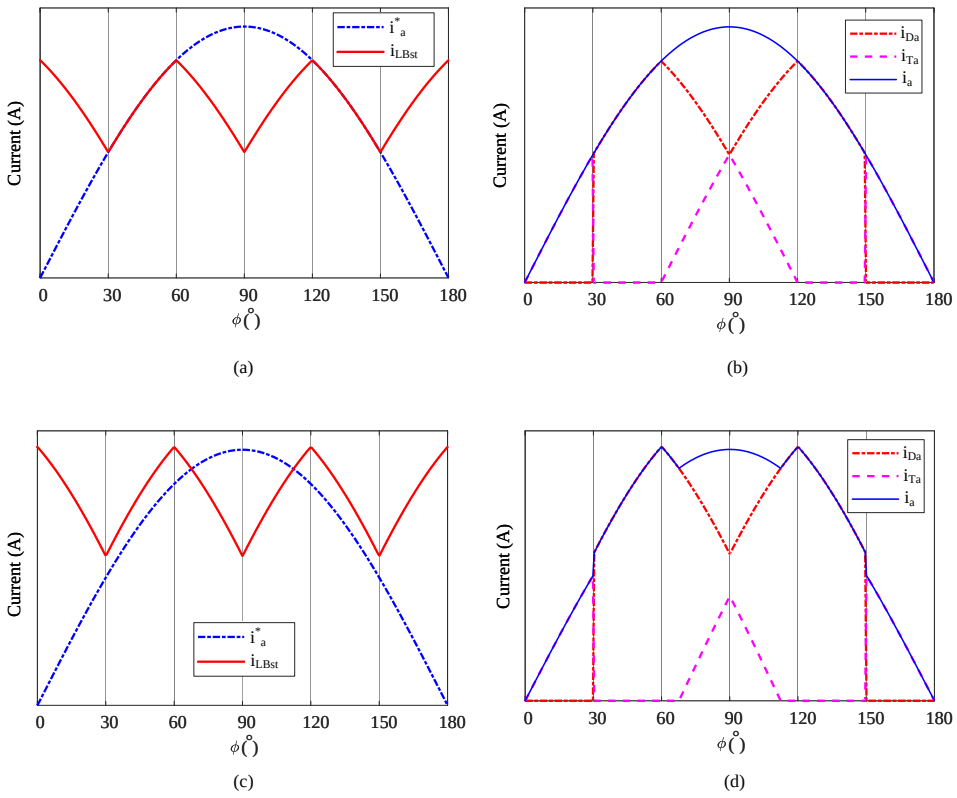

Figure 3.6: Analytical current waveforms: (a) Reference grid current and Boost inductor current, $\alpha = \alpha_{\mathrm{min}} = 0.23$. (b) Bridge diode current and T-type inductor current, $\alpha = \alpha_{\mathrm{min}} = 0.23$. (c) Bridge diode current and T-type inductor current, $\alpha < \alpha_{\mathrm{min}}$. (d) Bridge diode, distorted grid, and T-type inductor current, $\alpha < \alpha_{\mathrm{min}}$.

The unidirectional power flow of the T-type rectifier (i.e., it can only deliver voltage and current with the same sign simultaneously from AC to DC) imposes constraints on the current modulation and the range of the power-sharing ratio. The mathematical analysis of the power-sharing constraints is derived in Eq. 3.13-3.20 given the following prerequisites [24, 5].

- A purely sinusoidal and ohmic grid behavior;
- A balanced three-phase AC system;
- A lossless system;
- A constant DC-link voltage.

Therefore, the three-phase grid behavior can be expressed as,

$$\begin{cases} v_{\mathrm{a}}(\mathrm{t}) = \hat{V}_{\mathrm{a}} \cdot sin(\omega \mathrm{t}) \\ v_{\mathrm{b}}(\mathrm{t}) = \hat{V}_{\mathrm{a}} \cdot sin(\omega \mathrm{t} - \frac{2\pi}{3}) \\ v_{\mathrm{c}}(\mathrm{t}) = \hat{V}_{\mathrm{a}} \cdot sin(\omega \mathrm{t} - \frac{4\pi}{3}) \end{cases} \tag{3.11}$$

$$\begin{cases} i_{\mathrm{a}}(\mathrm{t}) = \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t}) \\ i_{\mathrm{b}}(\mathrm{t}) = \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t} - \frac{2\pi}{3}) \\ i_{\mathrm{c}}(\mathrm{t}) = \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t} - \frac{4\pi}{3}) \end{cases} \tag{3.12}$$

The input P_{in}, output power P_{o} and the average current through the boost inductor can be expressed as,

$$P_{\mathrm{in}} = P_{\mathrm{o}} = \frac{3\hat{V}_{\mathrm{a}}\hat{I}_{\mathrm{a}}}{2} = V_{\mathrm{o}} I_{\mathrm{o}} \tag{3.13}$$

$$i_{\mathrm{LBst,\,avg}} = \frac{(1-\alpha_{\mathrm{min}})\, P_{\mathrm{o}}}{\hat{V}_{\mathrm{a}}} \frac{\pi}{3\sqrt{3}} \tag{3.14}$$

Because of the parallel connection at the AC front-end, the AC input current is the addition of that of the T-type rectifier i_{Ta} and the passive diode bridge i_{Da}, which can be expressed as piecewise functions in Eq.3.15-3.18

$$\begin{cases} i_{\mathrm{Ta}}(\mathrm{t}) = \dfrac{2P_{\mathrm{o}}}{3\hat{V}_{\mathrm{a}}} \cdot sin(\omega \mathrm{t}) - i_{\mathrm{Da}}(\omega \mathrm{t}) \\ i_{\mathrm{Tb}}(\mathrm{t}) = \dfrac{2P_{\mathrm{o}}}{3\hat{V}_{\mathrm{a}}} \cdot sin(\omega \mathrm{t} - \dfrac{2\pi}{3}) - i_{\mathrm{Db}}(\omega \mathrm{t}) \\ i_{\mathrm{Tc}}(\mathrm{t}) = \dfrac{2P_{\mathrm{o}}}{3\hat{V}_{\mathrm{a}}} \cdot sin(\omega \mathrm{t} - \dfrac{4\pi}{3}) - i_{\mathrm{Dc}}(\omega \mathrm{t}) \end{cases} \tag{3.15}$$

$$i_{\mathrm{Da}}(\omega \mathrm{t}) = \begin{cases} 0, & (0 \le \omega \mathrm{t} \le \frac{\pi}{6}) \\ \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t}), & (\frac{\pi}{6} < \omega \mathrm{t} \le \frac{\pi}{3}) \\ -\hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t} - \frac{2\pi}{3}), & (\frac{\pi}{3} < \omega \mathrm{t} \le \frac{\pi}{2}) \\ -\hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t} - \frac{4\pi}{3}, & (\frac{\pi}{2} < \omega \mathrm{t} \le \frac{2\pi}{3}) \\ \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t}), & (\frac{2\pi}{3} < \omega \mathrm{t} \le \frac{5\pi}{6}) \\ 0, & (\frac{5\pi}{6} < \omega \mathrm{t} \le \pi) \end{cases} \tag{3.16}$$

$$i_{\mathrm{Ta}}(\omega \mathrm{t}) = \begin{cases} \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t}), & (0 \le \omega \mathrm{t} \le \frac{\pi}{6}) \\ \frac{2P_{\mathrm{o}}}{3\hat{V}_{\mathrm{a}}} \cdot sin(\omega \mathrm{t}) - i_{\mathrm{Da}}(\omega \mathrm{t} > 0, & (\frac{\pi}{6} < \omega \mathrm{t} \le \frac{5\pi}{6}) \\ \hat{I}_{\mathrm{a}} \cdot sin(\omega \mathrm{t}), & (\frac{5\pi}{6} < \omega \mathrm{t} \le \pi) \end{cases} \tag{3.17}$$

Due to the unidirectional power flow of the T-type rectifier, the minimum power-sharing ratio α_{min} of it can be expressed as,

$$i_{\mathrm{LBst,\,avg}} = \frac{2(\sqrt{3}-1)P_{\mathrm{o}}}{\pi \hat{V}_{\mathrm{a}}} \tag{3.18}$$

$$P_{\mathrm{o2}} \ge P_{\mathrm{o}} \cdot (1 + \frac{6\sqrt{3}-18}{\pi^2}) \tag{3.19}$$

$$\alpha_{\mathrm{min}} = 1 + \frac{6\sqrt{3}-18}{\pi^2} \approx 0.23 \tag{3.20}$$

As the result shows, a minimum power of $23\% \cdot P_{\mathrm{o}}$ needs to be processed by the T-type rectifier if the current modulation in Fig. 3.1 and Table. 3.1 is applied. A more detailed derivation is presented in Appendix A. Here the power-sharing ratio is the proportion of the power processed by the T-type rectifier plus the PSFB path. If the power processed by the Boost PFC is larger than $1 - \alpha_{\mathrm{min}}$, the magnitude of the imposed diode current i_{Da} will be larger than the grid current reference value in certain time intervals. The T-type will have to provide an input current i_{Ta} with an opposite sign such that the addition of these two currents can be sinusoidal (cf. [Fig 3.6(d) and (e)]). However, due to the unidirectional power flow, the current has to be positive since the line voltage is positive. Therefore, the current modulation is no longer valid in these time intervals, deteriorating the grid current $\mathrm{THD_i}$ and the PF.

It is worth noting that the power-sharing is still determined by the DC-link voltage proportion even with distorted grid current. The ratio α_{min} acquired from the piecewise function of i_{Ta} described by Eq. 3.15 is only the constraint to guarantee an effective PFC operation. Instead, if a bidirectional PWM rectifier is applied for

Rec.2, the line-commutated Rec.1 can process 100% of the output power P_o. The PWM rectifier will only process reactive power as a shunt filter [5].

3.3. PASSIVE COMPONENTS PARAMETER DESIGN

In order to achieve an effective PFC operation with a unity PF, a line current with low THD_i (< 5%) and a DC output with desirable ripple performance, the value of the passive components (inductors, capacitors) needs to be designed properly. The design of the passive components parameter of the Boost PFC rectifier, the T-type rectifier, and the PSFB have been well-established in [49, 54, 55, 56, 14]. In these publications, the parameter is designed based on FPP systems. Considering the IPOS hybrid rectifier system, each converter stage only processes the partial power. Therefore, the equations need to be adapted considering the power-sharing of the IPOS hybrid rectifier system. As a result, the derived equations may differ from the original ones. The value of all passive components are designed considering the maximum partial power processed of each stage to ensure a safe operation. For the sake of simplicity, only the crucial equations will be presented.

3.3.1. BOOST PFC RECTIFIER

The Boost PFC rectifier is operated in continuous conduction mode (CCM), where the ripple factor should be designed carefully to ensure the converter does not fall into discontinuous conduction mode (DCM) operaion. The inductance of the Boost inductor L_{Bst} is calculated based on the maximum inductor current ripple $\Delta I_{\mathrm{LBst,\,max}}$ requirement. As discussed in [49], the maximum current ripple should be attenuated to be 20%-40% of the peak value of the current waveform under selected switching frequency. The sizing of the inductance is relevant to the grid current THD_i and the safe operating range of the associated semiconductors. The output capacitor C_{oBst} is designed such that the dominant 6^{th} order harmonic component brought by the modulation technique is sufficiently attenuated. Here, the minimum power-sharing ratio is considered in the design. The equations are expressed as follows,

$$\hat{I_{\mathrm{D}}} = \frac{\pi^2(1-\alpha_{\mathrm{min}})\cdot\hat{I_{\mathrm{a}}}}{18-6\sqrt{3}} \tag{3.21}$$

$$\Delta I_{\mathrm{LBst,max}} = \frac{\sqrt{3}\cdot k_{\mathrm{iripple}}}{4}\cdot\hat{I_{\mathrm{D}}} \tag{3.22}$$

$$L_{\mathrm{Bst}} = \frac{\sqrt{3}\cdot\hat{V_{\mathrm{a}}}}{\Delta I_{\mathrm{LBst,max}}\cdot f_{\mathrm{swBst}}}\cdot(1-\frac{\sqrt{3}\hat{V_{\mathrm{a}}}}{V_{\mathrm{oBst}}}) \tag{3.23}$$

$$C_{\mathrm{oBst}} = \frac{(1-\alpha_{\mathrm{min}})\cdot P_{\mathrm{o}}}{12\pi\cdot f_{\mathrm{m}}\cdot V_{\mathrm{oBst}}^{2}\cdot k_{\mathrm{vripple}}} \tag{3.24}$$

where $\hat{I_{\mathrm{D}}}$ addresses the magnitude of the current on the bridge diode. k_{iripple} addresses the current ripple factor (usually a value of 20%~40% is assumed). V_{oBst} addresses the DC-link voltage of the Boost PFC rectifier. k_{vripple} addresses the voltage ripple factor (usually a value of 1% is assumed). f_{swBst} is the switching frequency of the Boost PFC rectifier. f_{m} is the line frequency.

3

3.3.2. UNIDIRECTIONAL T-TYPE RECTIFIER

The maximum inductor current ripple is derived from the current shaping method in . The inductance of the T-type filter inductor L_{T} is determined by the ripple requirement in the same manner as L_{Bst}. The output capacitor C_{oT} is designed such that the dominant 3^{rd} order harmonic component in the DC-link voltage V_{oT} caused by the current modulation is sufficiently attenuated. f_{swT} denotes the switching frequency of the T-type rectifier. The equations are expressed as follows,

$$\Delta I_{\mathrm{LT,max}} = \frac{k_{\mathrm{iripple}}}{2}\cdot\left(\hat{I_{\mathrm{a}}} - \frac{\sqrt{3}}{2}\cdot\hat{I_{\mathrm{D}}}\right) \tag{3.25}$$

$$L_{\mathrm{T}} = \frac{V_{\mathrm{oT}}}{8\cdot f_{\mathrm{swT}}\cdot\Delta I_{\mathrm{LT,max}}} \tag{3.26}$$

$$C_{\mathrm{oT}} = \frac{\alpha_{\mathrm{max}}\cdot P_{\mathrm{o}}}{6\pi\cdot f_{\mathrm{m}}\cdot V_{\mathrm{oT}}^{2}\cdot k_{\mathrm{vripple}}} \tag{3.27}$$

3.3.3. PSFB CONVERTER

Since the PSFB is operated within the hybrid rectifier, the power-sharing ratio α needs to be incorporated in the calculation of the values of passive components. Here, the maximum output voltage which determines the transformer turns ratio is related to the maximum power-sharing ratio α_{max}. The filter inductor and capacitor values are determined by the maximum allowed current and voltage ripple, respectively. The output current ripple is determined by the selected ripple factor, which is a proportion of the average output current [56]. The output capacitor is designed such that the output voltage ripple caused by the switching behavior can be sufficiently attenuated. Due to the duty-cycle loss caused by the leakage inductance of the HF transformer, the maximum effective duty cycle is less than 1. To achieve the desirable voltage gain range, this has to be considered to ensure the upper limit of the output voltage. Here, it is approximated to be 0.8 to further derive the parameter of the transformer for the required output voltage

range.

$$D_{\mathrm{fb,max}} = 0.8 \tag{3.28}$$

$$V_{\mathrm{ofb,max}} = V_{\mathrm{o}} \cdot \alpha_{\mathrm{max}} \tag{3.29}$$

$$n = \frac{V_{\mathrm{ofb,max}}}{V_{\mathrm{o2}} \cdot D_{\mathrm{fb,max}}} \tag{3.30}$$

$$\Delta I_{\mathrm{Lf,max}} = k_{\mathrm{iripple}} \cdot \frac{P_{\mathrm{o}}}{V_{\mathrm{o}}} \tag{3.31}$$

$$L_{\mathrm{f}} = \frac{(n \cdot V_{\mathrm{o2}} - V_{\mathrm{ofb,max}}) \cdot D_{\mathrm{fb,max}}}{\Delta I_{\mathrm{Lf,max}} \cdot f_{\mathrm{swfb}}} \tag{3.32}$$

$$C_{\mathrm{f}} = \frac{\Delta I_{\mathrm{Lf}}}{8 \cdot f_{\mathrm{sw,fb}} \cdot k_{\mathrm{vripple}} \cdot V_{\mathrm{ofb,max}}} \tag{3.33}$$

where α_{max} is the maximum power sharing the PSFB. $D_{\mathrm{fb,\,max}}$ is the maximum duty ratio of the PSFB. $V_{\mathrm{ofb,\,max}}$ is the maximum DC-link voltage of the PSFB. n is the transformer turns ratio. L_{f} is the inductance of the output filter inductor. C_{f} is the capacitance of the output filter capacitor. $f_{\mathrm{sw,fb}}$ is the switching frequency of the PSFB.

4

SIMULATION AND MODELLING

4.1. ANALYTICAL MODELLING

Analytical modelling is to benchmark the proposed IPOS hybrid rectifier system, with which the efficiency and losses of each converter stage will be obtained. The efficiency and loss modelling of the system under various load and power-sharing conditions is essential to evaluate the feasibility of the IPOS topology. However, directly building and testing a power electronic system under various operating points is costly and laborious. A more desirable method is to preliminarily calculate the losses of the system without hardware efforts [57]. The loss modelling can be performed by scripting, which is adaptable for varying design choices and load conditions. With an accurate loss modelling of the system, the optimal design and operating region of the power electronic system can be derived. The losses of a power electronic circuit mainly consist of semiconductor losses and passive component losses, which will be discussed below. The prerequisites of the analytical modelling are given as follows.

- Averaged circuit modelling;
- Steady-state analysis.

4.1.1. SEMICONDUCTOR LOSSES MODELLING

Semiconductor losses are the major contributors to the losses of power electronic systems despite the advance in the wide-bandgap semiconductor devices, such as SiC and GaN devices which feature low switching loss and on-resistance. In the case of high-power applications such as the HDEV chargers, the large current leads to significant conduction losses. And the switching frequency, which is closely related to the power density and the ripple performance of the system, is the determinant factor of switching losses. Semiconductor losses will also affect the thermal management of the power electronic system. Thus, it is of significance to determine losses under varying operating points and converter designs. Datasheet-based analytical modelling of semiconductor losses can be applied to preliminarily benchmark the system without hardware measurements. Semiconductor losses consist of conduction losses and switching losses, which will be discussed in the following sections.

CONDUCTION LOSSES

The conduction losses of semiconductors can be calculated by the current through the device and the temperature-dependent on-state resistance provided in the

datasheet. The current waveform through each device needs to be derived analytically. The on-state resistance can be extracted from the datasheet. A simple approach is to assume the worst-case scenario where the largest on-state resistance is taken at the highest allowable operating temperature. This reduces the efforts on the thermal modelling of semiconductor devices. The conduction losses of a semiconductor device can be expressed as [58],

$$P_{\mathrm{c}} = V \cdot I_{\mathrm{avg}} + r_{\mathrm{on}} \cdot I_{\mathrm{rms}}^2 \tag{4.1}$$

where V is the forward voltage drop in diodes and IGBTs ($V = 0$ for MOSFETs). r_{on} is the on-state resistance of the device. I_{avg} and I_{rms} are the average and root mean square (RMS) value of the current through the device respectively in a given time interval.

The active PFC of the hybrid rectifier system offers a sinusoidal phase current with line frequency and switching frequency harmonics. Here, an average model is applied assuming only the line frequency harmonic components are considered. The high frequency switching harmonics are not considered as the waveform depicts in Fig. 3.6. Considering a sinusoidal pulse width modulation (SPWM) which is applied in the control strategy in Chpt. 3.2, the ideal phase current can be expressed as,

$$I(\omega \mathrm{t}) = \hat{I} \sin(\omega \mathrm{t} + \varphi) \tag{4.2}$$

where φ is the phase shift between the fundamental line voltage and current. $\hat{I}$ is the amplitude of the phase current. ω is the fundamental radius frequency. The duty cycle $D(\omega \mathrm{t})$ of the semiconductor components is derived based on the applied modulation strategy. $I(\omega \mathrm{t})$ is the modulated current waveform as a function of time. Thus, I_{avg} and I_{rms} can be calculated as [58],

$$I_{\mathrm{avg}} = \frac{1}{2\pi} \int_a^b I(\omega \mathrm{t}) D(\omega \mathrm{t}) \mathrm{d}\omega \mathrm{t} \tag{4.3}$$

$$I_{\mathrm{rms}} = \sqrt{\frac{1}{2\pi} \int_a^b I^2(\omega \mathrm{t}) D(\omega \mathrm{t}) \mathrm{d}\omega \mathrm{t}} \tag{4.4}$$

Using the above equations and derived current waveforms, the average, and RMS current through each component of each converter stage can be derived. Only crucial equations are presented for the sake of brevity.

Boost PFC rectifier The duty cycle of a DC-DC Boost converter can be expressed as,

$$D = 1 - \frac{V_{\mathrm{in}}}{V_{\mathrm{o}}} \tag{4.5}$$

Since the Boost stage is connected in series with the three-phase passive diode bridge, the six-pulse output voltage V_{ll} of the diode bridge can be regarded as the input of the Boost stage ([cf. Fig. 3.1 and 4.1]). Therefore, the duty cycle base $D(\omega t)$ at steady-state can be expressed,

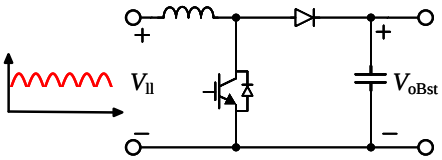

Figure 4.1: Boost stage input output characteristics

$$D(\omega t) = 1 - \frac{V_{\text{ll}}(\omega t)}{V_{\text{oBst}}} \tag{4.6}$$

The modulation index for the Boost PFC rectifier can be expressed as,

$$M_{\text{Bst}} = \frac{\hat{V}_{\text{ll}}}{V_{\text{oBst}}} = \frac{\sqrt{3}\hat{V}_a}{V_{oBst}} \tag{4.7}$$

Applying eqs. 4.2-4.4 and the averaged circuit modelling, the average and RMS currents on the passive bridge diode can be expressed as,

$$I_{\text{Bri, diode, avg}} = \frac{\pi(1-\alpha)}{6\sqrt{3}} \cdot \hat{I}_a \tag{4.8}$$

$$I_{\text{Bri, diode, rms}} = \frac{\pi(1-\alpha)}{6} \hat{I}_a \tag{4.9}$$

The average and RMS currents on the Boost switch can be expressed as,

$$I_{\text{Bst, sw, avg}} = \frac{\pi \hat{I}_a(1-\alpha)}{2\sqrt{3}} \left(1 - \frac{3M_{\text{Bst}}}{\pi}\right) \tag{4.10}$$

$$I_{\text{Bst, sw, rms}} = \frac{\pi \hat{I}_a(1-\alpha)}{2\sqrt{3}} \sqrt{1 - \frac{3M_{\text{Bst}}}{\pi}} \tag{4.11}$$

The average and RMS currents on the Boost diode can be expressed as,

$$I_{\text{Bst, diode, avg}} = \frac{3M_{\text{Bst}}(1-\alpha)\hat{I}_a}{2\sqrt{3}} \tag{4.12}$$

$$I_{\text{Bst, diode, rms}} = (1-\alpha)\sqrt{\frac{\pi M_{\text{Bst}}}{4}} \cdot \hat{I}_a \tag{4.13}$$

Unidirectional T-Type Rectifier The duty cycle of the SPWM implemented in each phase of the T-type rectifier in Fig. 3.5 can be expressed as,

$$D(\omega t) = 1 - \frac{\hat{V}_a \cdot sin(\omega t)}{\frac{V_{oT}}{2}} \tag{4.14}$$

The modulation index for the T-type rectifier can be expressed as,

$$M_T = \frac{2 \cdot \hat{V}_a}{V_{oT}} \tag{4.15}$$

Applying the averaged circuit modelling, the average and RMS currents on the bidirectional switch of the T-type rectifier can be expressed as [5],

$$I_{T,\,sw,\,avg} = \hat{I}_a \left[\frac{4 - \pi M_T}{4\pi} + \frac{(1-\alpha)(9M_T - 2\pi\sqrt{3})}{36} \right] \tag{4.16}$$

$$I_{T,\,sw,\,rms} = \hat{I}_a \left[\frac{4\pi - 3\sqrt{3} - 4\sqrt{3}M_T}{24\pi} + \frac{(1-\alpha)(\sqrt{3}M_T + \pi M_T + 4\sqrt{3} - 12)}{24} - \frac{\pi(1-\alpha)^2(3M_T - \pi)}{72} \right]^{\frac{1}{2}} \tag{4.17}$$

The average and RMS currents on the diodes of the T-type rectifier can be expressed as [5],

$$I_{T,\,diode,\,avg} = \frac{\alpha M_T \hat{I}_a}{4} \tag{4.18}$$

$$I_{T,\,diode,\,rms} = \hat{I}_a \sqrt{\frac{M_T(2\sqrt{3}+1)}{6\pi} - \frac{M_T\pi(1-\alpha)(2+\sqrt{3})}{24} + \frac{\pi M_T(1-\alpha)^2}{12}} \tag{4.19}$$

PSFB Converter The currents on the primary side leakage inductor and the filter inductor in CCM are depicted in Fig. 4.2. Here, the duty cycle loss and the cross-zero transitions are neglected for simplification. Applying the averaged circuit model, the duty cycle D_{FB}, output filter inductor current ripple ΔI_{Lf}, and the average output current $I_{Lf,\,avg}$ at steady-state can be expressed as functions

of characteristic operating points $I_{s1}, I_{s2}, I_{s3}, I_{p1}, I_{p2}$, and I_{p3} [56].

$$D_{FB} = \frac{V_{oFB}}{n \cdot V_{oT}} \tag{4.20}$$

$$\Delta I_{Lf} = \frac{(V_{oT} \cdot n - V_{oFB}) \cdot D_{FB}}{2 \cdot f_{swFB} \cdot (L_f + n^2 \cdot L_{lkg})} \tag{4.21}$$

$$I_{Lf,\,avg} = \frac{P_{oFB}}{V_{oFB}} \tag{4.22}$$

$$I_{s1} = I_{Lf,\,avg} - \frac{\Delta I_{Lf}}{2} = I_{s3} \tag{4.23}$$

$$I_{s2} = I_{Lf,\,avg} + \frac{\Delta I_{Lf}}{2} \tag{4.24}$$

$$I_{p1} = n \cdot I_{s1} = I_{p3} \tag{4.25}$$

$$I_{p2} = n \cdot I_{s2} \tag{4.26}$$

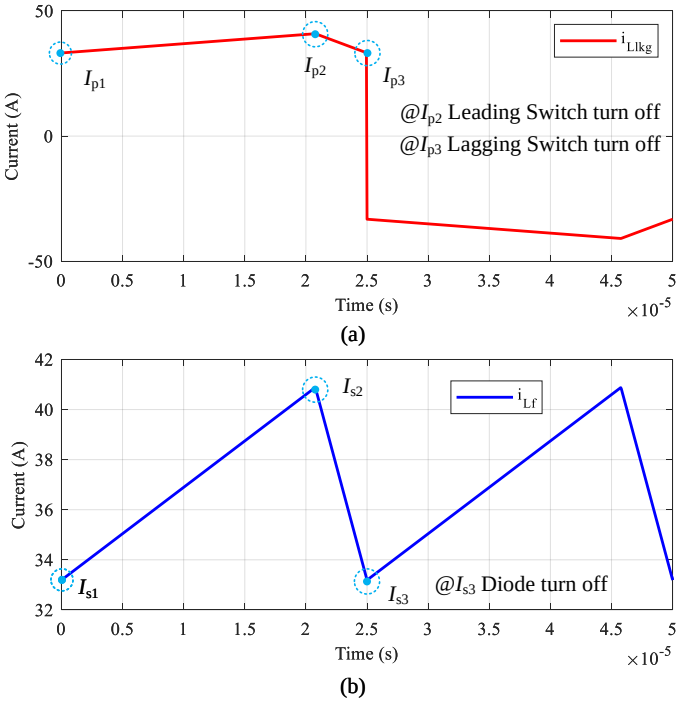

Figure 4.2: I_{Llkg} and I_{Lf} waveform

Due to the phase-shift modulation, the current stress on the leading leg and the lagging leg are different. The average and RMS currents on the primary side lead-

ing switch, its body diode, and the lagging switch can be expressed as,

$$I_{\text{FB, sw, lead, avg}} = \frac{D_{\text{fb}}\left(I_{\text{p1}} + I_{\text{p2}}\right)}{4} \tag{4.27}$$

$$I_{\text{FB, sw, lead, rms}} = \sqrt{\frac{D_{\text{fb}}\left(I_{\text{p1}}^2 + I_{\text{p1}} I_{\text{p2}} + I_{\text{p2}}^2\right)}{6}} \tag{4.28}$$

$$I_{\text{FB, swbd, lead, avg}} = \frac{(1 - D_{\text{fb}})\left(I_{\text{p1}} + I_{\text{p2}}\right)}{4} \tag{4.29}$$

$$I_{\text{FB, swbd, lead, rms}} = \sqrt{\frac{(1 - D_{\text{eff}})\left(I_{\text{p1}}^2 + I_{\text{p1}} I_{\text{p2}} + I_{\text{p2}}^2\right)}{6}} \tag{4.30}$$

$$I_{\text{FB, sw, lag, avg}} = \frac{I_{\text{p1}} + I_{\text{p2}}}{4} \tag{4.31}$$

$$I_{\text{FB, sw, lag, rms}} = \sqrt{\frac{I_{\text{p1}}^2 + I_{\text{p1}} I_{\text{p2}} + I_{\text{p2}}^2}{6}} \tag{4.32}$$

The average and RMS currents on the secondary side diodes can be expressed as

$$I_{\text{FB, diode, avg}} = \frac{I_{\text{o}}}{2} \tag{4.33}$$

$$I_{\text{FB, diode, rms}} = \sqrt{\frac{I_{\text{s1}}^2 + I_{\text{s1}} I_{\text{s2}} + I_{\text{s2}}^2}{6}} \tag{4.34}$$

SWITCHING LOSSES

The switching losses of the semiconductor devices is related to the switching frequency, and the characteristic current waveforms of the device during the switching transitions [57]. One commonly applied method is the averaged and linearized switching model. The linearized model denotes that the switching losses are expressed as the average switching energy which is linearly scaled by the reverse blocking voltage and the switching frequency in a switching cycle. The average switching energy is usually provided in the datasheet as a function of temperature and device current. The averaged switching losses can be expressed as [58],

$$P_{\text{s}} = \frac{f_{\text{sw}} V_{\text{b}}}{2\pi V_{\text{b,ref}}} \int_0^{2\pi} E_{\text{on,off,rr}} \text{d}\omega\text{t} \tag{4.35}$$

$$E_{\text{on,off,rr}} = c_2 \hat{i}^2 + c_1 \hat{i} + c_0 \tag{4.36}$$

where f_{sw} is the switching frequency, $E_{\text{on,off,rr}}$ are the device switching energies, which is expressed as a 2^{nd} order polynomial of the device current $\hat{i}$, with coefficients $c_{0,1,2}$, scaled by the device reverse blocking voltage V_{b} and reference voltage $V_{\text{b,ref}}$ from the datasheet. The currents required for calculating the switching energy in the line frequency cycle can be expressed as a piece-wise function in Fig. 3.6 using the averaged switching model, which are

Boost PFC Rectifier

$$I_{\text{Bri, diode, rr}}(\omega t) = \frac{(1-\alpha)\pi^2 \cdot \hat{I}_{\text{a}}}{18-6\sqrt{3}} \cdot sin(\frac{\pi}{6}) \tag{4.37}$$

$$\begin{aligned} I_{\text{Bst, sw, on, off}}(\omega t) &= D_{\text{Bst}}(\omega t) \cdot I_{\text{LBst, sw}}(\omega t) \\ &= \left(1 - \frac{V_{\text{ll}}(\omega t)}{V_{\text{oBst}}}\right) \cdot I_{\text{LBst, sw}}(\omega t) \end{aligned} \tag{4.38}$$

$$\begin{aligned} I_{\text{Bst, diode, rr}}(\omega t) &= (1 - D(\omega t)) \cdot I_{\text{LBst, diode, rr}}(\omega t) \\ &= \frac{V_{\text{ll}}(\omega t)}{V_{\text{oBst}}} \cdot I_{\text{LBst, sw}}(\omega t) \end{aligned} \tag{4.39}$$

Unidirectional T-Type Rectifier

$$\begin{aligned} I_{\text{T, sw, on, off}}(\omega t) &= D_{\text{T}}(\omega t) \cdot I_{\text{LT, sw}}(\omega t) \\ &= \left(1 - \frac{2\hat{V}_{\text{a}}(\omega t)}{V_{\text{oT}}}\right) \cdot I_{\text{LT, sw}}(\omega t) \end{aligned} \tag{4.40}$$

$$\begin{aligned} I_{\text{T, diode, rr}}(\omega t) &= (1 - D(\omega t)) \cdot I_{\text{LT, diode, rr}}(\omega t) \\ &= \frac{2\hat{V}_{\text{a}}(\omega t)}{V_{\text{oT}}} \cdot I_{\text{LT, sw}}(\omega t) \end{aligned} \tag{4.41}$$

PSFB Converter It is assumed that ZVS on is effective in the whole output voltage range. Therefore, the switching instance for the PSFB converter is shown in Fig. 4.2, yielding

$$I_{\text{FB, sw, lead, off}} = I_{\text{p2}} \tag{4.42}$$

$$I_{\text{FB, sw, lag, off}} = I_{\text{p3}} \tag{4.43}$$

$$I_{\text{FB, diode, rr}} = I_{\text{s3}} \tag{4.44}$$

Current on each device at all switching on/off transitions are derived. In order to further carry on the loss modelling, suitable semiconductor devices need

to be selected at a given power rating. With their datasheet specifications, the loss modelling of semiconductor devices can be completed. The power ratings of HDEV chargers are typically at Mega-Watt, where the semiconductor devices have to withstand current stress of thousands of Amperes if only one module of the IPOS hybrid rectifier is implemented. Semiconductor devices with such high current ratings are modular devices which are very expensive and scarce, resulting in a very limited design space. Therefore, paralleled modules can be deployed to downsize the power rating of each module. Here, a power rating of 50 kW is selected for a single module where an abundance of semiconductor devices are available. By a parallel connection of 20 modules, the charging unit can reach a power rating of 1 MW. The information of selected semiconductor components at 50 kW are shown in Table. 4.1. Because of the IPOS configuration, voltage ratings of all selected components are below 1200 V.

Table 4.1: Selected semiconductor devices

Component	Model	Qty.	Unit Price (€) [59]
3-Φ diode bridge	STTH6010	6	5,03
Boost IGBT	IXYK110N120B4	1	17,5
Boost diode	GC50MPS12-247	1	22,16
T-type IGBT	IKZ75N65ES5	6	6,76
T-type diode	STTH6010	6	5,03
PSFB MOSFET	FCH060N80-F155	4	12,01
PSFB diode	RFL60TZ6SGC13	4	6,45

4.1.2. PASSIVE COMPONENT LOSSES MODELLING

Losses of the passive components are also main contributors to the system power losses, especially losses of magnetic components such as inductors and transformers. An advantageous power electronic converter design is built around an optimized magnetic design. With the aim of obtaining the optimal design of the converter, an accurate loss modelling of passive components is indispensable.

INDUCTIVE COMPONENT LOSSES MODELLING

Since the inductive components contribute to considerable losses in power electronic systems, loss modelling of them is crucial in the optimization of converters in terms of power density and efficiency. The procedure of inductive components modelling can be summarized as follows [60].

1. Determine the corresponding reluctance model.
2. Determine the variation of flux density.
3. Determine core losses.
4. Determine winding losses considering the skin effect and proximity effect.
5. Determine the thermal behavior.

The inductive losses include core losses and winding losses, which are modelled applying the method in [60].

Reluctance Model The reluctance R_{m} of a given inductor/transformer core can be calculated based on the core dimensions, which can be expressed

$$R_{\mathrm{m}} = \frac{L_m}{\mu_0 \mu_{\mathrm{r}} A_m} \tag{4.45}$$

Where L_m is the mean magnetic length. A_m is the mean magnetic cross-sectional area. μ_0 is the permeability constant. μ_{r} is the relative permeability. The core reluctance model can be divided into many fragments and the the total reluctance model can be calculated in the magnetic circuit formed by these fragments.

Core Losses The core losses consist of hysteresis losses, eddy-current losses, and residual losses, which can be modelled using the empirical Improved Generalized Steinmetz Equation (IGSE). For the PFC operation, both the major (line frequency) and minor (switching frequency) magnetization loops should be considered [60].

$$P_{\mathrm{v}} = \frac{1}{T} \int_0^T k_i \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} (\Delta B)^{\beta-\alpha} \mathrm{d}t \tag{4.46}$$

$$k_{\mathrm{i}} = \frac{k}{(2\pi)\alpha - 1 \int_0^{2\pi} |\cos\theta|\alpha 2^{\beta-\alpha} \mathrm{d}\theta} \tag{4.47}$$

$$P_{\mathrm{C}} = V_{\mathrm{e}} \cdot P_{\mathrm{v}} \tag{4.48}$$

where ΔB is the peak-to-peak flux density. T is the switching cycle, and P_{v} is the time-average core loss per unit volume. coefficients k, α, β are extracted from the core material datasheet. V_{e} is the effective core volume. P_{C} are the total core losses.

Winding Losses The winding losses are the ohmic losses in the indutor windings [60]. The self/external induced eddy currents (i.e. skin effect and proximity effect) lead to increase in the resistance of a conductor as the magnetizing frequency increases. The winding losses of a Litz wire per unit length influenced by skin effect and proximity effect can be expressed as [60],

$$P_{\mathrm{S,L}} = n \cdot R_{\mathrm{DC}} \cdot F_{\mathrm{R}}(f) \cdot \left(\frac{\hat{I}}{n}\right)^2 \tag{4.49}$$

$$P_{\mathrm{P,L}} = n \cdot R_{\mathrm{DC}} \cdot G_{\mathrm{R}}(f) \left(\hat{H}_{\mathrm{e}}^2 + \hat{H}_{\mathrm{i}}^2\right) \tag{4.50}$$

$$P_{\mathrm{W}} = n \cdot l_{\mathrm{m}} \cdot R_{\mathrm{DC}} \cdot G_{\mathrm{R}}(f) \cdot \left(N^3 \cdot M \cdot \frac{4M^2 - 1}{12 b_{\mathrm{F}}^2} + \frac{\hat{I}^2}{2\pi^2 d_{\mathrm{a}}^2}\right) \tag{4.51}$$

where n is the number of strands of the litz wire, R_{DC} is the DC resistance per unit length per strand, $F_{\mathrm{R}}(f)$ and $G_{\mathrm{R}}(f)$ are the function to derive the AC resistance caused by the skin and proximity effect respectively. 1D approximation is applied to derive the external magnetic field strength $\hat{H}_{\mathrm{e}}$ caused by the neighbouring strand/conductor. For round conductor, $n = 1, \hat{H}_{\mathrm{i}} = 0$. N is the number of conductors per layer. M is the number of layers. l_{m} is the average winding length per turn. d_{a} is the diameter of a litz wire bundle. b_{f} is the window width of the core. The total winding losses can be expressed as the sum of losses at each frequency component [60].

$$P_{\mathrm{W}} = \sum_{n=0}^{\infty} \left(P_{\mathrm{S,i}} + P_{\mathrm{P,i}}\right) \tag{4.52}$$

And the total inductive losses can be expressed as,

$$P_{\mathrm{L}} = P_{\mathrm{C}} + P_{\mathrm{W}} \tag{4.53}$$

Thermal Behavior The thermal behavior of an inductive component should be modelled to ensure the temperature of the inductive component is within the safe operating region. The temperature of an inductive component can be calculated as,

$$T_{\mathrm{L}} = T_{\mathrm{amb}} + P_{\mathrm{L}} \cdot R_{\mathrm{th}} \tag{4.54}$$

Where T_{L} is the inductor temperature. T_{amb} is the ambient temperature. R_{th} is the thermal resistance of the core, which can be calculated based on the core dimensions.

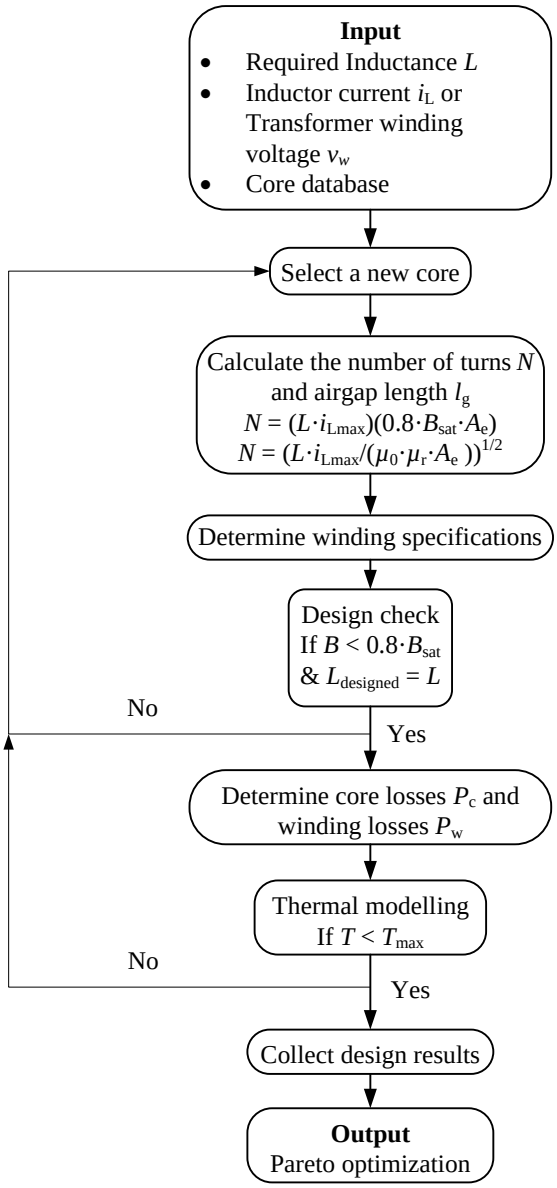

Figure 4.3: Inductor optimized design procedure

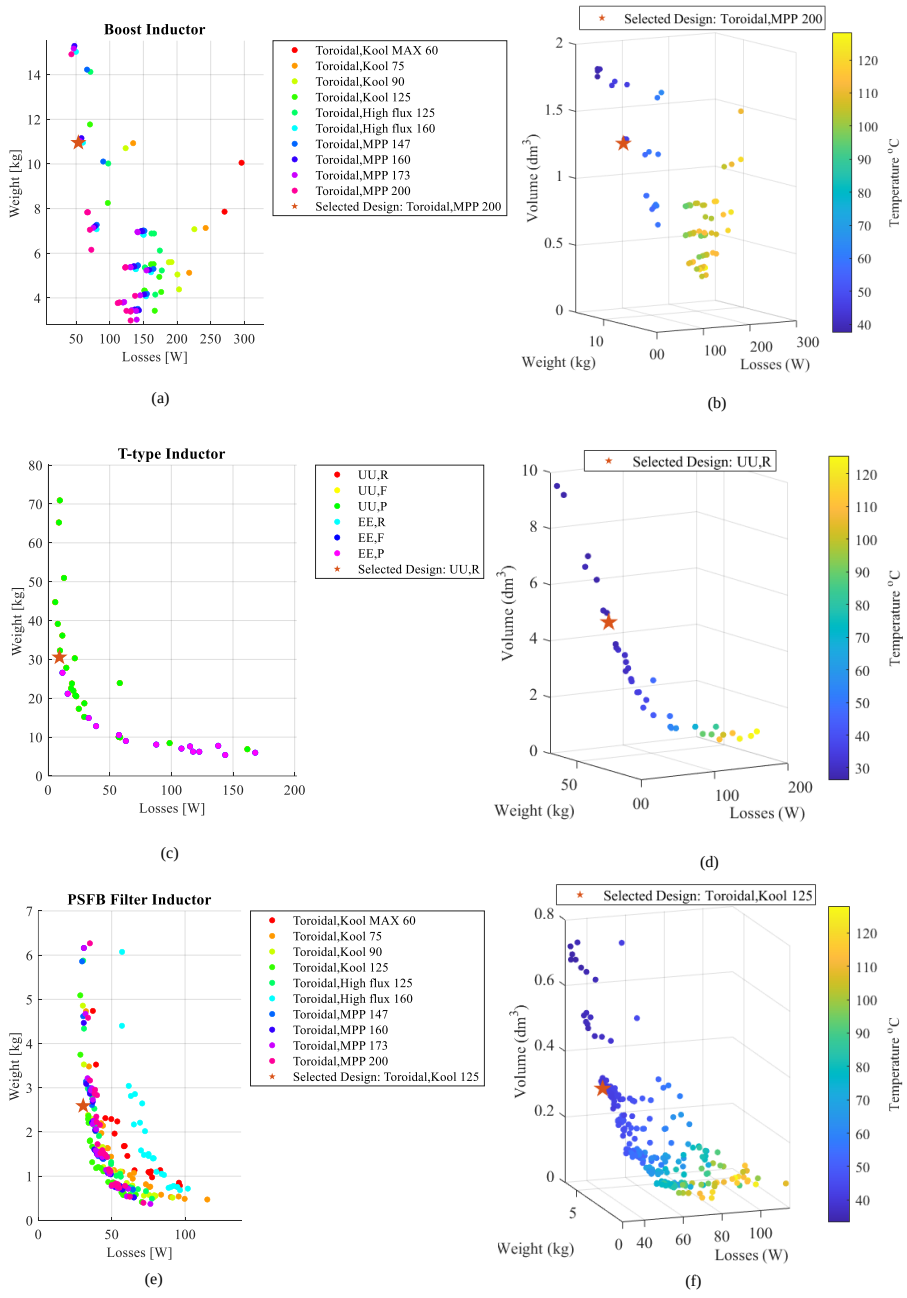

Figure 4.4: Inductor optimized design results: (a) L_{Bst} Optimized design 2D. (b) L_{Bst} Optimized design 3D. (c) L_{T} Optimized design 2D. (d) L_{T} Optimized design 3D. (e) L_{f} Optimized design 2D. (f) L_{f} Optimized design 3D.

INDUCTIVE COMPONENT OPTIMIZED DESIGN

The inductive components design procedure is shown in Fig. 4.3. The optimal design of the inductive components is obtained by the multi-objective optimization (Pareto optimization) of properties such as losses, volume, temperature, and weight. A weight is given to all these concerned properties to obtain a performance index, which can be expressed as

$$PI = \sum_{n=0}^{\infty} w_{\mathrm{i}} p_{\mathrm{i}} \tag{4.55}$$

Where w_{i} is the assigned weight, whose value is between 0 and 1. p_{i} is the normalized property, which are losses, weight, volume, etc. The optimal design of the inductor is the one with the smallest PI, which yields a design of lowest losses and highest power density. Applying the loss modelling and the Pareto optimization [61]. The specifications of the magnetic design is presented in Table. 4.2.

Table 4.2: Optimized magnetic design results

	L_{Bst}	$3 \cdot L_{\mathrm{T}}$	L_{f}
Core Material	MPP 200	R	Cool 125
Core Code	OD55740A2'	'0R49928EC'	'OD55740A2'
Number of Stacks	3	4	2
Number of Turns (N)	40	21	27
Airgap length (mm)	0	4.9	0
Wire	AWG 15	AWG 31	AWG 31
Total loss (W)	54.44	15.85	30.63
Total weight (kg)	10.96	31.17	2.59
Total volume (cm^3)	1300	3500	356

CAPACITIVE COMPONENT LOSSES MODELLING

Losses on DC-link capacitors are not significant compared to those of the semiconductors and inductive components. It can be expressed as [5],

$$P_{\mathrm{cap}} = I_{\mathrm{C,\,RMS}}^2 \cdot R_{\mathrm{ESR}} \tag{4.56}$$

Where $I_{\mathrm{C,\,RMS}}$ is the RMS current through the capacitor. R_{ESR} is the equivalent series resistance, which can be extracted from the capacitor datasheet. The RMS current of the DC-link capacitor of the Boost PFC recitifier can be expressed as,

$$I_{CoBst,RMS} = \hat{I}_a \sqrt{\frac{M_{\mathrm{Bst}}\pi}{4}\left(1 - \frac{3M_{\mathrm{Bst}}}{\pi}\right)} \tag{4.57}$$

The maximum RMS current of the DC-link capacitors of the T-type recitifier can be expressed as [5],

$$I_{CoT,RMS} = \hat{I}_a \sqrt{\frac{5\sqrt{3}M_T}{4\pi} - \frac{9M_T^2}{16}} \tag{4.58}$$

4.1.3. ANALYTICAL MODELLING RESULTS

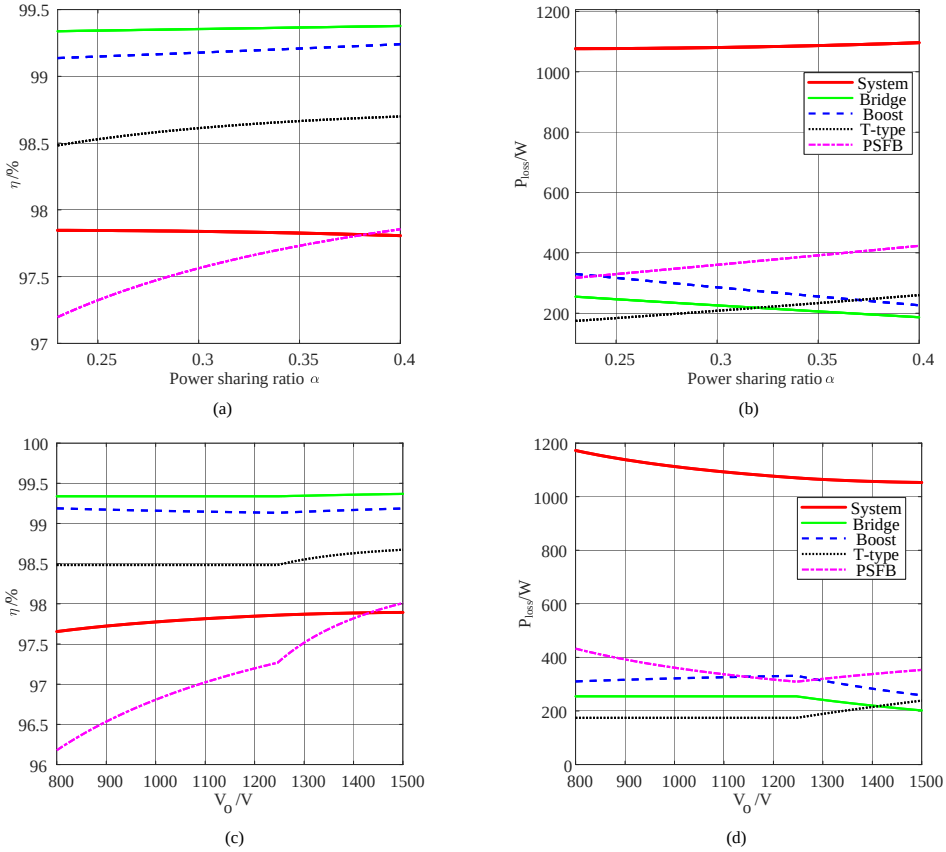

Figure 4.5: System efficiency modelling: (a) System efficiency vs. load voltage. (b) System losses vs. load voltage. (c) System efficiency vs. α when $V_o = 1200$ V. (d) System losses vs. α when $V_o = 1200$ V.

The losses and efficiency of the system and each stage can be obtained from the loss modelling under various power-sharing ratio $\alpha = 0.23 \sim 0.4$ and load condition ($V_o = 800 \sim 1500$ V) (cf. [Fig. 4.5(a) and 4.5(b)]). The system can achieve a peak efficiency of 97.89% under the system specifications in Table. 4.3. It can also be observed that the system efficiency declines with the increase of the power-

sharing on the T-type rectifier plus the PSFB. Notably, the passive diode bridge and the Boost stage are highly efficient (> 99%) while the T-type rectifier and the PSFB are less efficient, which is consistent with the analysis in Chpt. 3.

The system efficiency is also influenced by the load conditions. It can be observed that the system efficiency increases as the load voltage increases. When the output voltage varies from 800~1246 V (i.e., total output voltage at the maximum blocking voltage of the Boost switch, 1200×0.8/0.77), the power-sharing can be maintained as $\alpha_{\min}$ to achieve an optimal system efficiency. The discontinuity at the transition point is caused by the change in α. The further increase in the load voltage from 1246~1500 V can only be provided by the PSFB, rendering the α to increase from 0.23 to 0.36 (i.e., the power-sharing is determined by the output voltage proportion). The rated operating point should be set around V_o = 1000~1500 V with α = 0.23~0.36 to guarantee a high system efficiency.

4.2. SIMULATION RESULTS

The system specifications of the simulation are listed in Table. 4.3. The power rating is selected to be 50 kW where an abundance of available discrete semiconductors are available. The switching frequency of the Boost PFC is 5 kHz to reduce the switching losses. The switching frequency of the T-type rectifier is set to be 20 kHz to ensure the PFC and a low line current THD_i. The power rating and DC-link voltage range of each stage are determined by their maximum processed power.

The simulation results of the hybrid rectifier system are shown in Figs. 4.6 and 4.7. The results are obtained under two power-sharing conditions to attest the voltage/current modulation, i.e., $\alpha = \alpha_{\min}$ and $\alpha < \alpha_{\min}$. It can be observed that the DC-link voltage of each stage can be stabilized at their reference value, delivering a total 1200 V output voltage regardless of the power-sharing. For the current control, the T-type rectifier is able to compensate for the current shape of the imposed diode bridge when $\alpha \geq \alpha_{\min}$, forming a close-to-sinusoidal line current waveform (cf. [Fig. 4.7]). The line input current total demand distortion (TDD) is 1.97% < 5% with its individual harmonic component meeting the IEEE-519 requirements, implying that no added filtering stages are required (cf. [Fig. 4.8]).

Nevertheless, protection circuits, Electromagnetic Interference (EMI) filters, and LCL filters are necessary to guarantee a safe operation under various load conditions for industrial applications. When the power-sharing $\alpha < \alpha_{\min}$, the system loses the unity-power-factor operation, injecting distorted currents into the line,

Table 4.3: System specifications

RMS input line voltage $v_{a,b,c}$ (V)	230
Line frequency f_m (Hz)	50
System power rating P_o (W)	50k
Boost power rating $P_{o,Bst}$ (W)	30k-38.5k
T-type power rating $P_{o,fb}$ (W)	11.5k-20k
PSFB power rating $P_{o,fb}$ (W)	11.5k-20k
Boost switching frequency $f_{sw,Bst}$ (Hz)	5k
T-type switching frequency $f_{sw,T}$ (Hz)	20k
PSFB switching frequency $f_{sw,fb}$ (Hz)	20k
Total DC-link voltage V_o (V)	1200
Boost DC-link voltage $V_{o,Bst}$ (V)	924 (1200×0.77)
T-type DC-link voltage $V_{o,T}$ (V)	600
PSFB DC-link voltage $V_{o,fb}$ (V)	276 (1200×0.23)
Boost DC inductor L_{Bst} (mH)	2.5
T-type filter inductor L_T (mH)	0.3
PSFB filter inductor L_f (mH)	0.33
PSFB transformer leakage inductor L_{lkg} (μH)	30
Boost DC-link capacitor C_{oBst} (μF)	2350
T-type DC-link capacitor C_{oT} (μF)	2000
PSFB DC-link capacitor C_f (μF)	47
PSFB turns ratio n	1
PSFB maximum duty cycle $D_{fb,max}$	0.4

which is consistent with the analysis in Chpt. 3.2. It can be concluded that the voltage/current modulation technique originally applied in the IPOP topology is still effective in the IPOS topology.

Load step Simulation results under load step conditions are shown in Fig. 4.10 and 4.9. A step-up of load power from 25 kW to 50 kW is set at the time instance of 0.2s. It can be observed that the PFC functions desirably, offering a close-to-sinusoidal phase current and a unity power factor at steady-state. The DC-link voltage of each stage, despite some transients, is regulated to its reference value.

Phase loss Simulation results under the condition of a phase loss are shown in Fig. 4.11. In this case, the phase shift between the two phases of the grid is π. The PFC can be achieved by the Boost PFC rectifier alone with the T-type rectifier disconnected from the AC front-end. Now the total DC-link voltage is the DC-link voltage of the Boost PFC rectifier, which can be regulated between $650 - 960V$.

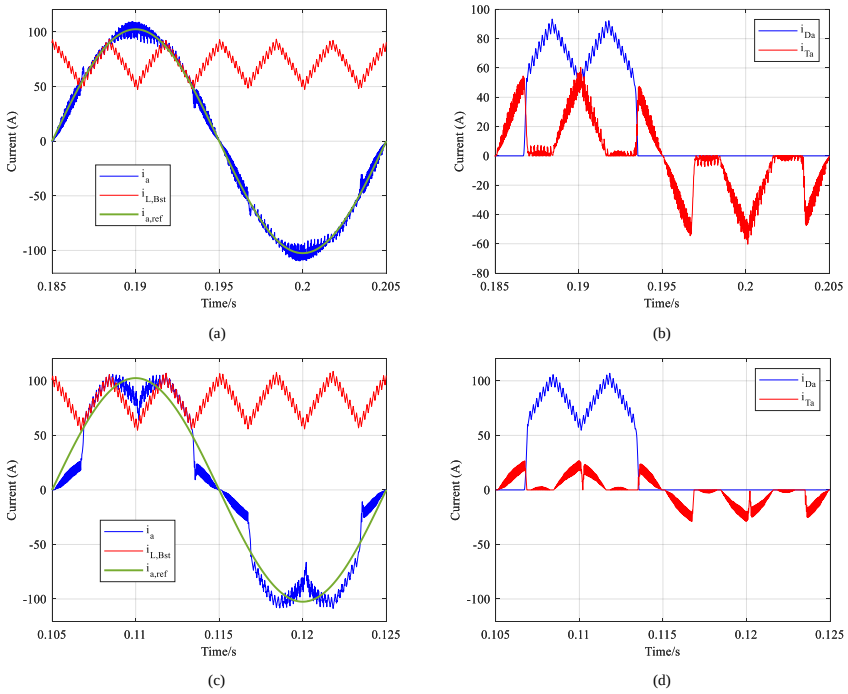

Figure 4.6: Simulation results: (a) line and Boost inductor currents, $\alpha = \alpha_{\min}$. (b) Bridge diode and T-type inductor currents, $\alpha = \alpha_{\min}$. (c) line and Boost inductor currents, $\alpha < \alpha_{\min}$. (d) Bridge diode and T-type inductor currents, $\alpha < \alpha_{\min}$.

And the output power is 25 kW considering the phase loss and the maximum power-sharing on the Boost PFC rectifier. It can be observed that grid currents of two phases can be regulated to a close-to-sinusoidal shape. The active PFC functions normally with only the Boost PFC stage.

Paralleled modules Simulation results of two paralleled modules are shown in Fig. 4.13 and 4.14. The schematic of the two paralleled modules are shown in Fig. 4.12. The power rating of the system is 100 kW with two modules of 50 kW. It can be observed that each module delivers a power of 50 kW and the current is evenly shared by two modules. At the AC front-end and the DC back-end, the total current is the addition of the currents of two paralleled modules. The PFC functions normally and the DC-link voltage regulation is not influenced by the parallel connection between modules, which attests the scalability of the proposed topology.

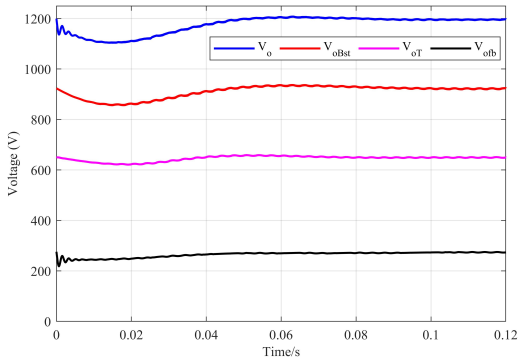

Figure 4.7: Simulation results: DC-link voltages

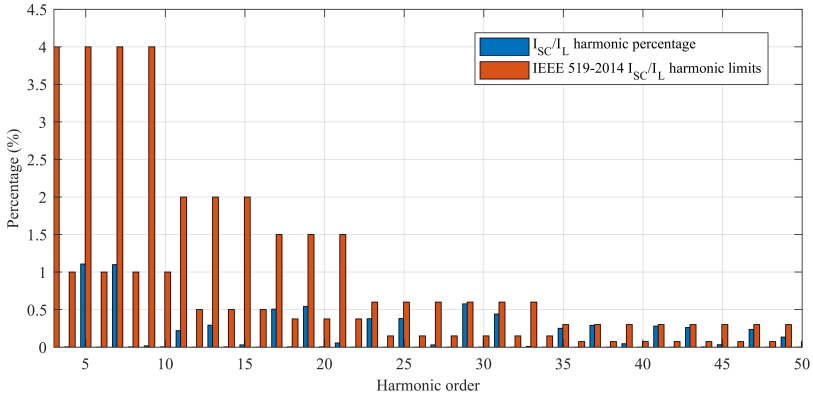

Figure 4.8: Simulation results: Line current harmonic component, $\alpha = \alpha_{\text{min}}$

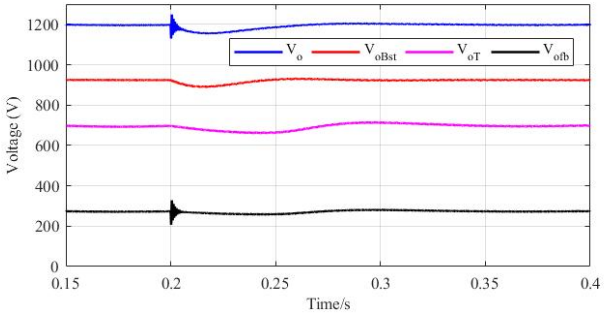

Figure 4.9: Voltage waveform at load variation at 0.2 s (25-50 kW)

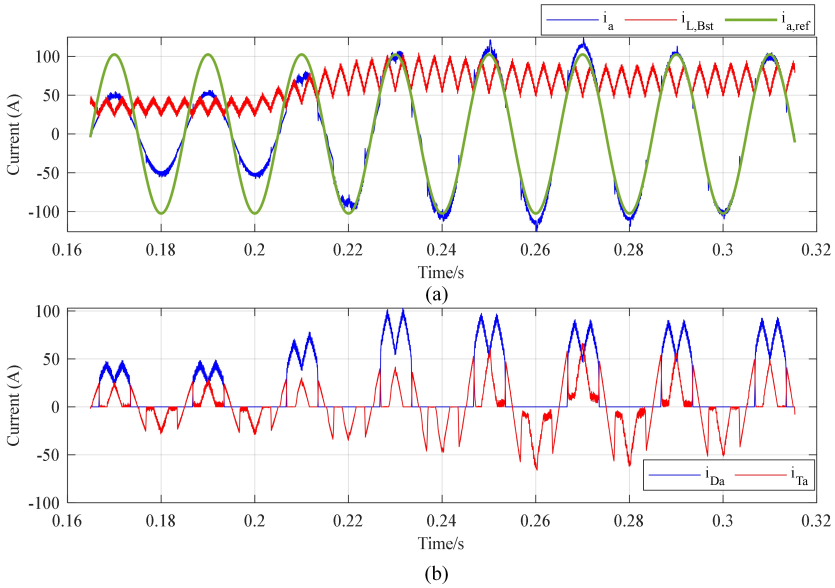

Figure 4.10: Load variation at 0.2 s (25-50 kW) : (a) Phase and Boost inductor currents, $\alpha = \alpha_{\min}$. (b) Bridge diode and T-type input currents, $\alpha = \alpha_{\min}$.

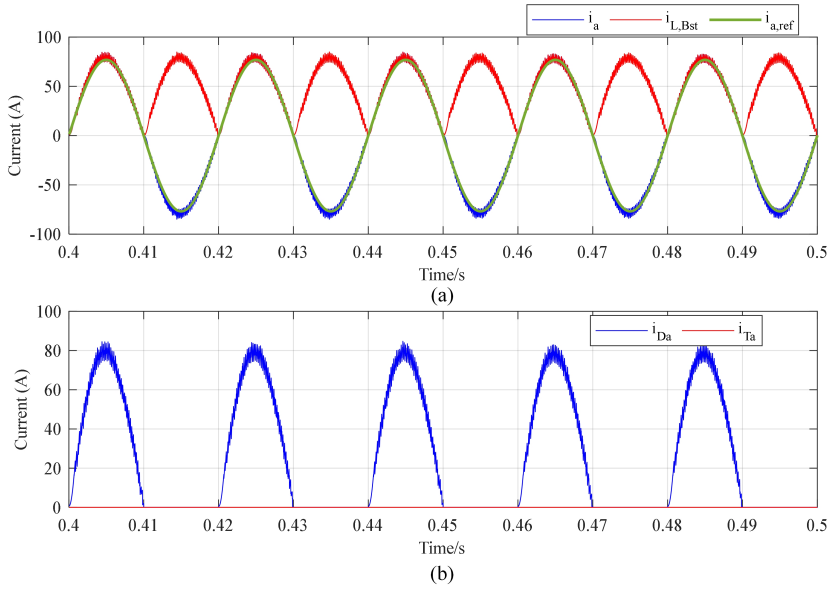

Figure 4.11: Simulation results for phase loss condition: (a) Phase and Boost inductor currents, $\alpha = \alpha_{\min}$. (b) Bridge diode and T-type input currents, $\alpha = \alpha_{\min}$.

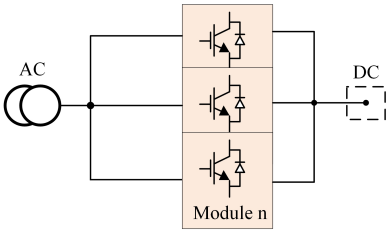

Figure 4.12: Paralleled modules

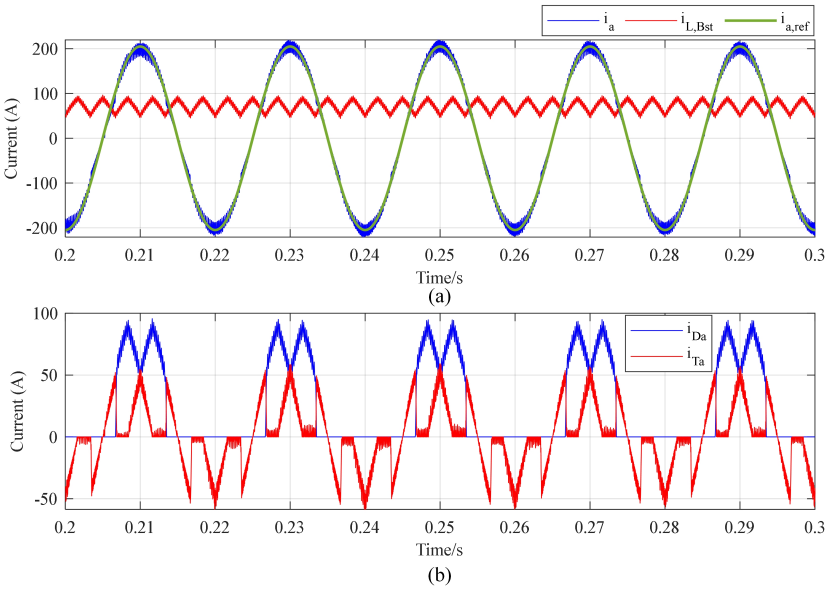

Figure 4.13: Simulation results for 2 paralleled modules (100 kW): (a) Phase and Boost inductor currents, $\alpha = \alpha_{\min}$. (b) Bridge diode and T-type input currents, $\alpha = \alpha_{\min}$.

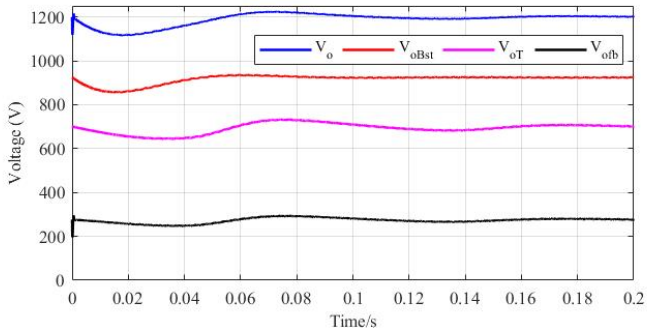

Figure 4.14: Simulation results: Voltage waveform for 2 modules (100 kW)

5

EXPERIMENTAL VERIFICATION

5.1. EXPERIMENTAL SETUP

The experimental verification was performed to attest to the feasibility of the active PFC control applied in the hybrid rectifier system, which allows the controllability of the DC-link voltage and the grid current. Here, the operation of the Boost PFC rectifier is validated. The system specifications are listed in Table. 5.1. The test setup is shown in Fig. 5.1. The passive diode bridge is implemented by a modular three-phase diode bridge. The Boost converter stage is implemented by a phase leg of a 2-level inverter in a rectifier configuration. The required inductors in the Boost converter stage are assembled. Because of the current ripple requirements and the low power rating, a larger inductance value is required to guarantee a CCM operation. The voltage and current sensors on the circuit board are calibrated to ensure the accuracy of the measurements.

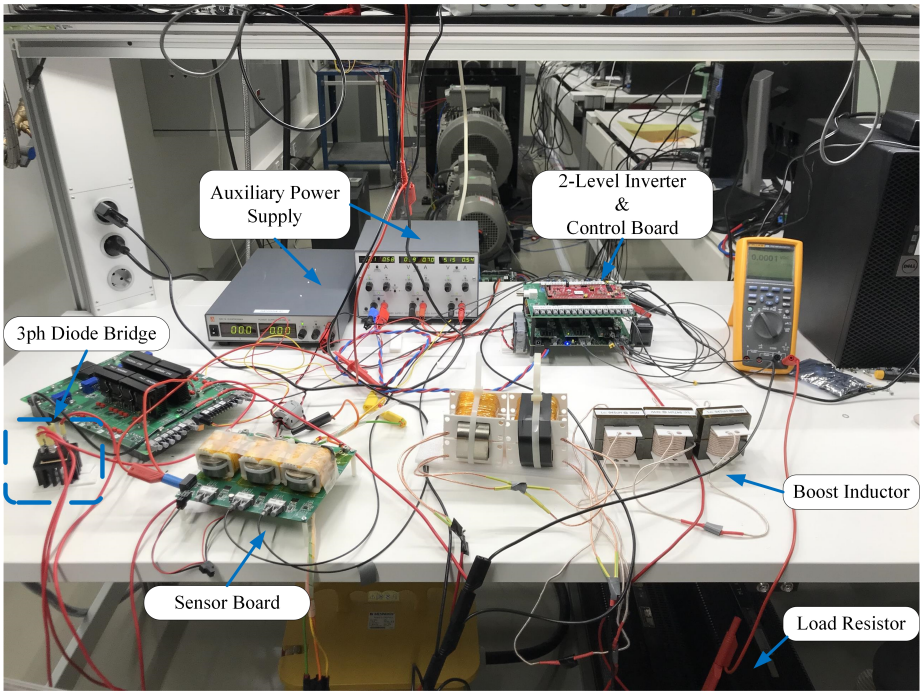

Figure 5.1: Lab setup

5.2. EXPERIMENTAL RESULTS

Firstly, an open-loop test was carried out to verify the current reference generation and the boost operation. The results are presented in Fig. 5.2 and 5.3. It can

Table 5.1: Experimental specifications

RMS input line voltage $v_{a,b,c}$ (V)	230
Line frequency f_m (Hz)	50
Power rating P_o (W)	1.2k
Boost switching frequency $f_{sw,Bst}$ (Hz)	36k
Boost DC-link voltage $V_{o,Bst}$ (V)	616 (800×0.77)
Boost DC inductor L_{Bst} (mH)	4.7
Boost DC-link capacitor C_{oBst} (μF)	360

be observed that the output voltage of the passive diode bridge is the expected six-pulse waveform in a line cycle. A resistive load is implemented and the six-pulse Boost inductor current waveform can be observed. The DC output voltage is boosted to 618 V, which is approximately the desirable value. The current reference signal is generated by taking fragments of the line voltage and calculated by the digital signal processor (DSP), which is identical to the waveform in Fig. 3.1. This implies that the control algorithm, communication, and the circuit function desirably under open loop operation.

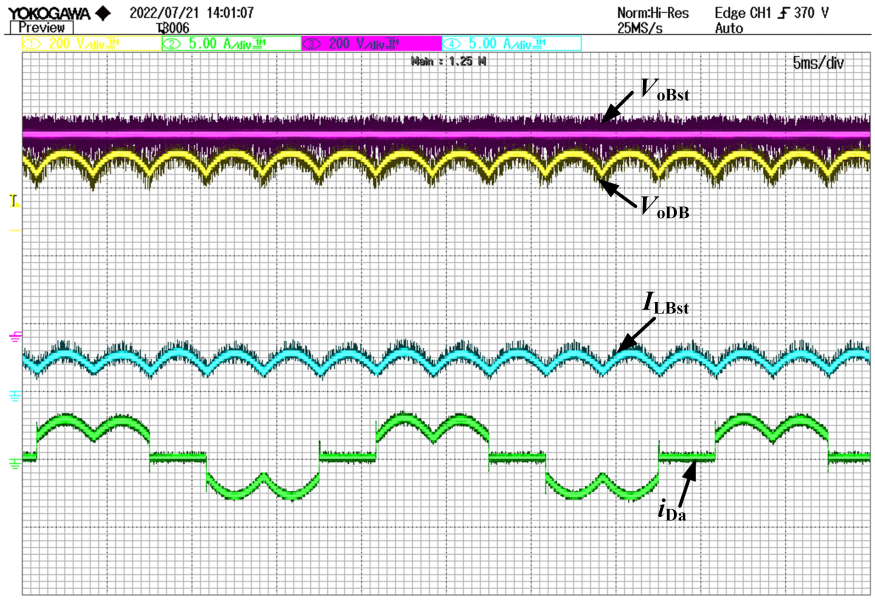

Figure 5.2: Open loop test results

Subsequently, the closed-loop control was implemented to regulate the DC out-

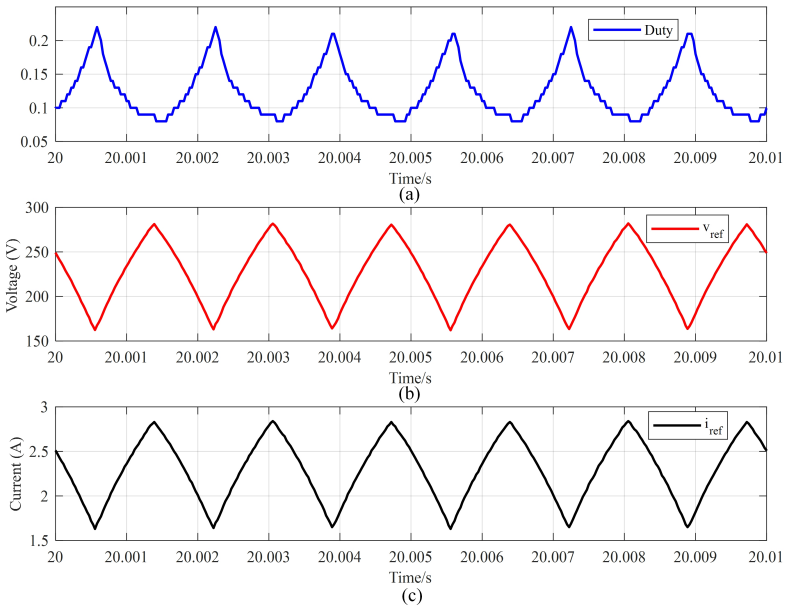

Figure 5.3: Duty cycle and current reference signal

put voltage and shape the AC input current. The results are shown in Fig. 5.4, 5.6, and 5.5. It can be observed in the multimeter that the DC-link voltage is stabilized at 615.3 V. The difference is caused by the offset of the sensor and the small voltage ripple of the DC output. The inductor current is controlled to follow the reference signal waveform which is in phase of the line voltage, implying that the PFC closed-loop control is effective. The switching frequency is indeed 36 kHz and the switching behavior matches the calculated duty ratio. Resonant behavior can be observed in the current waveform. This is caused by the resonance between the Boost inductor and the parasitic capacitance of the MOSFET in the phase leg of the 2-level inverter.

In conclusion, the active PFC control scheme is effective in the Boost PFC rectifier with desirable DC-link voltage and AC current modulation. With this current modulation technique, it is possible to parallel rectifier systems and shape the current separately to achieve a close-to-sinusoidal gird current and a unity PF. The current modulation for the unidirectional T-type rectifier is similar to that of the Boost PFC rectifier. Due to the limited resources and time, tests on the T-type rectifier and the IPOS hybrid rectifier system integration will be carried out in future work.

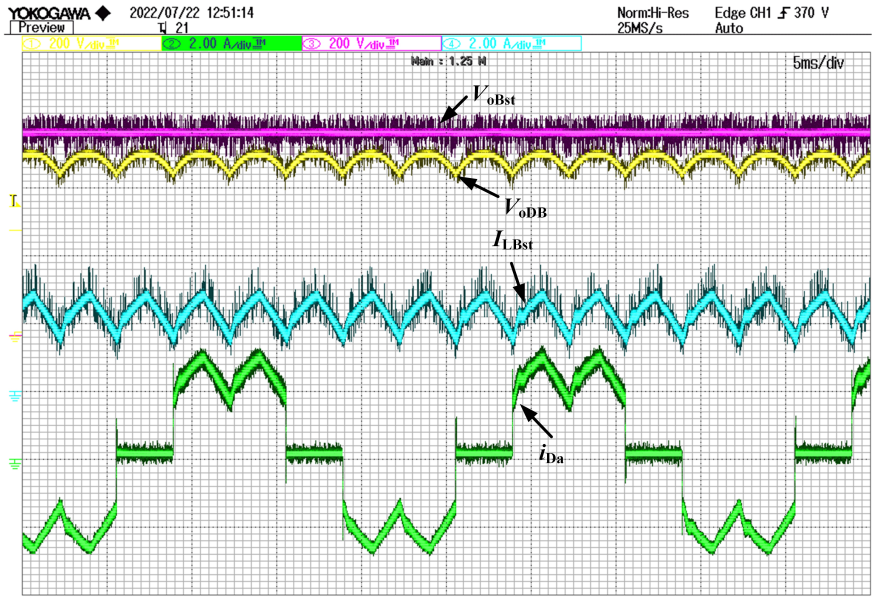

Figure 5.4: Closed loop test results

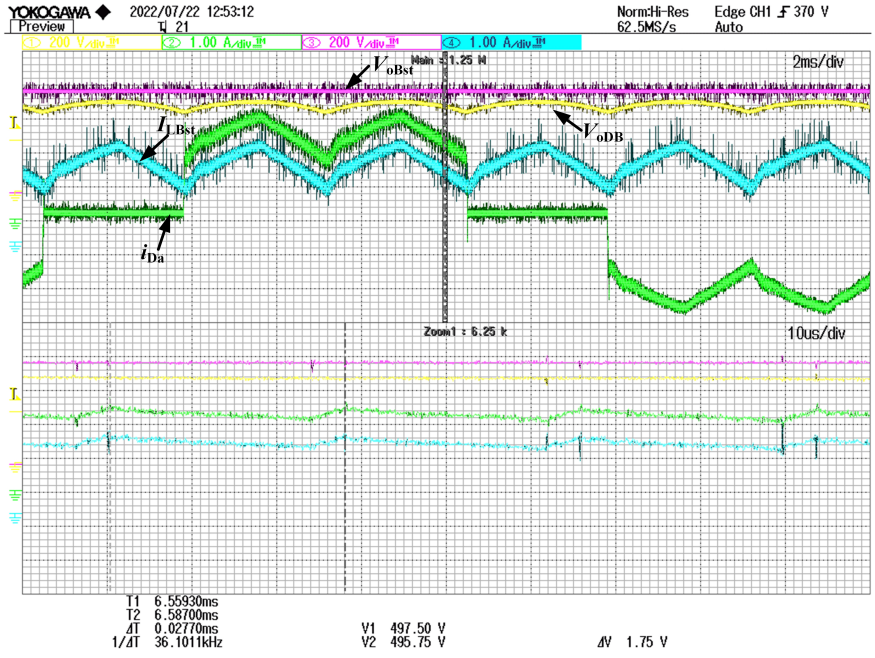

Figure 5.5: Closed loop test results

Figure 5.6: AC source and DC output voltage measurements

6

Conclusion And Future Work

6.1. CONCLUSION

This thesis proposed an Input-Parallel-Output-Series (IPOS) hybrid rectifier topology which is derived from the Input-Parallel-Output-Parallel (IPOP) hybrid rectifier in [5]. The hybrid rectifier system is able to deliver a high and wide output voltage range of 800~1500 V without the need of upscaling the 600/1200 V semiconductors to 1200/1700 V semiconductors. The PPP characteristic yields a high system efficiency under various power-sharing and load conditions without hindering the effective PFC and is thus suitable for applications such as ultra-high-power DC-type fast chargers. The feasibility and reasonableness of the proposed topology are verified using the combination of a Boost PFC rectifier, a T-type rectifier, and a Phase-Shifted Full-Bridge converter by simulation, analytical loss modelling, and experimental verification. The inductive components in the system are designed through multi-objective optimization. The results attest to the theoretical analysis, demonstrating that the proposed topology fulfills all the general/specific requirements placed on a high-power AC-DC PFC rectifier system.

- Scalable and can be paralleled to process ultra high power (> 1 MW);
- Capable of delivering a relatively high and wide output voltage (800-1500 V) to interface next-generation HDEV batteries;
- Unidirectional power flow;
- Active PFC which provides a close-to-unity power factor (PF) and a close-to-sinusoidal grid current in compliance with, e.g., IEEE-519 standard;
- Highly efficient and cost-effective;
- Handling of a phase loss condition.

6.2. FUTURE WORK

Directions of future work are listed as follows.

- The efficiency and power density of the proposed IPOS hybrid rectifier system shall be studied under a wide power rating range and switching frequencies;
- An experimental validation of the full system shall be carried out with a comparison of the conventional high-power charger solutions;

- More benefiting combinations of topologies and control schemes shall be benchmarked for the proposed IPOS topology.

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APPENDIX A POWER-SHARING RATIO CONSTRAINTS

Derivation of the minimum power-sharing ratio $\alpha_{\min}$

When $\alpha = \alpha_{\min}$, the average current of the Boost inductor can be calculated by

$$\begin{aligned} I_{\text{LBst, avg}} &= \frac{1}{2\pi}\int_0^{2\pi} i_{\text{LBst}}(\omega t)d\omega t \\ &= \frac{3}{2\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} i_{\text{LBst}}(\omega t)d\omega t \\ &= 4\times\frac{3}{2\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} i_{\text{LBst}}(\omega t)d\omega t \\ &= \frac{6}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} i_{\text{a}}(\omega t)d\omega t \\ &= \frac{6}{\pi}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} \hat{I}_{\text{a}}\cdot sin(\omega t)d\omega t \\ &= \frac{6}{\pi}\cdot\frac{2P_{\text{o}}}{3\hat{V}_{\text{a}}}\int_{\frac{\pi}{6}}^{\frac{\pi}{3}} sin(\omega t)d\omega t \\ &= \frac{2(\sqrt{3}-1)P_{\text{o}}}{\pi\hat{V}_{\text{a}}} \end{aligned} \tag{1}$$

The average current of the Boost inductor is equal to the average output DC current of the three-phase diode bridge in the Boost PFC topology. The average output current of a three-phase diode bridge can be derived from the relationship between the power processed by the Boost PFC and the average output voltage of the diode bridge.

$$\begin{aligned} V_{\text{db,avg}} &= \frac{2}{2\pi/6}\int_0^{\pi/6}\sqrt{3}V_m\cos\omega t d(\omega t) = \frac{3\sqrt{3}}{\pi}\hat{V}_{\text{a}} \\ I_{LBst,\text{avg}} &= \frac{(1-\alpha_{\min})P_{\text{o}}}{\hat{V}_{\text{a}}}\frac{\pi}{3\sqrt{3}} \\ &= \frac{2(\sqrt{3}-1)P_{\text{o}}}{\pi\hat{V}_{\text{a}}} \\ \alpha_{\min} &= 1+\frac{6\sqrt{3}-18}{\pi^2} \end{aligned} \tag{2}$$