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Genetic Algorithm–Assisted Design of Redistribution Layer Vias for a Fan-Out Panel-Level SiC MOSFET Power Module Packaging

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***Abstract*—A fan-out panel-level packaging (FOPLP) with an embedded redistribution layer (RDL) via interconnection reduces the size, thermal resistance, and parasitic inductance of power module packaging. In this study, the effect of the RDL via size on the reliability of a FOPLP SiC MOSFET power module was investigated. To improve the thermal management and thermal cycling reliability of the designed SiC module, genetic algorithm (GA)–assisted optimization methods were proposed to optimize the RDL via size. First, the heat dissipation and the plastic work density of the SiC MOSFET module with various via diameters and depths were simulated using finite element simulations. Next, both the ant colony optimization-backpropagation neural network (ACO-BPNN) with finite element simulation and the nondominated sorting genetic algorithm (NSGA-II) with theoretical model were developed to optimize the RDL via size. The results revealed that: (1) smaller via depth and size reduce the heat dissipation and thermal cycling reliability of the RDL via; (2) through both the ACO-BPNN and NSGA-II, the same optimal heat dissipation and plastic work density can be achieved in the designed module. (3) ACO-BPNN with assist of finite element simulation can provide a more effective optimization in complex packaging structure.**

Keywords-SiC MOSFET; FOPLP; ACO-BPNN; NSGA-II; Reliability optimization

I. INTRODUCTION

With the rapid development of novel energy power generation, electric vehicles, high-speed trains, smart grids, and other applications, power modules have received considerable attention [1]. Silicon carbide (SiC), a wide bandgap semiconductor, is widely used in power electronics because it exhibits superior industrial application potentials at high temperatures and voltages. SiC power electronics are superior to Si based ones due to their high switching speed, low switching loss, and high switching frequency, which improve the power density and efficiency of power systems. Moreover, Si Insulated Gate Bipolar Transistors (IGBTs) exhibit considerable switching loss at high temperatures, however, the SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) can keep relatively stable at higher temperatures [2].

In terms of packaging, the embedded redistribution layer (RDL) via interconnection technology ensures smaller size, lower thermal resistance, and parasitic inductance. Fan-out panel-level packaging (FOPLP) is a preparation of power semiconductor devices or modules that combine PCB panel-level production with chip packaging [3]. Furthermore, through their embedded integration in FOPLP technology, double-sided heat dissipation is used in the SiC MOSFET power module to reduce its thermal resistance.

However, optimization of the size and position of RDL via is necessary to achieve the reliable fan-out packaging of MOSFET power devices. Typically, ant colony and genetic algorithm optimization methods are used for package level reliability optimization. These methods mainly combine multiobjective optimization algorithms with the finite element method to optimize packaging material, structures, and processes. Furthermore, these methods are easy to implement for simple packaging structures. But they have limitations in the reliability optimization of complex packaging structures considering the multiphysics coupling effect. Machine learning algorithms have been widely used to realize more effective reliability optimization.

In this study, to improve the thermal management and thermal cycling reliability of the designed FOPLP SiC MOSFET, the RDL via size is optimized by using both the NSGA-II with theoretical model and the ACO-BPNN with finite element simulation.

II. THEORETICAL MODELS

The SiC MOSFET FOPLP packaging process (Fig. 1) is as follows.

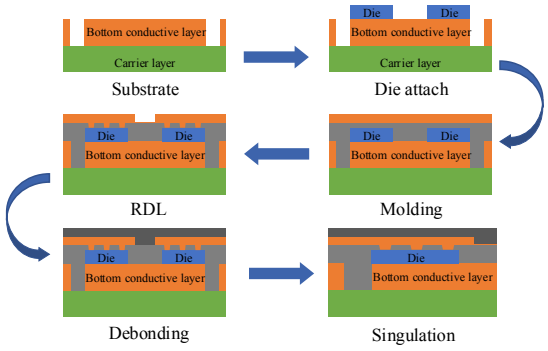

Figure 1. SiC MOSFET FOPLP packaging process

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Firstly, the bottom conductive layer is constructed on the carrier. Then, the SiC MOSFET dies (drain–source voltage V_{DS} = 600 V, continuous drain current I_D = 5 A, size = 3.85 mm × 2.62mm) are fixed on the pad by soldering. Next, the plastic encapsulation material and copper foil are molded on the carrier. A laser drilling process is used to drill through the via in the core plate to establish internal RDL. Furthermore, the surface heat-sink layer is pressed with plastic encapsulation material. Finally, the bottom carrier layer is removed, and the solder pads on the surface of device are treated with electroplating tin, then the whole board is cut into individual modules.

A. *Thermal resistance model*

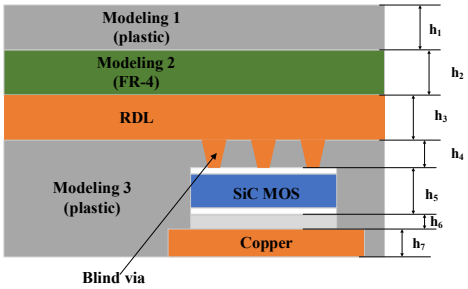


Figure 2. The cross-section of the SiC MOSFET module.

Fig. 2 displays the double-sided heat dissipation path of the designed SiC MOSFET module. Its total thermal resistance R_0 can be expressed as follows:

$$R_0 = \frac{R_{up} \bullet R_{down}}{R_{up} + R_{down}} \tag{1}$$

where R_{up} is the thermal resistance of upward heat transfer of the module and R_{down} is the thermal resistance of downward heat transfer of the module.

Considering the thermal spreading effect [4], the thermal resistance R of one-way heat transfer of the power module can be expressed as follows:

$$R = \sum_{i=1}^{n} \frac{h_i}{k_i A_i} . \tag{2}$$

where n is the number of layers of packaging modules, A_i is the equivalent heat transfer area of the layer i material, and k_i is the heat transfer coefficient of the layer i material.

In the particular module as designed in this study, R_{down} is firstly considered as displayed in Figure 2. Two layers are present in total. Therefore, Eq. (2) can be rewrote as follows:

$$R_{down} = \sum_{i=6}^{7} \frac{h_i}{k_i A_i} . \tag{3}$$

The equivalent heat transfer area A_6 can be expressed as follows:

$$A_6 = \left(l_c + \frac{k_5 h_6}{k_6} \right)^2 . \tag{4}$$

where l_c is the side length of the die in the package module.

Next, R_{up} is considered. A blind via structure is present in the first layer. Therefore, Eq. (2) should be modified. The blind via of the first layer leads to the complexity of thermal resistance formulation. Here, the blind via can be separated from the second layer to represent the heat transfer path in parallel between the shell and the blind via. The thermal resistance of the blind via can be approximated as follows:

$$R_m = \frac{h_4}{k_3 A_m} . \tag{5}$$

where R_m is the thermal resistance of the blind via and A_m is the contact area between the blind via and the chip.

Because the heat transfer area of the blind via overlaps with the aforementioned equivalent heat transfer area A_4, the equivalent heat transfer area A_g of the shell layer can be obtained as follows:

$$\begin{aligned} A_4 &= \left(l_c + \frac{k_5 h_4}{k_4} \right)^2 . \\ A_g &= A_4 - A_m \end{aligned} \tag{6}$$

Thus, the thermal resistance of the shell layer R_g can be calculated as follows:

$$R_g = \frac{h_4}{k_4 A_g} . \tag{7}$$

The thermal resistance of the fourth layer can be obtained as follows:

$$R_1 = \frac{R_g \times R_m}{R_g + R_m} = \frac{h_4}{k_4 A_g + k_3 A_m} . \tag{8}$$

Therefore, we have the following expression to represent R_{up}:

$$R_{up} = \sum_{i=1}^{3} R_i . \tag{9}$$

The final total thermal resistance R_0 can be obtained by substituting R_{up} and R_{down} into Eq. (1) for calculation.

B. *Thermal-stress model*

The package level failures caused by the thermal cycling is related to the volume average inelastic working energy density (W), which can be described by the Darveaux model [5] as follows:

$$\begin{cases} N_0 = \lambda_1 W^{\lambda_2} \\ da / dN = \lambda_3 W^{\lambda_4} \end{cases} . \tag{10}$$

where N_0 is the number of thermal cycles for generating the initial crack, λ_1 – λ_4 is the fitting coefficient, a is the length of the characteristic crack, and a_c is the width of the chip.

The energy density of the RDL via can be obtained as follows:

$$W_k = E_3 \alpha_3^2 \Delta T^2 \frac{S_k}{V_k h_4} . \tag{11}$$

where S_k is the contact area between the blind via and other layers, V_k is the volume of the blind via, α_i is the thermal expansion coefficient of the layer i material, and W_k is the average inelastic working energy density of the blind via layer.

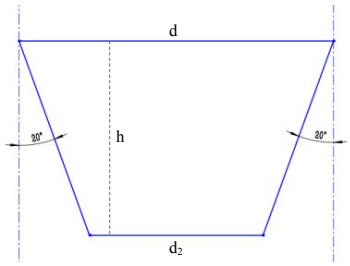


Figure 3. The cross section of conical via

As displayed in Figure. 3, the following expression can be obtained to geometrically model the conical via:

$$\begin{cases} S_k = \frac{1}{4}\pi d_2^{\,2} + \frac{1}{2}\pi \frac{d^2}{\sin 20^\circ} - \frac{1}{2}\pi \frac{d_2^{\,2}}{\sin 20^\circ} \\ V_k = \frac{\pi}{12\tan 20^\circ} d^3 - \frac{\pi}{12\tan 20^\circ} d_2^{\,3} \end{cases}. \quad (12)$$

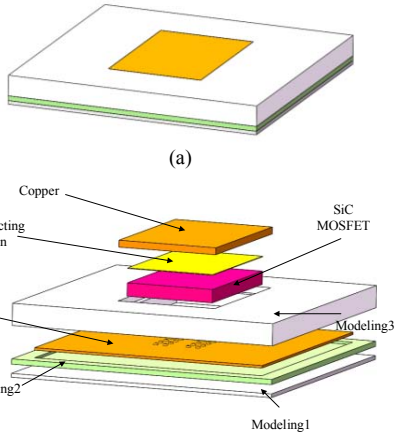
Finally, we can calculate the volume average inelastic working energy density of RDL via with the following expression:

$$W_k = 0.416 \frac{h\left[8.77d^2 - 5.77(d-0.72h)^2\right]}{d^3 - (d-0.72h)^3}. \quad (13)$$

III. FINITE ELEMENT SIMULATIONS

A. Three-dimensional modeling

A three-dimensional model of the designed FOPLP SiC MOSFET power module is displayed in Fig. 4(a). Referring to Fig. 4(b), the module simply consists of the SiC MOSFET chip, molding 1–3, RDLs, and copper.



(a)

(b)

Figure 4. (a) 3D model of the FOPLP SiC MOSFET power module, (b) its the components

B. Simulation parameters and conditions

According to JEDEC JESD22-A106B standard [6], the thermal cycling simulation condition selected in this paper is shown in Fig. 5. The temperature range is -38~152 °C. The conversion time from the high to the low temperature is 60 s, and the conversion speed can be estimated as 38 °C/s. Five thermal cycles are calculated in this simulation. The properties of components used in the thermal cycle simulation are listed in Table 1 [7-9].

Table 1: The properties of components used in the thermal cycle simulation.

Components	Modulus E (GPa)	Poisson ratio v	Coefficient of thermal expansion α (ppm/K)	Thermal conductivity k (W/mK)
SiC MOSFET	400	0.142	5.1	150
Plastic	9	0.35	28	0.65
FR-4	20.4	0.11	12.5	0.38
Conducting resin	4.41	0.3	40	2.5
Cu	See[10]	0.36	17	390

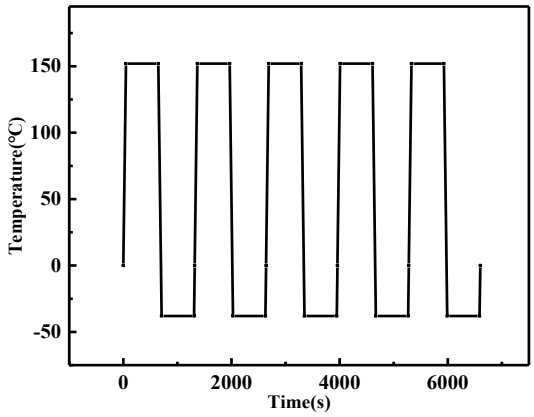
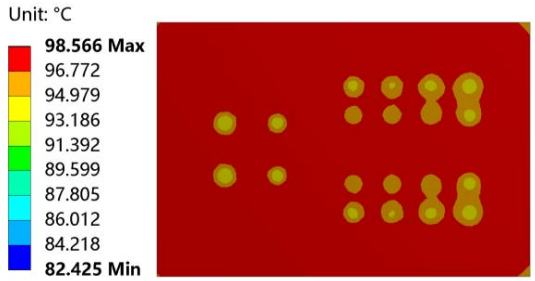


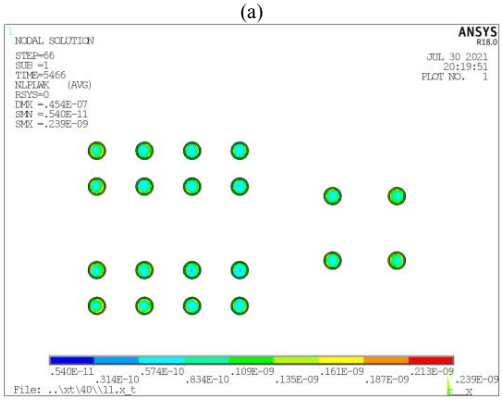
Figure 5. Smulated temperature condition during thermal cycling

C. Finite element simulation

One of heat dissipation simulation results of the designed SiC MOSFET power module is displayed in Fig. 6(a). RDL vias are directly affected by the heat because they are directly located on the SiC MOSFET chip. Furthermore, the simulated plastic work density distribution in blind vias during thermal cycling is displayed in Fig. 6(b). Referring to Fig. 6(b), the maximum plastic work density occurs at the edges of the blind vias. The thermal expansion coefficients of SiC and copper differ considerably, which leads to the potential interface crack failure.



(a)



(b)

Figure 6. Simulation results of (a) Heat dissipation; (b) Plastic work density distribution.

IV. Optimization and Discussions

A. ACO-BPNN

First, the ACO-BPNN was used to optimize the RDL via size, and its optimization process is displayed in Fig. 7 [10]. Based on the training set, the case temperature and plastic work density of each of the chip positions obtained by the ant colony algorithm (ACA) iteration were calculated. The *d* and *h* of each blind via were selected as the input, and the simulated plastic work density and junction temperature were regarded as the output. Next, the iteration of the ACA, the path with the highest concentration of accumulated pheromone was determined and considered as the optimal solution.

For the example presented in Table 2, as illustrated in Fig. 8, the optimal solution can be obtained when *d* is 150 μm and *h* is 40 μm.

Table 2: The size range of RDL via

	Lower limit (μm)	Upper limit (μm)
h	40	60
d	80	150

The results reveals that optimal heat dissipation and plastic work density were obtained when the *d* was 150 μm, and *h* was 40 μm. Table 3 indicates that ACO-BPNN can lower the chip junction temperature and plastic work density by 0.37% and 53.14%, respectively.

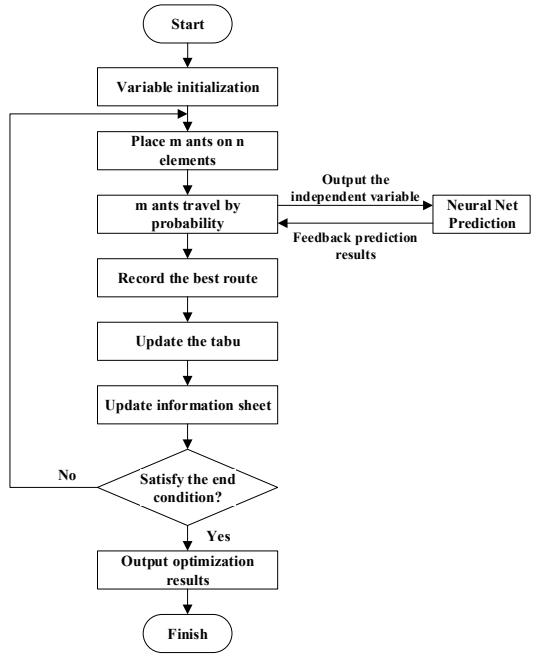


Figure 7. Flowchart of ACO-BPNN.

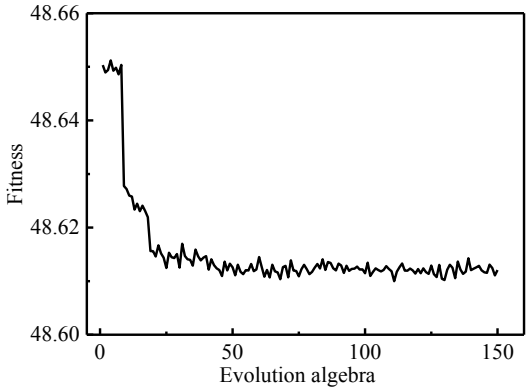


Figure 8. Fitness evolution curve.

Table 3: Comparison of the junction temperature and plastic work density before and after ACO-BPNN optimization.

	After ACO-BPNN	Before optimization	Percentage improvement by ACO-BPNN
Junction temperature T_j (°C)	89.5	89.83	0.37%
Plastic work density W (10^{-10}MPa)	2.39	5.1	53.14%

B. NSGA-II

Next, NSGA-II was used to optimize the RDL via size and it process is shown in Fig. 9 [4]. The NSGA-II algorithm can be used to obtain the Pareto front of thermal resistance R_k and energy density W_k.

The depth and diameter of the blind via were used as optimization variables. This study focused on the optimization of the steady-state thermal resistance and plastic work density. The multiobjective optimization mathematical model of power module packaging design is established, which can be expressed as:

$$\begin{cases} \min \quad R_k \\ \min \quad W_k \\ h_{\min} \le h \le h_{\max} \\ d_{\min} \le d \le d_{\max} \end{cases} . \tag{14}$$

where R_k is the thermal resistance of the blind via layer; W_k is the volume average inelastic working energy density; h is the depth of the blind via, and d is the diameter of the blind via.

NSGA-II was used to solve the problem. The NSGA-II calculation process is displayed in Fig. 9. The following parameters are set: optimal frontier individual coefficient 0.6, population size 100, and maximum iteration step 10 000. To ensure the convergence of the algorithm, the maximum number of iteration steps is set as the individual coefficient of the larger optimal front, which is defined as the proportion of the individual in the optimal front in the population. Its value range is 0–1, which only affects the presentation form of the solution, but does not affect the solution result and the population size. The coefficient is selected as 0.6, which can provide the Pareto multiobjective optimization pareto front [11, 12].

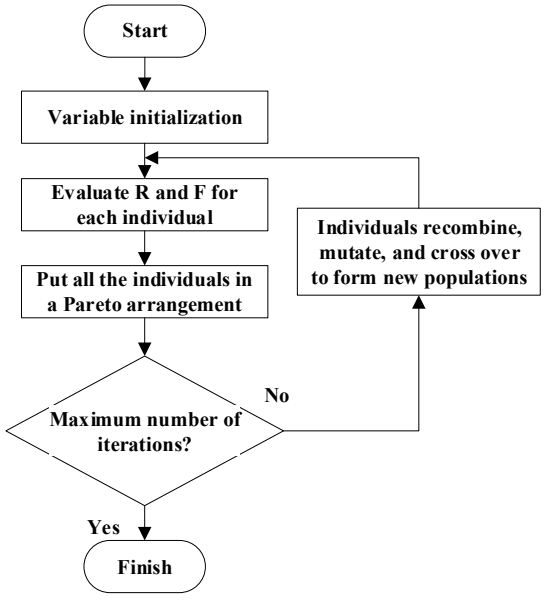
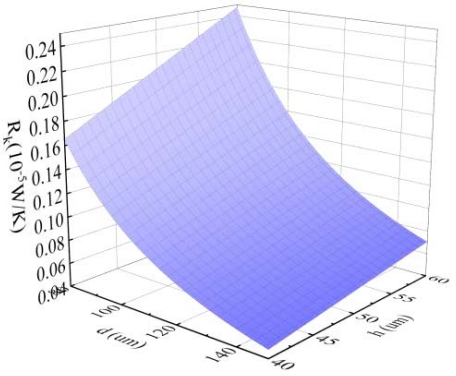
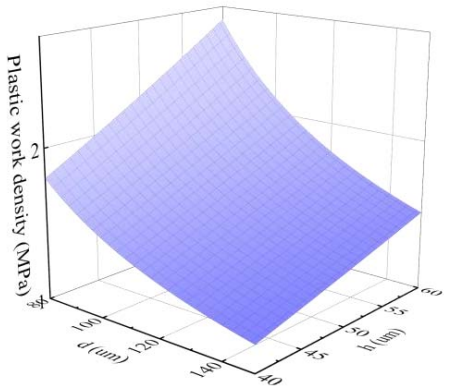


Figure 9. Flowchart of NSGA-II.

Fig. 10 shows the relationship between R_k, W_k and d, h. The optimal solution by the NSGA-II was obtained when d was 150 μm and h was 40 μm, which is the same as the results through ACO-BPNN optimization.



(a)



(b)

Figure 10. The surface contour of (a) R_k and (b) W_k.

V. Concluding Remarks

This study investigates the effect of the RDL via size on the thermal management and thermal cycling reliability of a designed FOPLP SiC MOSFET power module. Both ACO-BPNN and NSGA-II based genetic algorithms were proposed to optimize the RDL via size. The following conclusions can be drawn from the study: (1) The GA-assisted optimization methods proposed are simple in principle and exhibit excellent applicability, which can reduce the design cost and time of the SiC MOSFET power module during the prototyping process. (2) Both the ACO-BPNN and NSGA-II revealed that the optimal heat dissipation and plastic work density were obtained when the RDL via diameter and depth were 150 and 40 μm, respectively in the designed module. (3) Comparing to NSGA-II, ACO-BPNN can achieve the optimization without theoretical calculations, that will be more effective in optimize complex packaging structure.

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