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Single-Electron-Transistor Compact Model for Spin-Qubit Readout

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***Abstract*—Quantum computers process information stored in quantum bits (qubits), which must be controlled and read out by a traditional electronic interface. Co-designing and co-optimizing such a quantum-classical complex system requires efficient simulators to emulate the qubits and their interaction with classical electronics. For spin-qubit readout, a single electron transistor (SET) is often employed. To build a toolset that can co-simulate the spin qubit system with the classical control and readout interface, a compact and efficient SET model is needed. This paper presents a new compact empirical SET model based on state-of-the-art SET measurement and extracted by a custom function-fitting python program. Within the target source-drain voltage range of $\pm 1000 \mu V$, the model is accurate for circuit (SPICE) simulation. Furthermore, the empirical model is represented by a set of equations that enables instantaneous output response requiring a negligible simulation time. With this new SET model, a quantum-electronics co-simulator such as SPINE can now be enhanced to simulate the readout in addition to the control circuits of spin qubits, thus enabling the design of the complete integrated circuit (IC) required for large-scale quantum computers.**

***Index Terms*—nanoelectronics, quantum electronics, SET, spin qubit, quantum dots, readout, Macro-model**

I. Introduction

Quantum computers outperform classical computers in fields such as cryptography, search and optimization, and solving large systems of linear equations [1]. While a classical computer works with bits, quantum computers use quantum bits (qubits), which must be typically operated at cryogenic temperatures to exploit their quantum behavior.

At the core of the quantum computer, the qubits must be controlled and read out by a classical electronic interface. Although state-of-the-art quantum processors comprise over 100 qubits [2] [3], thousands or even millions of qubits are required to address relevant computational problems [4]. Spin qubits, in semiconductor quantum dots, have the advantage that they can be manufactured at a large scale with all-optical lithography, leveraged from conventional transistor fabrication while maintaining long coherence time and high fidelity [5]. Any quantum algorithm requires, in addition to single- and two-qubit operations, the measurement of the qubit state, which, for semiconductor spin qubits, is encoded in the spin of electrons or holes trapped in a quantum dot. The spin qubit's magnetic moment is too small to be detected directly. Therefore, a Single-Electron Transistor (SET) is typically employed to convert the spin information into a charge displacement in the quantum dot, such as in [6] [7], where the SET is capacitively connected to the quantum dot. The SET's impedance is measured to obtain the final outcome of the qubit measurement. Since SETs are typically also implemented as quantum dots, such readout occupies a very small silicon footprint on the same integrated circuit, thus promising an integrated readout in future quantum System-On-Chips (SoCs) [8]. Furthermore, for SET impedance readout, cryogenic CMOS (cryo-CMOS) circuits operating at temperatures close to the qubit's temperature can be placed next to the quantum dots, thus bypassing the wiring bottleneck otherwise limiting the scalability when employing room-temperature electronics.

CMOS technology offers the best scalability as required for readout circuits for large-scale quantum processors [9]. However, due to the limited cooling power available in cryogenic refrigerators, the CMOS circuits must dissipate minimum power while achieving the required performance. Therefore, a software toolset that co-simulates the classical electronic circuit together with the quantum system facilitates the development of control and readout circuits that meets the stringent performance requirements.

Towards that goal, we developed SPINE (Spin Emulator) [10], a software toolset in the Cadence environment to co-simulate CMOS control circuits with qubits. In this work, we augment SPINE by adding the co-simulation of spin-qubit readout, including an electrical SET model.

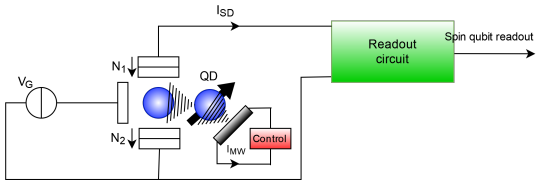

Fig. 1. An example of a readout system that is going to be simulated by SPINE.

An example of a readout and control schematic for a single spin qubit is in Fig. 1. I_{MW}, generated by the "Control" electronics, excites the spin qubit in the Quantum Dot (QD), the SET, placed in its proximity, detects the spin of the

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qubit based on the varying SET impedance and the readout electronics senses the current I_{sd} of the SET, thus resolving the spin state. In order to be able to simulate the readout scheme in Fig. 1, we developed a new compact SET model based on experimental SET data and implemented it in Verilog-A, which can be employed in electronic circuit simulators such as Spectre and is now used to extend SPINE with spin qubit readout functionality.

The paper is organized as follows. In section II, the theory of SET operation for spin qubit readout is briefly explained. Then, the methodology for extracting the parameters of the compact empirical SET model is introduced in Sec. III). Finally, Sec. V analyses the accuracy and performance of the SET model.

II. Single Electron Transistor Background

The SET has source, gate, and drain terminals, similar to the traditional MOS transistor. It also acts as a voltage-controlled current source but differs in that individual electrons tunnel through a quantum dot island [11]. A SET is a double barrier circuit containing two tunnel junctions with an island in between [11]. Tunneling through a barrier is dependent on the difference in chemical potential across the tunnel junction. The island's chemical potential can be tuned by varying the gate voltage. Tunneling can only happen when the island's chemical potential is within a narrow window, defined by the so-called Coulomb blockade, leading to current conduction only for specific conditions for the gate, source, and drain voltages. Fig. 2 shows a circuit representation of the SET, which includes the quantum dot in between two tunneling junctions, modeled by a capacitor and resistor. The gate is connected to the quantum dot via a capacitor. The two voltage sources, connected to the gate, V_g, and to the source, V_{sd}, are for biasing the SET; sweeping the two voltage sources will result in the stability plots of Fig. 3.

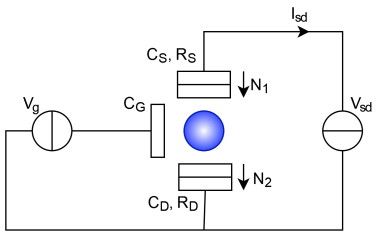

Fig. 2. Structure of a SET containing a quantum dot in the center, two tunneling junctions with its tunneling resistance and capacitance R_S, R_D and C_S, C_D. There is a capacitance at the gate denoted by C_G. Furthermore, voltage sources V_g and V_{sd} are for biasing the SET.

Stability diagrams are used to visually get an overview of how to bias a given SET with a certain Coulomb blockade structure, as shown in the diagram in Fig. 3. The periodic diamond shapes are called Coulomb diamonds. The boundaries are diagonal and not vertical lines due to capacitive coupling within the SET [12]. Ideally, inside the diamond, there is no current flowing, as the Coulomb blockade has not been overcome. Outside the diamonds, tunneling events are happening

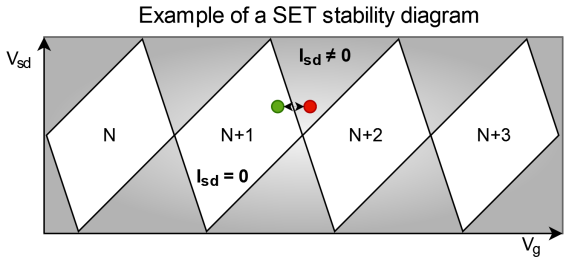

Fig. 3. Example of a stability diagram of a SET including a simplified biasing trajectory example for state $|1\rangle$ collapse. N is the number of energy levels that are occupied by an electron. Ideally, there is no tunneling when inside the diamond.

and therefore, current is flowing. Jumping to the next diamond is adding an electron to the island.

III. SET Empirical Model Methodology

A new SET model was developed for SPINE because of the absence of spin readout. In the absence of compact models, the Monte Carlo method is the most accurate but also the most time-consuming in terms of simulation time [13]. Fast Monte Carlo-based SET simulators exist, such as SIMON, but they are stand-alone applications not compatible to be integrated into circuit simulator environments such as Cadence [14]. Other models exploit the master-equation method or an equivalent circuit, which can be implemented in circuit simulators [13]. However, these physics-based models often neglect second-order effects that are relevant in real applications. For example, ideally, there is no current flowing inside the Coulomb diamond. However, real-world SET measurements show that there is a leakage current [15].

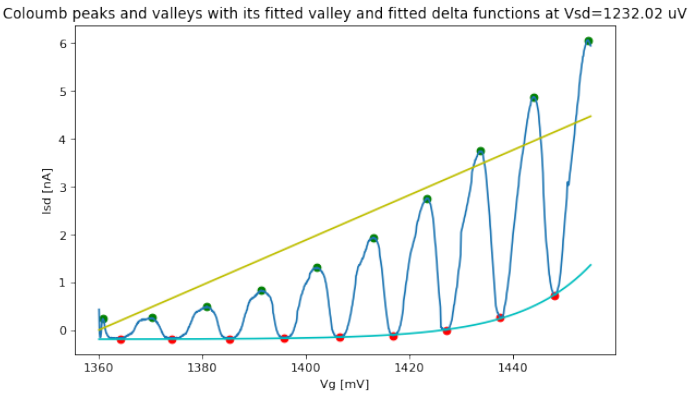

Fig. 4. The detected peaks, green, and valleys, red, of a V_{sd} slice with its fitted exponential valley function, cyan, and fitted linear delta function, yellow. The corresponding functions are in Eq. 2.

The proposed empirical model aims to reach a balance between accuracy and simulation time. The empirical SET simulation model is based on SET measurements corresponding to the stability plots in Fig. 5, and it can closely represent the SET's non-idealities, such as the offset current. The SET that is measured here is fabricated on an

$$\begin{bmatrix} a \\ b \\ c \\ d \end{bmatrix} = \begin{bmatrix} 0 & 0 & -7.164 \cdot 10^{-23}\mathrm{AV}^{-5} & 1.047 \cdot 10^{-19}\mathrm{AV}^{-4} & 1.443 \cdot 10^{-16}\mathrm{AV}^{-3} & -1.945 \cdot 10^{-13}\mathrm{AV}^{-2} & -8.007 \cdot 10^{-11}\mathrm{AV}^{-1} & -1.313 \cdot 10^{-7}\mathrm{A} \\ 0 & 0 & 0 & 1.387 \cdot 10^{-17}\mathrm{V}^{-3} & -5.965 \cdot 10^{-15}\mathrm{V}^{-2} & -2.636 \cdot 10^{-11}\mathrm{V}^{-1} & -3.613 \cdot 10^{-9} & 1.569 \cdot 10^{-3}\mathrm{V} \\ 0 & 0 & 0 & -2.161 \cdot 10^{-22}\mathrm{V}^{-3} & -2.185 \cdot 10^{-18}\mathrm{V}^{-2} & -1.449 \cdot 10^{-14}\mathrm{V}^{-1} & -1.195 \cdot 10^{-11} & 8.424 \cdot 10^{-8}\mathrm{V} \\ -6.091 \cdot 10^{-31}\mathrm{AV}^{-8} & 1.6022 \cdot 10^{-28}\mathrm{AV}^{-7} & 6.274 \cdot 10^{-24}\mathrm{AV}^{-6} & 1.112 \cdot 10^{-21}\mathrm{AV}^{-5} & -2.991 \cdot 10^{-17}\mathrm{AV}^{-4} & -8.827 \cdot 10^{-15}\mathrm{AV}^{-3} & 7.865 \cdot 10^{-11}\mathrm{AV}^{-2} & 8.979 \cdot 10^{-11}\mathrm{AV}^{-1} \end{bmatrix} \begin{bmatrix} V_{sd}^7 \\ V_{sd}^6 \\ V_{sd}^5 \\ V_{sd}^4 \\ V_{sd}^3 \\ V_{sd}^2 \\ V_{sd} \\ 1 \end{bmatrix} \quad (1)$$

The experimental data were examined and processed through machine learning using a custom curve fitting program in Python, from the SciPy library [17], which returns a set of equations function of V_g and V_{sd}, together with parameters fitted, to describe the measured SiGe SET with the least error. Equations 1 to 6 represent the empirical SET model. The model is based on the envelope principle, containing an offset current and modulated current as in Eq. 4.

Generating the equations from the experimental data goes through these stages:

1) Determine the peaks, valleys, duty cycle, and phase offset for each V_{sd} slice.
2) Function fit the valleys and the peaks-valleys for I_{offset} and $I_{amplitude}$. An exponential function with parameters a, b, and c, Eq. 2, is fitted through the valleys to determine I_{offset}, as exemplified in Fig. 4. The oscillation $I_{amplitude}$, i.e., the difference between the peaks and valleys is linearly fitted using the parameter d, Eq. 2.
3) Repeat and save the fitting for $>$ 1000 V_{sd} slices, $\Delta V_{sd} < 4\mu$V.
4) Plot the parameters with respect to V_{sd} and polynomial fit as a function of V_g. Additionally, plot the duty cycle and phase offset and fit them with line equations.
5) Construct the SET model by plugging in the parameter functions Eq. 1, 5 and, 6 in the core functions Eq. 2, 3 and 4.

The order of the polynomial fitting is optimized as a trade-off between high accuracy and overfitting. The resulting polynomial coefficients are shown in Eq. 1. For I_{offset}, ζ and η are experimental tuning coefficients bounded by $\zeta \leq 1\ \mathrm{A\,V}^{-1}$ and $\eta \leq 1$ V. The oscillatory behavior in I_{sd}, which is modeled by $f_{\text{modulation}}$ in Eq. 3, is a half-cosine function with duty cycle θ and phase ϕ, Eq. 5 and 6, which models the Coulomb diamond slopes. The θ and ϕ values are determined for each V_{sd} slice and are modeled with a linear fit as a function of V_{sd}.

$$I_{\text{offset}} = a + \zeta V_{sd} e^{\frac{(V_g - b) + c}{\eta}}, \quad I_{\text{amplitude}} = d(V_g - V_g[0]) \quad (2)$$

$$f_{\text{modulation}} = max\left(\frac{cos((6.0 \cdot 10^{-4}\mathrm{V}^{-1} V_g + \phi) - \frac{\theta}{2}) - cos(\frac{\theta}{2})}{1 - cos(\frac{\theta}{2})}, 0\right) \quad (3)$$

$$I_{\text{sd,model}} = I_{\text{offset}} + I_{\text{amplitude}} f_{\text{modulation}} \quad (4)$$

$$\theta = \begin{cases} -7.3 \cdot 10^{-10}\mathrm{V}^{-1} V_{sd} 2\pi & V_{sd} < 0 \\ 6.3 \cdot 10^{-10}\mathrm{V}^{-1} V_{sd} 2\pi & V_{sd} > 0 \end{cases} \quad (5)$$

$$\phi = \begin{cases} -3 + 8.0 \cdot 10^{-10}\mathrm{V}^{-1} V_{sd} & V_{sd} < 0 \\ -3 - 2.2 \cdot 10^{-9}\mathrm{V}^{-1} V_{sd} & V_{sd} > 0 \end{cases} \quad (6)$$

IV. SET EMPIRICAL MODEL RESULT

The final empirical SET model produces the 3D plot and stability diagram shown in Fig. 5. On visual inspection of the stability diagram, the model seems to deliver washed-out peaks at the extremes of V_{sd}, compared to the experimental data. This is due to the limitation of the modulation function, Eq. 3, as the duty cycle cannot go over 1 as it occurs in the SiGe SET. This is clearly visible in the Mean Squared Error (MSE) plot in Fig. 6. The accuracy diminishes significantly after $\pm 1000\mu V$, where the MSE [nA^2] increases quickly. The model's accuracy can be increased by expanding the modulation function for a duty cycle $>$ 1. For our application, we accept the V_{sd} region where the MSE is below 0.5 nA^2. For the target simulations, the SET's source-drain voltage biasing range is well below this value, thus the empirical model is suitable for readout simulations in SPINE. The set of equations is then implemented in Verilog-A as a module where coefficients are automatically updated via a script generator.

V. CONCLUSION

In this paper, we propose a novel compact empirical SET model based on a SiGe SET. A python function fitting program, utilizing machine learning, was developed to generate a final 3D equation, dependent on V_{sd} and V_g, that fits the SET measurement with the least error. Strategies such as peak and valley detection, envelope modeling, and polynomial fitting are used to acquire accurate source-drain current characteristics. The SET model's accuracy was estimated, by comparing the error with respect to the experimental data, that is compatible with the readout biasing range used when co-simulating the electronic-quantum interface in the Cadence environment. With this new SET model, full readout and control simulations for spin qubits, covering the quantum system and classical interface, can be developed, thus ultimately contributing to the design of the integrated circuits required for large-scale quantum processors.

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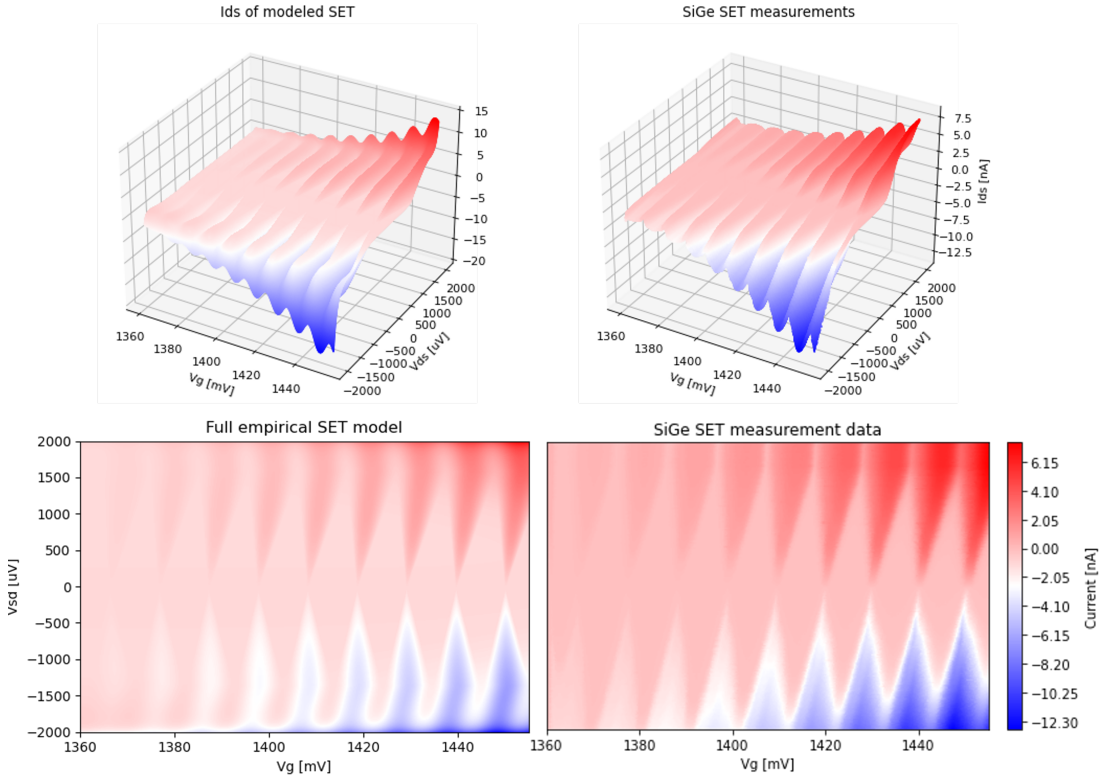

Fig. 5. The 3D and stability plots of the empirical SET model and SiGe SET side by side.

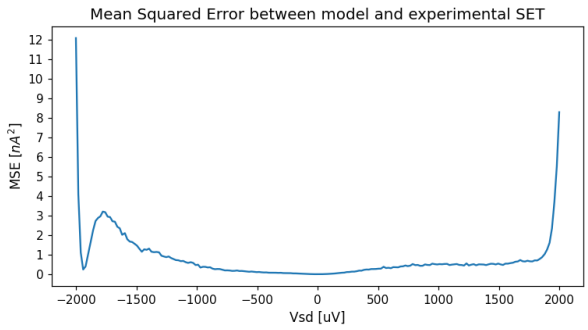

Fig. 6. Mean squared error plot between the modeled and experimental SET. At the extremes of V_{ds}, the model seems to stray away the most from the SET.

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