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DOI [10.1109/TCSII.2023.3342114](https://doi.org/10.1109/TCSII.2023.3342114)

Publication date 2023

Document Version Final published version

Published in IEEE Transactions on Circuits and Systems II: Express Briefs

#### Citation (APA)

Mahmoud, A. N., Ciubotaru, F., Vanderveken, F., Adelmann, C., Cotofana, S., & Hamdioui, S. (2023). Two Cascaded Spin Wave Majority Gates Operation Under Continuous and Pulse Modes. IEEE Transactions on Circuits and Systems II: Express Briefs, 71(4), 1919-1923. <https://doi.org/10.1109/TCSII.2023.3342114>

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# Two Cascaded Spin Wave Majority Gates Operation Under Continuous and Pulse Modes

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*Abstract***—Spin Waves (SWs), by their nature, are excited by means of voltage driven or current driven cells under two modes: Continuous Mode Operation (CMO), and Pulse Mode Operation (PMO). Moreover, the low throughput of the SW technology (caused by its high latency) can be enhanced by wavepipelining which is supported inherently by the SW under the two modes. Therefore, we propose wavepipelined SW based two cascaded Majority gates (SWMGs) circuit and validate it by means of micromagnetic simulations working under CMO and PMO. Our evaluation results indicate that PMO SWMGs circuit consumes 6***.***7x less energy than CMO SWMGs circuit. In addition, the evaluation shows that the wavepipelined PMO and CMO SWMGs circuit have the same throughput, while they are better than the non-wavepipelined circuit by 2x.**

*Index Terms***—Spin-waves, spin-wave computing, cascaded majority gates, wave pipeline, throughput, energy.**

#### <span id="page-2-1"></span><span id="page-2-0"></span>I. INTRODUCTION

**I**N THE last decades, information technology has seen a revolution resulting in the need to process increasingly revolution resulting in the need to process increasingly extensive data [\[1\]](#page-6-0). The energy consumption per processing operation is a key parameter that needs to be minimized using highly efficient computing platforms to reduce both the environmental footprint and cost. In the past, downscaling complementary metal-oxide-semiconductor (CMOS) devices has been the pathway to an enormous increase of the computing throughput  $[1]$ ,  $[2]$ . However, this has led to an increased power density. Consequently, further dimensional scaling are becoming increasingly limited because of device power consumption and heating; not to mention the economical and reliability concerns [\[3\]](#page-6-2). As a result, researchers have investigated alternatives to CMOS such as graphene devices  $[4]$ , memristors  $[5]$ , and spintronics  $[6]$ .

<span id="page-2-4"></span><span id="page-2-3"></span><span id="page-2-2"></span>In particular, spintronic approaches have recently gained much interest due to their potential to operate at very

Manuscript received 9 May 2023; revised 11 September 2023 and 14 November 2023; accepted 10 December 2023. Date of publication 12 December 2023; date of current version 27 March 2024. This work was supported by the European Union's Horizon 2020 Research and Innovation Program within the FET-OPEN Project CHIRON under Grant 801055. This brief was recommended by Associate Editor X. Miao. *(Corresponding author: Abdulqader Nael Mahmoud.)*

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<span id="page-2-7"></span><span id="page-2-6"></span>low power [\[7\]](#page-6-6) and the demonstration of scalable magnetic memories [\[8\]](#page-6-7). In particular, magnonic technologies that use spin waves (SWs), wavelike collective excitations of local magnetic moments in a ferromagnetic or antiferromagnetic material, as information carriers, have received attention for ultralow power scalable logic circuit [\[9\]](#page-6-8), [\[10\]](#page-6-9), [\[11\]](#page-6-10), [\[12\]](#page-6-11), [\[13\]](#page-6-12), [\[14\]](#page-6-13), [\[15\]](#page-6-14), [\[16\]](#page-6-15), [\[17\]](#page-6-16), [\[18\]](#page-6-17), [\[19\]](#page-6-18). Given the properties, researchers have realized the importance of this technology to the next level and develop logic gates and circuits.

<span id="page-2-12"></span><span id="page-2-11"></span><span id="page-2-10"></span><span id="page-2-9"></span><span id="page-2-8"></span>Different magnonic logic gates have been suggested and experimentally realized. A particular focus has been on spin-wave majority gates (SWMGs) at the conceptual level  $[20]$ , at the simulation level  $[21]$ , and at the experimental level [\[11\]](#page-6-10), [\[22\]](#page-6-21), mainly for two reasons: first, SW, inherently, provides intrinsic support for Majority logic function as the interference of odd number of waves results in a Majority decision; i.e., if the number of logic 1 waves are larger than the number of logic 0 waves then the resultant wave is logic 1, and otherwise, logic 0 [\[12\]](#page-6-11). Second, Majority gates (in addition to the inverter) constitute a universal Boolean logic gate set; i.e.; it provides the foundation for the potential implementation of complex SW circuits such as full adder [\[23\]](#page-6-22). Moreover, AND gate can be built from Majority gate by fixing one of the inputs to logic 0 while OR gate can be built by fixing one of the inputs to logic 1 [\[19\]](#page-6-18). Beyond logic gates, SW circuits have also recently been studied both at the conceptual level [\[16\]](#page-6-15) as well as by micromagnetic simulations  $[18]$ , and even cascading schemes have been reported in order to achieve complex circuits [\[19\]](#page-6-18). A unique feature of wave-based computing schemes is the possibility for parallelism and frequencydivision multiplexing by the independent propagation of SWs at multiple frequencies in the same waveguide [\[13\]](#page-6-12). This is possible in the regime of linear magnetic response, where inelastic interactions between SW are negligible. Despite this, SW technology is still developing technology and more complex circuits and wavepipelining investigation are highly desired.

<span id="page-2-5"></span>This brief advances the state-of-the-art by proposing an energy efficient and high throughput SW pipelined two cascaded Majority gate; both the continuous mode as well as pulse mode for excitation have been explored. The main contributions of this brief can be summarised as follows:

- Design: SW pipelined two cascaded Majority gates circuit (SWMGs) is proposed to evaluate the Continuous Mode Operation (CMO) and Pulse Mode Operation (PMO) in terms of energy and throughput.
- Validation: The correct functionality of the SWMGs has been validated by means of micromagnetic simulations.
- Evaluation: SWMGs performance has been evaluated in terms of energy and throughput. CMO SWMGs

Digital Object Identifier 10.1109/TCSII.2023.3342114

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<span id="page-3-1"></span>Fig. 1. a) Schematic of the studied cascaded SWMGs. b) Dispersion relation of backward volume spin-wave propagating in 50 nm wide and 1 nm thick  $Fe_{60}Co_{20}B_{20}$  waveguide with magnetic saturation  $M_s = 1.1$  MA/m, exchange stiffness  $A_{ex} = 18.5$  pJ/m, and damping constant  $\alpha = 2.5 \times 10^{-3}$ . No external field is applied as the shape anisotropy is strong enough to push the magnetization in the plane along the waveguide length. c) The resulting group velocity as a function of SW wavevector.

consumes 6.7x more energy consumption compared to PMO SWMGs due to continuous wave excitation in CMO, but the circuit periphery is less complex because CMO does not require shaping of the input signals as in PMO. In addition, the throughput is enhanced by a factor of 2 by realizing the wavepipelining in the CMO and PMO.

The rest of this brief is organized as follows. Section [II](#page-3-0) describes the proposed cascaded Majority gates circuit. Section [III](#page-4-0) presents the simulation setup, and Section [IV](#page-4-1) presents the simulation results. Section [V](#page-5-0) evaluates the performance. Section [VI](#page-6-23) concludes this brief.

#### <span id="page-3-2"></span><span id="page-3-0"></span>II. TWO CASCADED SPIN-WAVE MAJORITY GATES

Figure [1](#page-3-1) a) presents a schematic of two cascaded SWMGs, based on the design in [\[21\]](#page-6-20), [\[24\]](#page-6-24). Coherent SWs or SW wavepackets are generated at the 5 inputs  $I_1$  to  $I_5$  and subsequently propagate in the magnetic waveguides. Traditionally, SW is generated by applying a continuous signal with identical amplitude, frequencies and wavelengths at the inputs. When binary information is encoded in the phase of the waves (logic 0 and 1 corresponding to phases of 0 and  $\pi$ , respectively), their interference leads in a natural way to the computation of the majority function. The device is designed so that inputs *I*2, *I*3, and *I*<sup>4</sup> form a first majority gate, resulting in an output wave  $M_1$  with phase  $\phi_{M1} = MAJ(\phi_{I2}, \phi_{I3}, \phi_{I4})$ . The output wave then propagates towards a second majority gate with a resulting wave *O* with phase  $\phi_O = MAJ(\phi_{I1}, \phi_{M1}, \phi_{I5})$ . The operation principle of the two cascaded SW Majority Gates is as follows: Initially, *I*1,*I*2,*I*3,*I*4,*I*<sup>5</sup> excite SWs which propagate through the waveguides. After that, SW excited at *I*<sup>3</sup> and *I*<sup>4</sup> interfere constructively or destructively depending on their phase. Then, the resultant SW propagates to interfere with the SW excited at *I*2. Next, the result propagates to interfere with the SWs excited at  $I_1$ , and  $I_5$ . Finally, the resultant SW is detected at *O* based on phase detection, in which the captured SW is compared with a predefined phase; i.e., if the detected SW has a phase of 0, the output *O* is logic 0, and if the detected SW has a phase of  $\pi$ , the output *O* is logic 1.

However, SWMGs cannot be directly cascaded in a straightforward way since the large output amplitude of a first majority gate can dominate the interference in a subsequent one and lead to computing errors. Concretely, if all inputs are excited at the same amplitude, logic inputs of  $(I_1, I_2, I_3, I_4, I_5) = (1, 0, 0, 0, 1)$  lead to a logic output of  $O = 0$ instead of the correct result of  $O = 1$  [\[19\]](#page-6-18), [\[25\]](#page-6-25). To ensure that waves interferences for the above mentioned cases lead in all cases to correct output, the SWs at  $I_1$  and  $I_5$  should be excited with amplitude 2*A* each, while those of *I*2,*I*3, and *I*<sup>4</sup> each at *A* only. However, we found out from micromagnetic simulations that different inputs contribute differently to the output due to the scattering and reflection. Note that the energy loss is determined from micromagnetic platform (MuMax3) simulations by activating each input separately and determine the amount of energy at the output. For example, 27% of the excited spin wave energy at  $I_1$  and  $I_5$  reaches the output while the other 73% lost in the damping, scattering and reflection, whereas  $54\%$  of the excited spin wave energy at  $I_2$  reaches the output while the other 46% lost in the damping, scattering and reflection, and it has the highest contribution as there are two directions to propagate when reached to the main waveguide, while the  $I_1$  and  $I_5$  spin waves have three directions. Moreover, 18% of the excited spin wave energy at *I*<sup>3</sup> and *I*<sup>4</sup> reaches the output while the other 84% lost in the damping, scattering and reflection, and it contributed the least to the output as it has multiple directions to propagate to  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_5$ . Thus,  $I_1$ and  $I_5$  excite SWs with amplitude of 1A,  $I_2$  with amplitude of 0.25*A*, and  $I_3$  and  $I_4$  with amplitude of 0.75*A*.

Moreover, the structure dimensions must be chosen accurately to reflect the required functionality. For example, if the desired functionality for the SWs is to interfere constructively, if they have the same phase, whereas interfere destructively if they are out-of-phase, then the dimensions  ${d_1, d_2, d_3, d_4, d_5} = n\lambda$ , where  $n = 0, 1, 2, \dots$  and  $\lambda$  is the SW wavelength, which is the case for our design. In addition, the output must be detected at accurate location depending on the desired output if the output itself or its inverted version. If the inverted version is the desired one,  $d_6$  must be  $(n+1/2)\lambda$ . In contrast, if the desired output is the logic circuit output itself, then  $d_6$  must be  $n\lambda$ , which is the case in our design.

In case of applying a continuous wave at the inputs at the Continuous Mode Operation (CMO), the overall energy consumption is mainly determined by the transducer power and the gate critical path length (delay). This implementation results in a high energy consumption as SW is slow; this will be assessed and discussed in Section [V.](#page-5-0) In contrast, exciting SW by applying a pulse wave (at the Pulse Mode Operation (PMO)) is more energy efficient as the overall energy consumption will be determined by the transducer power and the pulse duration.

<span id="page-3-4"></span><span id="page-3-3"></span>One of the limitations of the SW technology is its slowness, resulting in low throughput. To deal with this, wavepipelining can be used; it handles multiple inputs' sets before the result of the first set is detected at the output without using registers or isolaters between the pipelined stages [\[26\]](#page-6-26). Spin wave has an intrinsic support for wavepipelining. We utilize the structure in Figure [1a](#page-3-1)) to illustrate the SW wavepipelining



<span id="page-4-2"></span>Fig. 2. Magnetization dynamics of 70 ps rectangular pulse excitation SW propagating in a) time domain, and b) frequency domain, 300 ps 15 GHz sinusoidal pulse excitation SW propagating in c) time domain, and d) frequency domain, and c) 300 ps 15 GHz gaussian pulse excitation SW propagating in i) time domain, and ii) frequency domain.

principle for both modes CMO and PMO. The aforementioned operation principle holds true for this case but with exciting multiple SW's sets distanced by a certain time gap. This time gap is determined such that each set does not affect the other excited sets for both modes. This allows for multiple SWs sets to co-exist in the waveguide without affecting each other, interfere properly at each intersection point between the waveguides, and detect the resultant SW for each set at the output. The throughput enhancement of such implementation will be assessed and discussed in Section [V.](#page-5-0)

#### <span id="page-4-3"></span>III. SIMULATION SETUP

<span id="page-4-0"></span>Micromagnetic simulations have been performed using the GPU-accelerated software MuMax3 [\[27\]](#page-6-27). In MuMax3, we utilized 50 nm wide and 1 nm thick  $Fe_{60}Co_{20}B_{20}$  waveguide with magnetic saturation  $M_s$ =1.1 MA/m, exchange stiffness *A<sub>ex</sub>*=18.5 pJ/m, and damping constant  $\alpha = 2.5 \times 10^{-3}$  [\[28\]](#page-6-28). Note that no external field is applied as the shape anisotropy is strong enough to push the magnetization in the plane along the waveguide length. This configuration allows the propagation of backward volume spin waves. The backward volume wave dispersion relation and SW group velocity were extracted for these parameters from MuMax3 simulation, and their graphs are presented in Figure [1](#page-3-1) b) and Figure [1](#page-3-1) c), respectively. In order to minimize the structure size, and maximize the throughput, we chose a frequency of 15 GHz, which makes wavelength  $2pi/k = 2pi/70$  rad/ $\mu$ m = 90nm. Since the dispersion sets the device dimensions, the dimensions were determined as follows:  $d_1 = 180$  nm,  $d_2 = 540$  nm,  $d_3 = 360$  nm,  $d_4 = 360 \text{ nm}, d_5 = 900 \text{ nm}, \text{ and } d_6 = 900 \text{ nm}.$  In addition, the inclined angle of the waveguides (in reference with the main waveguide) is 20<sup>o</sup>. Moreover, the overall size of the structure is  $1700nm \times 1700nm$ , which can be scaled down by changing the inclined angle, decreasing the size of the waveguides, and detecting the output at nearer position.

As mentioned previously, two excitation modes have been investigated: CMO and PMO. While CMO excites a single frequency SW as a result of the continuous excitation of the SW, the PMO excites multiple frequencies SW, which requires careful generation of the pulse. In order to properly choose the pulse which generates the desired results, we excited a SW at a single in-line waveguide using three different pulse signals: i) Rectangular pulse of 70 ps duration, ii) Sinusoidal pulse of 300 ps and 15 GHz carrier frequency, iii) Gaussian pulse  $\sigma = 300 \text{ ps}$  and 15 GHz carrier frequency. Figure [2](#page-4-2) presents the magnetization dynamics of the pulse propagation in a waveguide in time and frequency (Fast Fourier Transform (FFT) of the propagated pulse) domains.

*Results Related to Rectangular Pulse:* Figure [2](#page-4-2) a) and Figure [2](#page-4-2) b) show strong signal deformation in generated rectangular pulse due to the spin-wave dispersion. Moreover, shorter pulse generates broad frequency ranges that make very difficult to build logic functions based on interference using this kind of pulses.

*Results Related to Sinusoidal Pulse:* Figure [2](#page-4-2) c) and Figure [2](#page-4-2) d) show that although sinusoidal pulse improves the magnetization dynamics, multiple frequencies SWs are still excited; this makes such pulse also not efficient to build logic functions.

*Results Related to Gaussian Pulse:* Figure [2](#page-4-2) e) and Figure [2](#page-4-2) f) show that gaussian pulse filtered out all other undesired frequencies and just excited the desired 15 GHz frequency SW. As a result, shaping the input pulse signal is required to limit the frequency range. Therefore, we chose to excite the SWs at  $I_1$ ,  $I_2$ ,  $I_3$ ,  $I_4$ , and  $I_5$  using gaussian pulse  $\sigma = 300$  ps and 15 GHz carrier frequency under the PMO.

#### IV. SIMULATION RESULTS

#### <span id="page-4-1"></span>*Wavepipelining Through CMO Phase Jump Simulation Results*

First, we excited an input and made a  $2\pi$  phase jump from phase 0 to phase  $\pi$  to phase 0. We utilized a reference signal of phase 0 to compare the resultant SW as presented in Figure [3](#page-5-1) a). As it can be observed from the figure,  $2\pi$ phase jump is performed after 1 ns to avoid any distortion of the signal as the transient regime duration is approximately 0.3 ps, and the full synchronization duration is about 0.6 ns. Therefore, wavepipelining is limited by nearly full synchronization. Subsequently, the wave pipelining was performed using CMO by continuous wave excitation at the inputs and phase jump of  $2\pi$  when needed at repetition rate of 1 ns. In order to validate it, we utilized 8 inputs combinations; i.e.,  ${I_1, I_2, I_3, I_4, I_5} = {0, 0, 0, 0, 0}, {1, 1, 1, 1, 1}, {0, 0, 0, 0, 1},$  $\{1, 0, 0, 0, 1\}, \{0, 0, 0, 1, 0\}, \{0, 0, 1, 0, 0\}, \{0, 1, 0, 0, 0\},$ 

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<span id="page-5-1"></span>Fig. 3. a) Continuous wave operation with  $2\pi$  phase jump, b) continuous wave wavepipeline operation with  $2\pi$  phase jump at 1 ns repetition rate.



<span id="page-5-2"></span>Fig. 4. Pulsed wave wavepipeline operation with  $2\pi$  phase change at 1 ns repetition rate in a) time domain, and b) space domain.

and  $\{1, 1, 0, 1, 1\}$ . Consequently, the first set is excited at 0 ns, the second set is excited at 3.5 ns to avoid any initial effect, the third set is excited at  $4.5 \text{ ns}, \ldots$ , the eighth set is excited at 9.5 ns. Figure [3](#page-5-1) b) presents the MuMax3 simulation results for CMO wavepipelinig. In order to validate the results, we made use of reference signal, which is the resultant SW of  ${I_1, I_2, I_3, I_4, I_5} = {0, 0, 0, 0, 0}$ . As depicted in the figure, the first SW set result is obtained at the window time of 3.45 ns-3.7 ns which have phase difference of 0 with the reference signal, thus the output  $O$  is logic 0. In contrast, the second SW set result is obtained at the window time of 4.45 ns to 4.7 ns which have phase difference of  $\pi$  with the reference signal, thus the output *O* is logic 1. Likewise the other cases can be analysed, the output O is logic 0 for the cases  $\{0, 0, 0, 0, 1\}$ , {0, 0, 0, 1, 0}, {0, 0, 1, 0, 0}, and {0, 1, 0, 0, 0}, whereas the output *O* is 1 for  $\{1, 0, 0, 0, 1\}$ , and  $\{1, 1, 0, 1, 1\}$  as can be observed from Figure [3](#page-5-1) b), which are the correct result of the SWMGs.

#### *Wavepipelining Through PMO Phase Change Simulation Results*

Figure [4](#page-5-2) presents the simulation results for PMO wavepipeling in time and space domains where pulse signals are exciting the SW at the inputs and phase change of  $2\pi$  when needed at repetition rate of 1 ns. In order to validate it, we utilized the same 8 inputs combinations as in CMO and a reference signal, which is the resultant SW of  $\{I_1, I_2, I_3, I_4, I_5\} = \{0, 0, 0, 0, 0\}.$ The first SW set output is detected at the window time of 2.15 ns-2.65 ns which have a phase difference of 0 with the reference SW thus the output *O* is logic 0 as depicted in Figure [4](#page-5-2) a). One can also see the 0 phase difference in the space domain as presented in Figure [4](#page-5-2) b). Moreover, the second SW set output is detected at the window time of 3.15 ns-3.65 ns which have a phase difference of  $\pi$  with the reference SW thus the output  $O$  is logic 1 as presented in Figure [4](#page-5-2) a). In addition, the  $\pi$  phase difference can be noticed in the space domain in Figure [4](#page-5-2) b). Likewise, the other cases can be analysed, the output *O* is logic 0 for the cases  $\{0, 0, 0, 0, 1\}, \{0, 0, 0, 1, 0\}, \{0, 0, 1, 0, 0\}, \text{and } \{0, 1, 0, 0, 0\},\$ whereas the output *O* is 1 for  $\{1, 0, 0, 0, 1\}$ , and  $\{1, 1, 0, 1, 1\}$ as can be observed from Figure [4,](#page-5-2) which are the correct result.

#### <span id="page-5-0"></span>V. PERFORMANCE EVALUATION

In order to assess both modes CMO and PMO, we compare them in term of energy consumption. To determine the energy consumption, the power and the SW propagation delay must be estimated. The SW propagation delay is determined from micromagnetic simulations to be 2 ns. The power consumption Authorized licensed use limited to: TU Delft Library. Downloaded on April 08,2024 at 12:44:54 UTC from IEEE Xplore. Restrictions apply.

is mainly determined by the transducer assuming very small power consumption by SW propagation through waveguides as SW doesn't require electron movement and just electron spinning. Therefore, energy consumption of the cascaded Majority gates circuit for single operation can be identified by  $N \times P \times t$ , where N is the number of transducer, P is the power consumption of single transducer, and *t* is the operation time for the circuit per process. Note that the operation time for the CMO is the same as the propagation delay which is 2 ns, whereas the operation time for the PMO is the excitation pulse duration which is 300 ps. We make use of a 34 nW power consumption of a single ME transducer [\[17\]](#page-6-16), [\[23\]](#page-6-22). CMO results in an energy consumption of  $6 \times 34 \times 2$  aJ as the source is active for 2 ns and there are 6 transducers, whereas PMO induces a  $6 \times 34 \times 0.3$  aJ energy consumption as the source is active for 300 ps and there are 6 transducers. As a result, CMO consumes 6.7x more energy consumption compared to PMO due to continuous wave excitation in CMO. Note that due to the early stage development of the transducer, we excluded the needed external CMOS circuitry for both CMO and PMO at the input and output from the power consumption calculation, and we kept the power consumption estimation in the magnonic domain. However, it is expected that the circuit peripheries of the CMO excitation and detection are potentially less complex because CMO does not require the shaping of the input signals as in PMO.

In order to evaluate the SW wavepipelining potential, we compare the circuit throughput without wave-pipelining, with wave-pipelining through CMO, and with wavepipelining through CMO. For the proposed cascaded Majority gates circuit, if we write each input and wait until the resultant SW is detected at the output, each operation will require 2 ns. Therefore, if we want to process 8 SW sets, then the not wavepipelined sets can be processed in 16 ns. On the other hand, the 8 SW sets can be processed in 8 ns if wavepipelining through CMO or PMO is utilized as can be observed in Figure  $3$  b) and  $4$  a). Therefore, utilizing wavepipelining to process 8 SW sets for the proposed cascaded Majority gates improve the throughput by 2.

#### VI. CONCLUSION

<span id="page-6-23"></span>A wavepipelined Spin Wave (SW) cascaded Majority gates circuit was proposed and validated under two modes: Continuous Mode Operation (CMO) and Pulse Mode Operation (PMO) by means of micromagnetic simulations. Shaping the input pulse signal is required to limit the frequency range and achieve a higher throughput as shorter pulse generates broad frequency ranges. Our evaluation indicated that CMO cascaded Majority gates circuit consumes more energy than PMO cascaded Majority gates circuit due to continuous wave excitation. However, the CMO circuit periphery is potentially less complex because it does not require the shaping of the input signals as in the pulse wave excitation. Moreover, wavepipelining under CMO and PMO have the same throughput, where the CMO wavepipelining was performed through phase jump while PMO wavepipelining was done by phase change, while they improved the throughput of the nonwavepipelined cascaded Majority gates circuit.

#### **REFERENCES**

<span id="page-6-0"></span>[\[1\]](#page-2-0) N. D. Shah, E. W. Steyerberg, and D. M. Kent, "Big data and predictive analytics: Recalibrating expectations," *JAMA*, vol. 320, no. 1, pp. 27–28, 2018.

- <span id="page-6-1"></span>[\[2\]](#page-2-1) S. Agarwal et al., "International roadmap of devices and systems 2017 edition: Beyond CMOS chapter," Sandia Nat. Lab.(SNL-NM), Albuquerque, NM, USA, Rep. SAND2018-3550R, 2018. [Online]. Available: https://irds.ieee.org/images/files/pdf/2017/2017IRDS\_BC.pdf
- <span id="page-6-2"></span>[\[3\]](#page-2-2) D. Mamaluy and X. Gao, "The fundamental downscaling limit of field effect transistors," *Appl. Phys. Lett.*, vol. 106, no. 19, 2015, Art. no. 193503.
- <span id="page-6-3"></span>[\[4\]](#page-2-3) Y. Jiang, N. C. Laurenciu, H. Wang, and S. D. Cotofana, "Graphene nanoribbon based complementary logic gates and circuits," *IEEE Trans. Nanotechnol.*, vol. 18, no. 1, pp. 287–298, Mar. 2019.
- <span id="page-6-4"></span>[\[5\]](#page-2-4) F. Corinto, A. Ascoli, and M. Gilli, "Nonlinear dynamics of memristor oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 6, pp. 1323–1336, Jun. 2011.
- <span id="page-6-5"></span>[\[6\]](#page-2-5) P. J. Rajput, S. U. Bhandari, and G. Wadhwa, "A review on—Spintronics an emerging technology," *Silicon*, vol. 14, pp. 9195–9210, Jan. 2022.
- <span id="page-6-6"></span>[\[7\]](#page-2-6) S. Manipatruni et al., "Scalable energy-efficient magnetoelectric spin– orbit logic," *Nature*, vol. 565, no. 7737, pp. 35–42, 2019.
- <span id="page-6-7"></span>[\[8\]](#page-2-7) W. J. Gallagher and S. S. P. Parkin, "Development of the magnetic tunnel junction MRAM at IBM: From first junctions to a 16-Mb MRAM demonstrator chip," *IBM J. Res. Devel.*, vol. 50, no. 1, pp. 5–23, Jan. 2006.
- <span id="page-6-8"></span>[\[9\]](#page-2-8) A. Barman et al., "The 2021 magnonics roadmap," *J. Phys. Condens. Matter.*, vol. 33, no. 41, 2021, Art. no. 413001.
- <span id="page-6-9"></span>[\[10\]](#page-2-8) A. Mahmoud et al., "Introduction to spin wave computing," *J. Appl. Phys.*, vol. 128, no. 16, 2020, Art. no. 161101. [Online]. Available: https://doi.org/10.1063/5.0019328
- <span id="page-6-10"></span>[\[11\]](#page-2-8) F. Ciubotaru et al., "First experimental demonstration of a scalable linear majority gate based on spin waves," in *Proc. IEEE Int. Electron Devices Meet. (IEDM)*, 2018, pp. 36.1.1–36.1.4.
- <span id="page-6-11"></span>[\[12\]](#page-2-8) A. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdiou, and S. Cotofana, "Fan-out enabled spin wave majority gate," *AIP Adv.*, vol. 10, no. 3, 2020, Art. no. 035119. [Online]. Available: https://doi.org/10.1063/1.5134690
- <span id="page-6-12"></span>[\[13\]](#page-2-8) A. N. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdioui, and S. Cotofana, "Multifrequency data parallel spin wave logic gates," *IEEE Trans. Magn.*, vol. 57, no. 5, pp. 1–12, May 2021.
- <span id="page-6-13"></span>[\[14\]](#page-2-8) A. Khitun, "Multi-frequency magnonic logic circuits for parallel data processing," *J. Appl. Phys.*, vol. 111, no. 5, 2012, Art. no. 054307. [Online]. Available: https://doi.org/10.1063/1.3689011
- <span id="page-6-14"></span>[\[15\]](#page-2-8) A. Khitun, "Magnonic holographic devices for special type data processing," *J. Appl. Phys.*, vol. 113, no. 16, 2013, Art. no. 164503.
- <span id="page-6-15"></span>[\[16\]](#page-2-8) A. Khitun et al., "Non-volatile magnonic logic circuits engineering," *J. Appl. Phys.*, vol. 110, no. 3, 2011, Art. no. 034306.
- <span id="page-6-16"></span>[\[17\]](#page-2-8) O. Zografos et al., "Wave pipelining for majority-based beyond-CMOS technologies," in *Proc. DATE*, 2017, pp. 1306–1311.
- <span id="page-6-17"></span>[\[18\]](#page-2-8) T. Brächer and P. Pirro, "An analog magnon adder for all-magnonic neurons," *J. Appl. Phys.*, vol. 124, no. 15, 2018, Art. no. 152119.
- <span id="page-6-18"></span>[\[19\]](#page-2-8) A. N. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Cotofana, and S. Hamdioui, "Spin wave normalization toward all magnonic circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 1, pp. 536–549, Jan. 2021.
- <span id="page-6-19"></span>[\[20\]](#page-2-9) G. Csaba, Á. Papp, and W. Porod, "Perspectives of using spin waves for computing and signal processing," *Phys. Lett. A*, vol. 381, no. 17, pp. 1471–1476, 2017.
- <span id="page-6-20"></span>[\[21\]](#page-2-10) S. Klingler, P. Pirro, T. Brächer, B. Leven, B. Hillebrands, and A. V. Chumak, "Spin-wave logic devices based on isotropic forward volume magnetostatic waves," *Appl. Phys. Lett.*, vol. 106, no. 21, 2015, Art. no. 212406.
- <span id="page-6-21"></span>[\[22\]](#page-2-11) T. Fischer et al., "Experimental prototype of a spin-wave majority gate," *Appl. Phys. Lett.*, vol. 110, no. 15, Apr. 2017, Art. no. 152401.
- <span id="page-6-22"></span>[\[23\]](#page-2-12) A. Mahmoud, F. Vanderveken, F. Ciubotaru, C. Adelmann, S. Cotofana, and S. Hamdioui, "Spin wave based full adder," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2021, pp. 1–5.
- <span id="page-6-24"></span>[\[24\]](#page-3-2) S. Klingler, P. Pirro, T. Brächer, B. Leven, B. Hillebrands, and A. V. Chumak, "Design of a spin-wave majority gate employing mode selection," *Appl. Phys. Lett.*, vol. 105, no. 15, 2014, Art. no. 152410.
- <span id="page-6-25"></span>[25] Q. Wang, P. Pirro, R. Verba, A. Slavin, B. Hillebrands, and A. V. Chumak, "Reconfigurable nanoscale spin-wave directional coupler," *Sci. Adv.*, vol. 4, no. 1, 2018, Art. no. e1701517.
- <span id="page-6-26"></span>[\[26\]](#page-3-3) L. W. Cotten, "Maximum-rate pipeline systems," in *Proc. Spring Joint Comput. Conf.*, 1969, pp. 581–586.
- <span id="page-6-27"></span>[\[27\]](#page-3-4) A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, "The design and verification of MuMax3," *AIP Adv.*, vol. 4, no. 10, 2014, Art. no. 107133.
- <span id="page-6-28"></span>[\[28\]](#page-4-3) T. Devolder et al., "Time-resolved spin-torque switching in MgO-based perpendicularly magnetized tunnel junctions," *Phys. Rev. B*, vol. 93, Jan. 2016, Art. no. 024420.