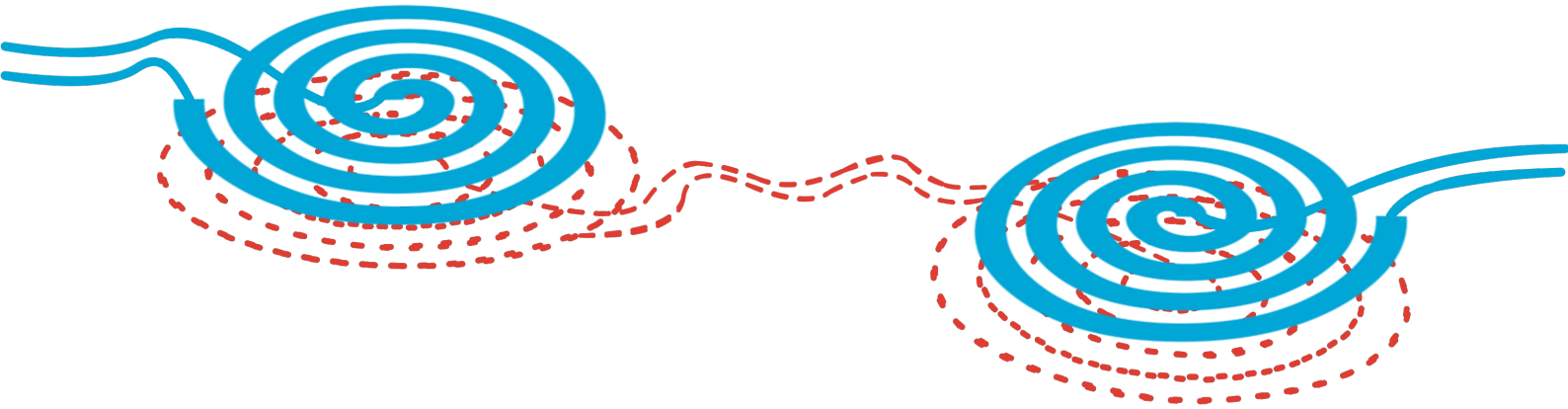
Contactless Inductive Power and Data Transfer

For use in E-Texiles

W.P. Lindeman



TU Delft

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by

W.P. Lindeman

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Thesis committee:	Dr. ir. A. Bossche,	TU Delft, supervisor
	Prof. Dr. P. J. French,	TU Delft
	Dr. Ir. J. Dong,	TU Delft
	MSc. A. S. M. Steijlen,	TU Delft, daily supervisor

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TU Delft

Abstract

Distributing power and data around a garment is a common problem in sensor enabled e-textiles, as connecting separate electronic subsystems together using connectors and wires has proven to be unreliable and cumbersome. In this work a solution is presented that will eliminate the connectors by using short-range wireless inductive links. This removes mechanical issues caused by wire strain, and will make removing or replacing electronics for washing or maintenance more straight forward. An impression of this system is shown in 1.

The proposed system is able carry power from one node to the next, while at the same time facilitating data transfer between the nodes. The system, as demonstrated in this work, consists of a master and a slave unit, connected via two sets of inductive links. Each inductive link consists of two planar coils placed at a distance of a few millimeters. The master generates a 13.56MHz carrier which is transmitted across the link. The slave uses this signal to extract power for both its own electronics, as well as external devices. Data is sent from the master to the slave by modulating this carrier (on-off keying), while data is sent back to the master using load modulation.

In this work the double inductive link is analysed, and a new compensation topology is presented which allows the system to be easily adapted to variations in coil spacing. A modified version of a class-E amplifier is presented to generate the carrier signal on the master side. A transformer based current sensing network is added to the output of the amplifier, which is used to detect the modulation of the slave input impedance. The slave uses a voltage doubler for harvesting energy from the carrier signal.

A proof of concept is built to demonstrate the working principles of the presented designs, and a basic placeholder data transmission protocol is devised to demonstrate its workings. Using this placeholder data protocol the system is able to transmit 62mW of regulated power to an external load at a total efficiency of 7.3%, while simultaneously transmitting data at a rate of 8.5kbit/s. The system is also shown to be capable of handling a theoretical maximum bitstream of 240kbit/s. Without data transmission it is able to deliver 185mW of DC power at 6.09V unregulated, at an efficiency of 23%. The system as demonstrated allows a sensor to be powered and read out from a central unit, without needing a direct wired connection.

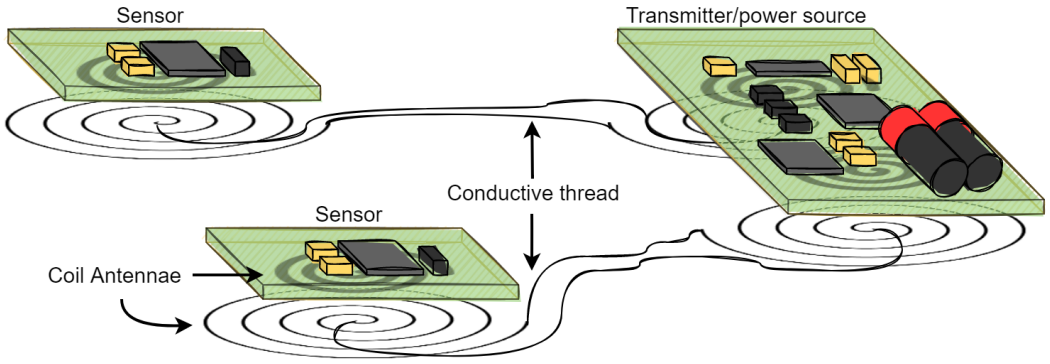

Figure 1: Illustration of what a contactless e-textile sensor network could look like.

Preface

The idea of harvesting energy from unconventional sources is something that has been chasing me throughout my academic career. I consider it poetic justice that in my final project I finally get the authority to not only harvest the energy, but also create its source, which massively simplifies the whole ordeal. Still, the project was very large in scope, testing my knowledge from amplifier design to data protocols, and from micro controllers to resonant circuits. It encapsulated nearly everything I have learned during my studies, and sometimes even a little more.

I would like to extend my gratitude to those who have kept me sane over the last year or so. This of course includes my supervisors Andre, Annemarijn en Jeroen, who together with my fellow students Adam, Zakaria and Tom, often unknowingly revitalised my enthusiasm for the project with insightful questions and comments during our weekly meetings. I would also like to thank my parents, who although far away supported me throughout the project.

Lastly I would like to thank my girlfriend Nuria. Who, despite not knowing anything about electronics, would insist that I explain her every milestone and roadblock. She even proof read an early version, pointing out several spelling errors. Thank you for always being there for me.

W.P. Lindeman
Delft, September 2022

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1

Introduction

The increasing miniaturisation and power efficiency of integrated circuits has allowed for electronic devices to be more easily integrated into everyday items. The clothing industry has not been blind to this trend and the interest in and market for electronics integrated into clothing, known as e-textiles, is growing [1] [2]. Over the last few years, various companies have released sensor-enabled clothing, in applications ranging from monitoring vital signs [3], to interfacing with smart phones [4], to supporting athletic activities [5] [6].

As the field of e-textiles develops, three generations have been identified.

- First generation: the smart component are largely an add-on to an otherwise normal piece of clothing, and only added after or during the final stage of production.
- Second generation: the smart components are directly integrated into the garment.
- Third generation: the fabric itself forms the smart component, with all the sensing, processing and communication done by structures of the fibres of the garment.

While never reaching main-stream popularity in the consumer market, first generation e-textiles are well developed and commercially available. Second generation products are still a subject of active research, but products in this category are starting to hit the market. A lot of research is currently being done into third generation products [7], but products in this category are yet to leave the research phase.

The most common use of smart clothing is the measurement of certain aspects of the body. For the sensing of certain body-wide metrics, such as body temperature [8], heart-rate [9] [10], breath-rate [11], blood pressure [12], etc. a single node is sufficient. However, the measuring of more complex metrics such as muscle activity [13] or limb movement [14] require a network of sensors distributed around the garment. For reasons of cost, efficiency, and spectral pollution it is not desirable to have each node in such a network wirelessly connected to the outside world. It is preferred to have all the sensor nodes within the garment connected to a central node. This central node will communicate with the outside world, and supply power to all other nodes. This is known as a body area network (BAN).

Most implementations of such a BAN involve connecting the nodes using conductive paths that are directly integrated into the clothing [15] [16]. These interconnecting paths carry data from, and supply power to the sensors, ideally without compromising on the comfortability and wearability of the garment. The use of conductive materials in clothing is traceable back to ancient times, usually in the form of gold or silver coated threads as a decorating feature. These could be manufactured by for example hammering a piece of gold flat, and using it to surround a piece of silk [17]. The same idea is still used for conductive threads today, although the manufacturing techniques are quite different. A common way of creating conductive strands for e-textiles is to take a conventional nylon or silk strand, and coat it in a conductive material [18]. These coatings commonly consist of either an intrinsically conductive polymer (ICP), a carbon-based coating or a metal. The carbon based approaches offer greater strength and durability, while the metal coatings have greater conductivity [18]. These conductive fibres can be woven directly into the textile, or embroidered on to it. Another way of creating conductive paths on a piece of textile is to print a conductive material directly onto the material [19] [20]. This technique better preservers the flexibility and feel of the textile it is printed on, which could result in more comfortable clothing. However, since textiles are generally very porous materials, it can be difficult to maintain a reliable electrical connection as the material stretches.

After many years of development, conductive paths in clothing can now be made to withstand the mechanical stresses of everyday wear [21]. However, these conductive paths need to be connected to the (usually rigid) electronics. While extensive research has been done on the conductive paths themselves, the work done in investigating the textile to electronics interface is quite limited. In the world of electronics, connections on printed circuit boards (PCBs) are usually made by soldering. While some success has been had recently using ultrasonic soldering [22], soldering is generally not compatible with textiles, as the high temperatures required for soldering are not compatible with fabrics, and the connections are quite brittle [23]. Other techniques such as crimped connectors and a polymer adhesive have been tested in [24], but showed limited mechanical strength. Success has also been had by embroidering flexible PCBs directly onto the fabric [25], but doubts still exist about the long-term reliability [26].

All of the above mentioned techniques result in permanent bonding of the fabric and the electronics. This presents an additional set of challenges. Firstly, in order for a smart garment to appeal to a wide market, it is important for the garment to be easily machine washed. This is especially important when it comes to smart sportswear. A typical wash cycle will impart very significant mechanical and chemical stresses [27], which puts significant extra constraints on the design of (the casing for) the electronics. The second problem is that textiles and electronics have very different failure modes. It would be a shame to discard a full clothing piece because a sensor contact has corroded. Conversely, it would be wasteful to throw away a working sensor system simply because its host garment has a tear in it. E-textiles are predicted to contribute significantly to global e-waste, and repairability and end-of-life care should not be an afterthought [28].

Some of the above mentioned problems can be solved by using connectors for the sensor nodes. While some connectors especially designed for e-textiles do exist, they have to address the same reliability and washability concerns mentioned before. In certain applications button connectors have been used [23]. Buttons are a proven method for creating connections in the textile industry, and have shown to be very reliable. However, they add a lot of bulk and can only implement a single electrical connection at a time, making them only suitable for certain applications.

In [29] electrical connectors embedded in both button and buckle connections are evaluated for military use. It was concluded that any sufficiently rugged and environmentally sealed connector was too bulky for practical use, although the authors do see some potential for buckle based designs in a civilian setting.

This project aims to find a solution to the reliability, washability and repairability problems. Instead of a galvanic connection between the conductive paths and the electronics, the power and data transfer will occur inductively. The conductors inside the textile terminate on both ends in planar coils embedded directly below pouches holding the electronics. The electronics are also provided with planar coils, which couple to the coils inside the garment as demonstrated in [30]. Across this link both data and power can be transferred. A schematic overview of this is shown in figure 1.1.

1.1. Smart Sensor Shorts Project

This project is part of the Sensor Shorts project, an initiative of the Citius Altius Sanius program. The goal of the program is make injury free sporting available to everyone. The Sensor Shorts are a sporting garment with embedded sensors which measure the movement of an athletes legs. This data will be used by movement scientists to predict when hamstring injuries are about to happen. In order to achieve this the sensor data must be read out and transmitted in real time, both during training and in matches.

Under the supervision of PhD candidate Annemarijn Steijlen several prototypes have already been made. In these prototypes, off-the-shelf inertial measurement units (IMUs) are mounted on the knees and lower back of a pair of sporting shorts. The IMUs measure the linear acceleration and angular velocity of the limbs. They also contain an electronic compass, to account for gyroscope drift. The data from these sensors is sent via an SPI bus to a central node on the lower back, where it is stored and transmitted. The central node also supplies power to the sensor nodes. The connection between the sensor nodes and the central node is made using off-the-shelf, flexible, embroidered wires. These wires terminate in a small clasp connector, to allow the nodes to be separated from the garment. The intended use for these connectors is to make semi-permanent connections within electronic equipment. As a result, they are not designed to withstand many connect/disconnect cycles. The researchers found these connections to be unreliable, and they formed a bottleneck in the user experience. Hence the start of this project.

The sensors used are the ICM-20649 gyroscope and accelerometer, and the AK8963 magnetometer. They are read out at 250 Hz and 100 Hz respectively, resulting in a combined data rate of 28.8 kbit/s. They have a combined power usage of roughly 32 mW. This serves as an outline for the requirements set for this project.

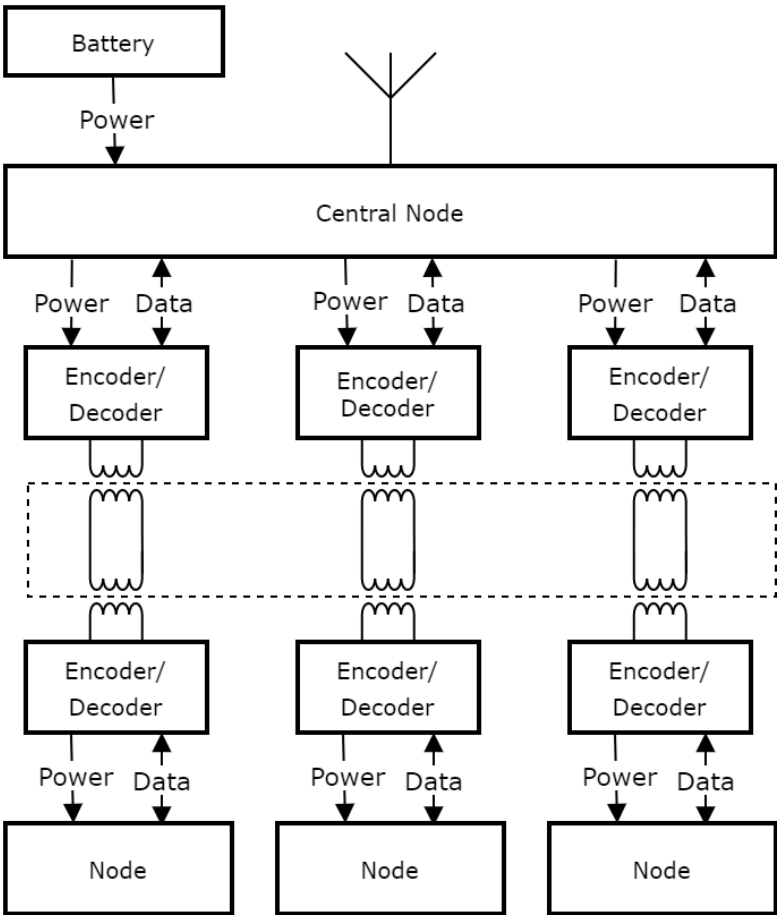


Figure 1.1: Overview of the wireless coupling system.

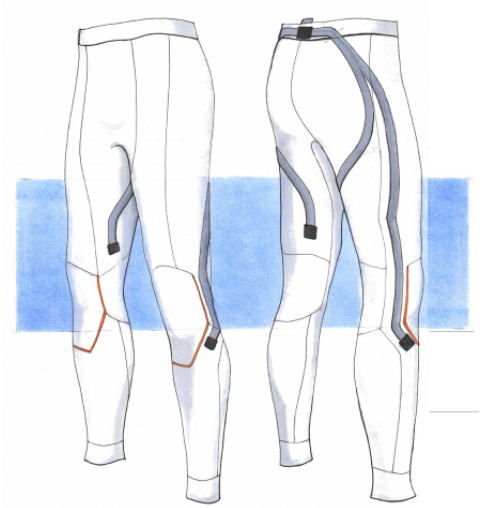


Figure 1.2: Drawing of the second prototype of the sensor pants [31]. The latest version only contains three sensor nodes, one on the lower back and one per knee.

1.2. Previous Research

A lot has been written on the broader topic of near-field battery-less sensors [32]. These are commonly referred to as Radio Frequency Identification (RFID) sensors. In an RFID sensor, the sensor does not contain its own power source. Instead, power is transmitted to it via radio waves. This power is used to both readout the

sensor, and transmit back the measured data (usually via back-scattering). Since the power contained in a radio wave is inversely proportional to the square of the distance to the source, most RFID sensors operate in the near field. This technology has also been implemented into clothing [33]. However, in most publications, the sensor and the antenna are combined. The sensed quantity alters the reflective properties of the antenna directly, without the need of any traditional readout electronics. This change in antenna properties can be measured from a distance using a readout antenna. Sensors that have been made in this way include, but are not limited to, sweat sensors [34], strain sensors [35], and even very low resolution accelerometers [36]. While the principles behind these types of sensors is similar to the ones used in this work, the techniques are quite different.

Not much has been published on the specific topic of textile-integrated inductive power and data transfer. However, the following papers have been found that are of particular relevance to this project.

In 2016, Saisai Wen et al. developed a battery-less, NFC-based sensor patch for measuring skin temperature, with the aim being to investigate the viability of wearable e-textile sensors for use in health monitoring [37]. The sensor consisted of a MLX90129 chip, mounted on a flexible polyamide substrate. The MLX90129 is a chip developed by Melexis that facilitates the communication and energy harvesting for RFID sensors. It has a temperature sensor built in, and can communicate with external sensors using SPI or I2C. It uses the ISO 15693 NFC protocol to both harvest power and wirelessly transmit the sensor data. In [37] a coil made of a conductive fabric, placed on top of the polyamide substrate, was used as the antenna for the MLX90120 chip. The sensor could be powered and read out from a short distance using an app on an NFC-capable smartphone. The authors do not elaborate on the process used to fabricate, the coil antenna, not do they provide details on its characteristics. They also do not provide any data on the achieved communication speed and power transfer of the inductive link.

Four years later, Rongzhou Lin et al. [38] published a design of a BAN network using inductively coupled sensors for posture and temperature monitoring. Several strain- and temperature sensors were positioned on various points on the body. These sensors would inductively couple to coils embedded into a flexible polyester-spandex shirt. Conductive threads embedded in the garment connected these coils to a central hub, where they would again inductively connect to a smartphone. All power and data transfer to and from these nodes occurred via these coupled inductors. The strain sensors were fabricated within a piece of e-textile, and were read out using a Texas Instruments RF430FRL152H chip, which also facilitated the temperature sensing. This chip is similar to the MLX90129 used in [37], as it also uses the ISO 15693 NFC protocol for wireless power and data transfer. The coils were embroidered directly into the fabric of the garment, using the same conductive threads that were used as interconnects. Further details on the design and characterisation of these coils was published separately [39]. Using an NFC enabled smartphone at the hub node, the researchers reported an 8 Hz sampling rate for one sensor, or a 1.3 Hz sampling rate when all six sensors where used. The sampling resolution was 14-bit, leading to an overall data-rate of 112 bit/s. This is the only publication found that investigates the use of two pairs of coupled coils, as is also used in our work. However, the paper does not elaborate on the challenges this introduces, nor does it attempted to model this arrangement.

The previous publications both rely on the ISO 15693 NFC protocol [40]. This is a protocol originally designed for near field identification of for example library cards. A reader sends out a signal requesting data from a card. The card uses the energy in this signal to send back an identifying code. Devices following this protocol operate at 13.56 MHz, and are theoretically capable of communicating at 26.69 kbit/s in both directions simultaneously. This is slightly less than the 28.8 kbit/s required in this project. They are capable of operating at ranges up to one meter, which is far beyond what this project requires.

In 2020, Ken Takaki et al. also developed an inductively coupled power and data transfer system [41]. This time with the aim of connecting electronics across the hinge of a pair of glasses. The researchers report a power transfer efficiency of 87%, and a communication speed of 50 Mbit/s, with a bit error rate of 10^{-6} at a coil separation of 1.6 mm. These results are however theoretical, based on measured S-parameters and estimated noise figures. As a result they are likely highly optimistic.

The above mentioned systems all rely on a single carrier wave that contains both the power and the data. However, in certain applications it is useful to use separate carriers for the power and data [42] [43] [44] [45]. This is particularly useful for high power applications, where power transfer is prioritized over data speeds, as the modulation required to transmit data will in most cases reduce the overall signal power. Transmitting the data at a higher frequency will allow it to utilize more bandwidth, increasing the data rate. The power electronics tend to operate more efficiently at lower frequencies. A major challenge associated with this technique is that the switch-mode power amplifiers commonly used to generate the power signal tend to produce a lot of high frequency noise, which can interfere with the data signal. Some publications therefore opt to transmit

the data at a lower frequency than the power [42] [45]. This improves reliability at the cost of data rate. A challenge faced with all designs of this nature is that the inductive link needs to be able to efficiently transmit signals at two different frequencies, which is not trivial.

Some publications take this a step further and use separate coils for the power and data transfer [46] [47] [48]. In most cases the power and data coils are aligned on the same axis, but radially or axially displaced from one another. While the design of such a system from a circuit design perspective is relatively straight forward, the design of the coils themselves is quite complex. In order to minimize cross-talk between the data and power coils the coupling between them needs to be minimized, while simultaneously maximizing the coupling to the corresponding coil on the secondary side. This presents significant design challenges, especially when lateral displacement between the primary and secondary side is involved.

1.3. This Work

As mentioned previously, the application requires a system with a data rate of at least 28.8 kbit/s, and a continuous power transfer of at least 32 mW. To leave some margin for error, the specifications for this project are set at 50 kbit/s and 50 mW. No specific requirement is set for the bit error rate, but it should be within the bounds correctable by a simple error correction scheme, although the details of this error correction are beyond the scope of this work. The power flow should not be interrupted under normal conditions. Total power transfer and transfer reliability have been emphasised over transfer efficiency, although the later should still be within reason. The physical size of the inductor should fit within a 5 cm x 5 cm square.

To limit the scope of this project, rigid planar coils are used instead of flexible or integrated coils. A prototype of the system has been built, and serves as a proof of concept. Since this is not intended as a final product, the electronics have been allowed to extend beyond the size limit. This allows the use of off-the-shelf components, instead of requiring all functionality to be housed within a single chip. These requirements are summarised in the list below, in the order of importance.

- Data rate of at least 50 kbit/s
- Continuous power transfer rate of at least 50 mW
- Stable power connection
- Stable data connection

In order to better understand the challenges in designing such a system, three research questions have been posed:

1. Under what conditions will an inductive link behave like a direct connection?
2. What techniques should be used to modulate and demodulate the data and power on both sides of the link?
3. What data transfer protocol is practical for use in a combined power and data transfer system, and what is the trade-off between power and data rate?

The system is divided into three distinct subsections: the master, the slave, and the link. The master interfaces with the battery and the transmitter on one side, and the link on the other. It is responsible for generating the carrier signal, and modulates this signal to send data and acknowledgements to the slave. It also demodulates the data coming from the slave, and presents this in a usable form to the transmitter. The slave acts as a bridge between the link and the sensor. It harvests energy from the carrier, and performs demodulation. It modulates the data from the sensor onto the carrier by way of load modulation. The link forms the connection between the master and the slave. It consists of four planar coils, forming two pairs, as well as some surrounding capacitors.

A diagram of these subsections, as well as the subsystems within them, is shown in figure 1.3.

Each of these subsystems will be discussed in detail in the thesis, starting with an analysis of the link. This is followed by a discussion of first the master and then the slave. After this the implementation of the controllers and the data protocol is discussed. The thesis concludes with a chapter on the measured results of the full system, followed by a discussion and some recommendations for future work.

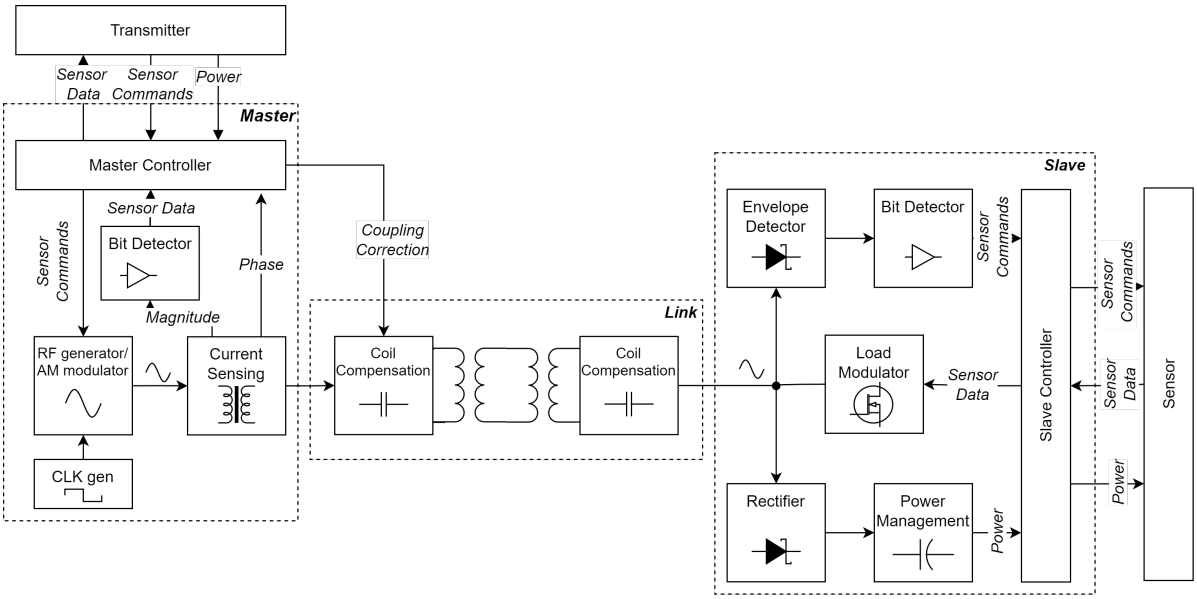


Figure 1.3: Block diagram of all the subsystems.

2

Inductive Link

In this chapter the design and characteristics of both the coils forming the inductive link, and the compensation circuits surrounding them will be discussed. As introduced in the previous chapter, the purpose of the link is to provide power to the sensor node, and to allow for bi-directional communication between the central node (master) and the sensor node (slave). In order to effectively do this the link should have the following properties:

1. For transmitting to the slave, the transmit voltage of the master should be measurable by the slave.
2. For transmitting to the master, the slave side impedance should be measurable by master.
3. For high data speeds, the quality factor of the link should be as low as possible.
4. For high power transfer efficiency, the link should introduce minimal losses.
5. For effective power transfer, the impedance on the master and slave side should be matched to the link impedance.

However, since the signal generator in the slave and the rectifier in the load are non-linear in nature, the exact values of these impedances are ill-defined. Moreover, the input impedance of the slave is dependent on its power draw, which cannot be guaranteed to be constant over time. In order to disconnect the design of the link from that of the slave and master, the link is designed in such a way that the impedance of the slave is mirrored to master. In this way, the inductive link essentially behaves as a direct wired connection. This also guarantees requirements 1 and 2.

The link can be analyzed as a two-port network with the master attached to port one and the slave to port two. In order to characterise the input-output characteristics of any two-port network, transmission matrices can be used [49]. A transmission matrix defines the input voltage and current (V_1 and I_1) in terms of the output voltage and current (V_2 and I_2) [49]. This is shown in equation 2.1. The polarities of the voltages and currents are given in figure 2.1.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{2.1}$$

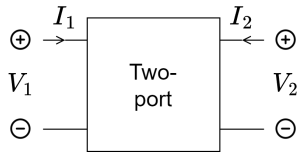


Figure 2.1: Voltage and current definitions of a two-port matrix.

As mentioned earlier, the link is considered optimal when the inductive coupling behaves the same as a physical wired connection. In a direct connection, the output voltage is the same as the input voltage, and

the same is true for the input and output currents. The optimal transmission matrix is therefore given by the identity matrix:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{2.2}$$

2.1. Analysis of the Double Inductive Link

The link consists of a pair of inductively coupled coils at the central node, and a pair at the sensor node. These two pairs are connected using a pair of wires that is integrated into the clothing. This link can be modeled using the circuit shown in 2.2.

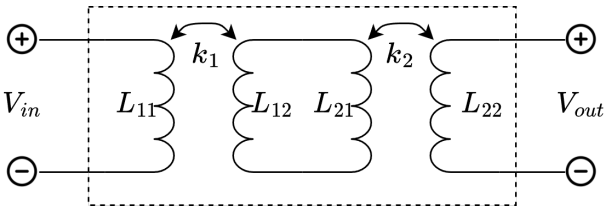


Figure 2.2: Simple electrical model of the link.

In this model L_{11} and L_{12} represent the coils near the central node, while L_{21} and L_{22} represent the coils on the sensor node. The coils by the central node and by the sensor node are coupled with coupling factor k_1 and k_2 respectively. Both the inductance L and the coupling k are gravely affected by the physical design of the coil, as well as many environmental factors. Furthermore, neither L nor k can be assumed to remain constant during operation. The coils are preferably made from a flexible material, in order for the clothing to remain comfortable. As the coils bend, both their mutual-inductance and their self-inductance will change.

In order to simplify the analysis in the coming sections, this model is kept quite simple. In reality, there would be many parameters, including the finite resistance of the coils, inter-winding capacitances, as well as non-idealities related to wires mounted in the clothing. The actual implementation of the system inside a garment is considered outside the scope of this work, so the parameters related to this are not further discussed. However, in order to validate this model some measurements on a prototype system using rigid planar coils are presented at the end of this chapter.

In order to analyze the full circuit, it is useful to first consider a single inductive link shown in figure 2.3. By applying Kirchhoffs voltage law equation 2.3 is obtained.

$$\begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} j\omega L_{11} & j\omega k_1 \sqrt{L_{11}L_{12}} \\ j\omega k_1 \sqrt{L_{11}L_{12}} & j\omega L_{12} \end{bmatrix} \begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} \tag{2.3}$$

Converting the Z-matrix from equation 2.3 to a transmission matrix gives equation 2.4:

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \frac{1}{k_1 \sqrt{L_{11}L_{12}}} \begin{bmatrix} L_{11} & j\omega L_{11}L_{12}(1-k_1^2) \\ \frac{1}{j\omega} & L_{12} \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \tag{2.4}$$

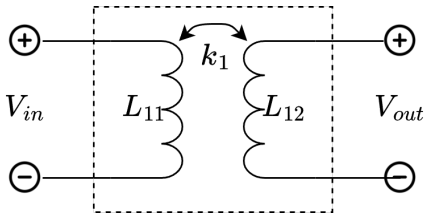


Figure 2.3: Ideal model of two coupled inductors.

Using the cascading property of the transmission matrix, the transmission matrix of the double link can be calculated by multiplying the transmission matrices of the individual links [49]. The result of this is given in equation 2.5.

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \frac{1}{k_1 k_2 \sqrt{L_{11}L_{12}L_{21}L_{22}}} \begin{bmatrix} L_{11}L_{21} - L_{11}L_{12}(k_1^2 - 1) & j\omega L_{11}L_{22}[L_{12}(1-k_1^2) + L_{21}(1-k_2^2)] \\ \frac{L_{12}+L_{21}}{j\omega} & L_{21}L_{22} - L_{21}L_{22}(k_2^2 - 1) \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \tag{2.5}$$

It is assumed that the design of the link is symmetrical. This is to say that the coils embedded into the fabric on both the slave and master side are of the same design. Furthermore, the coils on the slave and master boards are also designed to be the same. Finally, the mounting of the coils on both sides of the link is also considered to be equal. This allows for the following simplifications:

$$L_{11} = L_{22} = L, L_{12} = L_{21} = L_2, k_1 = k_2 = k \tag{2.6}$$

Substituting the simplifications from equation 2.6 into 2.5 gives:

$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \frac{1}{k^2} \begin{bmatrix} 2-k^2 & 2j\omega L(1-k^2) \\ \frac{2}{j\omega Lk} & 2-k^2 \end{bmatrix} \begin{bmatrix} V_{out} \\ I_{out} \end{bmatrix} \tag{2.7}$$

Note how equation 2.7 no longer contains L_1, meaning that as long as equation 2.6 holds, the performance of the link is not influenced by the self inductance of the coils embedded into the fabric. This does not mean the design of this coil requires no attention, as it still influences the coupling k. There are also several parasitic effects that have to be taken into account.

Rewriting the transmission matrix from 2.7 back into a Z matrix gives:

$$\begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} \frac{1}{2}j\omega L(2-k^2) & \frac{1}{2}j\omega Lk^2 \\ \frac{1}{2}j\omega Lk^2 & \frac{1}{2}j\omega L(2-k^2) \end{bmatrix} \begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} \tag{2.8}$$

Now, substituting $\hat{L} = \frac{1}{2}L(2-k^2)$ and $\hat{k} = \frac{k^2}{2-k^2}$ into 2.8, 2.9 is obtained:

$$\begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} j\omega\hat{L} & j\omega\hat{L}\hat{k} \\ j\omega\hat{L}\hat{k} & j\omega\hat{L} \end{bmatrix} \begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} \tag{2.9}$$

This shows that a system with a double inductive link behaves electrically identical to a single symmetrical link, with self inductance $\hat{L}$ and coupling $\hat{k}$ (assuming that equation 2.6 holds). This is illustrated in figure 2.4.

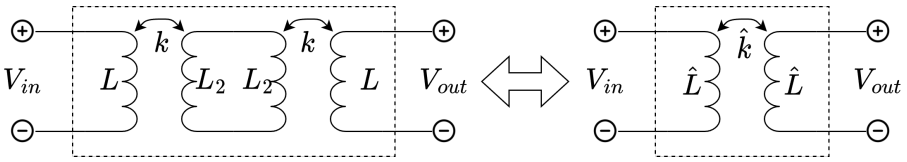


Figure 2.4: Electrically equivalent model of the double inductive link.

It is useful to convert the Z-matrix from equation 2.9 back into a transmission matrix for use later on:

$$T_{link} = \begin{bmatrix} \frac{1}{\hat{k}} & j\omega\hat{L}\frac{(1-\hat{k}^2)}{\hat{k}} \\ \frac{1}{j\omega\hat{L}\hat{k}} & \frac{1}{\hat{k}} \end{bmatrix} \tag{2.10}$$

2.2. Link Compensation

When comparing the transmission matrix in equation 2.7 to the ideal identity matrix from equation 2.2, it is clear that the double link on its own does not have ideal performance. This discrepancy between the real and ideal matrices will manifest itself into an apparent inductance parallel to the load, even at perfect coupling ($k = 1$). This inductance will reduce the current flowing into the load, and will make the load modulation less effective. In order to compensate for this, a capacitor network can be placed around the load, which will be in resonance with the apparent inductance of the system at the operating frequency ω_0. This effectively matches the link impedance to that of the load and the source, significantly improving both power and data transfer. This is known as Resonant Wireless Power Transfer (RWPT) [50].

Topology	C_p	C_s	$[T]$
SS	$\frac{1}{\omega^2\hat{L}}$	$\frac{1}{\omega^2\hat{L}}$	$\begin{bmatrix} 0 & \frac{\omega\hat{k}\hat{L}}{j} \\ \frac{j}{\omega\hat{k}\hat{L}} & 0 \end{bmatrix}$
SP	$\frac{\hat{1}}{\omega^2\hat{L}(1-\hat{k}^2)}$	$\frac{1}{\omega^2\hat{L}}$	$\begin{bmatrix} \hat{k} & 0 \\ 0 & \frac{1}{\hat{k}} \end{bmatrix}$
PP	$\frac{(1-\hat{k}^2)\hat{L}}{\omega^2\hat{L}^2(1-\hat{k}^2)^2+\hat{k}^4 Z_l^2}$	$\frac{1}{\omega^2\hat{L}}$	$\begin{bmatrix} \hat{k} & \frac{\hat{L}\omega(1-\hat{k}^2)}{\hat{k}} \\ \frac{j\omega\hat{L}\hat{k}(1-\hat{k}^2)}{\omega^2\hat{L}^2(1-\hat{k}^2)^2+Z_l\hat{k}^4} & \frac{Z_l\hat{k}^4}{\omega^2\hat{L}^2(1-\hat{k}^2)^2+Z_l\hat{k}^4} \end{bmatrix}$
PS	$\frac{Z_l^2}{\omega^2\hat{L}Z_l^2+\omega^3\hat{L}\hat{k}^4}$	$\frac{1}{\omega^2\hat{L}}$	$\begin{bmatrix} \frac{1}{\hat{k}} & \frac{\omega\hat{k}\hat{L}}{j} \\ \frac{\hat{L}\hat{k}^3\omega}{j\hat{L}^2\hat{k}^4\omega^2+jZ_l} & \frac{\hat{k}Z_l}{\hat{L}^2\hat{k}^4\omega^2+Z_l} \end{bmatrix}$

Table 2.1: Common values for primary compensation capacitors and their resulting transmission matrices at resonance ($\omega = \omega_0$).

2.2.1. Design of the Compensation Network

As previously established, the double link can be seen as behaving the same as the more conventional single link. This means that it is possible to use existing and well documented compensation techniques. Although others exist and are used, the most common compensation techniques are SS (series-series), SP (series-parallel), PS (parallel-series) and PP (parallel-parallel) [50] [51] [52] [53] [54]. In this naming convention the words refer to capacitors added to the primary and secondary side respectively. All four topologies are shown in figure 2.5.

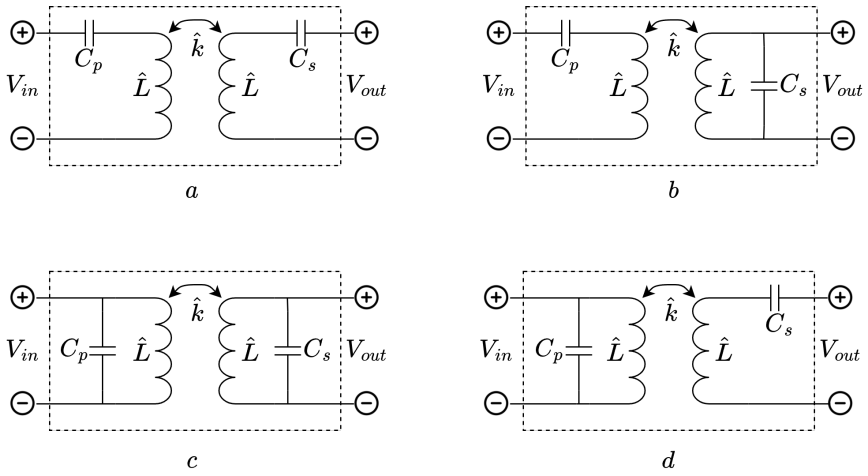


Figure 2.5: Common compensation techniques: Series-Series (a), Series-Parallel (b), Parallel-Parallel (c), and Parallel-Series (d).

In principle, the capacitor on the secondary side is chosen to be in resonance with the self-inductance of the secondary coil at the operating frequency [51], so $C_s = \frac{1}{w^2\hat{L}}$. The value of the primary capacitor is then chosen in such a way that at the operating frequency, the imaginary component of the input impedance equals zero [51] [54]. The values of these capacitors and their resulting transmission matrices are shown in table 2.1.

As mentioned before, the ideal transmission matrix would be the identity matrix, as the impedance seen by the master would simply be the slave impedance, with no impedance transformation occurring in the link. This rules out the SS and PS topologies, as even with perfect coupling ($k = 1$), their transmission matrix does not approach the identity matrix. The two remaining techniques do mirror the impedance properly, as long as the coupling is perfect. However, by looking at their input impedances (equations 2.11 and 2.12 for SP and PP respectively) a new problem presents itself.

$$Z_{in,SP} = Z_l\hat{k}^2 \tag{2.11}$$

$$Z_{in,PP} = \frac{\hat{L}^2\omega^2(\hat{k}^4-2\hat{k}^2+1)+Z_l^2\hat{k}^4}{Z_l\hat{k}^2} \tag{2.12}$$

While they both indeed converge to Z_l for $k = 1$, their behaviour is difficult to compensate for if this is not the case. Both apply a transformation to the real part of the impedance, which requires at least two reactive components to compensate for. If left uncompensated, a variation in the coupling between the coils will not be distinguishable from any intentional load modulation.

In order to find a more elegant solution, two additional compensation networks where considered. The first circuit,"A", uses a PP topology, but both capacitors are of equal value. The same goes for the second circuit, "B", although this one uses a SS topology. The transmission matrices can be calculated by multiplying the transmission matrices for series and parallel capacitors with the transmission matrix for the link given in 2.10, as shown below.

$$T_A = \begin{bmatrix} 1 & 0 \\ j\omega C_{p,A} & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{\hat{k}} & j\omega\hat{L}\frac{(1-\hat{k}^2)}{\hat{k}} \\ \frac{1}{j\omega\hat{L}\hat{k}} & \frac{1}{\hat{k}} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{s,A} & 1 \end{bmatrix} \tag{2.13}$$

$$T_B = \begin{bmatrix} 1 & \frac{1}{j\omega C_{p,B}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{\hat{k}} & j\omega\hat{L}\frac{(1-\hat{k}^2)}{\hat{k}} \\ \frac{1}{j\omega\hat{L}\hat{k}} & \frac{1}{\hat{k}} \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C_{s,B}} \\ 0 & 1 \end{bmatrix} \tag{2.14}$$

The resonance capacitors C_p and C_s are now chosen in such a way that for $\hat{k} = 1$ and $\omega = \omega_0$, the system matrix converges to the identity matrix. The resulting capacitor values and transmission matrices of the two networks are shown in table 2.2.

Topology	C_p	C_s	$[T]$
PP "A"	$\frac{1}{\omega_0^2\hat{L}(\hat{k}+1)}$	$\frac{1}{\omega_0^2\hat{L}(\hat{k}+1)}$	$\begin{bmatrix} \frac{\omega^2(\hat{k}-1)+\omega_0^2}{\hat{k}\omega_0^2} & \frac{j\hat{L}\omega(1-\hat{k}^2)}{\hat{k}} \\ \frac{j(\omega^2-\omega_0^2)(\omega^2(\hat{k}-1)+\omega_0^2(\hat{k}+1))}{\hat{L}\hat{k}\omega\omega_0^4(\hat{k}+1)} & \frac{\omega^2(\hat{k}-1)+\omega_0^2}{\hat{k}\omega_0^2} \end{bmatrix}$
SS "B"	$\frac{1}{\omega_0^2\hat{L}(1-\hat{k})}$	$\frac{1}{\omega_0^2\hat{L}(1-\hat{k})}$	$\begin{bmatrix} \frac{1}{\hat{k}}+\frac{\omega_0^2(\hat{k}-1)}{\hat{k}\omega^2} & \frac{j\hat{L}(\omega^2-\omega_0^2)(1-\hat{k})(\omega^2(\hat{k}+1)+\omega_0(\hat{k}-1))}{\hat{k}\omega^3} \\ \frac{1}{j\hat{L}\hat{k}\omega} & \frac{1}{\hat{k}}+\frac{\omega_0^2(\hat{k}-1)}{\hat{k}\omega^2} \end{bmatrix}$

Table 2.2: Component values and transmission matrix for the proposed "A" and "B" circuits

When operating at the operating frequency w_0, both A and B converge to the identity matrix as k approaches 1. As they stand they do not offer any benefits over the traditional SP and PP compensation networks shown earlier. However, they allow for much easier tuning to a specific coupling factor. By placing an additional capacitor in series (A) or in parallel (B), it is possible to tune the system to a specific estimated coupling $\bar{k}$. Whenever the coupling $\hat{k}$ is equal to the estimate $\bar{k}$, the transmission matrix will approach the identity matrix. The resulting schematics are shown in figure 2.6. The transmission matrices related to this circuits are calculated by multiplying the matrices is 2.13 and 2.14 by the transmission matrix of a series and parallel capacitor respectively:

$$T_A = \begin{bmatrix} 1 & \frac{1}{j\omega C_{comp,A}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{p,A} & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{\hat{k}} & j\omega\hat{L}\frac{(1-\hat{k}^2)}{\hat{k}} \\ \frac{1}{j\omega\hat{L}\hat{k}} & \frac{1}{\hat{k}} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_{s,A} & 1 \end{bmatrix} \tag{2.15}$$

$$T_B = \begin{bmatrix} 1 & 0 \\ j\omega C_{comp,B} & 1 \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C_{p,B}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{1}{\hat{k}} & j\omega\hat{L}\frac{(1-\hat{k}^2)}{\hat{k}} \\ \frac{1}{j\omega\hat{L}\hat{k}} & \frac{1}{\hat{k}} \end{bmatrix} \begin{bmatrix} 1 & \frac{1}{j\omega C_{s,B}} \\ 0 & 1 \end{bmatrix} \tag{2.16}$$

By choosing $C_{comp,A} = \frac{\bar{k}}{\hat{L}\omega_0^2(1-\bar{k}^2)}$ and $C_{comp,B} = \frac{1}{\hat{L}\bar{k}\omega_0^2}$. When $\bar{k} = \hat{k}$ both systems will approach the identity matrix at ω_0. This behaviour is summarized in table 2.3.

Circuit A provides another benefit when it comes to the coupling compensation. When $C_{p,s}$ and C_{comp} are rewritten in terms of k and L instead of $\hat{k}$ and $\hat{L}$, the following equations emerge:

$$C_{p,s} = \frac{1}{\omega_0^2 L} \tag{2.17}$$

$$C_{comp} = \frac{k^2}{2L\omega_0^2(1-k^2)} \tag{2.18}$$

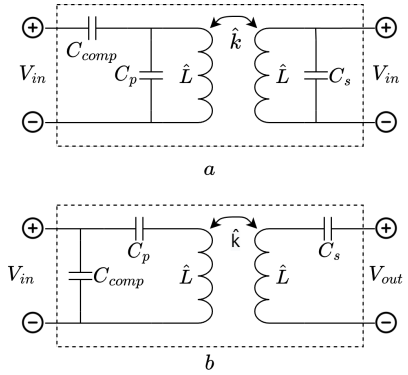


Figure 2.6: Circuit A with series compensation capacitor (a), circuit B with parallel compensation capacitor (b)

Topology	$C_{p,s}$	C_{comp}	$[T]$	Z_{in}
PP "A"	$\frac{1}{\omega_0^2\hat{L}(\hat{k}+1)}$	$\frac{\bar{k}}{\hat{L}\omega_0^2(1-\bar{k}^2)}$	$\begin{bmatrix} 1 & -j\omega_0\hat{L}\frac{\hat{k}^2\bar{k}-\hat{k}\bar{k}^2+\hat{k}-\bar{k}}{\hat{k}\bar{k}} \\ 0 & 1 \end{bmatrix}$	$Z_{in} - j\omega_0\hat{L}\frac{\hat{k}^2\bar{k}-\hat{k}\bar{k}^2+\hat{k}-\bar{k}}{\hat{k}\bar{k}}$
SS "B"	$\frac{1}{\omega_0^2\hat{L}(1-\hat{k})}$	$\frac{1}{\hat{L}\bar{k}\omega_0^2}$	$\begin{bmatrix} 1 & 0 \\ \frac{j(\hat{k}-\bar{k})}{\hat{L}\hat{k}\bar{k}\omega_0} & 1 \end{bmatrix}$	$\frac{\hat{L}Z_l\hat{k}\bar{k}\omega_0}{\hat{L}\hat{k}\bar{k}\omega+jZ_l(\hat{k}-\bar{k})}$

Table 2.3: Parameters for fully compensated A and B circuits at $\omega = \omega_0$.

This shows that $C_{p,s}$ should be in resonance with the uncoupled coil L at ω_0, and is independent of the coupling factor. This significantly reduces the tuning complexity, effectively turning the resonance tracking and coupling tracking into orthogonal problems. $C_{p,s}$ can be tuned during manufacturing to where it can be seen to be in resonance with L at ω_0. C_{comp} can then be adjusted during use to compensate for the coupling factor. Circuit B does not poses this property, as both $C_{p,s}$ and C_{comp} are dependent on k.

2.2.2. Frequency Characteristics

While both circuits are designed with a specific operating frequency w_0 in mind, it is not the case that the total power transfer or transfer efficiency are always optimal at this frequency. In [55], it is observed that as the coupling between the coils increases, there comes a point at which the power delivered to the load drops sharply. This effect is explained by Coupled Mode Theory [55] [56]. The WPT system essentially operates as two coupled resonators. As the coupling between two systems with the same resonant frequency f_0 increases, the resonant frequency of the combined system starts to deviate from f_0. Usually the resonance splits into two, with one resonant mode below f_0 and one above. This is known as frequency splitting. When the coupling is increased past a threshold value k_{split}, the power transferred to the load at f_0 drops significantly. In this case it might be beneficially to move the operating point to one of the split frequencies.

In order to investigate how this theory applies to the proposed circuits, a numerical matlab simulation has been performed to determine the total power received and the efficiency at which this transfer occurred for various frequencies and load resistances. The setup of the simulation was as follows (see also 2.7): a signal is provided by an ideal voltage source, followed by a linear source resistance R_s. This signal is fed to the input of a perfectly compensated link, modeled using the transmission matrix given in 2.3. Attached to the output of this link is a fixed load resistor R_l. In this setup, the current flowing through the voltage source $I_s = \frac{V_s}{R_s+Z_{in}}$, where Z_{in} is the input impedance of the link. Since the model of the link does not contain any resistive components, the power delivered to the load can be calculated as follows:

$$P_{load} = |I_s|^2 Re(Z_{in}) \tag{2.19}$$

The power lost in the source is given by $P_{load} = |I_s|^2 R_s$. The efficiency is defined as the delivered power divided by the total power, which simplifies to:

$$\eta = \frac{Re(Z_{in})}{R_s + Re(Z_{in})} \tag{2.20}$$

The simulation has been performed for both A and B circuit topologies, using $R_s = 4\Omega$, $k = 0.8$, $L = 550nH$,

and $\omega_0 = 2\pi \cdot 13.56MHz$. The resulting power transfer and transfer efficiency, as well as the real and imaginary parts of the input impedance are shown in figure 2.8 and 2.9. It is important to note that in this simulation and in the rest of this section it is assumed that the link is perfectly compensated, so $\bar{k} = \hat{k}$.

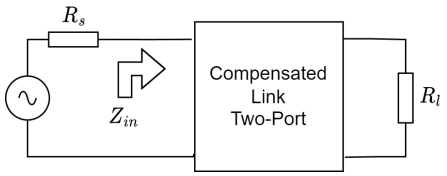


Figure 2.7: Circuit used for transfer efficiency simulations.

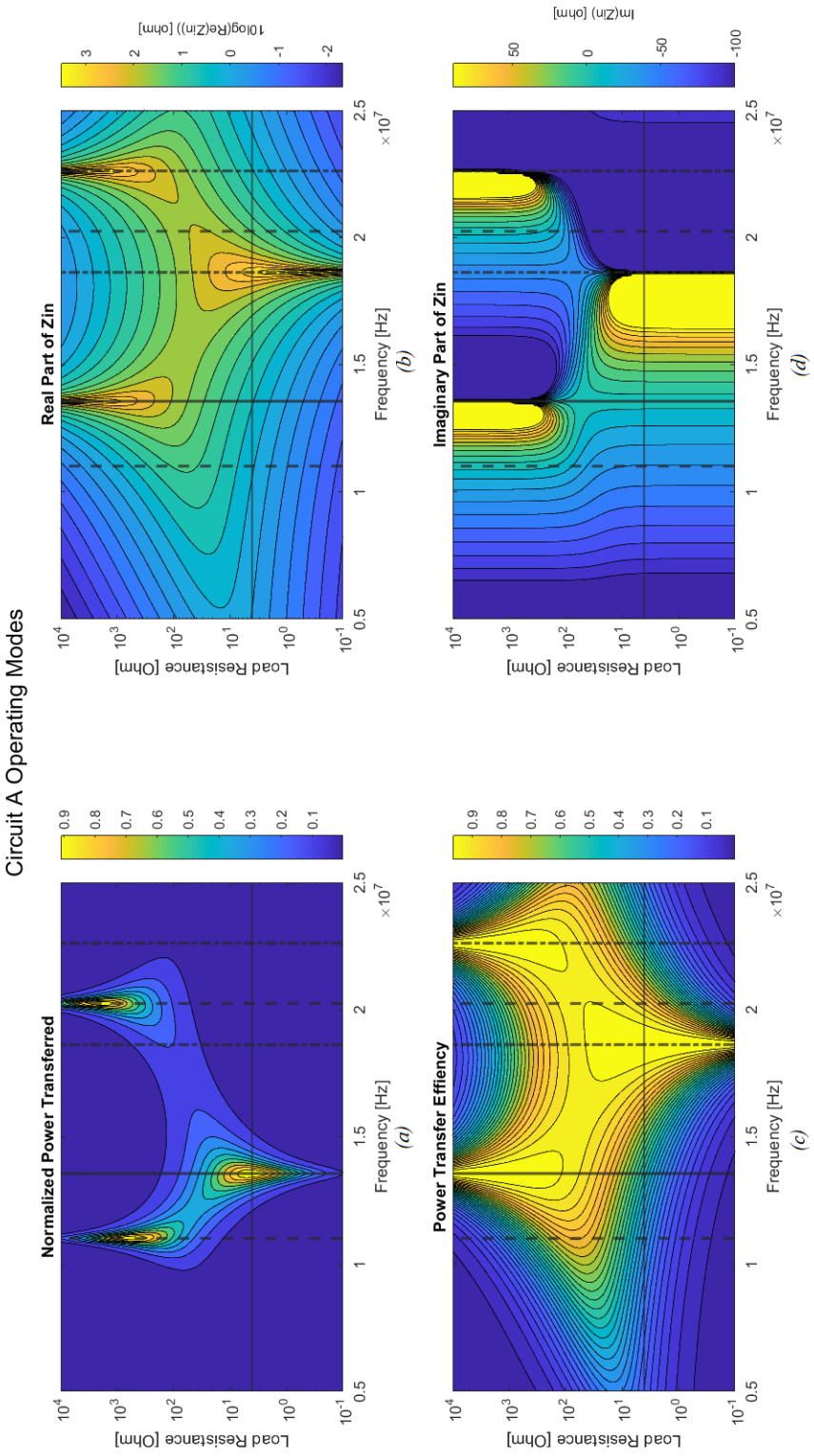


Figure 2.8: Power transfer (a), transfer efficiency (c), real part of link input impedance (b), and imaginary part of input impedance (d), as a function of frequency and load resistance for circuit A. The imaginary part of the input impedance (d) is capped at -100 and 100 Ω. The solid vertical line indicates the operating frequency, the dashed vertical lines indicates zero frequencies for Z_{in}, and the dash-dot vertical lines show pole frequencies for Z_{in}. The horizontal solid line indicates where $Z_{load} = Z_{source} = 4\Omega$.

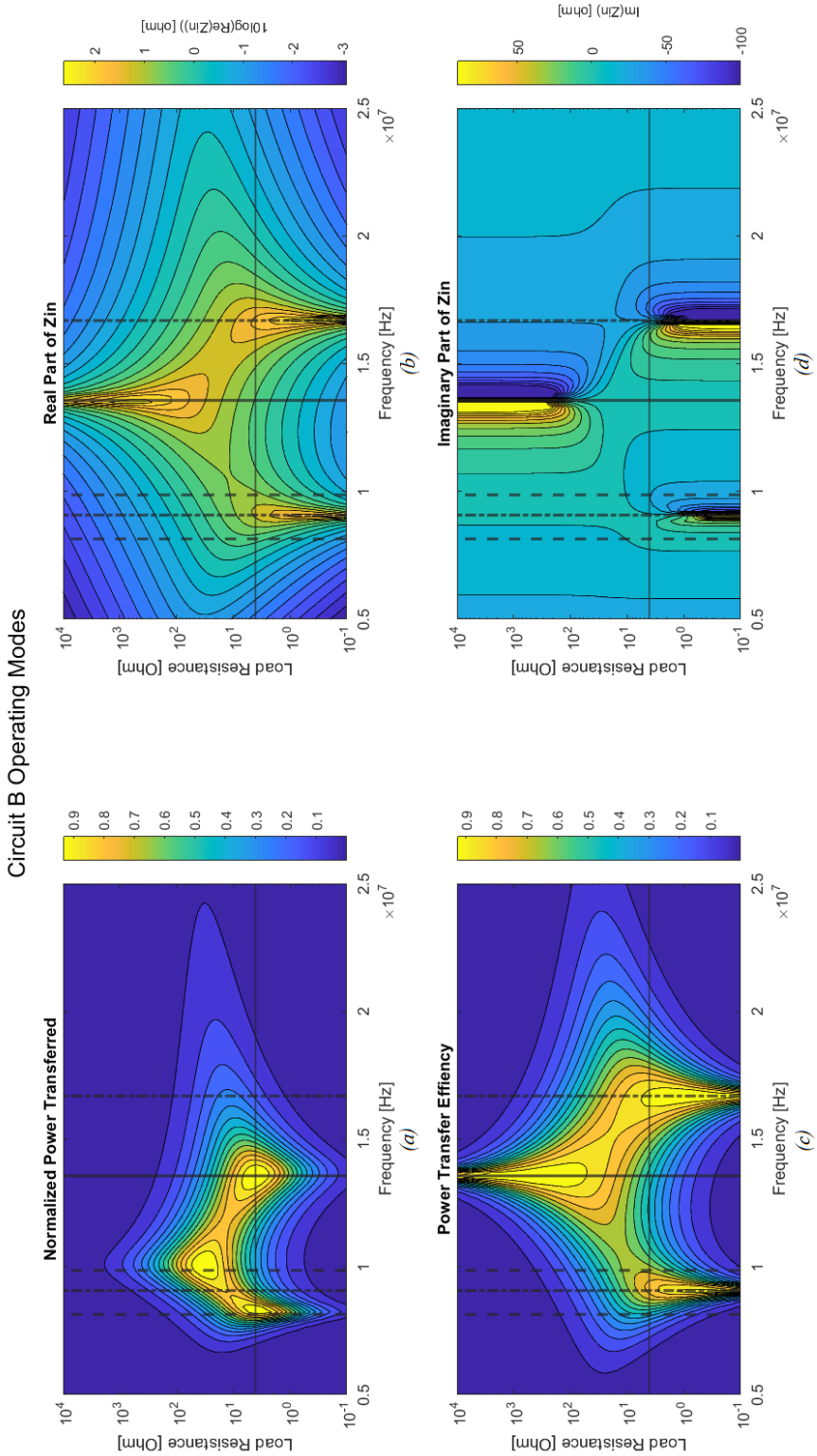


Figure 2.9: Power transfer (a), transfer efficiency (c), real part of link input impedance (b), and imaginary part of input impedance (d), as a function of frequency and load resistance for circuit B. The imaginary part of the input impedance (d) is capped at -100 and 100 Ω. The solid vertical line indicates the operating frequency, the dashed vertical lines indicates zero frequencies for Z_{in}, and the dash-dot vertical lines show pole frequencies for Z_{in}. The horizontal solid line indicates where $Z_{load} = Z_{source} = 4\Omega$.

As can be seen from figures 2.8 and 2.9, the frequency at which optimal performance is achieved is not the same for all values of R_l. It shows a similar behaviour as what would be expected from frequency splitting, but it occurs with varying Z_l, instead of varying k. This can be explained as follows. From [56] we learn that optimal performance is achieved whenever the system is in resonance. The presence of the resistive element R_l will dampen any resonance that take place. However, the amount of dampening depends not only on the value of R_l, but also on the type of resonance that is taking place. In electronics, there are two archetypal resonant circuits; a series resonance and a parallel resonance. In a series resonant circuit, an increase in R_l will result in more dampening, while the opposite is true in a parallel resonant circuit. The circuits being analyzed here cannot be determined to be either fully series or fully parallel resonant. Instead, there are different resonant modes present, some of which are "series" dampened, and some are "parallel" dampened. What is seen in figures 2.8 and 2.9 is that for low Z_l the series resonant modes are dominating, while for higher Z_l the parallel modes are dominant. This also suggests that frequency splitting will always occur, regardless of coupling factor, but that it might not be apparent unless the system is operated at impractically large or small loads. The two circuits show opposing behaviours: circuit A will split sooner when using a large ohmic load, while circuit B splits sooner when loaded with a small load.

A lot of research has been published about finding the frequencies at which the power transfer is optimal once the resonance has split [57] [58] [59] [60]. These rely on finding peaks using the derivative of the load power:

$$\frac{\partial P_{load}}{\partial \omega} = 0 \tag{2.21}$$

However, this technique requires solving very complex higher order polynomials. Instead, candidate frequencies at which optimum performance could occur can be found by looking at the possible resonant modes of the circuit. In order to find all resonant modes one should consider the input impedance Z_{in} of the link for the two extremes; $Z_l = 0$ and $Z_l = \infty$. These are shown in 2.22 and 2.23 for circuit A, and 2.24 and 2.25 for circuit B.

$$Z_{in\ A}(\omega)|_{Z_l=0} = j\frac{\hat{L}\omega_0^2}{\omega}(\hat{k}^2-1)\frac{\omega_0^2-\omega^2}{\hat{k}(\omega^2(\hat{k}-1)+\omega_0^2)} \tag{2.22}$$

$$Z_{in\ A}(\omega)|_{Z_l=\infty} = j\frac{\hat{L}\omega_0^2}{\omega}(\hat{k}+1)\frac{\omega^4(\hat{k}-1)+\omega^2\omega_0^2(2-\hat{k})+\omega_0^4(\hat{k}^2-1)}{\hat{k}(\omega_0^2-\omega^2)(\hat{k}\omega^2+\hat{k}\omega_0^2-\omega^2+\omega_0^2)} \tag{2.23}$$

$$Z_{in\ B}(\omega)|_{Z_l=0} = j\frac{\hat{L}\omega_0^2}{\omega}(\hat{k}-1)\frac{\hat{k}(\omega_0^2-\omega^2)(\hat{k}\omega^2+\hat{k}\omega_0^2+\omega^2-\omega_0^2)}{\omega^4(\hat{k}^2-1)+\omega^2\omega_0^2(2-\hat{k})+\omega_0^4(\hat{k}-1)} \tag{2.24}$$

$$Z_{in\ B}(\omega)|_{Z_l=\infty} = j\frac{\hat{L}\omega_0^2}{\omega}\frac{\hat{k}(\omega_0^2(\hat{k}-1)+\omega^2)}{\omega_0^2-\omega^2} \tag{2.25}$$

Firstly, it should be noted that all of these equations are fully complex, meaning that according to 2.19 and 2.20 the power and efficiency at these limits is zero. This is in line with the expectations, as it is not possible to deliver any power to a short or an open.

By analyzing at what frequencies the equations have poles and zeros, it is possible to determine the resonant frequencies of the circuits. These are given in 2.4 and 2.5 for circuits A and B respectively. The zero and pole frequencies are also indicated in 2.8 and 2.9 using dashed and dash-dot lines. The operating frequency f_0 is indicated using a solid line, as it is a pole and a zero in both circuits.

	zeros	poles
$Z_l = 0$	$f = f_0$	$f = f_0\sqrt{\frac{1}{1-\hat{k}}}$
$Z_l = \infty$	$f = f_0\sqrt{\frac{2-\hat{k}\pm\hat{k}\sqrt{5-4\hat{k}}}{2\hat{k}^2-2}}$	$f = f_0 \vee f = f_0\sqrt{\frac{1-\hat{k}^2}{(1-\hat{k})^2}}$

Table 2.4: Poles and zeros in the input impedance for circuit A

It is clear from the graphs that the points of highest efficiency occur when there is a pole in Z_{in}, while highest power transfer occur at zero frequencies. This cannot be seen as a general rule. In appendix A the same power transfer and transfer efficiency plots have been generated over a wider range of source resistances.

	zeros	poles
$Z_l = 0$	$f = f_0 \vee f = f_0\sqrt{\frac{1-\hat{k}^2}{(1+\hat{k})^2}}$	$f = f_0\sqrt{\frac{\hat{k}-2\pm\hat{k}\sqrt{5-4\hat{k}}}{2\hat{k}^2-2}}$
$Z_l = \infty$	$f = f_0\sqrt{1-\hat{k}}$	$f = f_0$

Table 2.5: Poles and zeros in the input impedance for circuit B

Here it can be seen that as the source resistance increases, the points of optimal power transfer migrate from the pole to the zero locations. It does appear that the points of optimal efficiency remain at the pole frequencies.

The behaviour of both circuits at f_0 is quite easily understood. Regardless of any frequency splitting that might occur, the property where at f_0 $Z_{in} = Z_l$ still holds for any $\hat{k}$. In this case, it is a simple case of impedance matching between Z_l and R_s. It follows from circuit theory that optimal power transfer occurs whenever the load and source impedances are complex conjugates. Since it is assumed that the source impedance is fully real, it can be reasoned that optimal power transfer will occur when $Im(Z_l) = 0$ and $Re(Z_l) = R_s$. At this point exactly half of the total available voltage will appear across Z_l, indicating an efficiency of 50%. Increasing the real part of Z_l will cause a drop in power delivered to the load, but an increase in efficiency. Reducing the real part of Z_l will result in less power being delivered and a lower efficiency, as more power will be lost in the source resistance.

The behaviour at frequencies outside f_0 is more complicated. It is clear from the numeric simulations that points of optimal performance likely only occur at poles or zeros in Z_{in}. However, why a resonant frequency under certain conditions acts as a point of optimal transfer, while under different conditions it acts as a point of optimal efficiency is not clear at this point. It is also difficult to predict what performance can be expected at a resonant frequency given a load and source impedance. Further research into this will be required. It can also be noted from appendix A that when the optimal performance transitions from one resonant frequency to another, the frequency in between the peaks might offer higher performance than can be found on either resonant frequency. However, the performance at the resonant frequencies will likely not be significantly worse than the maximum.

In this application the system will perform at f_0. There are several reasons for this. The first is that this is the only resonant peak that does not depend on $\hat{k}$. As it cannot be assumed that $\hat{k}$ remains constant during use, operating at any frequency other than f_0 would require the system to actively track the resonant frequency. This would significantly increase complexity and might even pose problems with spectrum regulations. In addition to this, the impedance mirroring property that exist at f_0 makes load modulation very predictable. This is crucial when it comes to the transmission of data from the slave to the master.

2.2.3. Analyzing the Quality Factor

Only one of the proposed circuits can be implemented in the final prototype, and the analysis up to now does not indicate that one circuit will perform better than the other. However, up to this point only steady state analysis is performed. To make a decision between the circuits it is important to also analyze their dynamic properties. When data is transmitted from either the master or the slave, the state of the system changes. Since the systems contains many reactive components, it takes some time before the system settles into its new state. The shorter the time needed for the system to settle, the faster the data can be transmitted. The speed at which a system settles is determined by its quality factor Q. The quality factor is defined as the ratio between the energy stored in a system and the energy dissipated per oscillation cycle [61]. In practice, this can be expressed using equation 2.26.

$$Q = \frac{\omega E_s}{P_{dis}} \tag{2.26}$$

Here E_s is the average energy stored in the system, and P_{dis} is the average power dissipated.

In order to calculate the quality factor of both circuits, first the total energy stored E_s needs to be determined. This is simply the sum of all the energy stored in the capacitors and the inductors.

$$E_s = \sum E_C + \sum E_L \tag{2.27}$$

To simplify the analysis, it is assumed that the system is perfectly matched (so $\bar{k} = \hat{k}$). In this configuration, the input impedance of the systems are equal to the load impedances. It is also assumed that the load is the

only resistive element in the circuit, meaning that it is responsible for all the dissipation in the circuit. Finally, it is assumed that the load impedance is fully real. Due to the impedance mirroring property of the link this also implies that the link input impedance will be fully real. This indicates that all the reactive elements in the circuit are in resonance. When a circuit is in resonance, all energy stored in the capacitors will be exactly delivered to the inductances in each cycle, so:

$$\sum E_C = \sum E_L \tag{2.28}$$

This simplifies equation 2.27 to:

$$E_s = 2\sum E_C \tag{2.29}$$

The mean stored energy per capacitor can be calculated using 2.30.

$$E_{c,i} = C(\frac{V}{\sqrt{2}})^2 = \frac{1}{2}CV^2 \tag{2.30}$$

Here C is the capacitor value, and V is the magnitude of the AC voltage present over the capacitor. Using conventional circuit analysis, the magnitude of the voltage across each of the capacitors in both circuits during normal operation can be determined. The capacitor voltages found are shown in table 2.6. This analysis was greatly simplified by the fact that the only resistive element in the circuit is the load impedance. Also, since the circuit is assumed to be perfectly matched, the impedance seen at the input is the same as the load impedance. From this we can deduce that $V_{in} = V_{out}$ and $I_{in} = I_{out}$.

Combining equation 2.30 and 2.29 with the equation in table 2.6 gives the following expressions for the energy stored in circuits A and B respectively:

$$E_{s,A} = \frac{1}{2}V_{in}^2[(C_{p,A} + \frac{C_{p,A}}{\omega^2 C_{comp,A}^2 Z_L^2}) + C_{s,A} + \frac{1}{\omega^2 C_{comp,A} Z_l^2}] \tag{2.31}$$

$$E_{s,B} = \frac{1}{2}V_{in}^2[(\frac{1}{\omega^2 C_{p,B} Z_l^2} + \frac{C_{comp,B}^2}{C_{p,B}}) + \frac{1}{\omega^2 C_{s,B} Z_l^2} + C_{comp,B}] \tag{2.32}$$

Plugging in the values for C_p, C_s and C_{comp} from table 2.3 gives:

$$E_{s,A} = \frac{1}{2}V_{in}^2(\frac{1}{\omega^2 \hat{L}(\hat{k}+1)} + \frac{\hat{L}(1-\hat{k}^2)^2}{\hat{k}^2(\hat{k}+1)Z_l^2} + \frac{1}{\omega^2 \hat{L}(\hat{k}+1)} + \frac{\hat{L}(1-\hat{k}^2)}{Z_l^2 \hat{k}}) \tag{2.33}$$

and

$$E_{s,B} = \frac{1}{2}V_{in}^2(\frac{\hat{L}(1-\hat{k})}{Z_l^2} + \frac{1-\hat{k}}{\hat{L}\hat{k}^2\omega^2} + \frac{\hat{L}(1-\hat{k})}{Z_l^2} + \frac{1}{\hat{L}\hat{k}\omega^2}) \tag{2.34}$$

These equations can be simplified algebraically to read:

$$E_{s,A} = \frac{1}{2}V_{in}^2(\frac{\hat{L}(1-\hat{k}^2)}{Z_l^2\hat{k}^2} + \frac{2}{\hat{L}\omega^2(\hat{k}+1)}) \tag{2.35}$$

$$E_{s,B} = \frac{1}{2}V_{in}^2(\frac{\hat{L}(2-2\hat{k})}{Z_l^2} + \frac{1}{\omega^2\hat{L}\hat{k}^2}) \tag{2.36}$$

	topology A	topology B
C_p	$V_{in}\sqrt{1+\frac{1}{\omega^2 C_{comp,A}^2 Z_l^2}}$	$V_{in}\sqrt{\frac{1}{\omega^2 C_{p,B}^2 Z_l^2} + \frac{C_{comp,B}^2}{C_{p,B}^2}}$
C_s	V_{in}	$V_{in}\frac{1}{Z_l\omega C_s,B}$
C_{comp}	$V_{in}\frac{1}{\omega C_{comp,A} Z_l}$	V_{in}

Table 2.6: Magnitude of the voltages across the various capacitors in both A and B circuit topologies.

As explained earlier, the input voltage is the same as the output voltage and all power in the system is delivered to the load. It can thus be stated that:

$$P_{dis} = \frac{V_{in}^2}{2Z_l} \tag{2.37}$$

Combining equations 2.35, 2.36 and 2.37 with the definition of the quality factor given by 2.26 results in equations for the quality factors of both circuits:

$$Q_A = \frac{\omega\hat{L}}{Z_l}\frac{1-\hat{k}^2}{\hat{k}} + \frac{Z_l}{\omega\hat{L}}\frac{2}{\hat{k}(\hat{k}+1)} \tag{2.38}$$

$$Q_B = \frac{\omega\hat{L}}{Z_l}(2-2\hat{k}) + \frac{Z_l}{\omega\hat{L}}\frac{1}{\hat{k}} \tag{2.39}$$

In order to give a more intuitive understanding of what these equations imply, the values for Q over various loads and coupling factors in a typical system have been plotted in figure 2.10. In this simulation $\omega = 2\pi \cdot 13.56MHz$, and $L = 500nH$, which are considered typical values for such a system.

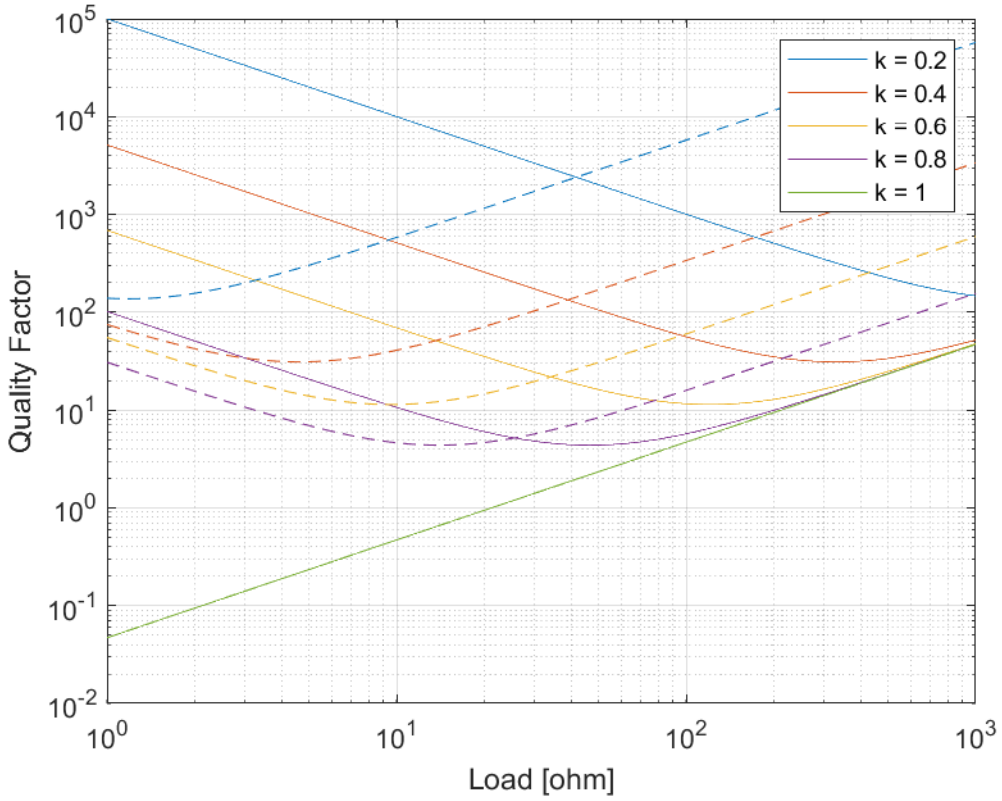


Figure 2.10: Quality factor vs load resistance for various coupling factors for circuit A (solid line) and circuit B (dashed line).

The first conclusion that can be drawn from 2.10 is that both circuits behave the same for $k = 1$. In this case the quality factor will always increase with an increase in the load resistance, in which case the lowest possible load will result in the best performance. Secondly, it can be noted that for any given coupling factor, one topology does not inherently perform better than the other. The only difference is the load impedance at which optimum performance is achieved, with circuit A being better suited to high impedances, while circuit B performs better with lower impedances.

2.2.4. Choosing a Topology

Only one topology can be implemented in the final prototype. While the steady state properties of both circuits are very similar, figure 2.10 shows that circuit A should have better dynamic properties for loads larger

than 30Ω. The system is expected to mostly be operating at these larger loads. Combining this with the manufacturing advantage circuit A has over circuit B, as discussed at the end of section 2.2.1, circuit A has been chosen to be implemented for further testing and verification.

2.3. Coil Design

The physical design of the coils can have a large impact on the performance of the system. Since the coils have to be mounted inside a piece of clothing, they have to be very low profile. For this reason only planar coils where considered for the design. In addition to being planar, it should also be considered that in future developments the coils might be mounted on a flexible substrate, or even sown directly into the fabric. This means that the shape of the coil might distort during use, which could impact performance. The coils designed in this section are only for the proof of concept however. For practical purposes and to limit the scope of the project the coils are made using rigid materials. Actually implementing flexible coils would likely require further analysis.

To reiterate, in section 2.1 it was assumed that the design of the slave and master coils where the same, and had a self inductance of L. The coils in between where also identical to each other, and had a self inductance of L_2. In order to simplify the manufacturing and to maintain the link with the theoretical analysis all four coils are of the same design.

2.3.1. Coil Parameters

When designing a planar coil there are several parameters that should be considered. Firstly there is the number of turns N. This is the dominant factor when determining the self-inductance of the coil. Ideally, the self inductance is proportional to N^2. There is also the track width w and the track spacing s. The track width relates to the quality factor of the coil; as the width increases the resistance of the coil will decrease. The track spacing determines coils capacitance, this sets the self-resonance frequency of the coil. The self resonance effectively acts as an upper bound to the operating frequency. Decreasing the track width decreases the resonant frequency. Finally there are the inner and outer diameters of the coil, d_{in} and d_{out}. These do not directly contribute to the self-inductance of the coil. However, it can be assumed that a larger coil will result in better coupling. The definitions for these parameters are shown in figure 2.11. It should be noted that these are only broad indications of how the parameters affect the characteristics of the coil. In reality the way these parameters interact is quite complex, as will be discussed further in this section.

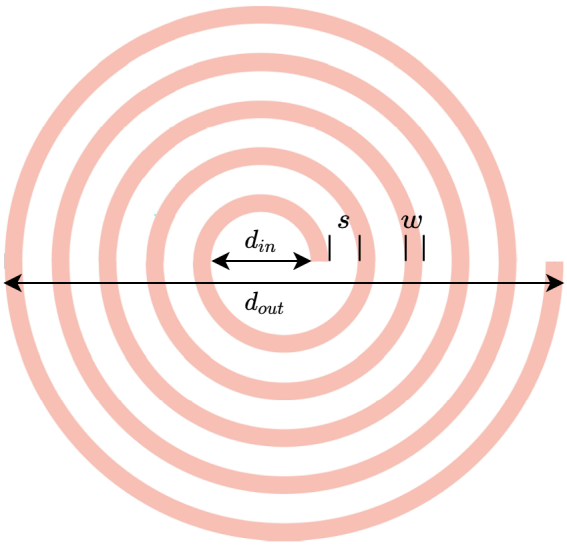


Figure 2.11: Example of a planar coil with the parameter definitions.

According to the link model introduced in the previous chapter, the self-inductance of the coils should not affect the performance of the system. However, this is only true if, among other things, the link is perfectly compensated (meaning that $\bar{k} = \hat{k}$). This can not always be guaranteed. From the equations given in table 2.3 it can be seen that the error caused by mismatched coupling is proportional to $\hat{L}$. $\hat{L}$ is directly correlated to the self inductance of the master and slave coils L. This suggests that coils with a small self inductance are

preferred over those with a large self inductance.

Similarly, according to the same table the actual value of the coupling factor $\hat{k}$ should, under ideal circumstance, not affect the transmission matrix of the link. However, according to figure 2.10, a lower coupling factor will result in a higher quality factor. This will have a detrimental effect on the data transfer speed that can be achieved. It is therefor preferred to have coil pairs that maximize the coupling factor.

Finally, the resistive losses in the coil will also hamper performance. Any real inductor will, in addition to its self inductance, also have a resistive component. This is caused by the limited conductivity of the material the coil is made of. Due to the skin effect, the conductivity will decrease as the signal frequency increases. The prevalence of this effect can be affected by the cross-sectional design of the conductor making up the coil. The resistance of a coil is usually expressed in terms of a coil quality factor, which is defined as:

$$Q_{coil} = \frac{\omega L}{R_{coil}} \tag{2.40}$$

2.3.2. Coil Shape

Before the dimensions of the coil can be determined, a decision has to be made as to the general shape of the coil. In [62] the performance of flexible square, circular, octagonal and hexagonal coils is compared in both a flat and bent position. It is shown that for an equal radius the circular coil has the lowest self-inductance and the highest quality factor. It also showed the least variation when bending; in a fully bent state its self inductance is reduced only by around 20%. For these reasons a circular coil shape is chosen for the design.

2.3.3. Coil Dimensions

The outer diameter of the coil is bounded by what is practical in terms of integration into the fabric. It can generally be assumed that a pair of larger coils will have better coupling and will be less affected by misalignment of the coils. For this reason larger coils are preferred. However, a coil that is too large will be impractical to integrate into a full system. In this design the outer diameter of the coil is set at $50mm$. Determining the optimal inner diameter of the coil require models that predict the self-inductance and coupling of the coils based on their dimensions. In [63] three simple mathematical models for predicting the self inductance of a planar coil are presented. The method based on the current sheet approximation [64] seems most appropriate for this situation. This gives the following expression for the self-inductance of the coil [63]:

$$L = \frac{\mu N^2 (d_{out} + d_{in}) c_1}{4} (ln(\frac{c_2}{\rho}) + c_4 \rho^2) \tag{2.41}$$

where, for a circular coil, $c_1 = 1.00$, $c_2 = 2.46$, $c_4 = 0.2$, and $\rho = \frac{D_{out}+D_{in}}{D_{out}-D_{in}}$. This model does not take w and s into account. In [63] it is noted that the accuracy of the model reduces as $\frac{s}{w}$ increases. However, since the goal is to design a coil with a low self-inductance the number of turns is likely quite low, allowing the use of wide traces to minimize the coil resistance.

Similarly, in [65] a model is presented for determining the mutual inductance of two planar coils. This method relies on the coupling between two concentric current carrying filaments, a technique first shown in [66]. This model is adapted to allow for both lateral and axial displacement of the loops. To determine the complete mutual inductance M between two coils, the mutual inductance between each pair of loops is summed, resulting in a model for M [65]:

$$\begin{aligned} M &= \sum_{i=1}^{N} \sum_{j=1}^{N} M_{i,j} \\ M_{i,j} &= \frac{\mu_0 \pi a_i^2 b_j^2}{2(a_i^2 + b_j^2 + d^2)^{\frac{3}{2}}} (1 + \frac{15}{32}\gamma_{i,j}^2 + \frac{315}{1024}\gamma_{i,j}^4) \\ \gamma_{i,j} &= \frac{2 a_i b_j}{a_i^2 + b_j^2 + d^2} \end{aligned} \tag{2.42}$$

where $a_i = D_{out} - \frac{D_{out}-D_{in}}{N-1}(i-1)$ and $b_j = D_{out} - \frac{D_{out}-D_{in}}{N-1}(j-1)$. The terms caused by the lateral displacement are omitted from this model. As the model is based on zero width filament currents, the track track width is again not taken into account by the model. Because of simplifications made in [65], the model

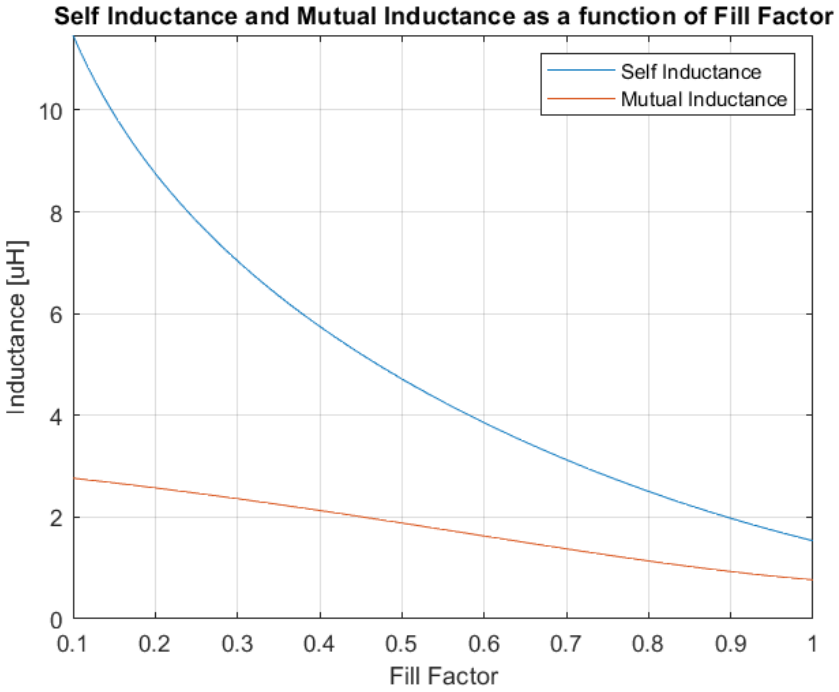


Figure 2.12: L and M as a function of η_{fill} for $N = 5$, $D_{out} = 50mm$, and $d = 5mm$.

becomes more accurate as the coils move apart. In this application the coils are very close ($d << D_{out}$). For this reason the absolute values obtained by the model are not considered accurate. Nevertheless, the trends that appear when varying one of the coil parameters over a fixed separation are considered representative.

To determine the optimal inner diameter, it is useful to consider the fill factor η_{fill}. This is a dimensionless parameter that determines how much of the area inside a coil is taken up by traces. An η_{fill} of 1 represents the situation where the spiral continues all the way to the center of the coil, where in a coil with a fill factor of close to 0 all the windings are concentrated on the outer ring. It is formally defined as:

$$\eta_{fill} = 1 - \frac{D_{in}}{D_{out}} \tag{2.43}$$

By applying the models from equation 2.41 and 2.42 to a fixed coil and varying the fill factor plot 2.12 can be obtained. In the simulation two identical coils where placed at a distance of $5mm$ apart. The coils both had 5 turns, and an outer diameter of $50mm$.

From 2.12 it can be seen that both M and L increase with a decreasing η_{fill}. However, it is clear that L increases faster than M. As stated earlier, an optimal coil maximizes M while minimizing L. The optimal coil therefor has a fill factor of 1, which equates to an inner diameter of 0. Intuitively, this can be explained as follows: the closer two current carrying wires are to each other, the more magnetic interaction there will be between them. In an ideal situation, the traces within a coil would have a minimum of interaction, while maximally interacting with the traces in the coupled coil. By using all the available area to space the traces out, the internal interaction is minimized, while not significantly affecting the interaction with the coupled coil. This results in better performance.

2.3.4. Determining Optimal Number of Turns

The number of turns is an important factor in both the self-inductance and coupling factor of the coils. From 2.41 and 2.42 it can be seen that both L and M are roughly proportional to N^2. However, the number of turns is also relevant to capacitance and resistance of the coil. Given a fixed inner and outer diameter, the turn ratio poses significant restrictions on the width and spacing of the tracks. This can be expressed as $w+s = \frac{D_{out}-D_{in}}{2N}$, meaning that as N increases either the capacitance, resistance, or possibly both will suffer. Additionally, both the coil capacitance and resistance are proportional not only to w and s, but also the total trace length l. This is given by $l = \frac{\pi N(D_{in}+D_{out})}{2}$ [67], indicating that more turns will again result in an increase in capacitance and

resistance. It can therefor be reasoned that the number of turns should be kept as low as possible, while still achieving a decent coupling factor.

To better quantify this trade-off, an ADS Momentum simulation was performed on a number of coils. The number of turns per coil was varied from 2 to 10. The spacing between the traces was set to $0.5mm$. The coils are made up of $35\mu m$ copper, and are backed by an FR-4 substrate. In the simulation setup two identical coils where placed parallel to each other at a distance of $3mm$. The simulation was performed with the coils coaxial, as well as with a lateral displacement of $5mm$ and $10mm$. This should give an indication as to how the coupling factor will vary as the coils move. The results of this simulation are shown in figure 2.13.

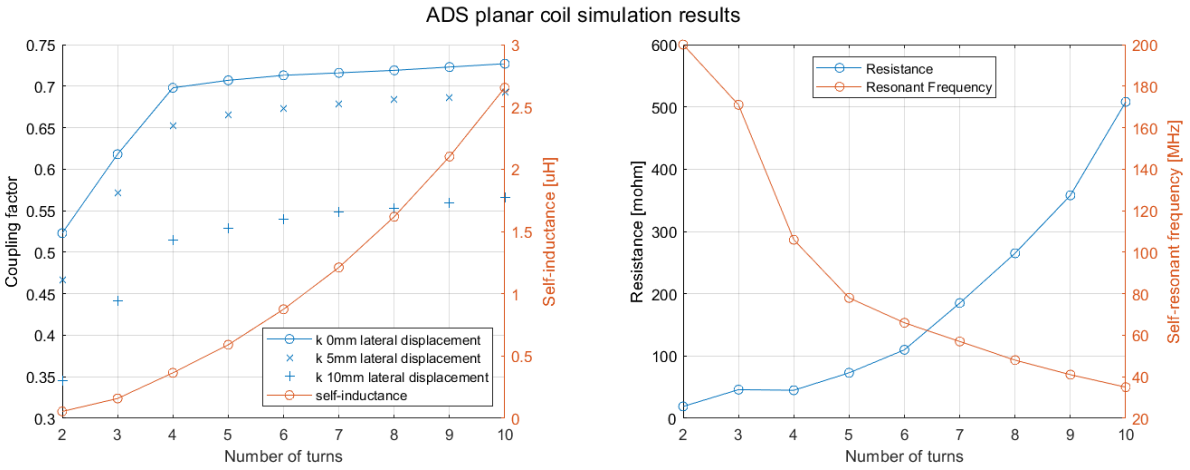


Figure 2.13: ADS Momentum simulation of the self-inductance, coupling factor, coil resistance and resonant frequency as a function of the turn count.

From the simulations it is clear that beyond a turn count of about five, the increase in coupling factor starts to diminish. The self-inductance, coil resistance, and resonant frequency do however continue to worsen. For this reason the number of turns is set at five. A summary of the design specifications of the coil are shown in table 2.7.

N	D_{out}	D_{in}	s	w	L	R	f_{res}
5	$50mm$	$0mm$	$0.5mm$	$4.5mm$	$590nH$	$73m\Omega$	$78MHz$

Table 2.7: Coil design specifications

2.4. Practical Implementation

2.4.1. Compensation Network

A prototype of the compensation network has been build to validate the theory discussed earlier in this chapter. As mentioned before at the end of section 2.2.3, only topology A (figure 2.6 a) is selected for further testing and verification. The side with the compensation capacitance is made as part of the master board, which is the side that contains the power source and therefor generates the signal that travels over the link. The other side is integrated on the same board as the slave, where the power is received. When designing the physical layout of the boards, care has been taken to make the connections between the components as short as possible. This reduces the impact of any potential transmission line effects. For simplicity the wires connecting the inside coils are also kept very short, eliminating any possible transmission line effects there.

On both the master and the slave side, the resonant capacitors consist of a $220pF$ ceramic SMD capacitor in parallel with a $30-90pF$ variable trim capacitor. This allows the compensation network to be tuned to be precisely in resonance with an unloaded coil after manufacturing. The resonant tanks where tuned by applying a $13.56MHz$ signal to a resistor in series with the resonant tank. The capacitor is then tuned until an oscilloscope shows the voltage over just the tank to be perfectly in phase with the voltage over the entire series connection.

For the compensation capacitance a voltage controlled capacitor is used. This is to allow the system to adapt to changes in coupling if required. The capacitor used is a *Murata LXRW19V201*. This is a $100-200pF$

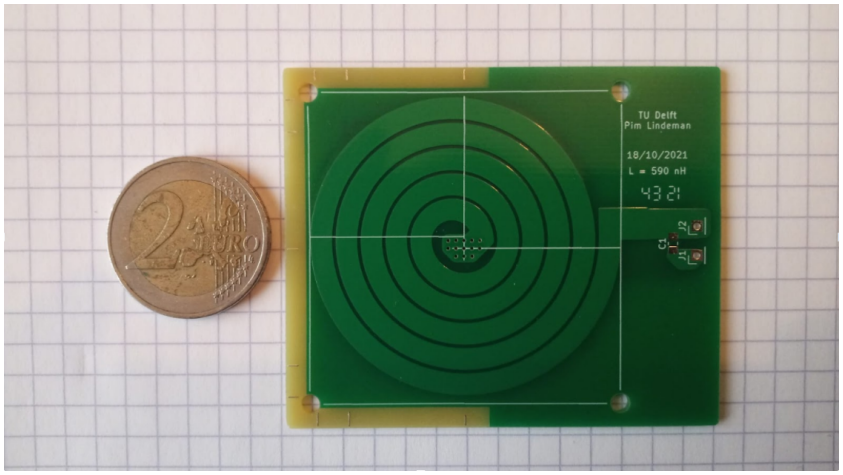


Figure 2.14: Finished coil

voltage controlled trimmer capacitor, designed for use in NFC type applications. It is controlled using a $0-5V$ control signal, and both of the capacitor leads can be floating. This capacitor allows perfect compensation in the range of $0.65 < k < 0.77$. In order to further increase the range, and optional second compensation capacitor can be put in parallel with the first using header pins. This shifts the range to be from 0.77 to 0.86.

2.4.2. Coils

The coil where printed using standard PCB printing techniques onto an FR-4 substrate, according to the parameters specified in table 2.7. The coils themselves are made from $35\mu m$ thick copper foil. A photograph of a finished coil is shown in figure 2.14. The actual measured characteristics of this coil are discussed in the next section.

2.5. Measured Results

2.5.1. Coil Self Inductance

The self inductance of the manufactured coils was measured using an LCR-meter at its maximum frequency of $300kHz$. While it would have been better to measure this at the operating frequency of $13.56MHz$, the resulting inductance should not be greatly affected by the signal frequency. The LCR meter measured an average self inductance of $488nH$, which is significantly lower than the $590nH$ designed inductance. This could be because of some additional parasitic capacitances, most notably caused by the signal return trace on the back of the PCB, as this would likely be registered as a reduction in inductance by the meter. It is expected that this will not have a significant affect on the performance.

2.5.2. Coupling Factor

The same LCR meter was used to measure the coupling between the coils at various axial separations. By connecting the coils in anti-series, the mutual inductance can be calculated by measuring the apparent inductance seen at the input of the circuit. A diagram of the test setup is shown figure 2.15. The equation used to translate from the measured inductance to the coupling factor is shown in equation 2.44.

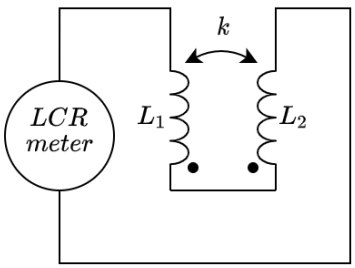


Figure 2.15: Setup for measuring coupling factor

$$k = \frac{L_1 + L_2 - L_{meas}}{L_1 + L_2} \tag{2.44}$$

The coil PCBs where mounted in a rigid holder, with the copper plating facing each other. The holder held the coils co-axially, preventing any lateral movement. The distance between the coils was set by inserting paper shims of varying thicknesses in between the coils. A small weight would be put on top of the top coil to push it down slightly. Using this setup distances could be set with an error of about 7%. In figure 2.16 it is shown that the coupling factor is very close to 1 when the coils are right on top of each other, decreasing to about 0.5 at a coil distance of $5mm$.

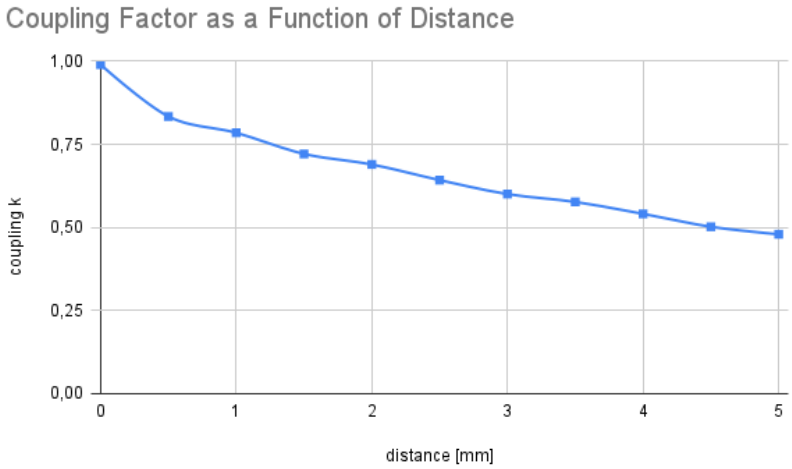


Figure 2.16: Coupling coefficient as a function of distance

2.5.3. Coil Resistance

The resistance of the coil is also a important factor when it comes to the overall efficiency of the system. However, since the expected resistance of the coil is very small, this is difficult to measure accurately. This difficulty was exacerbate by the fact that the resistance must be measured at the operating frequency. Due to the skin effect the resistance of a wire increases with an increase in frequency. In order still to get a good estimate of the resistance, two different measurement setups where used.

The first method is based on measuring the decay time of a resonator formed by the coil undergoing testing. The coil is connected through a switch to a reference capacitor. The value of this capacitor is tuned such that the coil and capacitor pair form a resonant tank with a natural frequency of $13.56MHz$. To measure the resistance, the coil is first disconnected and the capacitor is charged to a fixed voltage. Then the switch is pulled, disconnecting the capacitor from the voltage source and connecting it to the coil. The voltage over the coil will now appear as a exponentially decaying sine wave, which can be measured using an oscilloscope. A schematic overview of the measurement setup, as well as an example waveform, is shown in figure 2.17.

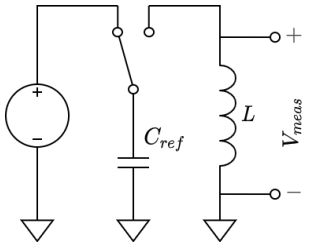
By measuring the voltage at two peaks, as well as the time between them, this decay can be characterised. From here the total resistance in the resonator can be determined:

$$R = \frac{2Lln(\frac{V_1}{V_2})}{\Delta t} \tag{2.45}$$

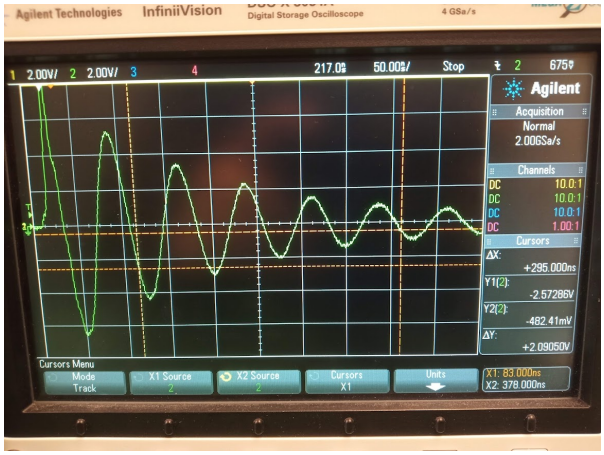
Here V_1 and V_2 are the voltages measured at two of the peaks, with Δt being the delay between them.

This method measures the entire resistance in the loop. However, it is assumed that coil resistance is dominant over the other components. The results from this setup proved somewhat inconsistent. The results after 10 runs was a mean RF resistance of 4.90Ω, with a standard deviation of 1.45Ω. This large deviation could in part be caused by variations in the conductivity of the switch.

The second setup also also revolves around measuring the performance of the coil when made part of a resonator tank. However, this time the measurements are done in the frequency domain. The coil is again connected in parallel with a reference capacitor, such that their resonant frequency is $13.56MHz$. A



(a) Schematic of measurement setup



(b) Example of a measured waveform

Figure 2.17: Setup for measuring coil resistance using time domain decay

13.56MHz signal is applied through a known 20Ω shunt to the resonant tank. By measuring the voltage before and after the shunt, the current flowing into the tank can be determined. From this the total resistance in the tank can be calculated. A schematic representation of this setup is shown in figure 2.18.

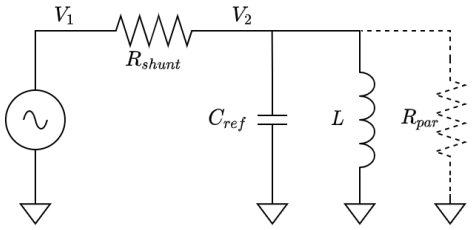


Figure 2.18: Schematic of the second setup used to determine the coil resistance. R_{par} is an apparent resistance caused by the parasitic resistances of the resonant tank.

In the ideal case, the parallel combination of C_{ref} and L can be seen as an open circuit at the resonant frequency. However, due to parasitic resistances in the loop, some current can still flow into the tank. This behaviour can be modeled as an ideal capacitor and inductor in parallel with a resistance, as shown in figure 2.18. By measuring the voltages at V_1 and V_2 this parallel resistance can be determined:

$$R_{par} = \frac{R_{shunt} V_2}{V_1 - V_2} \tag{2.46}$$

This equivalent resistor encapsulates the entire resistance of the loop. Again, it is assumed that the coil resistance is dominant. In order to relate this equivalent parallel resistance to the series resistance of the coil, the quality factor of the resonator is considered. If the same components where placed in a series resonant tank, the quality factor would not change. However, in that case the cumulative parasitic resistance would have appeared to be in series with both the capacitor and the inductor. Since it is assumed that the entire parasitic resistance is caused by the coil, this apparent series resistance would be equal to the coil resistance. The quality factor for the parallel resonator is given by:

$$Q_{par} = R_{par} \sqrt{\frac{C_{ref}}{L}} \tag{2.47}$$

And for a series resonator it is:

$$Q_{ser} = \frac{1}{R_{ser}} \sqrt{\frac{L}{C_{ref}}} \tag{2.48}$$

Equating Q_{par} and Q_{ser} and solving for R_{ser} gives:

$$R_{coil} = R_{ser} = R\frac{L}{C_{ref}R_{par}} \tag{2.49}$$

Based on the above shown method an average coil resistance of 4.44Ω was found. This is somewhat in agreement with the previous experiment, which showed an average coil resistance of 4.90Ω. However, both values are more than an order of magnitude higher than what was predicted in chapter 2.3. Additionally, the results obtained in later experiments involving coupled coils are not consistent with such high coil resistances. The current hypothesis is that the energy loss measured in these experiments are not due to resistive heat losses, but is rather energy lost in the form of EM radiation. This would explain why the losses do not appear in cases where the coils are coupled. The energy radiated out would then not be perceived as energy lost, but rather as energy being transferred from one coil to another. However, this hypothesis has not been tested.

2.5.4. Impedance Mirroring

The defining characteristic of the link compensation network as described in this chapter is that, if it is tuned correctly, it mirrors the impedance at the output to the input. In order to verify that the circuit indeed has this property, an experiment was devised. In this experiment the circuit was loaded with resistances ranging from a short to 200Ω, while the value of the compensation capacitor was stepped in steps of $5pF$. The resulting impedance at the input of the link was measured by measuring the voltage before and after a 20Ω shunt at the input. A schematic of this setup is shown in 2.19. The input signal was provided by a function generator. This experiment was performed at coil distances of $1mm$, $1.5mm$ and $2mm$. Both coil pairs where set at the same distance.

The RMS values of the voltages at V_{gen} and V_{in}, as well as the phase difference between them θ, are measured using an oscilloscope. Using this the current flowing into the link can be determined:

$$I_{in} = \frac{V_s - V_{in}e^{j\theta}}{R_{shunt}} \tag{2.50}$$

This is then used to calculate the magnitude of the input impedance:

$$|Z_{in}| = |\frac{V_{in}}{I_{in}}| \tag{2.51}$$

The resulting impedances are plotted in 2.20.

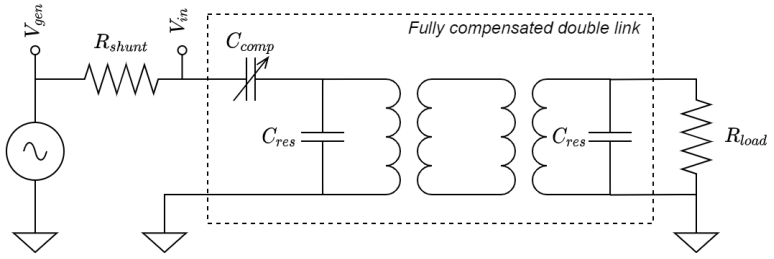


Figure 2.19: Schematic of the setup used to measure the power efficiency of the double link

From the graphs in 2.20, it can be seen that there exists an optimum value for the compensation capacitance. At this point a variation in the output impedance will result in a maximum variation of the input impedance. As the distance between the coils changes, the value of the compensation capacitance at which this optimum is achieved shifts.

It can also be noted that at this optimal point, the input impedance of the link matches the load impedance most closely, especially at lower values of R_{load}. This is the impedance mirroring that was expected from this circuit. However, the higher ohmic loads show quite a large deviation between the input impedance and the load impedance, even at the optimal operating point. There are two plausible reasons for this: the first is that there is a systematic error in the measurements. The two voltage signals where measured simultaneously using two separate oscilloscope probes. While great care was taken to tune these probes, it is inevitable that

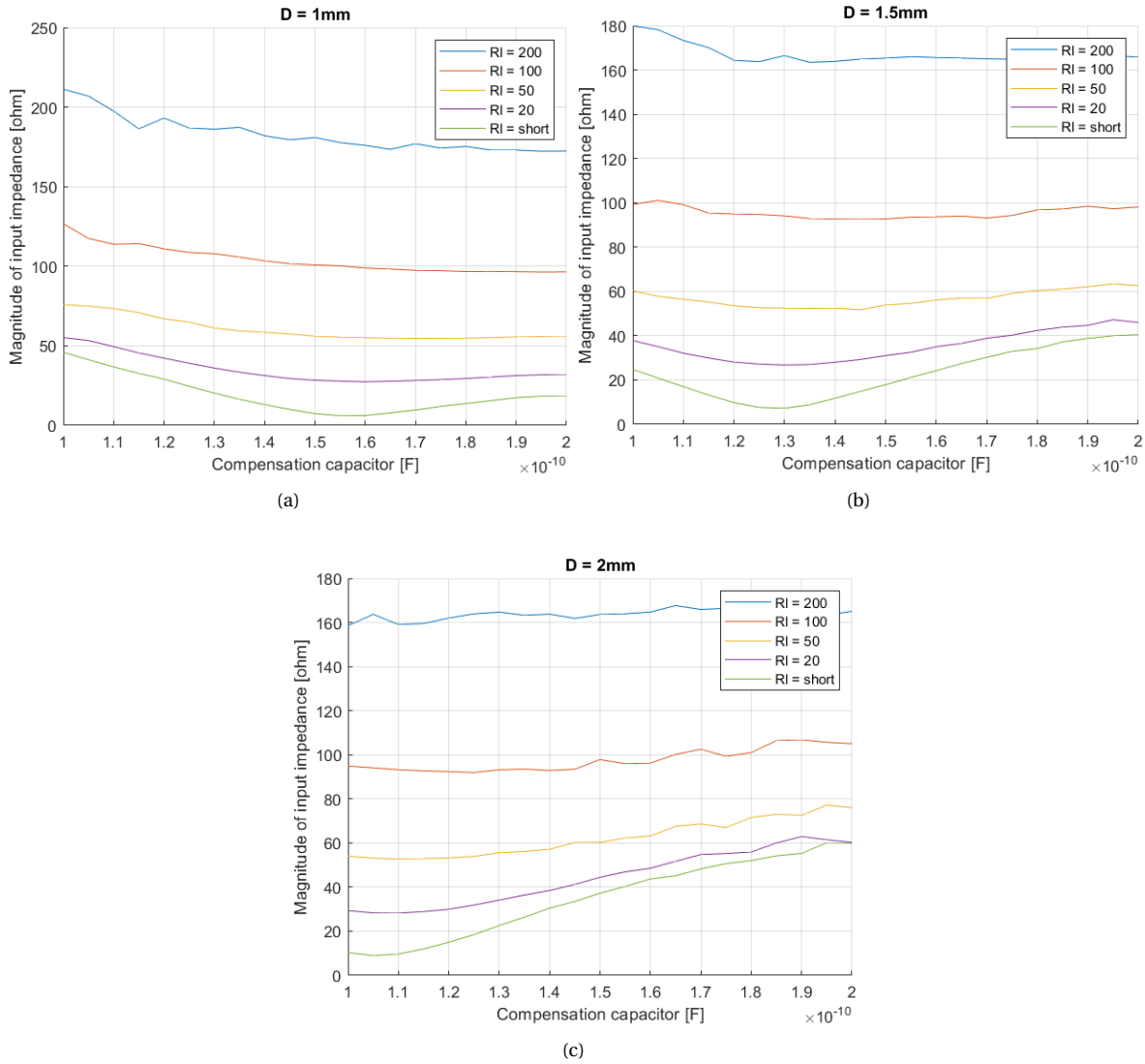


Figure 2.20: Graphs showing the magnitude of the input impedance of the link as a function of C_{comp} and load resistance. Each graph corresponds with a different coil separation D.

there was still a small deviation in their signal response. This error will be most apparent at the higher ohmic loads, as the current that is being measured is much smaller.

Secondly, it is also possible that the resonant capacitors where not perfectly tuned. The technique for tuning the resonant capacitors is discussed in 2.4, and involves measuring the voltage over the coil using an oscilloscope. The parasitic capacitance associated with the oscilloscope probe could introduce a small error when tuning the capacitance. Simulations show that a miss tuned resonant capacitor will introduce some impedance transformation.

It should also be noted that these measurements are not consistent with the coil resistance of $4-5\Omega$ that where found in 2.5.3. Because of the aforementioned measurement errors it is not possible to use these measurements to quantify the coil resistance with any accuracy, but the results are most consistent with an R_{coil} of several hundreds of $m\Omega s$. This is much more in line with the values expected from the simulations done in section 2.3.

2.5.5. Phase Characteristics

Also of particular interest to the working of the system is the phase difference between the voltage and the current at the input of the link. Using the same raw data as in the previous section, the current phase angle

can be plotted against compensation capacitance. The results of this are shown in figure 2.21.

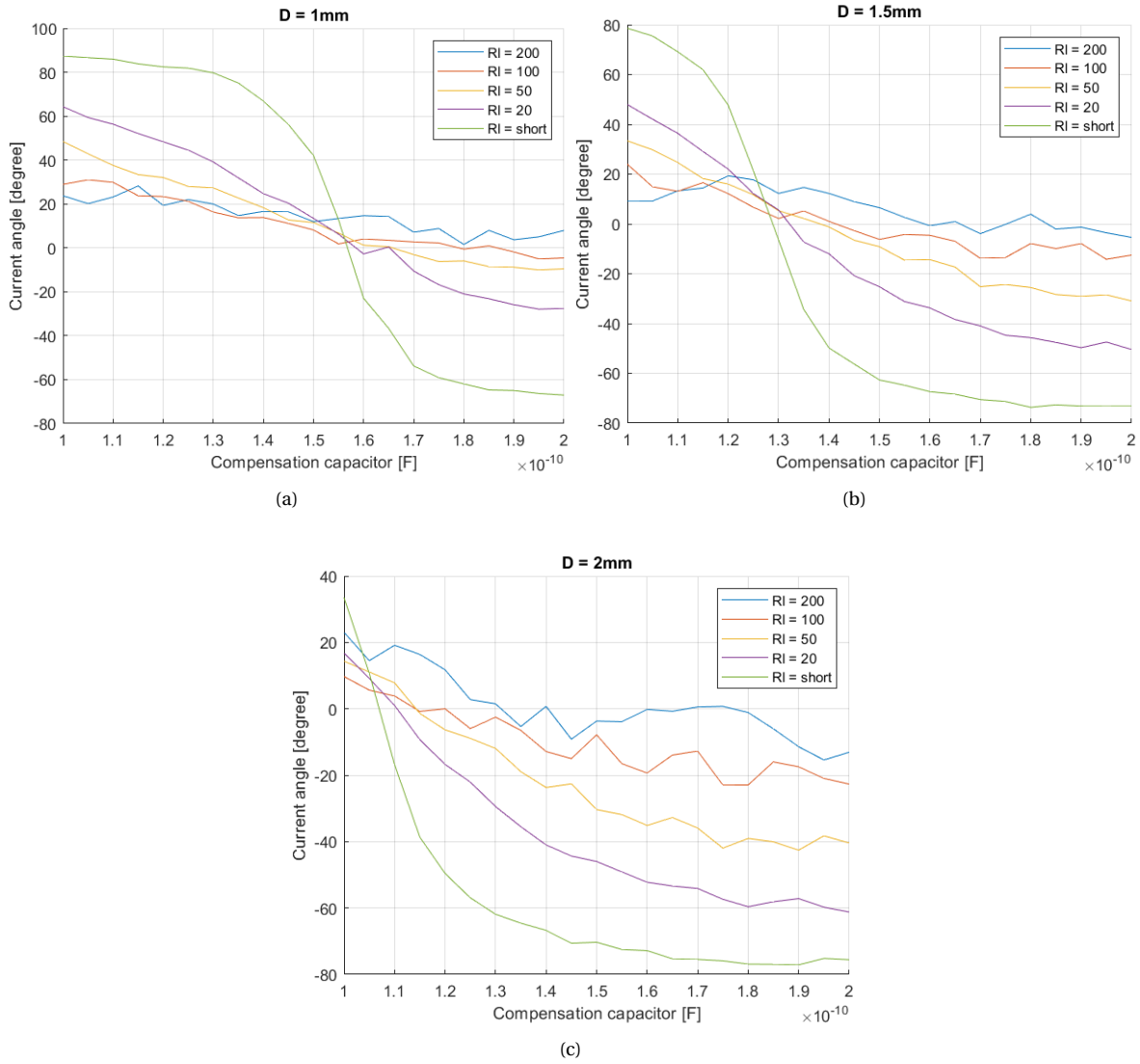


Figure 2.21: Graphs showing phase difference between the current and voltage at the input of the link.

The theory suggests that when the compensation capacitor is perfectly tuned, the voltage and the current are perfectly in phase. The results in 2.20 and 2.21 confirm this. The point where the link input impedance most closely matches the load resistance is also the point where in 2.21 the current phase passes through 0.

There are some further things that can be noted from these results. Firstly, the lower ohmic loads show a more drastic phase shift when moving past the point of optimal compensation. This also follows from the theory.

Secondly, it appears that the value of the load resistance has a slight impact on the place where the current phase crosses the 0 degree line. As the ohmic load increases, the zero crossing moves further right. This is likely due to the fact that the phase measurements suffer from the same errors as the impedance measurements.

3

Master Design

In this chapter the design of the master is discussed. The master serves as an interface between the link and the central node. It receives power from a $5V$ supply on the central node, and transmits this across the link via the slave to the sensor node. It is also responsible for decoding the sensor data send by the slave, and it has to be able to issue commands to the sensor. Finally, it is responsible for maintaining the link by actively tracking and compensating for variations in the coupling between the coils. A block diagram of the master and how it relates to the other parts of the design are shown in figure 1.3 in chapter 1.

3.1. Theory and Design

3.1.1. Carrier Generator

The purpose of the carrier generator is to generate the signal that will drive the coil. Since this is the signal the slave will extract the power from, the generator needs to be able to source quite a large current. In addition, the voltage also needs to be relatively high. The reason for this is twofold: firstly, having a higher voltage signal means that less current is required to deliver the same amount of power to the load. Since the resistive losses in the coils are proportional to the current, operating at a higher voltage will reduce the coil losses. Secondly, it simplifies the design of the slave. Since the link is designed in such a way that the load impedance is mirrored to the input, there is no voltage transformation occurring in the link. This means that the AC voltage seen at the slave side is at most equal to carrier voltage. Since both the efficiency of the rectifier and any subsequent DC-DC conversion increases with voltage, having a higher voltage signal will improve the efficiency of the slave.

There are essentially two RF power amplifier types commonly used in WPT systems: class-D [68][69][70][71] and class-E [72][73][74][75][76][77] systems.

Both topologies are switch-mode amplifier designs, meaning that the transistors (usually MOSFETs) act as switches, being either fully open or fully closed. These types of amplifiers generally have greater efficiency than their linear counterparts. When designed properly, voltage and current will not exist simultaneously in the transistors. Since the consumed power is the product of voltage and current, no power is dissipated in them, resulting in a theoretically maximum efficiency of 100%. In order to reach this maximum efficiency, it is important that the transistors only turn off if the voltage across them is 0. This is known as Zero Voltage Switching or ZVS. This is because all transistors have parasitic capacitances associated with them. Any charge build up in these capacitors will drain away through the transistor when it turns on. When the source-drain voltage is 0, this source of energy loss is minimized.

Another often quoted requirement for switch-mode power amplifiers is Zero Voltage Derivative Switching (ZVDS). This implies that the slope of the voltage should be (near to) zero as the switch closes. This is not a hard requirement for efficient operation; instead it allows for some wiggle room when implementing ZVS [78]. If the slope of the voltage is low, a small deviation in turn-off timing will not result in a large voltage being switched. It also allows for more graceful handling of the non-instant switching of the transistor.

Class-D amplifiers come in two types: half bridge and full bridge. Common topologies for both are shown in 3.1, although other variants do exist [79]. In a half bridge design, the two transistors M_1 and M_2 sequentially turn on at the operating frequency. This generates a square-wave going from $0V$ to V_{DD} at the drain of M_2. The higher order harmonics of this square wave are then filtered out by L_{res} and C_{res}, resulting in a

(mostly) sinusoidal signal with an amplitude of V_{DD} being supplied to the load. The full-bridge version works essentially like a differential version of the half bridge design; instead of the load being referenced to ground, it is referenced to a second half-wave inverter operating at a 180°phase shift.

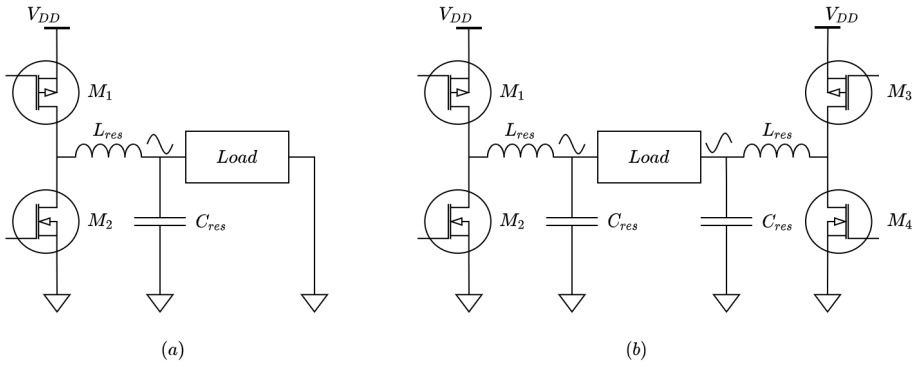


Figure 3.1: Class-D half bridge (a) and full bridge (b) schematic.

In a figure 3.2 a class-E inverter is shown [78]. This topology relies on only a single transistor. This transistor is connected through a large choke inductor to the positive supply. This choke inductor is large enough that it will act as a DC current source. When the switch is closed, this current can flow through the transistor to ground. When the switch opens, current flows through a series resonant tank into the load. The resonant tank is tuned to allow signals at the operating frequency to pass to the load. However, the sudden switching of M_1 will also introduce many higher order components, which are blocked by both L_{res} and L_{choke}. To prevent these from causing large voltage spikes, C_{par} is added to allow the high frequency components of the current to escape to ground.

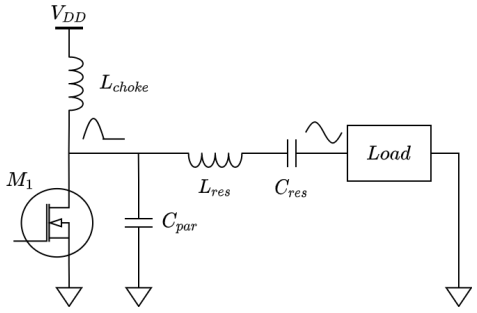


Figure 3.2: Class-E schematic.

The class-D design has several benefits over the class-E inverter. Firstly, in a class-E inverter the voltage over the transistor can be upwards of $3V_{DD}$ [80]. This puts a lot of strain on the transistor, which may cause it to fail sooner. In addition, the large choke inductor required in the class-E design might be difficult to implement in an integrated design.

However, the class-D implementation also has some limitations compared to the class-E. In a class-D amplifier the timing of the signal driving the transistors is crucial. M_1 and M_2 can at no point both be conducting, as this would cause a short circuit from V_{DD} to ground. Because of this there needs to be some dead-time in between the turning on and off of the transistors. Making this dead-time too long will reduce the output power, while making it too short will increase the risk of short circuit. Although this effect generally does not pose an issue at low frequencies, as the frequency increases this becomes increasingly more difficult to address. Another advantage of the class-E design is that the parasitic drain-source capacitance of the transistor can be absorbed into C_{par}.

Because of the complex timing required for a class-D system, a class-E type amplifier has been chosen in this design. However, some modifications from the design shown in figure 3.2 have been made. The resonator tank at the output has been removed. The idea behind this is as follows: the compensation network that proceeds the amplifier is itself a resonant network. Any higher order frequency components should therefor

not make its way very far through the signal chain. The addition of a series resonant tank would however increase the energy stored in the system. As stated in chapter 2, this will result in a higher overall quality factor. This will have a detrimental affect on how fast data can be transmitted across the link.

The modified inverter will now be analyzed. In figure 3.3 two equivalent circuits are shown, one where the switch is open (a) and one where the switch is closed (b). An open switch is modeled using an open circuit. When the switch is closed it is assumed to have a resistance R_{on}, the impedance of which is assumed to be small enough that C_{par} is shorted. The choke inductor has also been renamed L_{shunt}, as it no longer only functions as a choke. The switch opens and closes periodically at the operating frequency f_{op}. The switch opens at $t = 0 + kT$, and closes again at $t = DT + kT$. Here T is the period $\frac{1}{f}$, D is the duty cycle, and k is any integer, from here on considered to be 0.

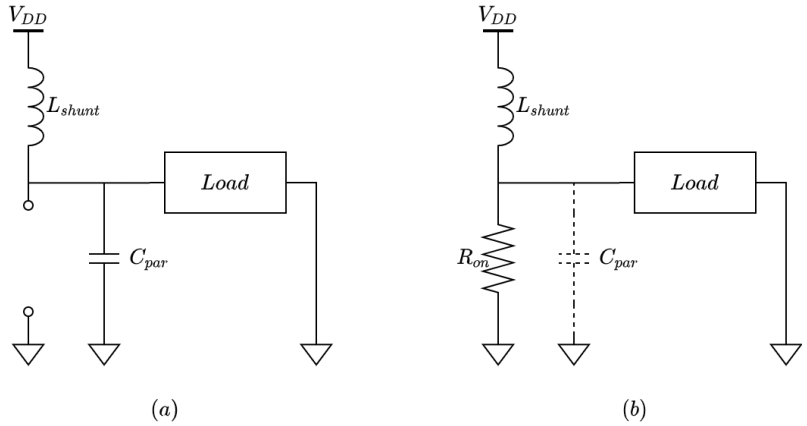


Figure 3.3: Equivalent circuit of the modified class-E inverter for $0 < t < DT$ (a) and $DT < t < T$ (b).

When the switch is open (3.3 (a)) the circuit behaves as a parallel resonant tank with a DC offset. It is assumed that over the time period of interest the load is not able to significantly dampen the oscillation. The voltage at the output of the inverter can therefor be assumed to be in the general form of:

$$V(t) = Asin(\omega_0(t-\tau)) + V_{DD}, \quad 0 < t < DT \tag{3.1}$$

where $\omega_0 = \frac{1}{\sqrt{L_{shunt}C_{par}}}$. When the switch closes, the output voltage is forced to be zero:

$$V(t) = 0, \quad DT < t < T \tag{3.2}$$

This behaviour is visualized in figure 3.4.

ω_0 and D are design parameters, while A and τ follow from the boundary conditions of the system. The goal is to determine what ω_0 is optimal for a given D, and determine the waveform characteristics A and τ for the system. In order to do this the circuit is analyzed in steady state. In steady state it can be assumed that the state of the circuit at the end of a cycle is the same as at the beginning of a cycle. Applying this logic to the inductor current and capacitor voltage gives:

$$I_L(0) = I_L(T) \tag{3.3}$$

$$V(0) = V(T) \tag{3.4}$$

The inductor current can be defined as the integral over the inductor voltage:

$$I_L(t) = \frac{1}{L_{shunt}} \int_0^T V_L(t)dt + I_L(0) \tag{3.5}$$

Combining equations 3.1, 3.3, and 3.5 gives the following boundary condition:

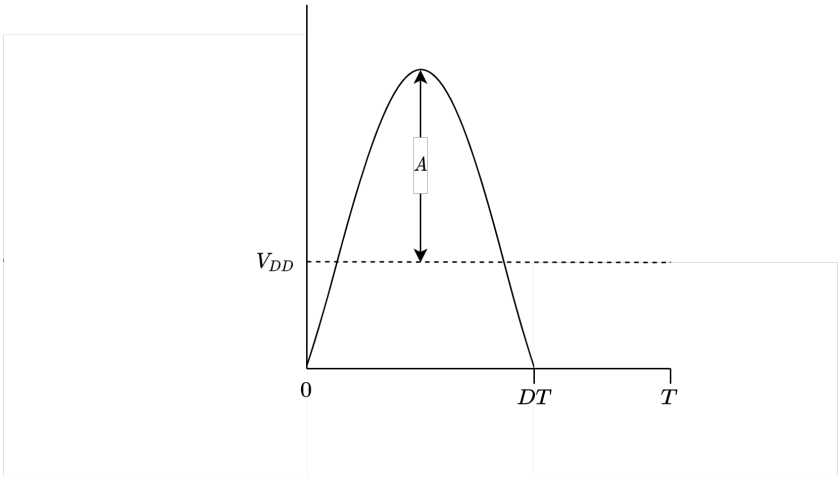


Figure 3.4: Sketch of the expected voltage waveform.

$$\int_0^{DT} Asin(\omega_0(t-\tau))dt - \int_{DT}^{T} V_{DD}dt = 0 \tag{3.6}$$

During the second half of the cycle the output voltage is pulled to zero by the transistor. Combining this with equations 3.4 and 3.1 gives the second boundary condition:

$$V(0) = -Asin(\omega_0\tau) + V_{DD} = 0 \tag{3.7}$$

Finally, imposing ZVS on the system gives a third boundary condition:

$$V(DT) = Asin(\omega_0(DT-\tau)) + V_{DD} = 0 \tag{3.8}$$

Sadly, a way in which 3.6, 3.7 and 3.8 can be combined to give an ω_0, A and τ for a given D has not been found. However, by combining 3.6 and 3.7, an optimal ω_0 and τ can be determined from a given A and D:

$$\omega_0 = \frac{-2arcsin(\frac{V_{DD}}{A}) - \frac{\pi}{2}}{DT} \tag{3.9}$$

$$\tau = \frac{DT}{2} - \frac{\pi}{2\omega_0} \tag{3.10}$$

Similarly, a closed form solution for A for a given ω_0, D and τ can also be obtained:

$$A = \frac{\omega_0(1-D)TV_{DD}}{cos(\omega_0\tau) - cos(\omega_0(DT-\tau))} \tag{3.11}$$

It is possible to numerically determine valid values for all parameters. By sweeping A in equations 3.9 and 3.10 and checking if the obtained values satisfy the boundary conditions (to a given precision) valid waveforms can be generated. In figure 3.5 the waveforms as well as their spectral components for duty cycles ranging from 0.5 to 0.9 are shown.

From figure 3.5 it is clear that as the duty cycle approaches one the waveform converges to a sine wave with an amplitude of V_{DD}. A duty cycle close to one also approaches ZVDS. A lower duty cycle does increase the signal amplitude, which does also partially translate to an increase in power transmitted at the fundamental frequency.

In order to further quantify the efficiency for various duty cycles it is also useful to consider the spectral efficiency. This is defined as the power transmitted at the fundamental divided by the total transmitted power. The spectral efficiency for a wide range of duty cycles is plotted in figure 3.6. From the plot it is clear that for a duty cycle of 50% the efficiency is not much better than that of a square wave. However, at duty cycles of upwards of 80% the spectral efficiency is near to 100%.

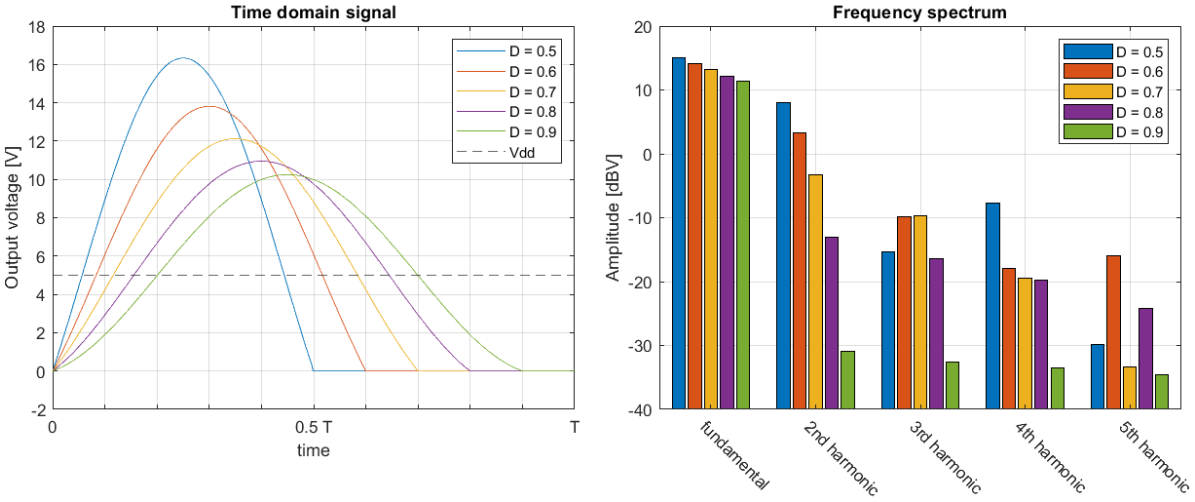


Figure 3.5: Time domain waveforms for different duty cycles and their frequency spectra.

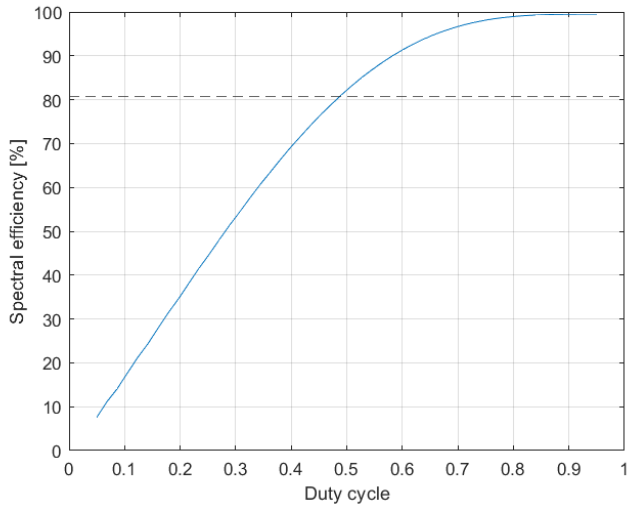


Figure 3.6: Spectral efficiency as a function of duty cycle. The dotted line represents the spectral efficiency of a 50% duty cycle square wave.

In the above analysis it is assumed that the quality factor of the resonator formed by L_{shunt} and C_{par} is infinite. SPICE simulations show that the shown model is still valid for $Q > 6$ for a duty cyle of 50%, and $Q > 25$ for a duty cycle approaching 100%. If the quality factor drops to far ZVS will no longer be maintained, resulting in a significant loss in efficiency. The quality factor for a parallel resonator is given by $Q = R_{load}\sqrt{\frac{C_{par}}{L_{shunt}}}$, meaning that in order to drive small impedances a large capacitor along with a small inductor is preferred.

In addition, any capacitive load, as well as any parasitic drain-source capacitance in the transistor, will be in parallel with C_{par}. If C_{par} is designed to be very small, these capacitances become dominant in determining ω_0. In some cases this might not pose a problem or might even be desired, but sometimes these capacitances might be ill defined or time-variable. In these cases it can be difficult to achieve ZVS. A large C_{par} will increase the systems resilience to this effect.

There are however drawbacks to using a large capacitor. If the duty cycle is not perfectly aligned with the resonant frequency, the transistor might switch with a small voltage still being present over the capacitor. The losses incurred by this are proportional to the energy still stored in the capacitor: $E_c = \frac{1}{2}CV^2$. Having a large capacitor will increase the losses caused by imperfect timing.

There are also drawbacks to operating at very high duty-cycles. While this significantly increases the spectral efficiency of the inverter, it requires the clock signal driving the inverter to be very well defined. As the

duty cycle of a square wave deviates from 50%, the bandwidth the signal occupies increases. This could pose a problem when trying to drive the gate capacitance of the MOSFET.

3.1.2. Coupling Estimation

As explained in chapter 2, it is required for the master to have an estimate of the coupling in the inductive link. Based on this estimate the master can adjust the compensation network to maintain optimal performance. This can be done on either the side with the power source (primary side estimation), or the side that is harvesting the energy (secondary side estimation).

The most direct method of estimating this is to measure the power received by the WPT receiver [81], which is a form of secondary side estimation. This is a very sensible approach, as it often is not the actual coupling factor that needs to be optimized, but rather the power being transmitted across the link. If required, it is possible to determine what the coupling factor would have been to produce these results [82] [83], although this is computationally quite complex [84]. The downside of secondary side estimation is that this information is only known at the receiver side, meaning that the coupling needs to be either corrected on this side, or transmitted to the primary side in some way.

Because the primary side generally is less constrained in power use and area, it is preferred to have both the estimation and correction be performed here. There are several ways of achieving this. In [85] the coupling is estimated by looking at the bifurcation frequencies. The link between bifurcation and coupling factor is further explored in chapter 2. This method is however difficult to implement, as it requires analyzing the performance over a wide frequency spectrum. k can also be estimated by analyzing the relation between the voltage and current in the primary coil [86] [87]. The equations required for this are quite complex. In [84] an attempt is made to simplify them by analyzing the fifth harmonic, instead of the fundamental.

However, in some systems it might not be necessary to know the exact coupling factor. If the polling rate and the speed at which the system can adapt is significantly faster than the rate at which the coupling naturally varies, it can be sufficient to measure if the current estimate $\bar{k}$ is too high, too low, or "good enough". If the performance is not satisfactory, the estimate can be adjusted up or down based on the measurements.

It has been suggested to detect a mismatch in source and impedance by measuring the reflected EM wave [88]. Here the carrier signal is send to the receiver via a directional coupler. A directional coupler is a transmission line device which has the property of isolating the reflected wave to a separate port, instead of sending it back to the source. The amplitude of this reflected wave determines how well the system is compensated, it being optimal when the amplitude reaches zero. Based on the phase between the reflected and transmitted signals a decision can be made on what action should be taken to optimize the system.

In our design, the current phase is used to estimate the coupling factor. As is demonstrate in section 2, for a purely resistive load the current and the voltage are only in phase if C_{comp} is tuned perfectly. If the compensation capacitor is set too low, the current will lead the voltage, and if it is set too high, it will lag. By measuring the current phase it should therefor be possible to tune the system.

Accurately measuring the current is not trivial. In order for the phase to be measured, the current would have to be converted to a voltage, which can then be compared to the carrier signal. Ideally, this current measurement would not impact the carrier signal in any way, and would also not introduce any additional distortion or phase shift. The simplest way of measuring the current would be to introduce a shunt resistor into the signal path, and to measure the voltage over this resistor. This does require an unpleasant trade-off: a small resistor would only produce a small signal, which would be difficult to measure accurately. If the resistor is increased in size, it would increase the measurement accuracy, but also start to dissipate more energy. This would result in a significant reduction in power transfer efficiency.

In order to avoid this trade-off, the current is instead measured using a transformer. The current flowing to the coil will pass through the primary side of the transformed. This will induce a current in the secondary side, which is then fed to a trans-impedance amplifier to convert to a voltage. A schematic of this circuit is shown in figure 3.7. The voltage-current behaviour of a transformer is defined as:

$$\begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} j\omega L_1 & j\omega k_1\sqrt{L_1 L_2} \\ j\omega k\sqrt{L_1 L_2} & j\omega L_2 \end{bmatrix} \begin{bmatrix} I_{coil} \\ I_{sense} \end{bmatrix} \tag{3.12}$$

Assuming the trans-impedance amplifier presents a load Z_{amp} at the output, the following current relation is obtained:

$$I_{sense} = \frac{j\omega\sqrt{L_1 L_2} I_{coil}}{Z_{amp} j\omega L_2} \tag{3.13}$$

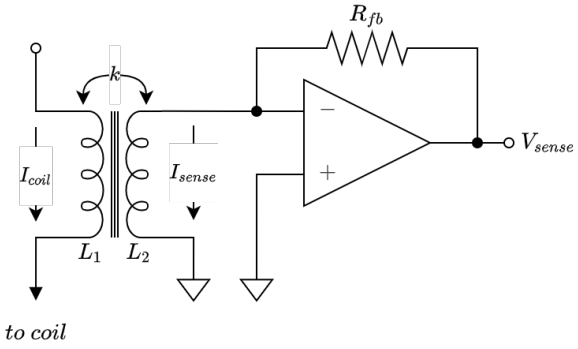


Figure 3.7: Schematic of the current sense network, including the trans-impedance amplifier.

In the ideal case $Z_{amp} = 0$. The output current then approaches:

$$I_{sense} = k\sqrt{\frac{L_1}{L_2}} I_{coil} \tag{3.14}$$

Because any impedance at the secondary side of a transformer is seen from the primary side, the current sense circuit will still load the carrier signal. This load can be represented as an impedance Z_{sense} in series with the transmitting coil. The value of this load is given by:

$$Z_{sense} = j\omega L_1 + \frac{\omega^2 k^2 L_1 L_2}{Z_{amp} + j\omega L_2} \tag{3.15}$$

The secondary side of the transformer is attached to an op-amp based current-to-voltage amplifier. Assuming a limited gain amplifier, the output voltage of such a circuit is given by:

$$V_{sense} = \frac{I_{sense} R_{fb} A_v}{A_v + 1} \tag{3.16}$$

Where A_v is the voltage gain of the op-amp at the operating frequency. The input impedance is given by:

$$Z_{amp} = \frac{R_{fb}}{A_v + 1} \tag{3.17}$$

Combining the above equations with equations 3.13 and 3.15 gives the following expressions for the sense voltage and load impedance:

$$V_{sense} = \frac{-j\omega k\sqrt{L_1 L_2} A_v R_{fb} I_{coil}}{R_{fb} + j\omega L_2 (A_v + 1)} \tag{3.18}$$

$$Z_{sense} = j\omega L_1 - j\omega k^2 L_1 + \frac{j\omega R k^2 L_1}{R + j\omega L_2 (A_v + 1)} \tag{3.19}$$

In the ideal case, the sense voltage given in 3.18 would be as high as possible, and would be fully real, indicating no phase shift. Maximizing the amplitude is done by increasing R_{fb}. However, there is a limit to how far this can be increased, as it has a detrimental effect on both the phase performance and the input impedance. Conversely, increasing L_2 will decrease the gain, but will have a positive effect on both the phase performance and the input impedance. The only factors that have an unequivocally positive effect when increased are the op amp gain A_v and the coupling factor k. Finally, from the equation for the sense impedance in 3.19 it can be noted that in order to minimize Z_{sense} the self inductance of the primary coil L_1 should be minimized.

In order to make sense of this trade-off, the performance of a system as a function of the op-amp gain is plotted in figure 3.8. Here $L_1 = 200nH$, $L_2 = 2\mu H$, $k = 0.98$, and $R_{fb} = 10\Omega$. These are considered typical values.

As is clear from figure 3.8, after a voltage gain of about 100 the performance will no longer increase significantly. This is beneficial, as high gain op-amps tend to require more power. While this is not very high for an

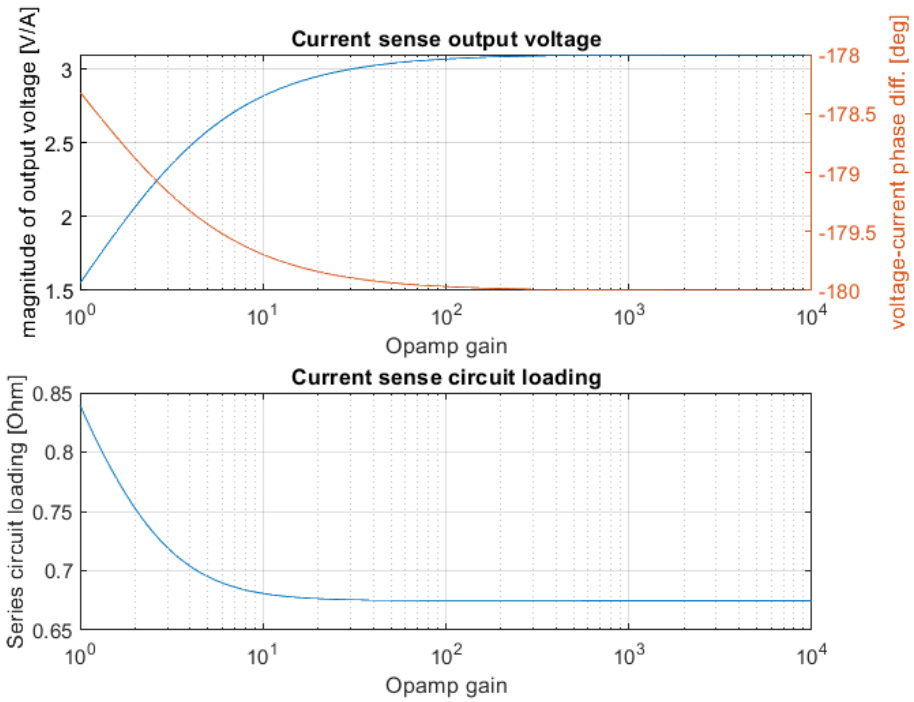


Figure 3.8: Current sense performance as a function of op-amp gain.

op-amp, it is important that the selected op-amp has a relatively high bandwidth, as it needs to achieve this gain at the operating frequency.

The output signal of the current detection circuit is fed to a phase detector, where it is compared to the voltage signal coming from the inverter. This detector outputs an analog signal based on the phase difference between the two signals. This signal can then be fed to an analog input of a controller, which can use it to determine if and how the link can be optimized.

3.1.3. Data Demodulation

Data is send from the slave to the master using load modulation. This can be detected on the master side as a variation in the current flowing into the link. In order to measure this current, the same current sensing circuit as described in the previous section is used. While this was mainly designed to accurately capture the phase, the magnitude of the output signal is also linearly proportional to the magnitude of the current flowing into the link. By measuring changes in this current, it is possible to detect the change in impedance presented by the slave.

The signal from the current sense network is passed to an RF power detector. This outputs the signal envelope. In order to translate this into a usable bit-stream, a special bit decoding network is designed. The purpose of this network is to amplify the sharp changes in current caused by the load modulation to a digital signal, while also filtering out any low frequency components caused by the motion of the coils. The circuit used for this is shown in figure 3.9.

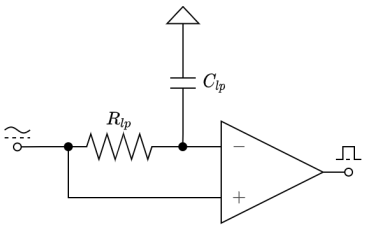


Figure 3.9: Bit-detection circuit

The idea behind this circuit is quite simple. Using an RC low-pass filter the average value of the input

signal is obtained. This is used to set the trigger level of a comparator, implemented using an open-loop op-amp. This signal is compared to the unfiltered input signal. The sudden spikes caused by the load modulation will not make it through the filter, and will therefor trigger the comparator. However, any slower variations in amplitude will make it to both inputs of the op-amp, cancelling each-other out. The output of the op-amp can be connected directly to a digital input pin on a controller.

There are of course downsides to this system. There is a trade-off that has to be made in setting the cut-off frequency of the low-pass filter. The lower it is set, the less it will affect the data transmission. But, setting it too low will reduce its ability to filter out the unwanted low frequency components. Setting it closer to the expected bit frequency will mean that more noise can be filtered out, but it will make it more likely that bits will get lost.

The circuit also requires frequent bit-transitions to function correctly. Otherwise the voltage difference between the inputs of the op-amp will become very small. This will result in a poorly defined output signal. A solution to this would be to use a variant of manchester encoding, which will ensure frequent transitions between ones and zeros. Another downside of this circuit is that there can be quite a lot of variation between units due to variations in the op-amp input offset.

3.1.4. Data Modulation

Data is send from the master to the slave using amplitude shift keying (ASK). This means that the master must be able to vary the amplitude of the carrier based on an external bit stream. In the carrier generator proposed in the previous section, this can be achieved by modulating the supply voltage. When sending a zero, the supply voltage could be reduced to a percentage of the "normal" supply, resulting in a lower amplitude signal. It is important that this lower supply is properly regulated, otherwise the modulation depth will become correlated with the current draw of the load. In setting the modulation depth there would be a trade-off between the power and data transfer. When using a higher modulation depth, the bits would be easier to distinguish on the slave side, but the power transmitted would be lower than when using a lower modulation depth.

However, in this first proof of principle the data is modulated using on-off keying (OOK). This is essentially equivalent to ASK with a 100% modulation depth. The reasoning behind this is as follows: since the proposed application is a sensor readout system, the majority of the data being transmitted is sensor data going from the slave to the master. The master will only be sending acknowledgements and the occasional command to the sensor. The loss in energy transferred due to the deep modulation will likely be minimal. Using OOK does however simplify the design of the master, as the carrier signal can simply be disabled by turning of the clock signal. This removes the circuitry required to vary the supply of the carrier generator.

3.2. Practical Implementation

The previous section discussed the theory surrounding the various subsystems of the master. In this section it is discussed how these theoretical designs are implemented in practice. The master was build on a single PCB using discrete off-the-shelf components. The full schematics of the master PCB, including all jumpers and test points can be found in appendix B. The resulting PCB layout is shown in appendix C.

3.2.1. Carrier Generator and Modulator

The hearth of the carrier generator is a RHU003N03FRA discreet NMOS, which acts as M_1 in figure 3.2. The main reason for picking this particular transistor is that it had a relatively low gate-source capacitance. This is important as it allows the MOSFET to be driven directly by the clock generator, without needing any extra current amplification steps. A low input capacitance also reduces the switching losses associated with driving the transistor. It is of course also important that the transistor is able to handle the required currents and voltages, which this one is narrowly able to.

For the resonating coil, the most important characteristic was that it had a low self-inductance. It was implemented by wrapping a piece of lacquered copper wire twice around a toroidal ferrite core, creating an inductor with an inductance of roughly $580nH$. Completing the resonant circuit was a $15-220pF$ variable trim capacitor. This allows the zero-voltage switching to be fine tuned with the aid of an oscilloscope.

The clock signal is provided by an LTC1799 current controlled oscillator. This allowed the operating frequency to be fine tuned by either an analog control signal or a potentiometer. This clock circuit does not allow any control over the duty cycle. As a result the duty cycle is fixed at around 50%, depending on the rise and fall times of the oscillator. To modulate the data onto the carrier, the clock signal is grounded via a

50Ω resistor in series with an NMOS. When the NMOS is turned on, the clock signal is grounded through the resistor, stopping the carrier generator. A schematic overview of the carrier and clock generators as they are implemented is shown in figure 3.10.

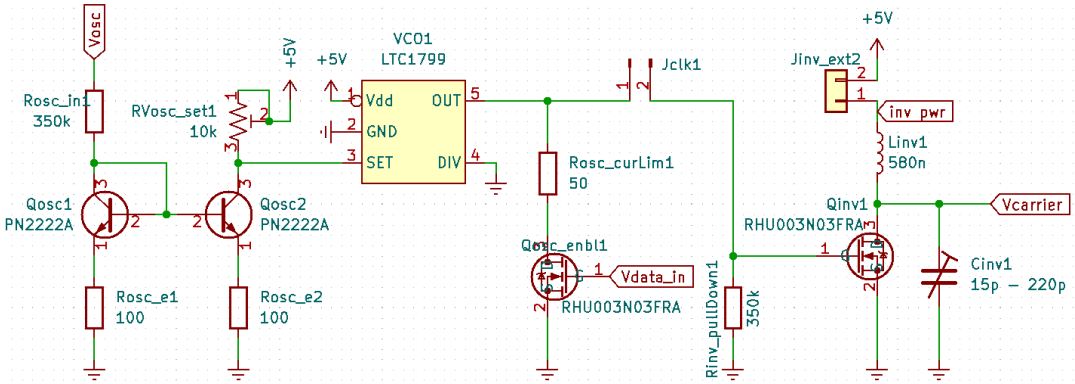


Figure 3.10: Full schematic of the clock and carrier generators.

3.2.2. Current Sense Circuit

The current sense circuit relies on a very specific transformer, with a low primary turns ratio and a relatively high operating frequency. For this reason, a custom transformer was made using a material 61 ferrite ring. This particular type of ferrite is optimized for operation up to $25MHz$. On the primary side, a piece of stranded copper wire is wrapped around the core once. On the secondary side a piece of lacquered copper wire was wrapped around the core seven times, resulting in an inductance measured at $1,59\mu H$.

The secondary side of the transformer was connected to the negative input of an AD8058 op-amp. As mentioned before, the gain and bandwidth of the op-amp can have quite a large influence on the performance. This op-amp has a gain-bandwidth product of 325 MHz, allowing for a maximum gain of about 30 at the operating frequency of 13.56 MHz. According to figure 3.8, this is about the point where a further increase in gain starts to have diminishing returns. A feedback resistor of 10Ω was chosen, as this presented a good trade-off between gain and phase accuracy.

In order for the op-amp to operate correctly, the signal applied to it cannot exceed the supply rails. For this reason, a $2.5V$ TL431LP reference voltage is connected to the positive rail. Due to the negative feedback of the amplifier, the input signal will be lifted to $2.5V$, allowing for maximum headroom in both directions. To prevent significant current draw from the reference, the secondary winding is referenced to ground, and coupled to the op-amp via a $100nF$ capacitance. This will work with the secondary inductance to create a second order high-pass filter with a cut-off at around $400kHz$. This is actually beneficial, as this will block any low-frequency noise. However, as it is, the quality factor of this filter would be too high, creating a resonance peak at the cut-off frequency. To dampen this resonance, a 10Ω resistor is added in series with the secondary coil. This dampens the resonance, but will add to the overall impedance seen when looking at the primary coil. Simulations show that this added resistance does not have a significant impact on the performance, largely due to the high turns ratio of the transformer. The circuit is further band-limited by introducing a $300pF$ capacitor in parallel with the feedback resistor, creating a first-order low-pass characteristic with a cut-off frequency of $53MHz$.

3.2.3. Phase Detection and Magnitude Demodulation

For both the phase and magnitude detection an off-the-shelf AD8302 detector chip is used. This chip takes two input signals, and outputs their phase and magnitude differences as analog voltages. For both the phase and magnitude detection the carrier signal is used as a reference. Since the signal coming directly from the carrier is way to high in amplitude, it is attenuated by both a fixed and a variable resistor. The current sense signal is also optionally attenuated using a trimmer resistor. The gain and phase output sensitivity can be tuned using two further trimmer resistors, as suggested in the datasheet. This chip is designed to be able to operate at frequencies into the GHz. In order to use it at $13.56MHz$, series capacitors need to be added to OFSA and OFSB ports. These will decrease the high-pass cut-off frequency to $11MHz$, allowing the signals of interest to pass. The other external components are placed as suggested in the datasheet.

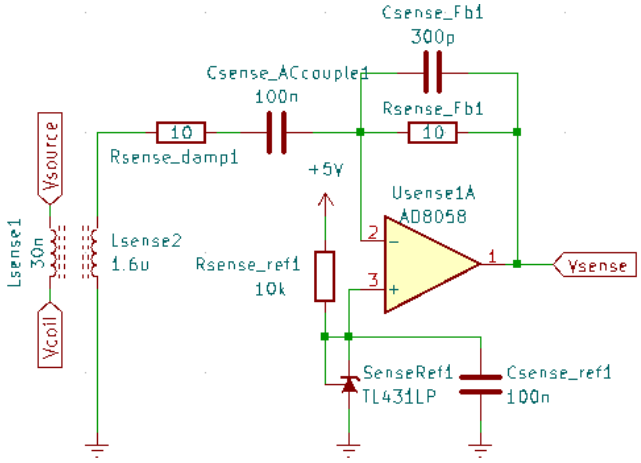


Figure 3.11: Full schematic of the current sense network.

The phase signal is passed to an output pin, where it can be used by a controller to predict the coupling. The magnitude signal on the other hand is passed to the bit detection circuit discussed previously in section 3.1.3. The low-pass filter is implemented using a $10k\Omega$ resistor and a $3.3nF$ capacitor, resulting in a cut-off frequency of $4.8kHz$. This is judged as far enough away from the intended nominal data transmission rate of 50 kbit/s, while still keeping up with any gradual changes in current amplitude. The op-amp used is the same AD8058 as used in the current sensing circuit, as they come in two per package. A full schematic of the phase and bit detection circuit is shown in figure 3.12.

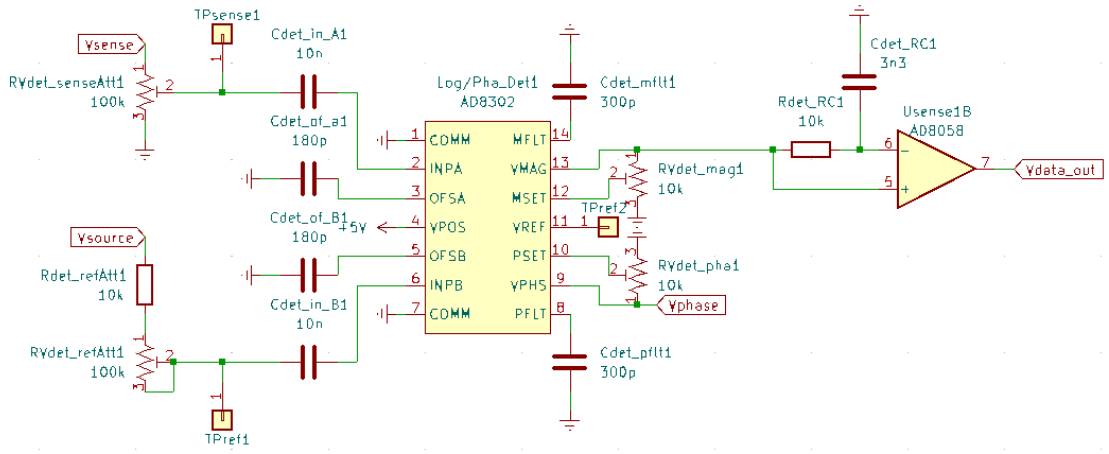


Figure 3.12: Full schematic of the phase and bit detector circuits.

3.3. Measured Performance

Most of the measurements of the master can be found in chapter 5, where the master is assessed as part of the full system. Nevertheless, the performance of some select subsystems are measured and discussed in the coming section.

3.3.1. Carrier Waveforms

In order to assess the effectiveness of the carrier generator, the output signal in various conditions was observed. First the oscillator and variable capacitor where tuned to their optimal values. The output signal was then measured with no load, with a 100Ω AC load, and finally with a 100Ω DC load. More information on the loads used can be found in section 6.2.1. The resulting waveforms are shown and discussed in the following section.

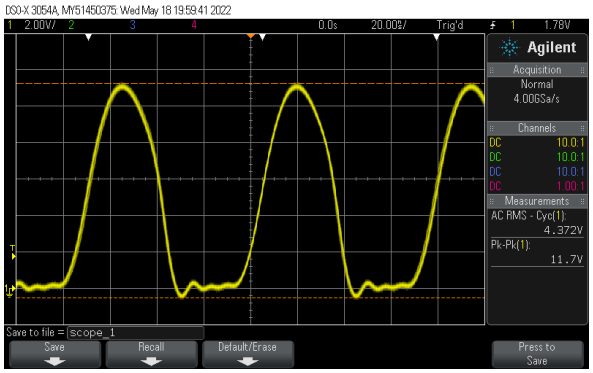
In figure 3.13, the time and frequency domain wave forms in a no-load state are shown. Based on the

fourier analysis in 3.5, the measured waveform correlates best with a signal of a a duty cycle between 60% and 70%. This can be explained; the current sourcing capability of the clock generator was quite small compared to the size of the gate capacitance of the MOSFET, causing the clock waveform to deviate quite a lot from the intended square wave. As a result, the switch in the inverter was not triggered with the intended duty cycle of 50%. In this case, this has worked to improve to efficiency.

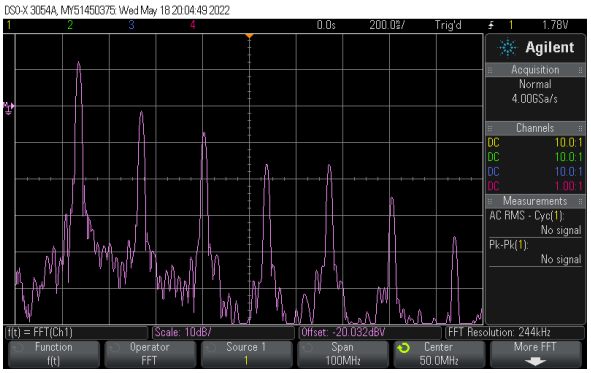
When an AC load is applied to the system, the waveforms change. This is shown in figure 3.14. Comparing the time domain signals in the loaded and unloaded states, it is clear that the loading has somewhat affected the signal. There is a slight reduction in amplitude, and the oscilloscope also determines the power in the loaded signal to be slightly reduced. It appears as if the tops of the peaks are “chopped off”. Based on this it would appear the the loaded signal is more distorted than the unloaded one, however this is not backed up by the frequency spectrum. The most significant difference is a slight reduction in the second harmonic when loading the circuit. In fact, all of the higher order components either reduce in power or stay the same, except for the 6th harmonic, which shows a very slight increase. This reduced distortion can be explained by the addition of the compensation network. For frequencies far above the design frequency, the compensated double link will essentially behave like a capacitor, decreasing in impedance with increasing frequency. This means that the higher order harmonics are presented with a lower ohmic load, resulting in an increased voltage drop.

Finally, the DC loaded signal in figure 3.15 shows the effects caused by rectification on the slave side. The first thing that can be noted is that the signal power drops again. This can be attributed to the fact the rectifier has some voltage transforming properties. When unloaded, the rectifier will output roughly the peak-to-peak value of the input signal as a DC output voltage. This voltage transformation means that any load at the output of the rectifier cannot be equated with the same size load at the input [89]. In this case, the 100Ω load at the output of the rectifier will appear significantly smaller, causing a further drop in the signal voltage.

The time domain waveform of the DC loaded signal also appears more distorted then in the AC or unloaded case, but again the frequency spectrum proves the opposite. The harmonics are almost universally lower when comparing to the AC loaded signal. There are several possible explanations for this. One reason could be that because the rectifier is presenting a lower apparent load, the filtering effect caused by the compensation network becomes more apparent. This is only a hypothesis at this time, and will require further testing and analysis, which is considered outside of the scope of this work.

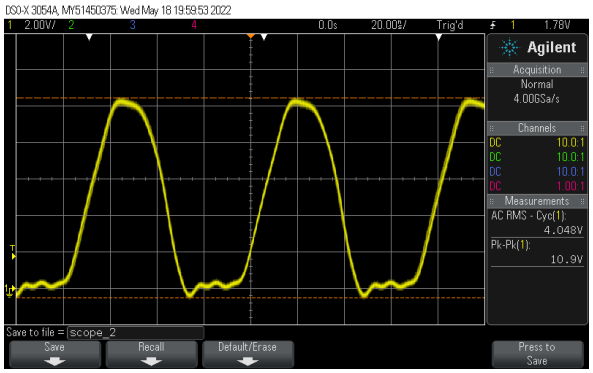


(a) Time domain signal

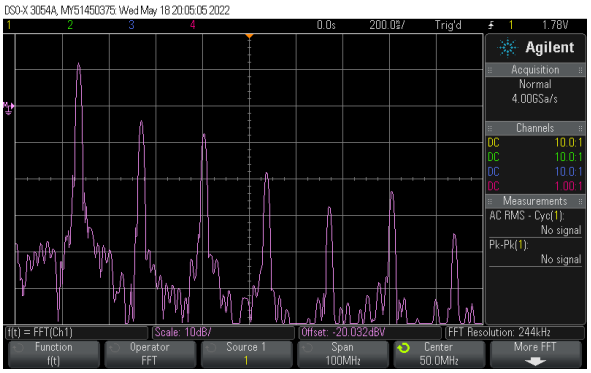


(b) Frequency spectrum. Vertical scale is 10 dBV per division.

Figure 3.13: Unload carrier signal

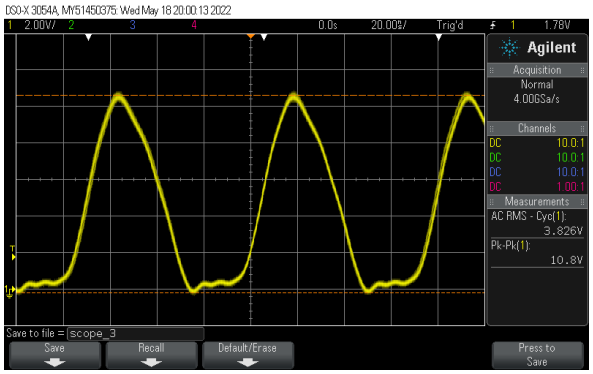


(a) Time domain signal

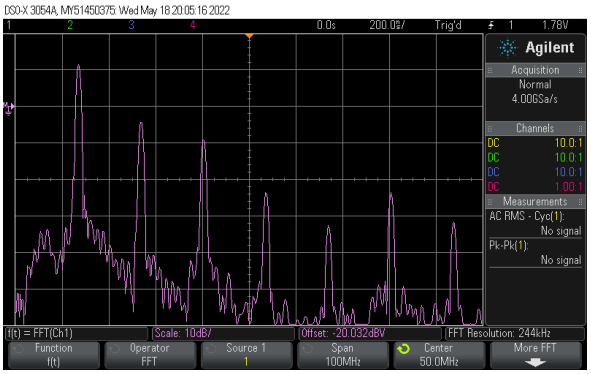


(b) Frequency spectrum. Vertical scale is 10 dBV per division.

Figure 3.14: Carrier signal terminated in 100Ω AC load



(a) Time domain signal



(b) Frequency spectrum. Vertical scale is 10 dBV per division.

Figure 3.15: Carrier signal terminated in 100Ω DC load

3.3.2. Current Sense Performance

In order to analyze the performance of the current sensing circuit, a known current was forced into it, and the output signal was observed using an oscilloscope. To generate this current, a known shunt resistor is placed in series with the primary coil of the current sense network. A voltage is applied to this series combination using a function generator, and the voltage over the resistor is measured. By combining the output voltage with the voltage over the shunt, the phase accuracy and current-to-voltage gain can be determined. The resulting waveforms for two 13.56MHz signals are shown in figure 3.16.

(a) Sinusoidal current

(b) Square wave current

Figure 3.16: Voltage over 22Ω shunt (yellow line) and output voltage (green line).

From the measurements with a sinusoidal currents in figure 3.16 (a), a phase error between the input current and output voltage of about 5°can be observed. The current to voltage gain is about 1.9, which is consistent with what would be expected from the component values used. The output waveforms shows some non-linearities, which could be caused by saturation of the ferrite core. This will likely not significantly impact the performance. In figure 3.16 (b) a square wave signal is applied to the circuit. This allows an assessment of how well the circuit is able to cope with non-linear waveforms. While the measured signal is showing some additional ringing, it is still a reasonable approximation of the input current.

To further quantify how well the measured current translates to an accurate phase measurement, the output of the phase detector for various current-voltage phase differences was measured. To do this the following setup was devised: a sinusoidal current was injected into the detector in the same way as in the previous setup. Then, a second signal coming from the same function generator was applied to the reference input of the phase detector. Using the generator, the phase between these two signals can be controlled. The phase was varied in steps of 5°. The output signal amplitude is plotted in 3.17. The test was performed at two input levels, to determine if the signal amplitude had an affect on the measured phase.

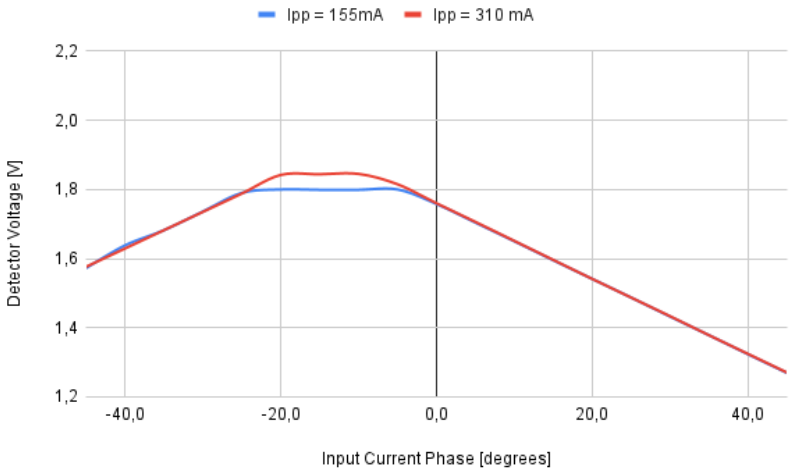


Figure 3.17: Measured phase detector output voltage for various set current phases.

The measurements show a very linear phase response, that is not significantly impacted by the current amplitude. There are however two things to note about these results. Firstly, there is a clear dead-zone, where a change in phase will not result in a change in output voltage. An increase in signal amplitude will reduce this dead-zone. This can only be explained as an artifact of the detector chip used. Secondly, there is a systematic error being made in the phase detection. According to the datasheet of the detector chip, the output voltage should be maximum at 0°phase shift. However, the signal is maximum at about -15°, which is beyond the 5°that would be expected due to the error in the current detector. This is actually beneficial; since the phase differences of interest mostly reside around 0°, the region of interest is pushed away from the dead-zone. It also allows both positive and negative phase differences to be measured, which the chip would otherwise not be able to distinguish.

Finally, a similar measurement can be taken with regards to the current amplitude detection. The results of this are shown in figure 3.18. As expected, a logarithmic relation is seen between the current magnitude and the detector output voltage. No unexpected behaviour is noted.

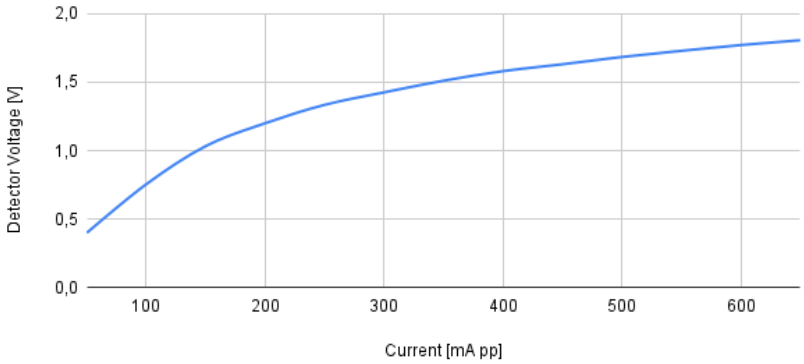


Figure 3.18: Measured magnitude detector output voltage.

4

Slave Design

This chapter will go into detail on the design of the slave module. The slave is responsible for demodulating the data coming from the master, and facilitates the load modulation that is used to send data back. It also harvests energy from the signal send by the master, and regulates this in such a way that it can be used by any subsequent electronics. The slave PCB will also contain a part of the compensation network as designed in chapter 2.

4.1. Theory and Design

4.1.1. Rectification

In order for the slave to extract any power from its input signal, it needs to be converted to a DC voltage. This is done using a rectifier. Rectifier topologies can be divided into two categories: passive and active.

In a passive rectifier diodes are used to control the flow of current [90] [91] [92]. There are many possible topologies, but they all rely on the same principle; allowing current to flow into the input terminal, but not out. The various topologies do have different voltage, impedance and efficiency characteristics [93].

Active rectifiers rely on the same principles as passive rectifiers, only transistors (usually MOSFETs) are used instead of diodes [94] [95] [96]. Whereas in a passive rectifier the switches (diodes) are activated by the rising voltage of the input signal, the switches in an active rectifier require an external signal to trigger. This removes the inherent losses caused by the diode threshold voltage, meaning that an active rectifier can be much more efficient, especially when dealing with low voltage signals. An active solution also allows for more dynamic control over the characteristics of the rectifier. It has been shown that it is possible to regulate the output voltage by varying the timing of the switches, removing the need for a DC-DC converter [97]. In [98], an active rectifier is used to reduce the harmonic distortion that is often associated with rectifiers.

On the other hand, there are also downsides to implementing an active solution. Most notably, the timing for the signal driving the transistors is absolutely critical for good performance. The driving signals need to be exactly in sync with the incoming signal. If this is not the case, the efficiency of the rectification will drop drastically. Generating these driving signals requires complex and potentially power hungry circuitry. These problems exacerbate as the frequency of the incoming signal increases. As a result, active rectifiers in WPT applications make most sense either when the operating frequency is relatively low, or in high power applications where there are more resources available on the receiving side.

The operating frequency in this application is relatively high, and the resources available at the slave side are quite limited. This favors a passive implementation. This is reinforced by the fact that the rectifier will be implemented using discrete components. This would make the accurate timing required for an active rectifier even more difficult.

The most well-known rectifier topology is the full-bridge rectifier. A schematic representation is shown in figure 4.1. The output voltage is approximated by:

$$V_{DC} = V_{peak} - V_{th} \tag{4.1}$$

where V_{th} is the threshold voltage of the diodes. However, this design can be improved to better suit the needs of this application. The main issue is that in a full bridge rectifier the AC signal is differential, instead of

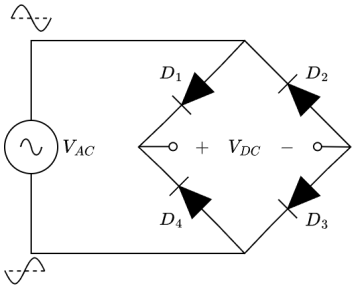


Figure 4.1: Schematic representation of a full bridge rectifier.

being referenced to ground. While this might be an advantage in certain application, it significantly increases the complexity and effectiveness of the load modulation network required for communication. Referenced to DC-ground, each input terminal will oscillate between V_{peak} and $-V_{peak}$ at a 180°phase difference. Due to the body diode, it would be impossible to implement a transistor connecting each terminal to DC ground. Any load modulation would have to take place after rectification. Here the load modulation would not be exempt from the non-linearities introduced by rectification.

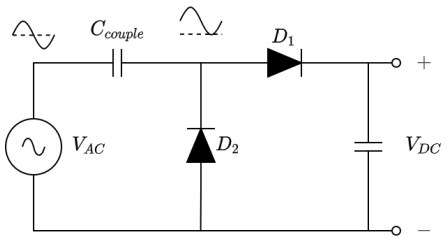


Figure 4.2: Schematic representation of a voltage doubler.

This problem can be solved by connecting the lower AC input terminal to ground, and capacitively coupling the signal to the rectifier. In this way, diode D_3 becomes redundant, since both of its terminals are grounded. In addition, diode D_4 is also redundant, since the voltage at its cathode will never drop below its anode. The resulting circuit is known in the literature as a voltage doubler, and is shown in figure 4.2.

4.1.2. Load Modulation

Communication from the slave to the master happens by way of load modulation. In order for this to work the slave needs to be able to dynamically vary its input impedance. This is done by introducing a resistor in parallel with the receiving coil, that can be connected and disconnected using a transistor. The value of this resistor sets the modulation depth. Here a trade-off will have to be made between power and data transfer; a small resistor will be easier to detect by the master, but it will also dissipate more energy.

As mentioned in the previous section, care has been taken in the design of the rectifier to allow for easy implementation of the load modulation circuitry. Because the anode of D_2 in figure 4.2 is connected to ground, the voltage at its cathode cannot drop below the diode threshold voltage. This allows an NMOS with its source connected to ground to be inserted next to D_2. The drain of this transistor is connected through a resistor to the cathode of D_2. By turning on the transistor, the resistor will be seen in parallel with the rectifier and the overall input impedance of the slave will be lowered. A schematic showing the load modulation network integrated into the voltage doubler is shown in figure 4.3.

4.1.3. Demodulator

Data is send from the master to slave using amplitude modulation. In this prototype the master uses on-off-keying (OOK), but the slave should be able to handle signals with a lower modulation depth. In order to translate the modulated signal into usable bits, an off-the-shelf envelop detector is connected in parallel with the rectifier. In order to convert the envelop signal into a usable bit-stream, the output of the detector is connected to an opamp network. This setup is in essence identical to the bit detection circuitry used in the master, and further information on this can be found in section 3.1.3.

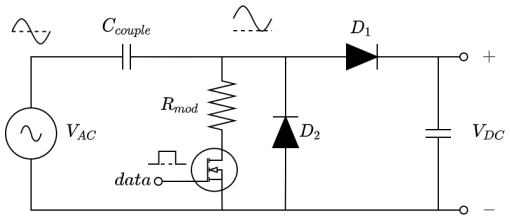


Figure 4.3: Schematic representation of a voltage doubler with load modulation.

4.1.4. Power management

The DC voltage available at the output of the rectifier will be largely dependent on among others the coil distance, compensation capacitance, current draw, etc. In order to maintain a stable supply voltage an off-the-shelf buck-boost DC-DC converter is used. This produces a steady $3.3V$ output, regardless of input the input voltage, assuming enough power is available. This $3.3V$ supply voltage is used to power the opamp, envelope detector, and controller, as well as any external sensors or other electronics.

4.2. Practical Implementation

The previous sections discus the theoretical design of the circuits that comprise the slave. This section will focus on the specific practical implementation of these circuits.

The slave was build using discrete components using standard PCB techniques. Many of the resistors and diodes were implemented as through-holes, instead of the more conventional surface mount components. This was due to better availability, and made the boards easier to modify after manufacturing. The downside of this is that the components are more spread out, requiring longer traces, which are generally associated with more parasitics. A full circuit diagram, including all the selectable load resistances and test points, is shown in appendix B. The final PCB layout is shown in appendix C.

4.2.1. Rectifier and Load Modulator

The rectifier was build to match the schematic shown in figure 4.3. The size of the coupling capacitor C_{couple} is not critical, it simply needs to be large enough to appear as a negligible at the operating frequency. Therefor a size of $100nF$ has been chosen. For the MOSFET controlling the load modulation a RHU003N03FRA discreet NMOS is used. The modulation resistor R_{mod} is implemented as a $0-500\Omega$ trimmer resistor, to allow the modulation depth to be tuned. For the diodes a low threshold voltage and a fast switching time are crucial. For this reason, BAT86 schottky diodes are chosen over traditional junction diodes. Finally, the output voltage of the rectifier is filtered using a $100\mu H$ coil and a parallel connection of a $100nF$ and $10\mu F$ capacitor. This filtered signal is then passed to a $470\mu F$ electrolytic capacitor, which acts as energy storage. A schematic representation of this circuit is shown in figure 4.4.

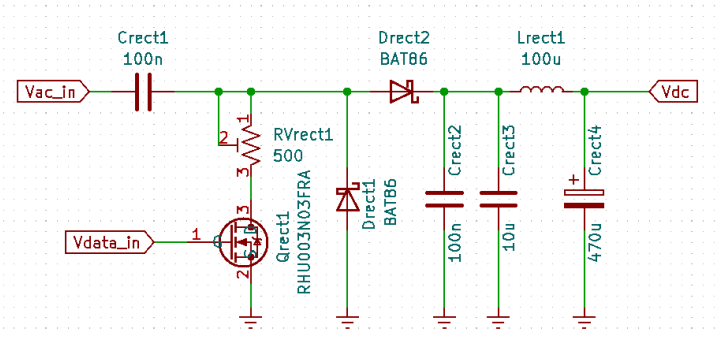


Figure 4.4: Rectifier and load modulator as implemented on the PCB.

4.2.2. Demodulator

For the envelope detection a LTC5507 linear RF power detector is used. As per the datasheet recommendation, two $3.3nF$ capacitors are used to set the high-pass cut-off at $10MHz$. The output of the RF detector is connected directly to the negative input of an AD8058 opamp. The same signal also goes through an RC low-pass filter to the positive input of this opamp. The RC filter consists of a $10k\Omega$ resistor and a $3.3nF$ capacitor, resulting in a cut-off frequency of $4.8kHz$. This setup is identical to the one used in the master. A schematic representation of this circuit is shown in figure 4.5.

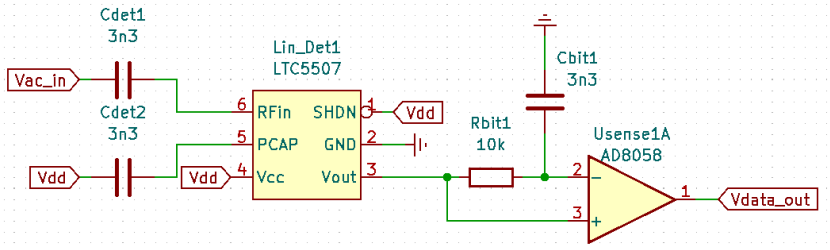


Figure 4.5: Slave side demodulator as implemented on the PCB.

4.2.3. Power Management

For the DC-DC conversion a MAX1724EZK33 step-up converter is used. According to the datasheet, this chip is able to convert an input of between $0.8V$ and $5V$ to a regulated $3.3V$ output. As suggested by the datasheet, the input and output signals are filtered using $10\mu F$ capacitors. The chip requires an external inductor to function, which is added in the form of a $10\mu H$ through-hole component. In order to prevent the input voltage from rising so far that it could damage the chip, a $5.1V$ zener diode is put in parallel with the input. The board contains a jumper header which allows the onboard electronics to be powered from either this internal source, or an optional external source. A schematic representation of this circuit is shown in figure 4.6.

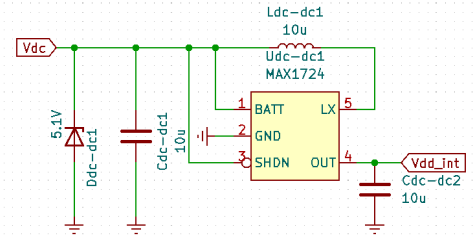


Figure 4.6: DC-DC converter as implemented on the PCB.

4.3. Measured Results

Assessing the performance of the slave only makes sense in the context of a full system. Therefor, the performance of the slave is covered in the next chapter on the full system performance.

5

System Implementation

In order to test how all of the previously discussed subsection interact, they are all combined into a prototype of a full system. In this chapter the design choices regarding the full system are discussed. Aside from the previously discussed subsystems, the full system also includes some placeholder controllers for both the master and the slave, as well as a simple proof-of-concept data transfer protocol. The viability of the system for actively adjusting the coil compensation to differing coupling conditions is also discussed.

An overview of how the various subsystems interact is again included in figure 5.1.

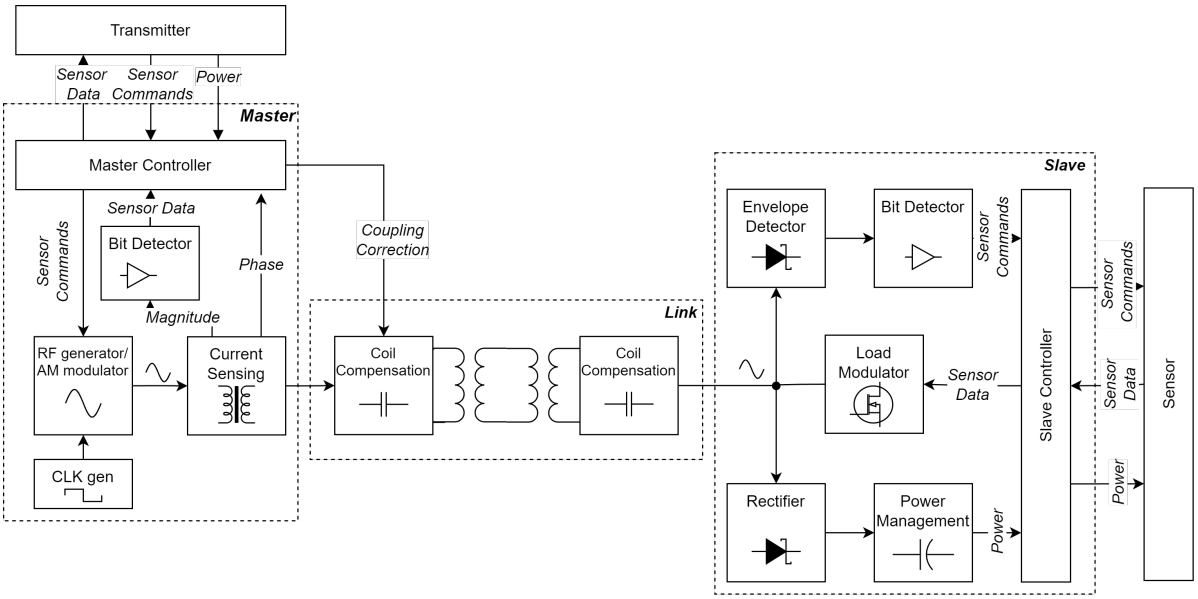


Figure 5.1: Overview of how all the subsystems interact.

5.1. Master and Slave Controllers

Both the master and the slave will need a controller to act as an interface to the transmitter and the sensor. These controllers will receive data from their respective input via an SPI or I2C connection, and control the modulating circuitry to send this data across the link, where the opposing controller will have to decode it again. The main consideration for both controllers is that they are fast enough to handle communications up to at least 50 kbit/s. In addition, they also need to be energy efficient. This is especially important for the slave controller, as energy is in short supply at the slave end.

Finding and optimizing these controllers can be a project all on its own, and is considered outside of the scope of this project. For this proof-of-concept, a pair of *STM32f303VCT6* development boards are used, one for the master and one for the slave. These micro-controllers are far more powerful and feature rich than is required for this application, but this makes them more flexible and easy to use when it comes to prototyping.

5.2. Data Communication

In the design of the communication protocol a careful trade-off has to be made between data transfer and power transfer. While the protocol is very important to the performance of the system, it's optimization is considered outside of the scope of this work. In this section, some considerations regarding the protocol are discussed, and the design of a simple protocol for measurement and demonstration purposes is presented.

While the actual modulation and demodulation network is quite complex, a valid simplification would be to think of the communication as occurring over a single line. This line is kept high by default, and both the slave and the master are able to pull it low. Though, it should be kept in mind that due to the way the bit detection circuitry works, there should be regular voltage transitions. Additionally, there might be a delay between one side pulling the line low and this being detected on the other side. This delay is not necessarily equal for rising and falling edges. The line can also not be held low too often, as the slave harvest energy a lot more efficiently when the line is high.

These constraints favour the use of Manchester encoding, as opposed to standard binary encoding. In a Manchester encoded datastream, it is not the voltage on the line that indicates a 1 or a 0. Rather, a transition from low to high is marked as a 1, while a transition from high to low is interpreted as a 0. This not only guarantees frequent voltage transitions, it also ensures that the line is kept high 50% of the time.

There are however some downside to Manchester encoding. Firstly, it requires double the bandwidth of regular binary encoding to transmit the same amount of data. Additionally, Manchester encoding requires very good synchronization between the two communicating parties. Since transitions can occur both at the beginning of a bit and half-way through a bit, it is more difficult to synchronise based on this.

Another modulation protocol that has been designed to deal with very similar restrictions is the one-wire protocol [99] [100]. This protocol is designed to allow two-way communication between a single master and multiple slaves across two wires, a data wire and a ground wire. It also takes in to consideration that the slave(s) might use the line for energy harvesting, making sure that the line stays high for a portion of the time. The default one-wire protocol is able to send data at either 15.6 or 125 kbit/s.

In the one-wire protocol, all communication is initiated by the master. If the master wishes to send something to the slave, it pulls the line low. Depending on how long the line is kept low, the slave will interpret the send data as either a 1 or a 0. If the slave wants to transmit data to the master, the communication is again initiated by the master. The master pulls the line low. The slave detects this. If the slave wishes to transmit a 0 it also pulls the line low, otherwise, it does nothing. After a set period, the master releases the line, and checks the signal. If it finds that the line is still being kept low by the slave, it registers it as a 0. If the line bounces back to being high, the slave must have intended to send a 1. After each bit the line always remains high for a short period of time, to allow the slave to harvest energy from it.

Because each bit starts with the master pulling the line low, it is very easy to keep the two devices synchronized. But this frequent pulling low of the line reduces the energy harvesting potential, and will result in slower data speeds than what could otherwise be achieved.

For prototyping purposes, a simple custom data protocol is designed. This allows the greatest amount of flexibility and transparency, as the bit-rate and other timing parameters to be very easily changed. The protocol only allows communication from the slave to the master, but it does include synchronisation and acknowledgement pulses send by the master.

Before any communication can take place, a handshake must occur. When the master is turned on, it enters into a searching pattern. It will repeatedly pull the line up and down with a period of $300\mu s$. If a slave is present, it will detect the pulses, and start pulling the line low as well. The master will notice that the line will no longer go high when it releases it, telling it that a slave is present.

Now that both the master and the slave are aware of each others presence, the communication can begin. First, both devices will leave the line high for a while, to allow the slave to harvest some energy. After $600\mu s$ of charging, the slave will pull the line low to indicate that the sending of data is about to begin. $20\mu s$ later, the slave will send one byte of data using binary encoding. Once $500\mu s$ has passed, all the data is send. The master acknowledges this by pulling the line low for $50\mu s$, serving as both an acknowledgment and a synchronization pulse. The charging phase can now start again, repeating the cycle. If the master sees that the slave does not end the charging phase, it will time out and go back to the searching pattern. The same happens to the slave if it does not receive an acknowledgement within a set time. A flowchart of this protocol is shown in figure 5.2.

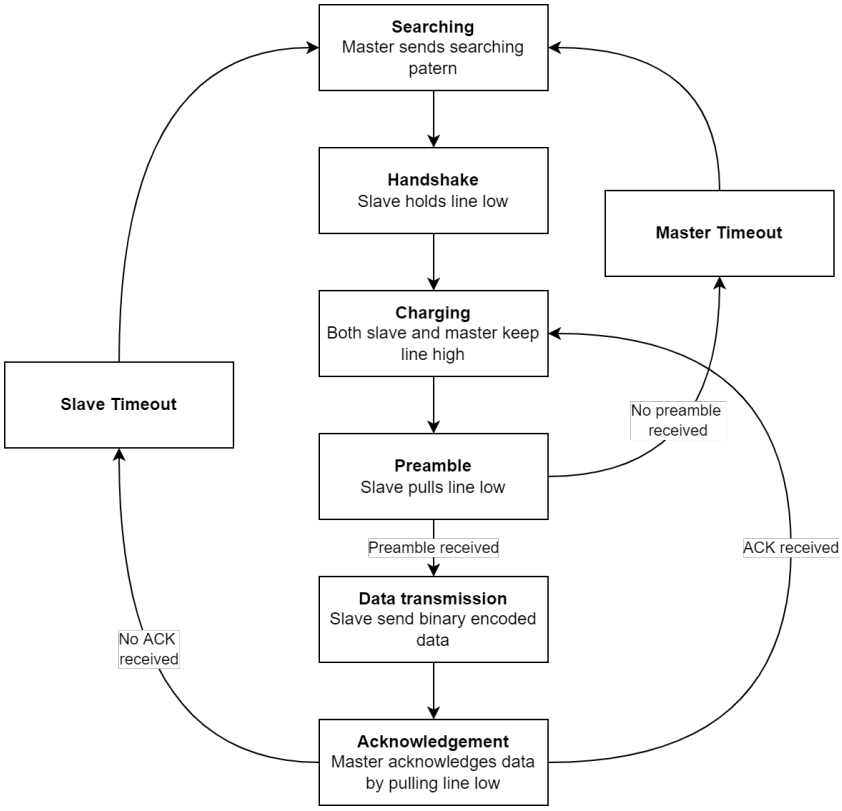
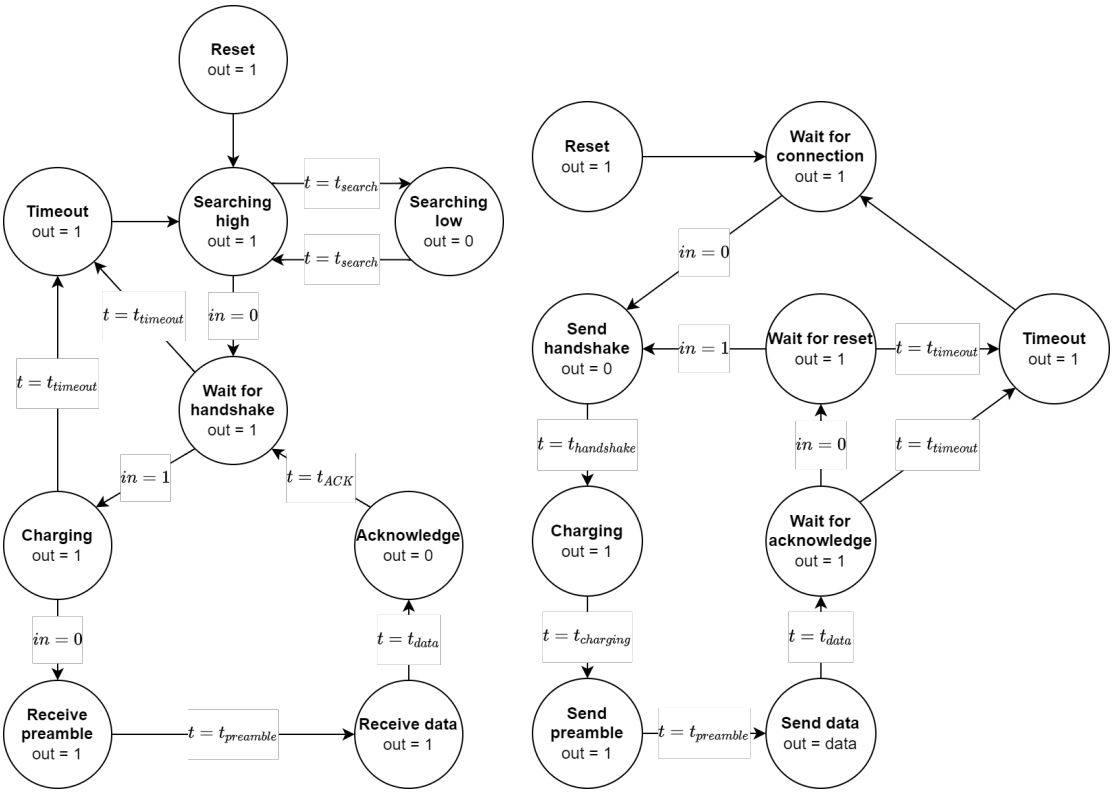


Figure 5.2: Flowchart showing the progression of the data protocol.



(a) Master controller

(b) Slave controller

Figure 5.3: State diagrams for the master and slave controllers

The data protocol is implemented on the two micro-controllers as finite state machines. The state diagrams of the master and the slave are shown in figure 5.3. Please note that the output state in the diagram refers to the line level. If a state in the diagram sets the output to 0, the line is pulled low. This is inverted from the signal that is actually outputted by the controller, as a transistor needs to be turned on to pull the level low.

A $1MHz$ timer is used to keep track of how long the system stays in each state. This timer is reset every time the system enters a new state. When the slave controller enters the *send data* state, a second timer is started to control the flow of bits. One bit lasts $50\mu s$, and the least significant bit is send first. The master also uses a separate timer when in the *receive data* state. It uses this to sample the input $10\mu s$ after the planned start time of a bit.

With the timings as mentioned in this section, the overall effective bit-rate is 8.5 kbit/s. This is significantly slower than the intended bit-rate of 50 kbit/s. Sadly, shortening the timing in this protocol would lead to the master and slave going out of sync. However, as will be discussed further in the next chapter, the modulation and demodulation electronics are more than capable of handling these data speeds. It appears that the data speed is currently being limited by the software implementation on the micro-controllers.

5.3. Active Coupling Tracking

The previous subsystems have been designed in such a way that the coupling of the system could be tracked using a phase detector. The controller would measure the signal coming from this detector, and output an analog voltage signal to tune the compensation capacitor. However, measurements showed that while there is a correlation between the system performance and the output of the phase detector, the detected signal is also sensitive to other signal properties. Moreover, the relation between the measured current phase and the system performance is not quite linear. These measurements are discussed in more detail in the next chapter.

Because the measured signal is not as clean as expected, further signal processing would be required to implement the active coupling tracking. This strayed out of the bounds of this project. So while the current sense signal has been measured, and the effect the compensation capacitor has has been characterised, the control system combining these two is not implemented.

6

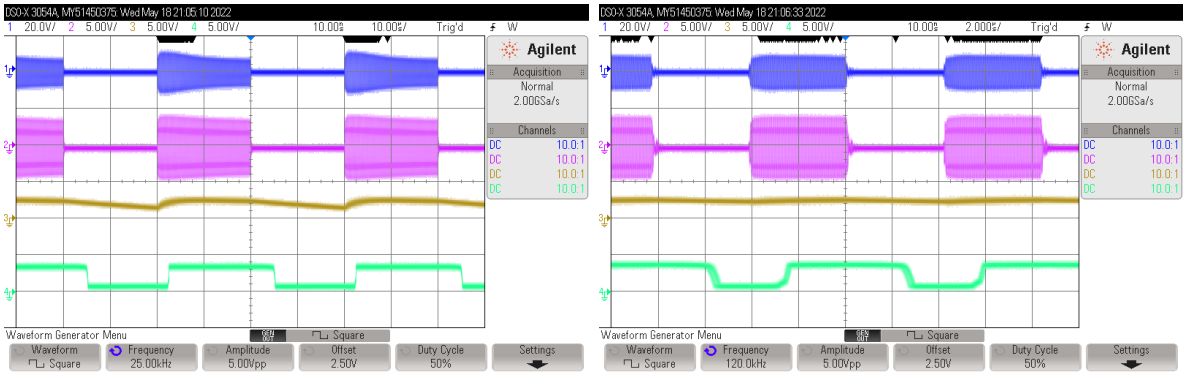
Full System Measurements

In this chapter the performance of the full system is evaluated. First the power transfer performance is analyzed under various conditions. After this the maximum data speed and data transfer performance in characterized. Finally, power and data transfer is tested simultaneously to see how they affect each other, and to quantify the achieved specifications of the prototype.

6.1. Data Transfer Performance

6.1.1. Master to Slave Signal Integrity

The goal of the first experiment is to determine the maximum bit-rate the system is able accommodate when sending data from the master to the slave. It also gives an insight in the delay between the master sending a bit, and it arriving at the slave. To do this, square wave signal is applied to the data input of the master. This simulates a data stream of alternating ones and zeros. By measuring the signal at various points across the signal chain it is possible to determine where in the signal path delays are introduced. By increasing the frequency of the input signal, we are also able to determine the maximum data-rate at which the output signal is still well defined. The measurement is performed first at 25 kHz, which represents a bit-stream at the specified data-rate of 50 kbit/s. The results of this are shown in figure 6.1 (a). The experiment is repeated at a frequency of 120 kHz, which was found to be the highest frequency at which the bit-stream was still well defined. This is shown in figure 6.1 (b).



(a) Master to slave communication at 25 kHz.

(b) Master to slave communication at 120 kHz.

Figure 6.1: Signal waveforms for master to slave communication. The top waveform is the carrier signal on the master side. The second signal is the carrier as received by the slave. The third signal is the output of the slave side magnitude detector, and finally the fourth signal shows the waveform after the bit detector.

The plots in 6.1 show that the rising and falling edges of the signal received by the slave are very well defined, even at high data rates. However there is a noticeable delay between the master sending a bit, and it being received and processed by the slave. Moreover, this delay is not constant. When sending data at 50

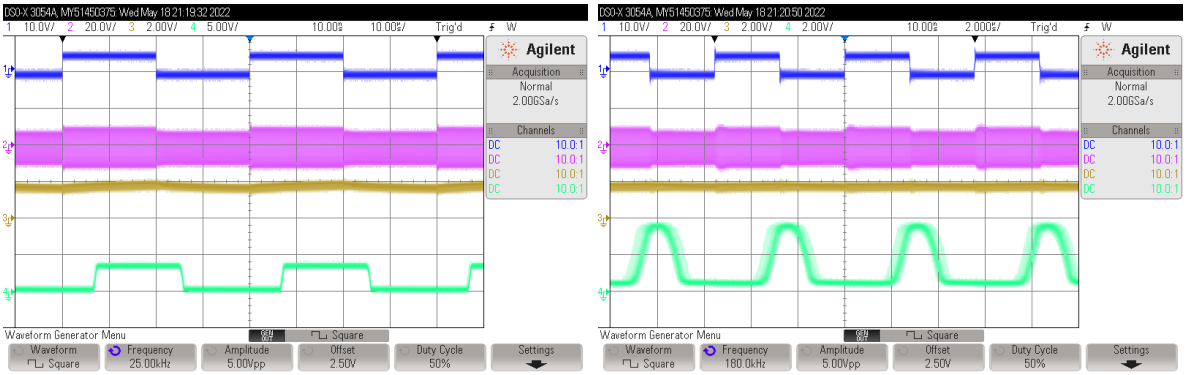
kbit/s, a rising edge is delayed by roughly $2\mu s$, while a falling edge has a delay of $5\mu s$. When the data-speed is increased to 240 kbit/s, the rising edge delay reduces to be around $1.6\mu s$, and the falling edge delay becomes $2.5\mu s$.

This variation in delay with different data-speeds can be explained as follows: the longer the system has to settle in a certain state, the more energy it will take to move out of this state. This results in longer delay times. These varying delays can be a problem when transmitting real data, as the gaps between ones and zeros will not be consistent, meaning that the delay will also not be consistent.

The difference in delay between rising and falling edges appears to be an artifact of the RF detector chip used. It seems to respond more quickly to an increase in RF power than to a decrease. This imbalance between the rising and falling edge delays result in an elongation of the pulse at high data rates. This is what is currently limiting the data rate of the system; when the data rate increases beyond 240 kbit/s the pulses become so long that they merge together.

6.1.2. Slave to Master Signal Integrity

The same experiment was repeated, but now the signal was applied to the data input of the slave. Again, the test was first performed at 25 kHz, to mimic the specified data rate. After which the data speed was increased to the maximum rate that would still produce a usable signal. In this configuration that was 180 kHz. The results of this test are shown in figures 6.2 (a) and (b).



(a) Slave to master communication at 25 kHz.

(b) Slave to master communication at 180 kHz.

Figure 6.2: Signal waveforms for slave to master communication. The top waveform is bit-stream that is presented to the slave data input. The second signal is the carrier as measured on the master side. The third signal is the output of the master side magnitude detector, and finally the fourth signal shows the waveform after the bit detector.

The signals seen in figure 6.2 are broadly similar to the ones obtained in the previous experiment. At 50 kbit/s, the rising edge delay is about $7\mu s$, while the falling edge delay is approximately $6\mu s$. Because the rising and falling edge delays are closer together, the slave to master communication allows for slightly higher data speeds before collapsing. At 360 kbit/s, the rising edge delay is roughly $2.5\mu s$, while the falling edge delay is about $1.5\mu s$.

The rise and fall time of the signal is again satisfactory, even at the higher data rates. Comparing these results with the ones shown in 6.1, shows that the increased consistency in rise and fall times are likely due to a more consistent magnitude detector. The master uses a different chip than the slave, and from the raw detector output it can be seen that the analog output of the detector rises at roughly the same rate as it falls.

Finally, it can be seen that while the master side carrier voltage should ideally not be influenced by the slave load modulation, a small decrease can be observed. This is evidence of the non-zero output impedance of the inverter. While this drop should not severely impact the system performance, it will affect the performance of the current magnitude detector. This is because the master side current magnitude detector uses the carrier voltage as a reference signal. In this case, this should result in an increased modulation of the detector output voltage, which should make the bit detection perform better.

6.1.3. Performance of the Data Transfer Protocol

In order to test the data transfer capabilities under real-world circumstances, the system was assessed while transferring data according to the data protocol introduced in the previous chapter. In figure 6.3 the wave-

forms sent and received by the slave and master are shown. As mentioned in section 5.2, the length of one bit was set at $50\mu s$ due to timing problems on the controller side. Combining this bit speed with the required charging time, handshaking and acknowledging sets the total data rate at 8.5 kbit/s. Two bits are shown being sent. One of them is annotated to indicate the various phases in the transmission.

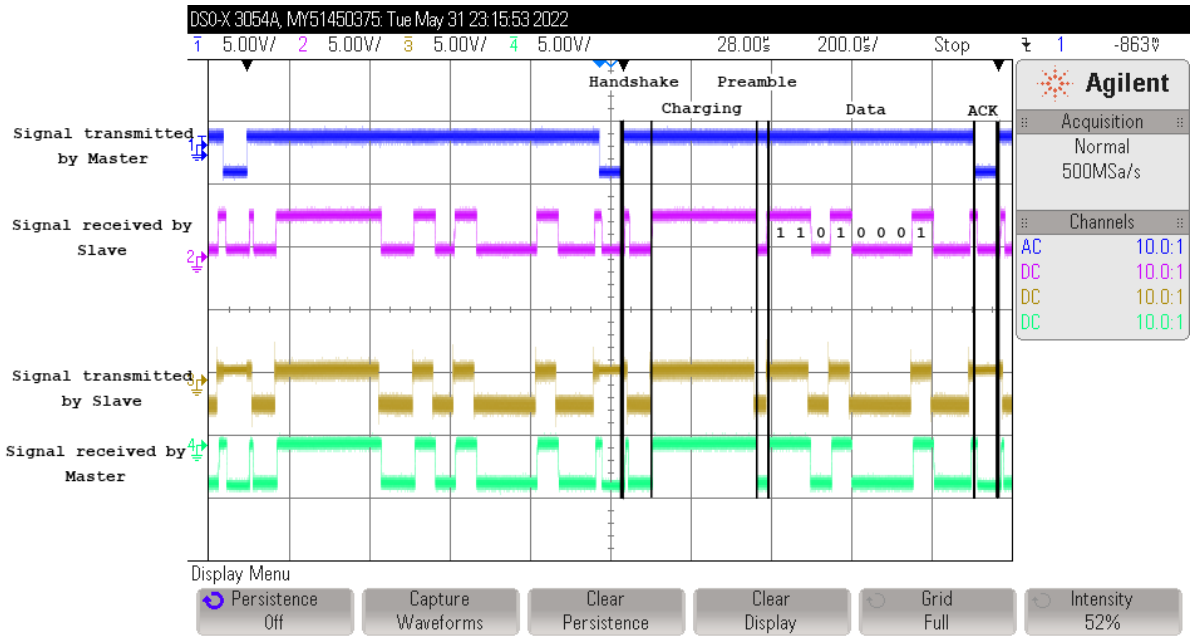


Figure 6.3: Waveforms of the data send and received by the slave and master.

The received waveforms in figure 6.3 look very well defined, and the delays in transmitting and receiving are not significant at this scale. It is also clear that both the slave and the master are receiving their own signal. This was expected from the way the system works, and the data transfer protocol was build to deal with this. It unfortunately does mean that full-duplex communication will not be possible with this system as it is now.

6.2. Power Transfer Efficiency

6.2.1. Measurement Setup

The power transferred across the link under various circumstances has been measured. In order to get a sense of the efficiency of the various subsystems, measurements where performed using three setups. These are laid out in figure 6.4. In 6.4 (a) the slave side output of the double link is terminated directly in a resistor. By measuring the DC power flowing into the master, as well as the voltage over the AC load resistance, an estimate of the efficiency of the master can be made. In 6.4 (b) the slave is built out further by adding the rectifier. Now the output power is defined as the power flowing into the DC load resistor at the output of the rectifier. This allows the loss in efficiency caused by the rectifier to be quantified. Finally, 6.4 (c) shows the full signal chain, including the DC-DC voltage regulator. This can be used to evaluate the voltage regulator, as well as determine the maximum output power the system is able to provide.

6.2.2. Raw Efficiency Measurements

Using the above mentioned setups the efficiency was measured at various coil distances, compensation capacitor values, and circuit loadings. The coil distances where $1mm$, $1.5mm$ and $2mm$, and both sets of coils where separated by the same amount. The compensation capacitor was stepped from $100pF$ to $200pF$ in steps of $20pF$. All of the measurements where first performed without any data transfer, after which setup 6.4 (c) was evaluated again, this time with data transmission according to the protocol discussed in section 5.2. Various circuit loadings where achieved by changing the load resistance. Both the slave and master processors where powered from separate sources, as the development boards contain other power drawing components that are not relevant to the system. Their power draw is not included in these measurements. The raw data from these measurements are shown in figure 6.5.

There are already several conclusions that can be drawn from this raw data. First of all, it does not appear

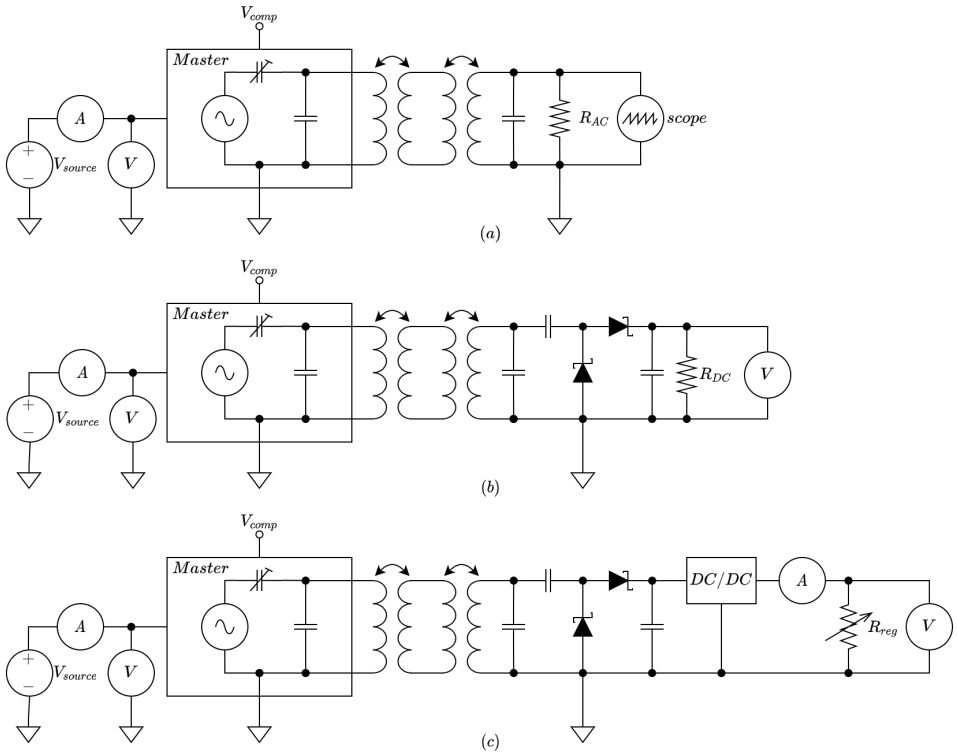


Figure 6.4: Measurement setups with AC termination (a), DC termination (b), and regulated DC termination (c).

that an increase in distance will automatically result in a decrease in either efficiency or output power. In fact, having the coils at 1.5 mm seems to slightly outperform the other two setups.

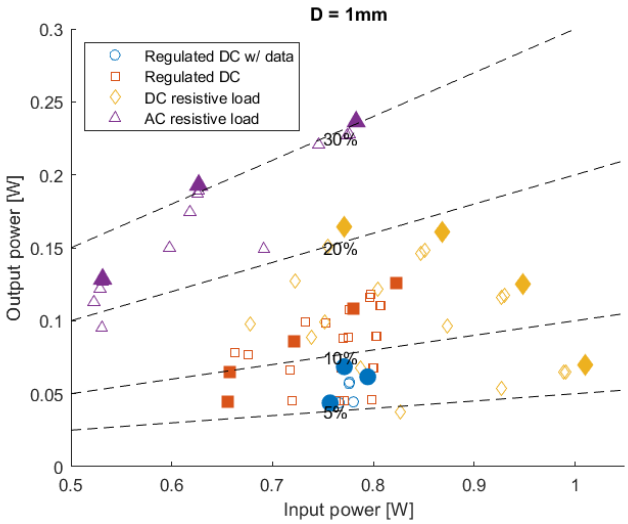
It can also be noted that the efficiency of the system is highly dependent on the power being drawn. It appears that there is a point of maximum efficiency at around 0.8 W of input power, although there are not quite enough data points to fully confirm this. It would follow from the theory that there is a point at which the efficiency is optimal. When running at low power, there are several subsystems that draw the same amount of power regardless of the load. If the load is drawing little power, these systems will reduce the efficiency. If the load is drawing too much on the other hand, the waveform from the carrier generator will start to distort. This will not only reduce the spectral efficiency of the circuit, but will also cause the carrier generator to no longer achieve zero-voltage switching. This will greatly reduce its efficiency.

6.2.3. Subsystem Power Usage

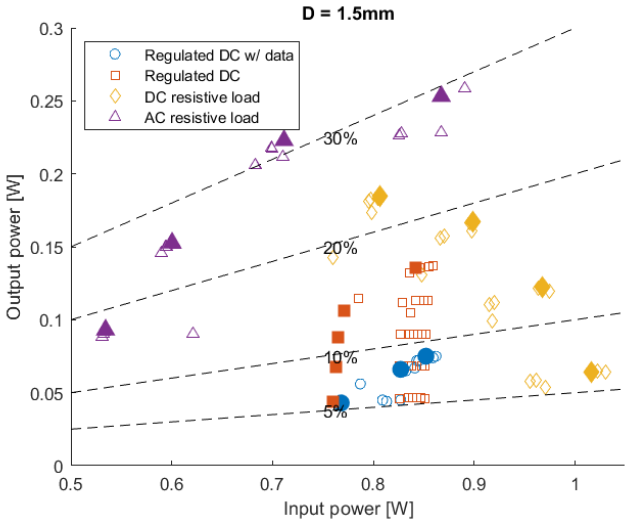
Using the raw data gathered in the previous section, it is possible to make an estimate of the power use of the various sub systems. Only the measurements corresponding to the optimal setting for the compensation capacitor are considered. These are depicted as solid markers in 6.5. Initially, the system is analyzed without any data transfer.

However, before the setups can be compared, some data processing has to take place. As can be seen from 6.5, the power drawn has a large impact on the system efficiency. So for a proper comparison, only measurements corresponding to the same input power can be considered valid. This requires the data to be interpolated. For transparency, this interpolation is shown in appendix D. The breakdown of power usage is done at a single power level. Care has been taken to pick a power level close to as many actual data-points as possible.

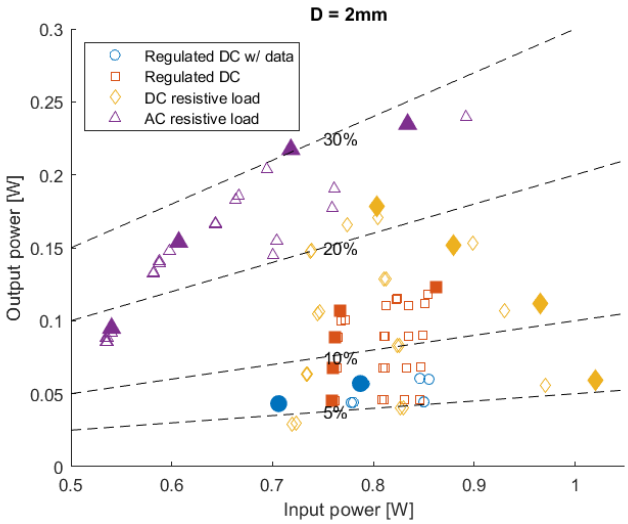
To estimate the power usage of the subsystems, some more assumptions have to be made. First, it is assumed that the energy required by the master and slave modulation and demodulation electronics, the master clock circuit, and the power LED are constant. The power consumption of these systems is measured with a multimeter with the carrier generator disabled. In addition, it is assumed that loss in efficiency when moving from an AC loaded system to a DC loaded system is solely caused by the addition of the rectifier. It is easy to assume that this energy is lost due to the limited efficiency of the rectifier, but this does not necessarily



(a) Input and output power at 1 mm coil distance.



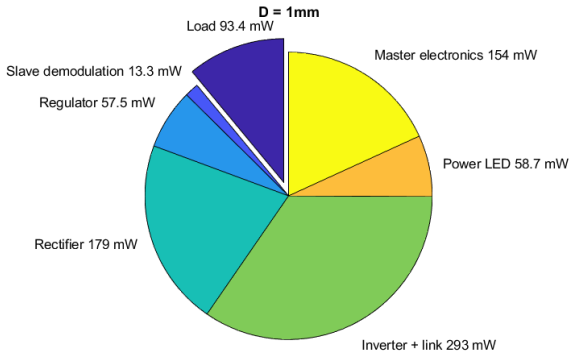
(b) Input and output power at 1.5 mm coil distance.



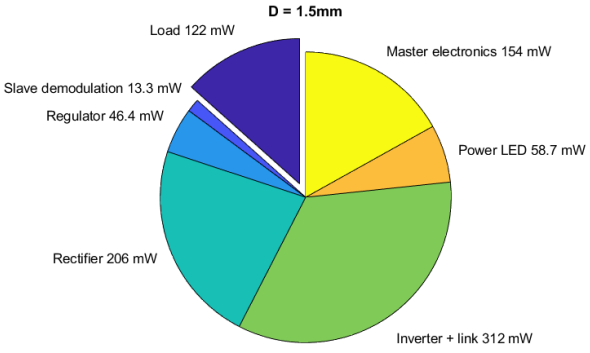
(c) Input and output power at 2 mm coil distance.

Figure 6.5: Input and output power measured under various circuit loadings and compensation capacitances. Each point in the graph represent a unique set of conditions. The different colored and shaped markers represent the different test setups (see figure 6.4). Each setup was measured with between 3 and 5 different circuit loadings. The markers for these different loads are not visually distinguished. For each circuit loading up to 6 measurements where taken, with the compensation capacitor varying from 100pF to 200pF in steps of 20pF. The solid marker represents the highest efficiency achieved in each set of 6 measurements. Some reference lines are provided to indicate certain efficiencies.

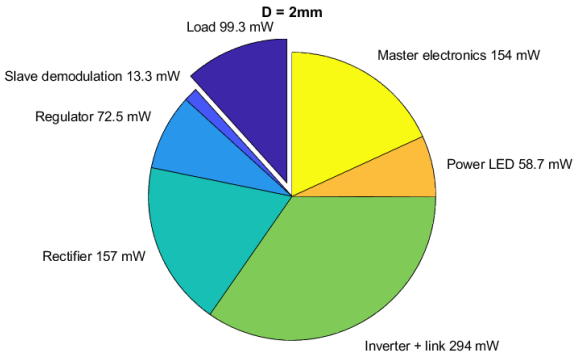
have to be the case. It could be that due to the rectifier an impedance mismatch is created at the input of the carrier generator, lowering the power output. When comparing the DC loaded system to the regulated system, the same assumptions are made regarding the regulator. The results obtained using the above assumptions are shown in figure 6.6.



(a) $D = 1mm$, total power adds to 777 mW.



(b) $D = 1.5mm$, total power adds to 841 mW.



(c) $D = 2mm$, total power adds to 777 mW.

Figure 6.6: Pie charts indicating the estimated power loss due to various subsystems. Additional losses due to data transfer are not taken into account.

From these pie charts several conclusions can be drawn. Firstly, it again appears that the different coil distances do not have a significant effect on the system performance, although $1.5mm$ distance again appears optimal.

The graphs show that the inverter and link account for the largest power loss. From the available data is was not possible to distinguish between power lost in the link and power lost due to inefficiencies in the inverter, although it can be assumed that the heat losses in the link are relatively minimal. While it is not surprising that the inverter accounts for a large portion of the energy lost in the system, these numbers do indicate that the zero-voltage switching condition is not being met. This could be a result of a larger than intended power draw from the inverter, causing the inverter resonant tank to be dampened too much. It could also be that the inverter has a significant real part in its equivalent output impedance, in which a large amount of energy is lost when large currents are being drawn.

The pie charts also show that a significant amount of power is being drawn by the master electronics, which includes the current sense circuit, amplitude and phase detector, clock generator, and the bit detector, as well as an unused but still powered second magnitude detector. This is the same detector that is used on the slave, where it was shown to draw 61 mW of power when no RF input signal was provided. It is likely that it is responsible for this same power draw on the master circuit, although this is not confirmed.

6.2.4. Efficacy of the Coupling Estimation

As discussed extensively in the previous chapters, the master contains a current phase detector to estimate the coil coupling factor. This was done so the compensation capacitor could be adjusted to match the current coupling factor. When the compensation capacitor is properly tuned, both the energy and data transfer should perform at optimal efficiency. In order to test this, both the power transfer efficiency and the output from the phase detector are measured with varying values for the compensation capacitor. The power efficiency was measured to a DC load, as shown in figure 6.4 (b). The experiment was performed for distances of $1mm$, $1.5mm$ and $2mm$, and with AC loads of 20Ω, 50Ω, 100Ω and 200Ω. The results of this are shown in figure 6.7.

The behaviour of the system as measured in figure 6.7 is largely as expect from the theory. There is a clear peak in the transfer efficiency, which moves from right to left as the distance between the coils increases. The values of C_{comp} at which these peaks of maximum efficiency occur are in agreement with the measurements done in chapter 2.

However, contrary to the theory there are some measurements where not one but two peaks in the efficiency can be seen, most notable in figure 6.7 (b) and (c). This is in contradiction with what is dictated by linear circuit theory. Varying the compensation capacitance varies the imaginary component of the input impedance of the link in a linear fashion. The transfer efficiency of the link is maximized whenever this imaginary part is opposite to the imaginary part of the source impedance. This can only happen at a single value of C_{comp}. Therefor this second peak must be a result of non-linearities in the system.

When analyzing the output of the current phase detector there is a clear correlation between the detected phase and the transfer efficiency. This is most obvious at a coil distance of $1mm$. This indicates that the current phase can be a useful metric for optimizing the coupling capacitor while the system is operating. When the phase detector output peaks, there is also a peak in the power transfer efficiency.

At a distance of $1.5mm$ there is still a clear correlation, but for higher ohmic loads the peaks in the phase detector voltage become less pronounced, and start to deviate from the peaks in efficiency. This trend is continued in 6.7 (c). At $2mm$ coil distance the phase detector still shows a correlation with the power transfer efficiency at low loads, but this correlation diminishes with an increasing load. At a load of 200Ω there no longer is a correlation between the detector and the efficiency.

It can also be noted that the phase detector output not only correlates with the coupling factor, but also with the load resistance. It was expected from the theory that the phase detector would be more sensitive when the system is load with a small ohmic load. However, it can also be seen that the average output of the phase detector is affected by the load. This is most clear in 6.7 (a), where the peak value of phase output can be seen to decrease with an increasing load. This is a problem when implementing any form of active coupling correction. The variations in phase signal due to the size of the load has to be filtered out. This can probably be done by correlating the current phase measurements with the measured current amplitude, but the implementation of this is considered outside of the scope of this work.

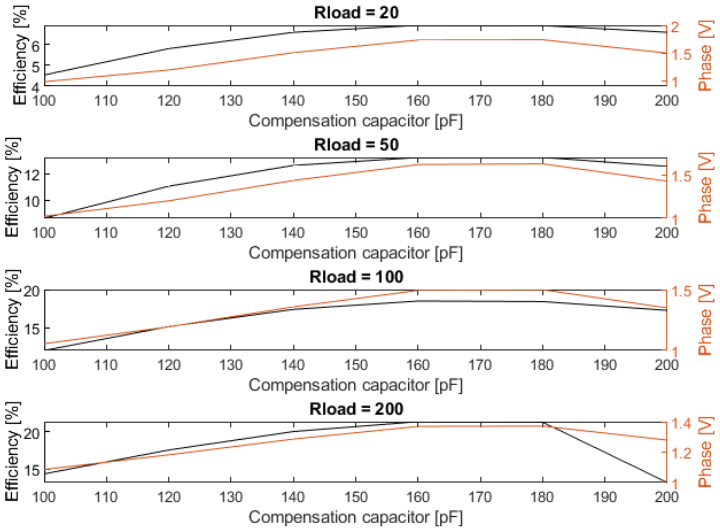
	P_{out}	efficiency
$D = 1mm$	$48.3mW$	6.22%
$D = 1.5mm$	$61.6mW$	7.32%
$D = 2mm$	$47.2mW$	6.07%

Table 6.1: Maximum regulated power deliverable to external load without compromising data transfer.

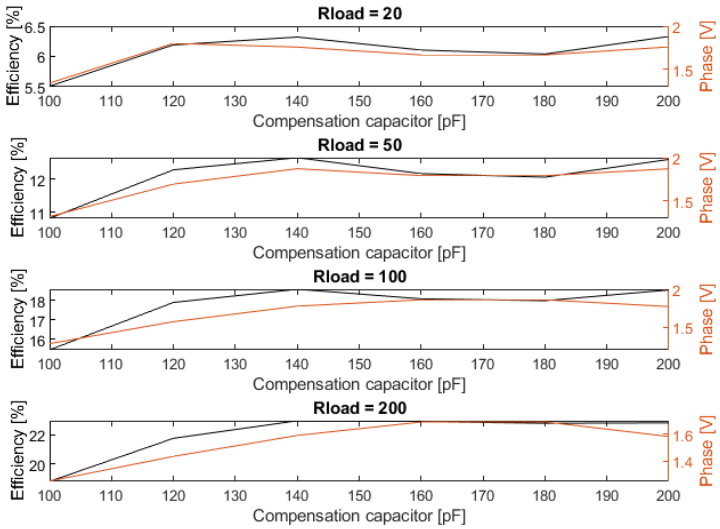
6.3. Power and Data Transfer

In the previous sections the power and data transfer capabilities are assessed separately. In this section the interaction between them is investigated. It is expected that if more power is drawn by the load, the load modulation on the slave side becomes less effective, reducing the data transfer capabilities. Conversely, since the sending of data involves adding parallel resistances and turning of the carrier signal (on-off keying), a loss in power transfer efficiency can be expected.

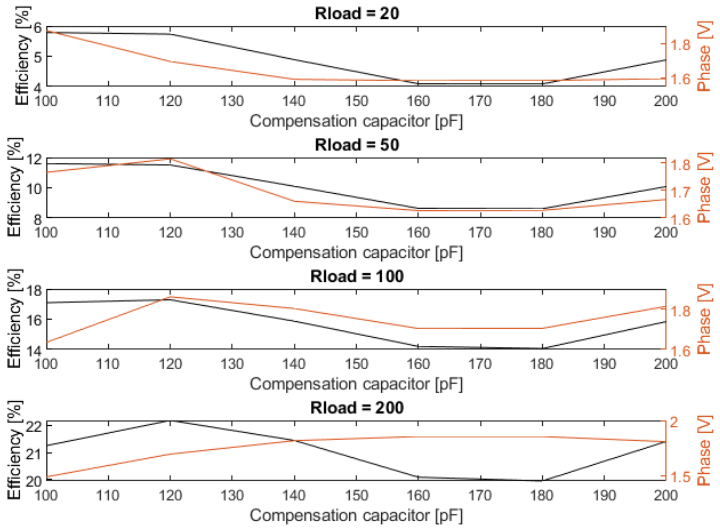
To quantify the limits of the system, an experiment has been performed to find the maximum power draw at which the system is still able to transfer data without significant data loss. “No significant data loss” has been defined as being able to transmit the numbers 0 through 255 without any errors, using the protocol defined in section 5.2. The compensation capacitor was varied from $100pF$ to $200pF$, just like in the previous measurements. Only the results at the optimum value for C_{comp} were recorded. The results from this experiment are shown in table 6.1



(a) 1 mm coil separation.



(b) 1.5 mm coil separation



(c) 2 mm coil separation.

Figure 6.7: DC transfer efficiency and current phase detector output as a function of C_{comp}.

7

Conclusion, Discussion and Recommendations

7.1. Inductive Link

It appeared that the double inductive link with the proposed compensation network performed well. While no accurate measurement of the losses inside the link was done, both the simulations and the achieved results suggest that they were likely small. There are no measurements that suggest that a link containing two coil pairs is less efficient than a link consisting of only a single air gap, and the presented compensation network proved easy to build and tune.

Sadly, because of difficulties measuring the characteristics of the link, it was not possible to completely verify the proposed model. The oscilloscope that was used in many of the measurements was found to not be accurate enough for quantitative measurements. For this reason it is recommended that future research into this should make use of a vector network analyzer.

Nevertheless, the tuning of the link to specific coil distances was shown to be effective. It was demonstrated that when the link is properly tuned, the load impedance is indeed transferred across the link to the input impedance. It could also be seen that when the system was optimally tuned, the phase angle between the current and the voltage at the input of the link was zero. This indicates that there is no imaginary component in the input impedance of the link.

The effectiveness and characteristics of the designed the coils was difficult to assess. Especially the measured value for the coil resistance differed wildly from the expected value. It also proved difficult the measure the self-inductance and mutual inductance of the coils at the operating frequency. Again, it is recommended that future work looking into the design of the coil makes use of more suitable equipment.

An interesting topic for future investigations would be the effect of the coil parameters on the overall performance of the system. This is especially relevant when embedding the coils inside the textiles, as it will likely significantly increase the coil resistance. It will also introduce coil flexing as an additional challenge. Any future work should also consider the effect of the wires between the coils. Preliminary test indicate that even short wires might not be negligible.

7.2. Master Design

The design of the master met all the requirements that where set for it. The carrier generator was able to provide sufficient power at a high enough amplitude for the slave to extract energy from. The demodulation circuitry was shown to be able to demodulate signals at data rates well in excess of the requirements, and the current sense network was able to measure the phase and the amplitude of the current with reasonable accuracy.

Still there are several improvements that could be made to the design. Firstly, it was shown in chapter 6 that the carrier generator is likely the largest source of energy loss in the system, making it the most obvious candidate for improving the systems efficiency. The cause of this is not entirely known, but it it is suspected that with large current draw the quality factor of the resonator drops significantly, causing the zero-voltage switching condition to no longer hold. A possible solution for this could be to reduce the size of the resonant

inductor in the carrier generator, increasing the quality factor. Other solutions could include reducing the clock duty cycle, although this would reduce the spectral efficiency.

Another possibility would be to forego the modified class-E inverter entirely in favour of a more traditional class-E design with a resonant tank at the output. This would allow much more control over the switching characteristics of the inverter, making it easier to maintain zero-voltage switching and likely also improving spectral efficiency. As explained in chapter 3, the resonant tank was omitted to decrease the settling time when transmitting data, in an effort to optimize the data transfer rate. However, in chapter 6 it is shown that maximum bit-rate far exceeds the specifications. Moreover, the measurements suggested that it was not the system quality factor that was the limiting factor in data transfer, but rather the bit detector circuit discussed in section 3.1.4. So it is possible that reintroducing the resonant tank to the carrier generator would allow for the same data-rate, but would increase the power efficiency.

The current sense network can be improved. While the measurements showed that it was adequate at reproducing the current with reasonable phase and gain errors, the circuit was more complicated than it needed to be. The transformer it relies on also does not lend itself well to miniaturization. While theory behind the circuit was sound, its performance was let down by the limited specifications and performance of off-the-shelf op-amps in the high frequency range. The principle might find use in higher power applications or devices operating at lower frequencies, but in this design a simple shunt resistor would have been a better choice, especially considering the sensitivity of modern RF detector chips.

The coupling estimation using the current phase is also a candidate for future developments. While this system was shown to perform well under certain circumstances, it would sometimes produce unexpected results. This would occur at larger coil distances, and at higher ohmic loads. The cause of this is unknown, but it is suspected that this might be caused by higher order harmonics in the carrier signal. This not only produces harmonics in the measured currents, but the carrier signal is also used as a reference signal by the detector. So reducing the harmonics not only improves the spectral efficiency, but will hopefully also result in more consistent performance of the current phase detector.

Finally, there are possible gains to be made when reviewing the data modulator. The data is currently modulated using on-off keying, which is implemented in a rather crude way. While chapter 6 shows that this is an effective way of transmitting data, it does likely have a not insignificant effect on the power being transmitted to the slave. By reducing the modulation depth from 100%, it is possible to mitigate some of this loss in power. Finding the optimal modulation depth would be an interesting topic for future research.

Taking this a step further would be to forego amplitude modulation entirely, in favour of phase or frequency modulation. This would not only allow for full-duplex communication between the master and slave, but also ensures that the slave will always receive the maximum amount of power, regardless of any data being transmitted by the master. However, this would also require a significant redesign of many parts of the system, and would undoubtedly introduce many new challenges.

7.3. Slave Design

It was found to be difficult to assess the performance of the slave on its own, as its performance is very much dependent on the preceding systems. In figure 6.6 in chapter 6 an estimate of the power usage of the various subsystems of the slave is shown. These estimates suggests that about half of all the power entering the slave is lost in the rectifier. This makes it the most obvious candidate when it comes to improving the slave.

No further investigation was done into what was causing the losses introduced by the rectifier. It could be due to an impedance mismatch between the output of the link and the input of the rectifier. It is also possible that a lot of energy is simply lost as heat due to the voltage drop over the diodes in the rectifier. If this is the case some gains might be made by either using different diodes, or possibly by increasing the AC amplitude at the input of the rectifier. Investigating and improving the efficiency of the rectifier would be an interesting topic for future research.

Significant losses where caused by the DC power regulator. The regulator was also found to be somewhat unstable. If current draw became too high, the output voltage would collapse and would not recover unless all current drawing elements where disconnected. The output voltage was also generally too high, commonly reaching above $4V$, while the design required an output voltage of $3.3V$. It is recommended that in future iterations of this design a different voltage regulator is used.

The modulation and demodulation worked as intended. Just like with the master the limiting factor in the data transmission appeared to be the bit detection circuit, so efforts in improvements in the data transfer rate should probably start there.

7.4. Full System Performance

While the full system as measured did not quite meet the requirements, it was shown that the system is effective, and could with software updates could likely exceed specifications. As mentioned in chapter 5, the data protocol and its implementation was only a place holder for demonstration purposes. The data protocol itself has a large potential for improvements in both the data and power transfer rates, and especially its implementation on the controllers is key in utilizing the full data transfer potential of the system.

The system used to adapt to changing coupling factors holds potential for future developments. While this system was not fully implemented in this prototype, some improvements in the current phase detector, combined with a smart algorithm to determine the optimal setting for the compensation capacitance, would allow the system to better cope with changes in coil distance. This could improve performance and make the system more reliable.

A

Additional numeric efficiency and power simulations

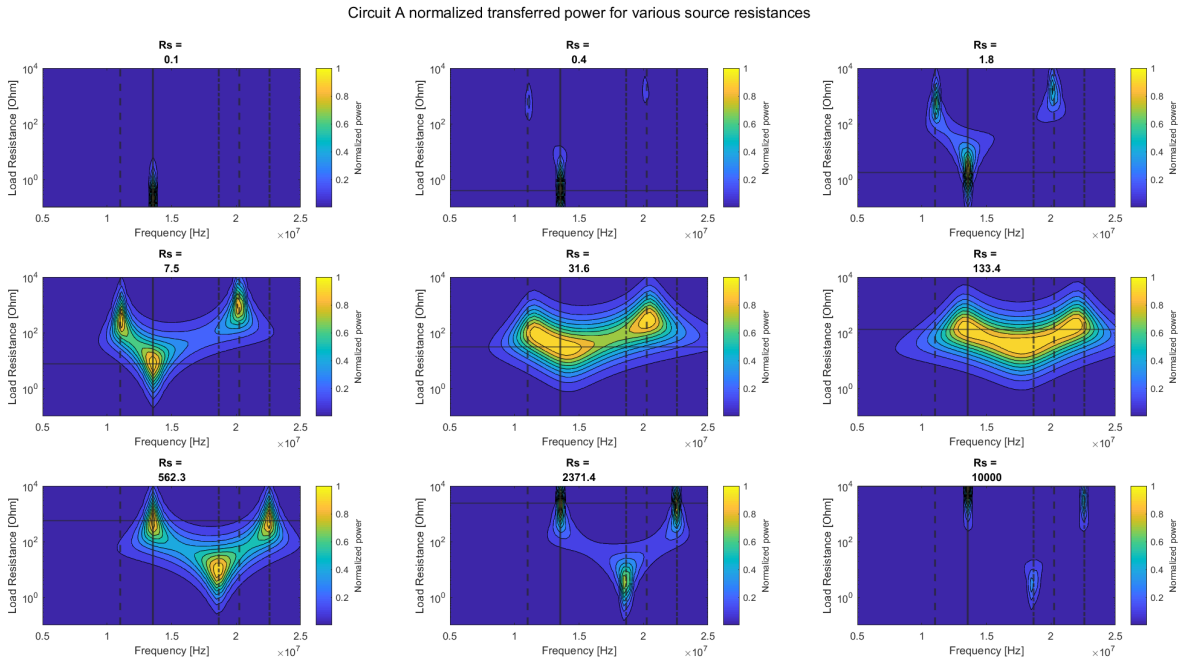


Figure A.1: Normalized power transfer as a function of frequency, load resistance and source resistance for circuit A. The solid line indicates the operating frequency, the dashed lines indicates zero frequencies for Z_{in}, and the dash-dot lines show pole frequencies for Z_{in}. The solid horizontal line indicates $R_l = R_s$.

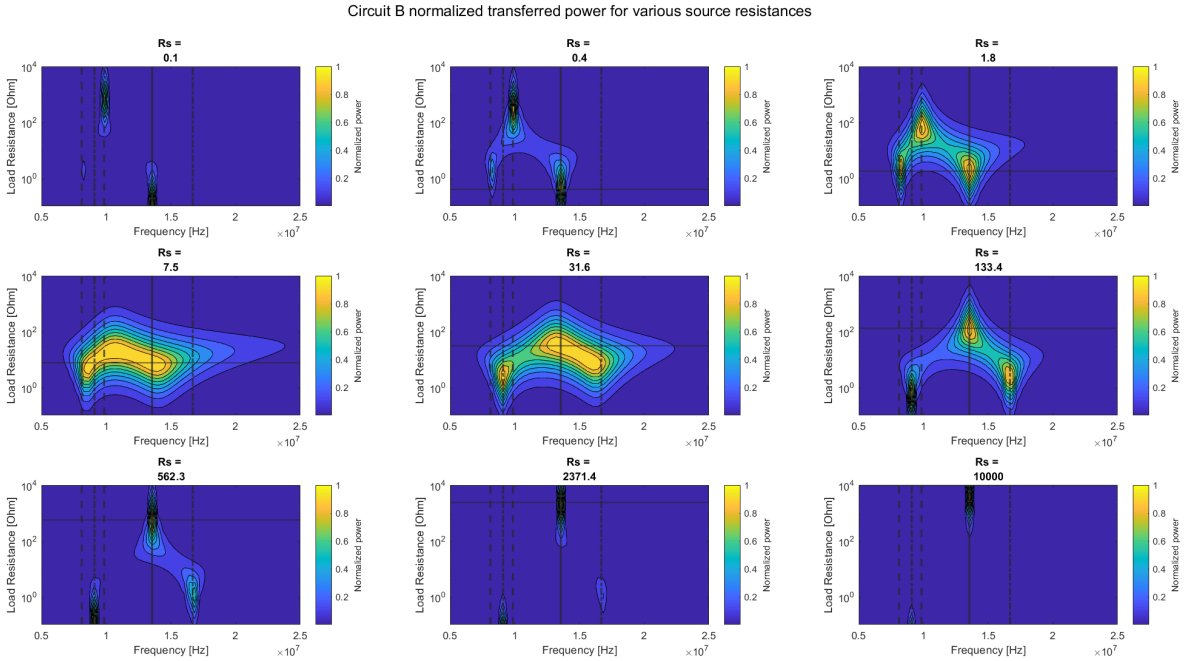


Figure A.2: Normalized power transfer as a function of frequency, load resistance and source resistance for circuit B. The solid line indicates the operating frequency, the dashed lines indicates zero frequencies for Z_{in}, and the dash-dot lines show pole frequencies for Z_{in}. The solid horizontal line indicates $R_l = R_s$.

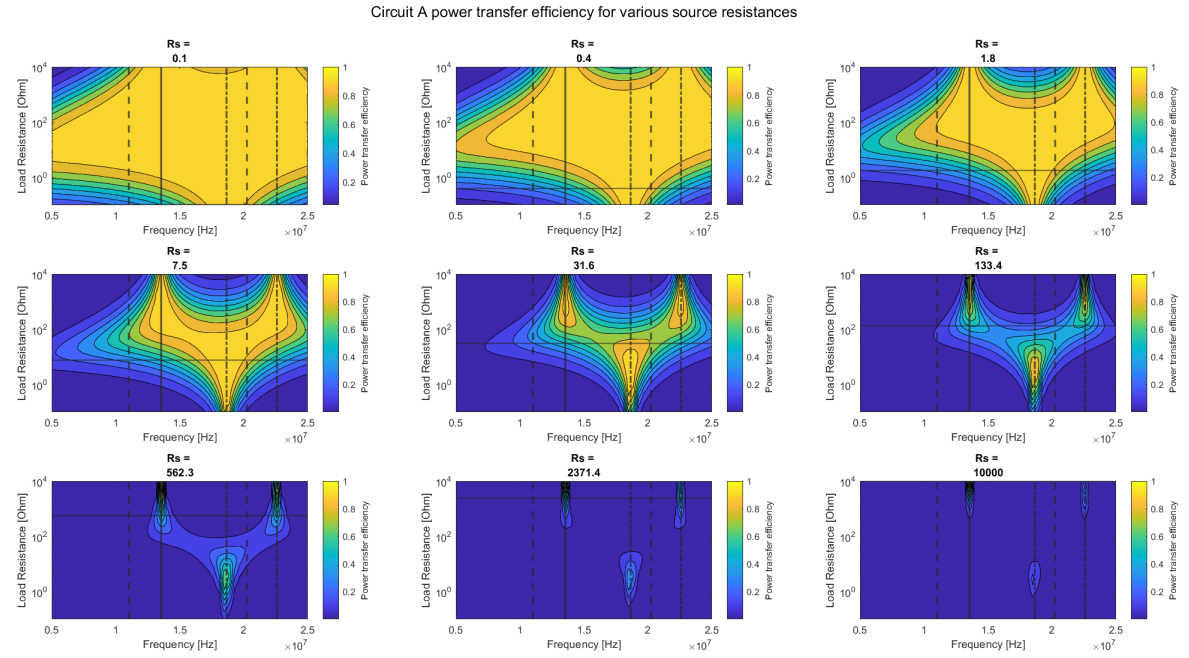


Figure A.3: Power transfer efficiency as a function of frequency, load resistance and source resistance for circuit A. The solid line indicates the operating frequency, the dashed lines indicates zero frequencies for Z_{in}, and the dash-dot lines show pole frequencies for Z_{in}. The solid horizontal line indicates $R_l = R_s$.

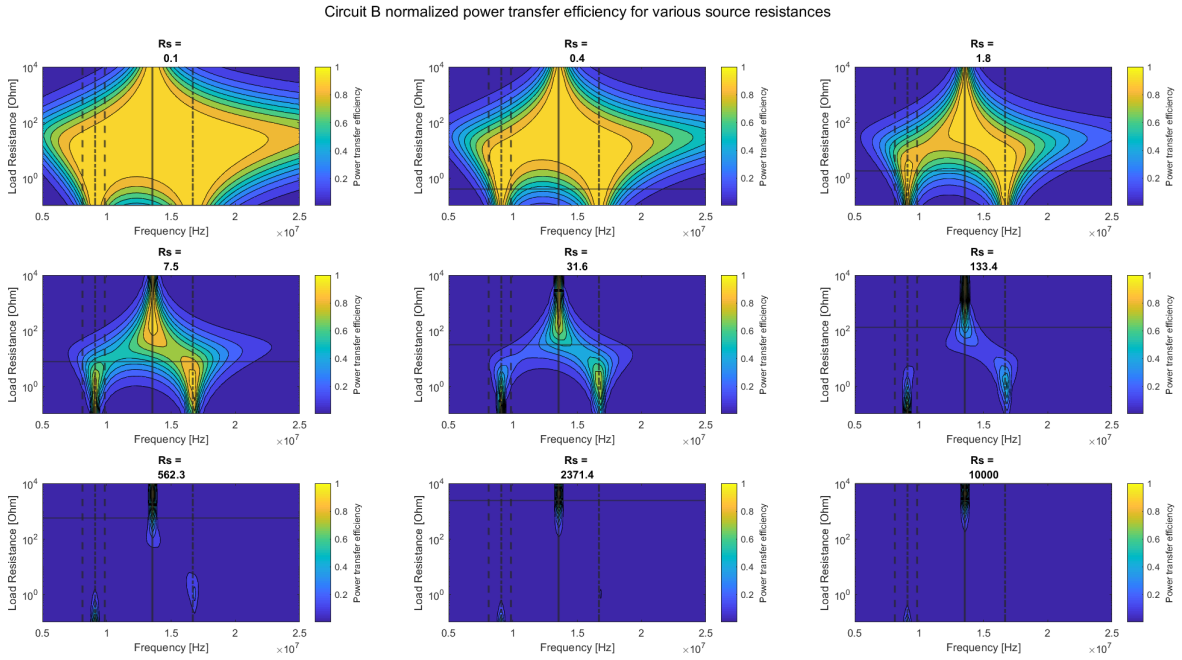


Figure A.4: Power transfer efficiency as a function of frequency, load resistance and source resistance for circuit B. The solid line indicates the operating frequency, the dashed lines indicates zero frequencies for Z_{in}, and the dash-dot lines show pole frequencies for Z_{in}. The solid horizontal line indicates $R_l = R_s$.

B

Full Prototype Schematics

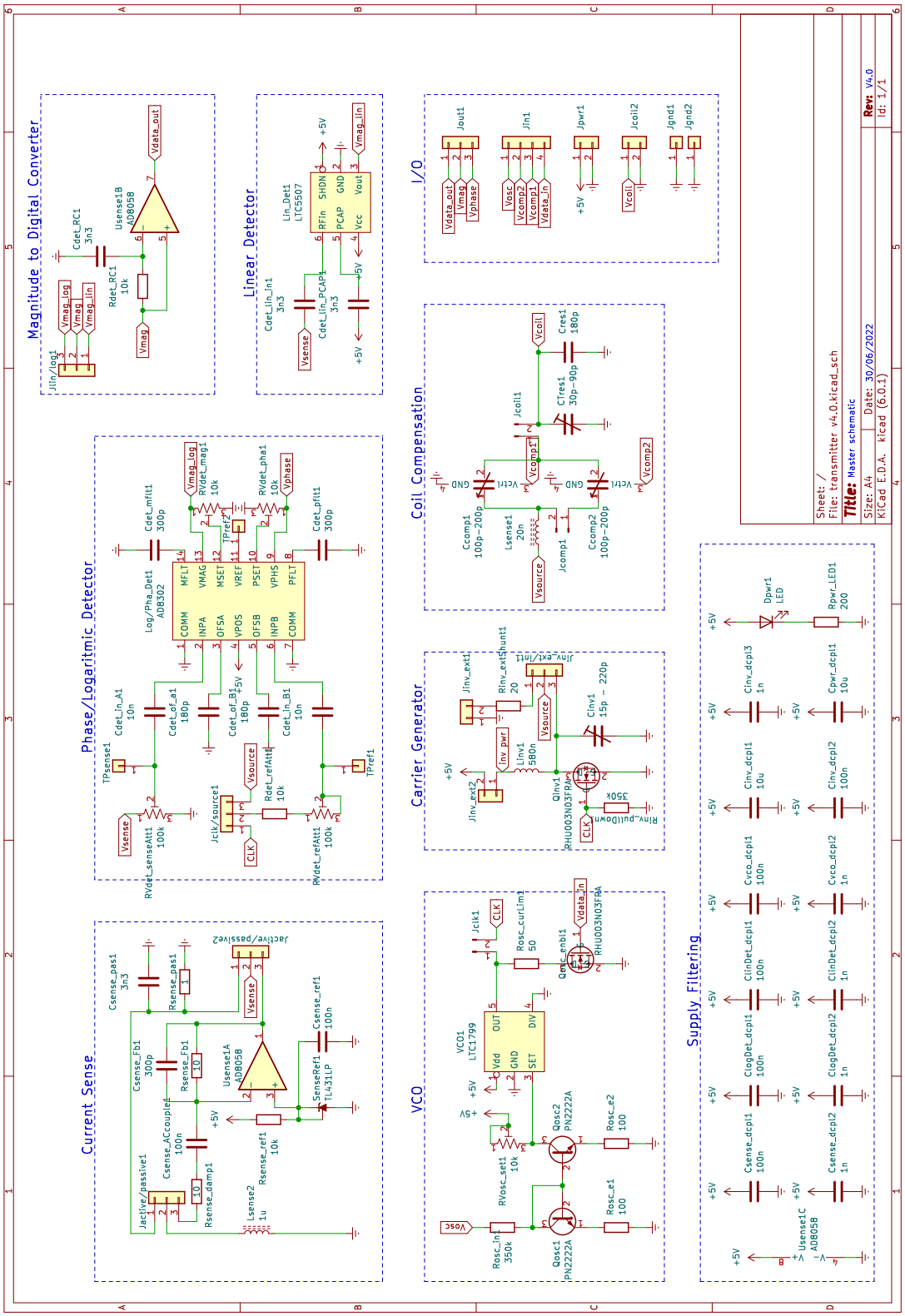


Figure B.1: Full master schematic

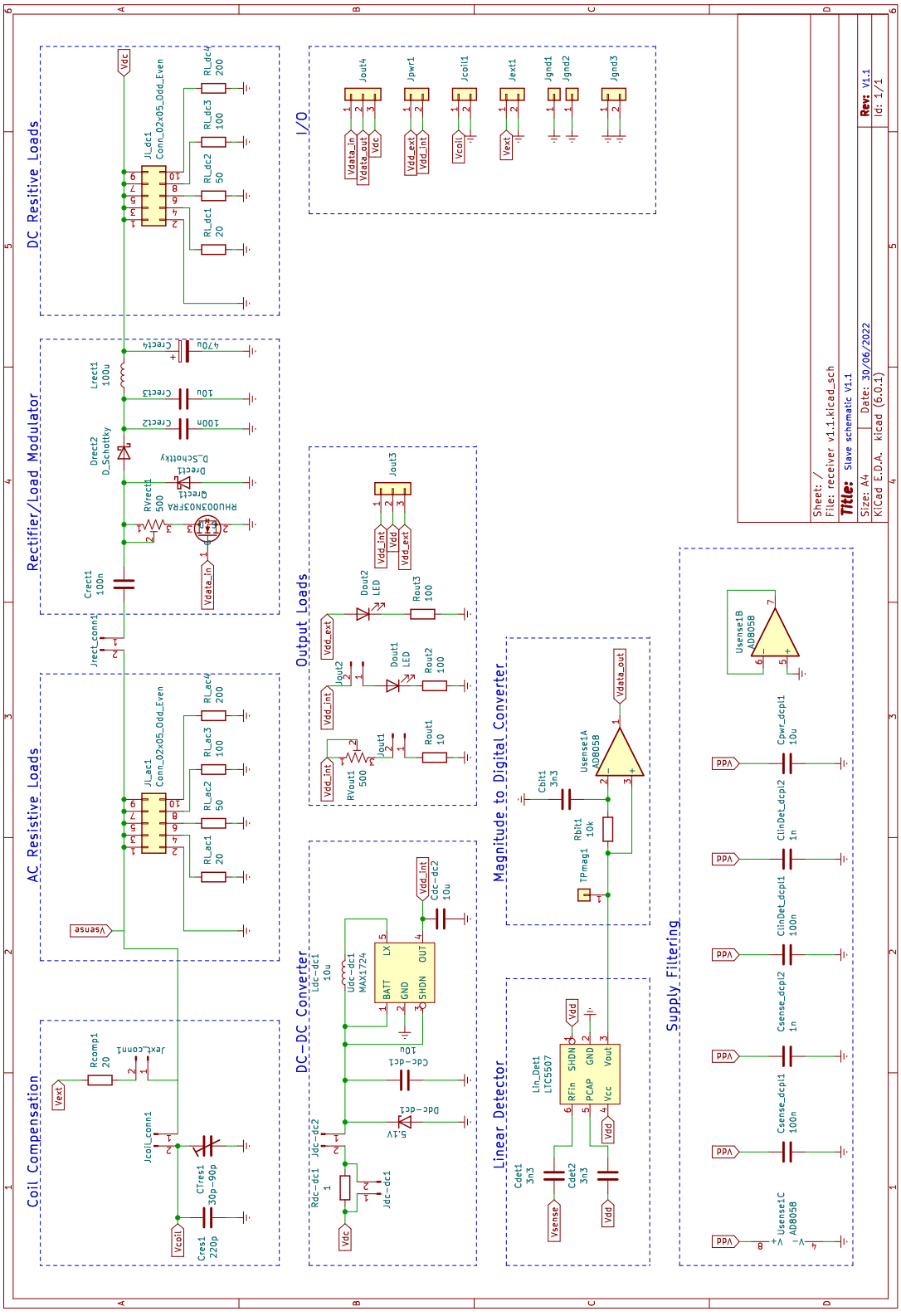
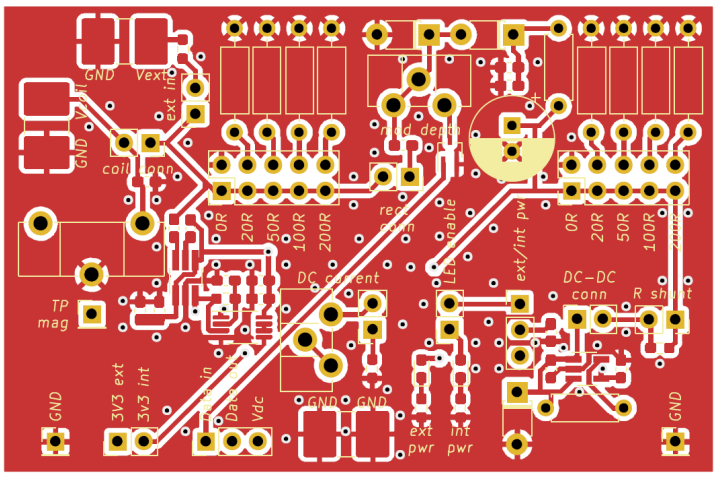


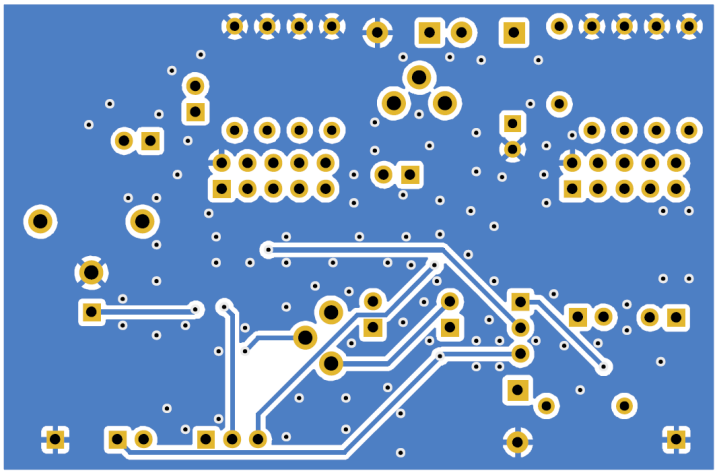
Figure B.2: Full slave schematic

C

PCB layouts

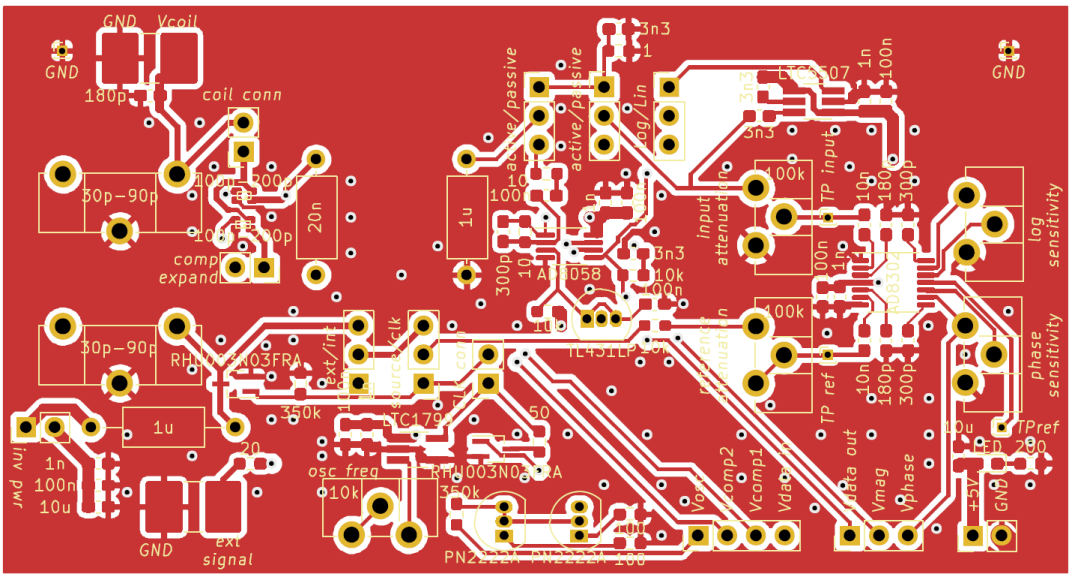


(a) Front copper and silk screen.

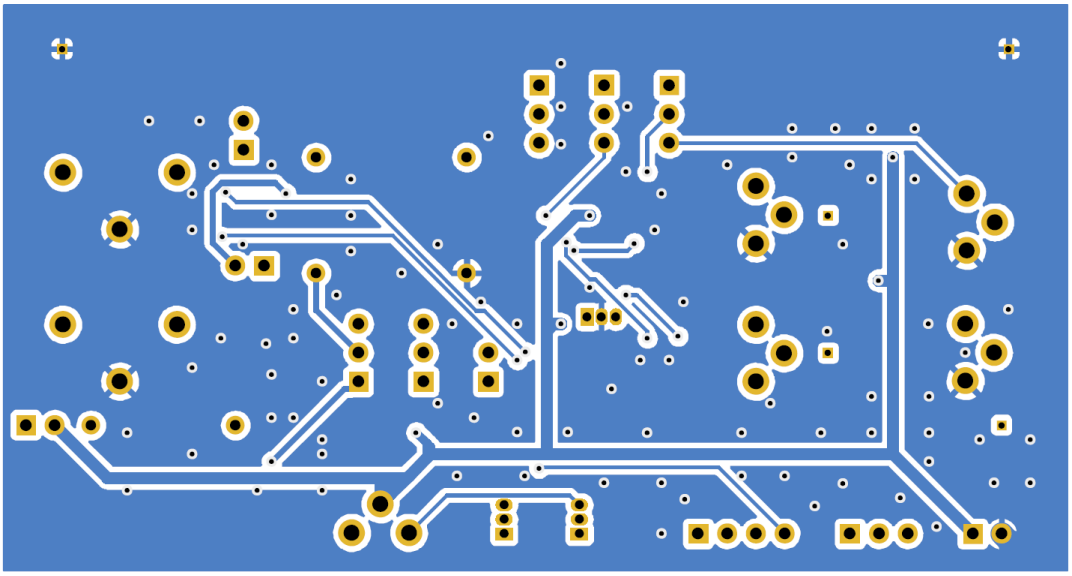


(b) Back copper.

Figure C.1: Layout for the slave PCB



(a) Front copper and silk screen.



(b) Back copper.

Figure C.2: Layout for the master PCB

D

Power Draw Interpolations

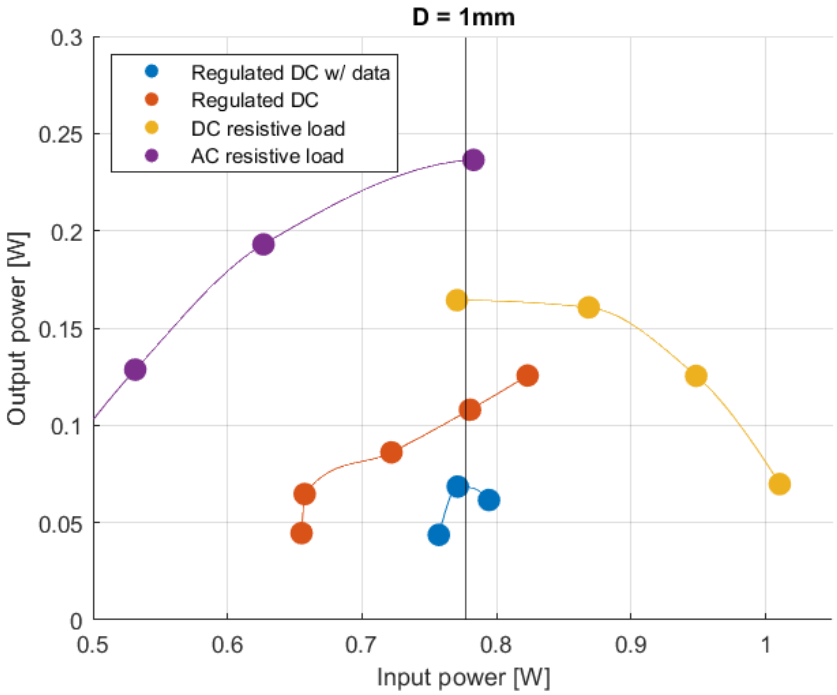


Figure D.1: Optimal input and output power for various loads at 1 mm coil separation. The solid black line indicates where the data was sampled to generate the sub-system power usage breakdown.

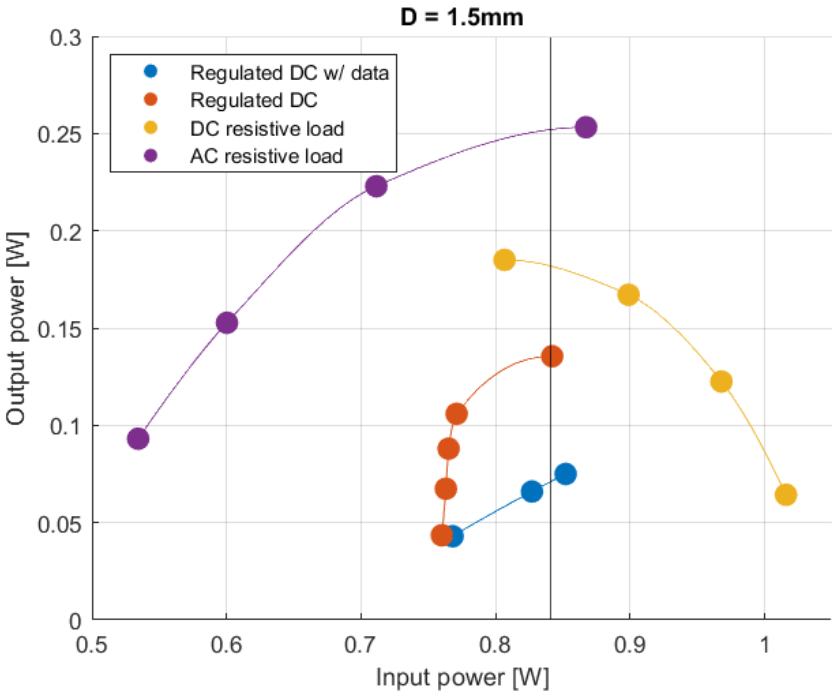


Figure D.2: Optimal input and output power for various loads at 1.5 mm coil separation. The solid black line indicates where the data was sampled to generate the sub-system power usage breakdown.

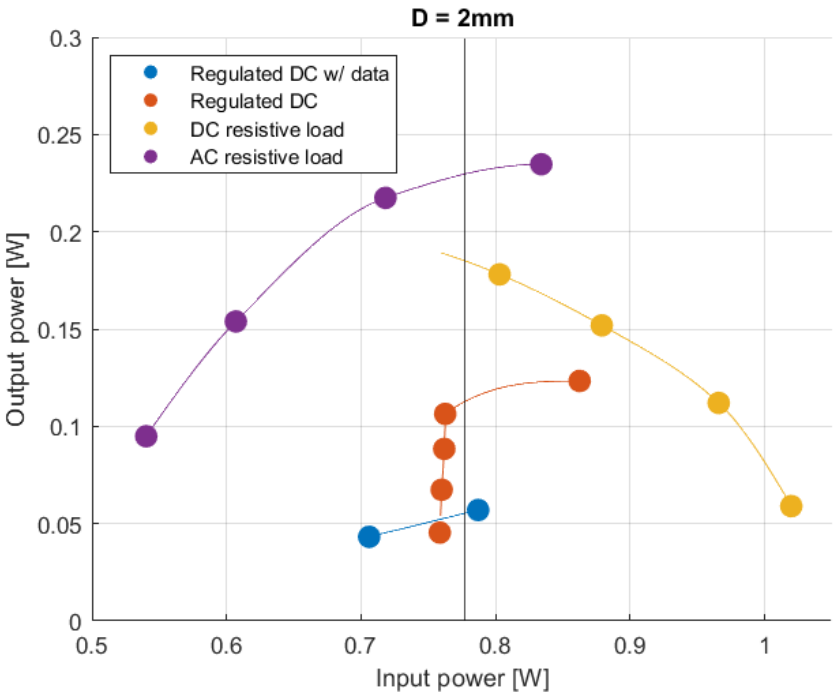


Figure D.3: Optimal input and output power for various loads at 2 mm coil separation. The solid black line indicates where the data was sampled to generate the sub-system power usage breakdown.

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