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A 10-mV-Startup-Voltage Thermoelectric Energy Harvesting System With a Piezoelectric Starter

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***Abstract*—An ultra-low-startup-voltage thermoelectric energy harvesting system assisted by a piezoelectric generator (PEG) is presented in this paper. When the energy harvesting system is implemented in a place where there is mechanical vibration, the associated PEG can generate a stable clock signal and drive the boost converter to start from the cold state even at extremely low thermoelectric generator (TEG) voltage. The proposed system is designed and simulated in a 180-nm BCD process. The simulations show that the proposed system can start the TEG system from the cold state from as low as 10 mV of TEG voltage while keeping a 63.9% efficiency. The peak power conversion efficiency is achieved at 74.9% when the TEG voltage is 50 mV.**

***Index Terms*—Thermoelectric energy harvesting, piezoelectric generator, cold-startup, maximum power point tracking.**

I. Introduction

Collecting energy from the ambient environment has a promising future and has attracted great interest from researchers. The energy harvesting system can be applied to power the low-power devices which require no battery replacement and a long operation lifetime. The most common energy sources include thermal energy, kinetic energy, RF energy, and solar energy. Among which the thermoelectric generator (TEG) can provide stable power and require only low-temperature difference.

However, due to the restriction on the dimension of the TEG and the variation of the temperature difference on it, the induced voltage from TEG can be as low as tens of millivolts. Therefore, a DC-DC converter is necessary to convert the low input voltage to a high output voltage to supply power for the following stages. In addition, a startup block is mandatory at the initial stage of the operation. In the past years, researchers have proposed various designs to startup the DC-DC converter without any external battery power. In [1], Yogesh et al. utilized a mechanical switch that is triggered by the movement of human body. Although it enables the system to start at 35 mV input voltage, the switching of the mechanical switch is not subtly controlled. Po-shuan et al. [2] proposed a low-voltage starter that converts the input DC voltage into an AC form via an oscillator, and then converts it back to a boosted DC level by a voltage multiplier. In [3], a reconfigurable TEG array is used to directly charge the output. Although these works used low-voltage startup design, the required minimum voltage is still higher than 20 mV.

The engines of airplanes and vehicles generate a lot of heat while working, besides, they also vibrate. Therefore, they are ideal thermal sources for the TEG to power the wireless sensors mounted on them. Meanwhile, the periodic kinetic vibration energy can be collected by a piezoelectric generator (PEG) to generate a clock signal which can be used to start up the DC-DC converter in a TEG system. In this paper, a thermoelectric energy harvesting system using PEG to achieve ultra-low start up voltage is proposed. The proposed system uses the PEG output as a clock signal to drive the switches in the boost converter during the startup stage.

The paper is organized as follows. Section II presents the operation principle of the proposed energy harvester and the system topology. The circuit implementation of key blocks is introduced in section III. The simulation results and discussions are presented in section IV. Section V draws the conclusion.

II. Proposed energy harvesting system

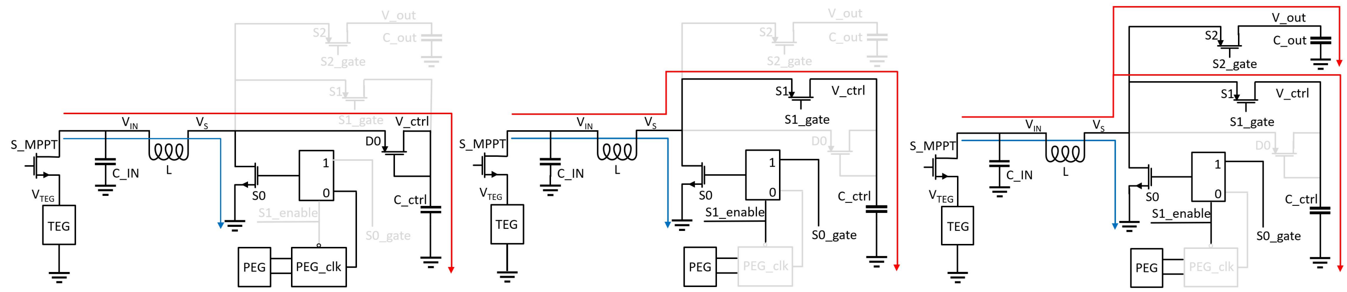
A. Operation principle

Fig. 1 shows the block diagram of the proposed boost converter. The TEG works as the input voltage source and the PEG_clk block provides the initial startup clock signal from the external PEG device to drive switches in the converter. The converter stores the power in two capacitors, C_ctrl provides the supply voltage, V_ctrl, for the internal control circuit, C_out is for the external output voltage, V_out.

There are three stages for the startup of the converter. In the first startup stage, as illustrated in Fig. 1(a), the PEG startup circuit is enabled to control the switch S0. As S0 turns ON, the current flowing through the inductor will keep increasing and store energy in it. After S0 turns OFF, the energy stored in the inductor flows into C_ctrl through the PMOS diode D0. This phase continues until V_ctrl is charged to 600 mV.

Fig. 1(b) shows the second startup stage. Once the V_ctrl reaches 600 mV, the signal $S1\_enable$ is pulled up and disables the PEG_clk block. Meanwhile, the MUX selects the signal $S0\_gate$ as the drive signal for S0, which is generated by the internal system clock powered by V_ctrl. After the switch S0 turns OFF, the switch S1 will be turned ON by signal $S1\_gate$ to transfer the energy stored in the inductor to capacitor C_ctrl. By disabling the diode D0, the system achieves higher efficiency and faster charging speed.

The third stage takes place after the V_ctrl goes above 1.2 V, as shown in Fig. 1(c). The switch S2 is turned ON periodically during the inductor discharging mode. In this phase, the energy harvested by TEG is transferred to C_out.



(a) (b) (c)

Fig. 1. Operation stages of the proposed converter. (a) First startup stage. (b) Second startup stage. (c) Third startup stage and Output stage.

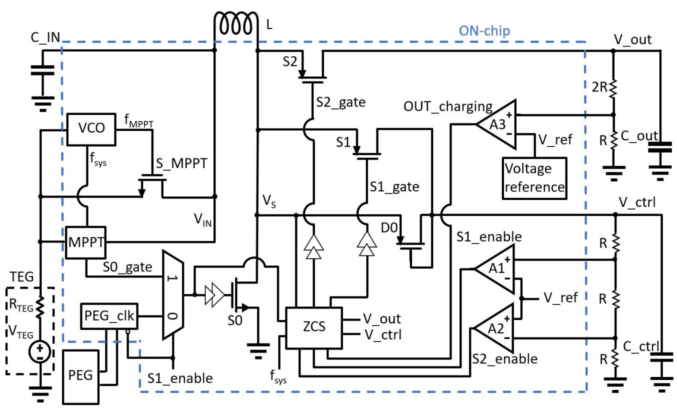
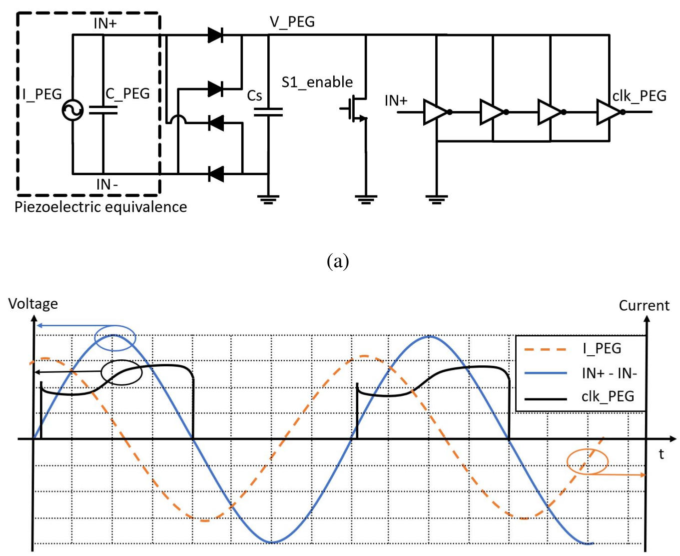


Fig. 2. Architecture of the proposed TEG energy harvesting system.



(a)

(b)

Fig. 3. PEG startup block and its waveform. (a) Circuit diagram of the PEG startup block. (b) Associated waveform in two periods.

In the meantime, the internal control circuit keeps consuming the energy stored in C_ctrl so that V_ctrl slowly drops. Since V_ctrl has the highest priority, once it decreases below 1.2 V, the switch S2 will be disabled temporarily, and S1 will be controlled to charge C_ctrl again. This phase continues until V_out is charged to 1.2 V.

As V_out goes above 1.2 V, the system stops the startup operation and enters the output stage. The switches S1 and S2 turn ON alternately to ensure the output port can provide a stable 1.2-V supply.

B. System architecture

Fig. 2 illustrates the architecture of the proposed TEG harvesting system. It consists of a PEG clock generator (PEG_clk), a voltage reference generator, voltage dividers, comparators, a voltage-controlled oscillator (VCO), a zero current switching (ZCS) block, and a maximum power point tracking (MPPT) block. The TEG and PEG are off-chip devices. The voltage dividers provide the comparators with a portion of V_ctrl and V_out. The operation stage of the system is indicated by the singles generated by comparators A1, A2 and A3. As the converter works in discontinues conduction mode, a ZCS block is required to determine the ON time for each PMOS gate.

The overall end-to-end efficiency is largely decided by both the MPPT efficiency and the converter efficiency. On one hand, the MPPT block together with C_IN monitors the V_{TEG} and stabilizes the input voltage of the inductor to half of V_{TEG}. It is realized by adjusting the duty of $S0\_gate$ to ensure that the circuit extracts maximum power from the TEG. On the other hand, the efficiency of the converter is further improved by the VCO which adjusts the system frequency adaptively based on the TEG voltage.

III. Circuit Implementation

A. PEG startup block

The primary goal of the startup block is to collect the vibrational energy to generate a clock signal, clk_PEG, which can drive the boost converter to work at extremely low TEG voltage. In order to realize this, a full-bridge rectifier (FBR) followed by four serially connected inverters is adopted, as shown in Fig. 3(a). By converting the sinusoidal input current I_PEG into a DC voltage, V_PEG, via the FBR, the capacitor can provide supply for the inverters. Fig. 3(b) illustrates the signal waveform in the startup block. As the PEG has an internal capacitor, which is charged and discharged periodically by the current, the polarity of $IN+$ and $IN-$ is also reversed periodically. Although the output of the inverter is not a very good square wave due to the fluctuation in the supply, the falling edge is sharp enough to close the NMOS in the boost converter in a short time without reducing the current in the inductor too much.

It is noted that all the harvested energy from the TEG source can be stored without sharing any portion for the startup clock generation, which dramatically decreases the required minimum TEG voltage.

B. ZCS

As the input power is relatively low, the discontinuous mode is more suitable for the operation of the boost converter to prevent the negative current. To achieve this, a ZCS circuit is required, which is illustrated in Fig. 4. The S1_select signal is used to select between V_ctrl and V_out to compare with V_S according to the operation stage. After the rising edge of either PMOS gate in the boost converter, the comparator will generate an increasing or decreasing signal, INC/DEC. For each clock period, only one of the counter is enabled and refreshed, which corresponds to the operating PMOS switch. The corresponding counter decides the ON time of signal $S1\_gate$ or $S2\_gate$ for the next period.

C. MPPT and VCO blocks

To achieve the maximum extractable energy from the TEG, the input resistance of the converter, R_{IN}, should be equal to the internal resistance of TEG source, R_{TEG}. R_{IN} is given by

$$R_{IN} = \frac{2L}{t_{on}^2 f_{sys}} \tag{1}$$

where L is the value of inductor, t_{on} is the ON time of the NMOS and f_{sys} is the switching frequency. Based on equation (1), by fixing either t_{on} or f_{sys} and adjusting another parameter, R_{IN} can be equal to R_{TEG}. However, as derived in [4], while the boost converter operates at its optimal frequency, f_{sys_opt}, the converter has the highest power efficiency. And the f_{sys_opt} is nearly proportional to V_{TEG}. Therefore, to minimize the total power consumption as well as matching the input impedance to the TEG source, a MPPT block is used to select the t_{on} for the NMOS and a VCO dynamically tunes the switching frequency for the whole system.

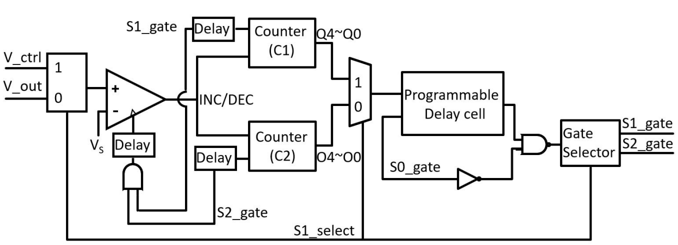


Fig. 4. Circuit diagram of ZCS block.

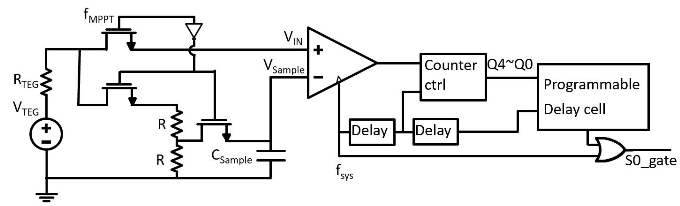


Fig. 5. Circuit diagram of MPPT block.

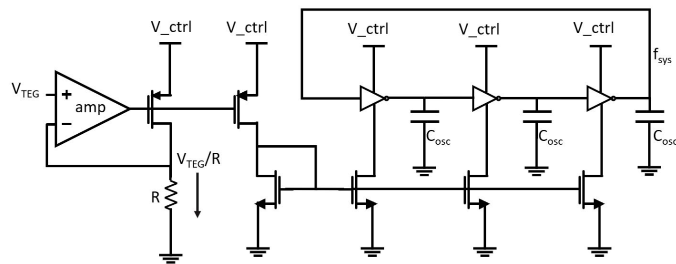


Fig. 6. Circuit diagram of VCO.

The circuit schematic of the MPPT block is shown in Fig. 5. A half of V_{TEG} is periodically sampled on C_{Sample}, thus $V_{Sample} = 1/2V_{TEG}$. Then it is compared with V_{IN} to decide the ON time for switch S0. If V_{IN} is large than $1/2V_{TEG}$, which means R_{IN} is larger than R_{TEG}, the counter will increase the delay of f_{sys}, then the input impedance is reduced based on equation (1) and vice versa.

Fig. 6 shows the circuit diagram of the VCO. The amplifier together with its feedback loop makes up a voltage-to-current generator. The generated current is V_{TEG}/R which is replicated by a current mirror to bias the ring oscillator. Thus, the output frequency of the oscillator is proportional to the biasing current, which can be expressed in

$$f_{sys} = \frac{V_{TEG}}{RC_{osc}V\_ctrl} \tag{2}$$

where C_{osc} is the capacitor in the oscillator.

IV. Simulation results

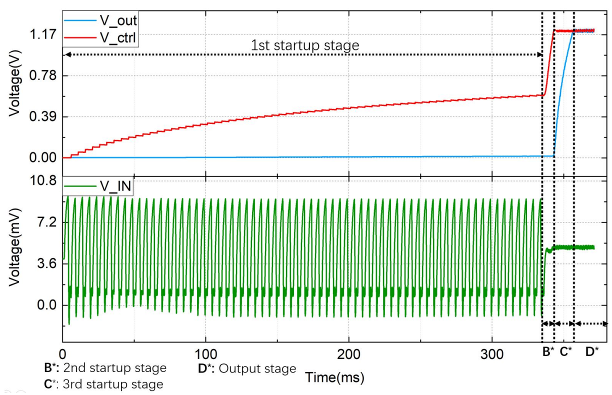
The proposed TEG energy harvesting system is designed and simulated in a 180 nm BCD process. The TEG is imitated by a DC voltage source with a serially connected resistance of 5 Ω. A 200 Hz sinusoidal current source in parallel with a 10 nF capacitor are used as the equivalence model of the PEG, which corresponds to a miniature PEG with several mm^2 size. The off-chip components also include a 220-μH inductor with a 290 mΩ DC resistance and several capacitors.

Fig. 7 shows the key signals during the cold-startup of the system. It takes 356 ms in total for the whole system to startup. The achieved minimum V_{TEG} for cold-startup is 10 mV. At the initial stage, only the PEG startup circuit works. This stage takes up the longest time during the startup, even though

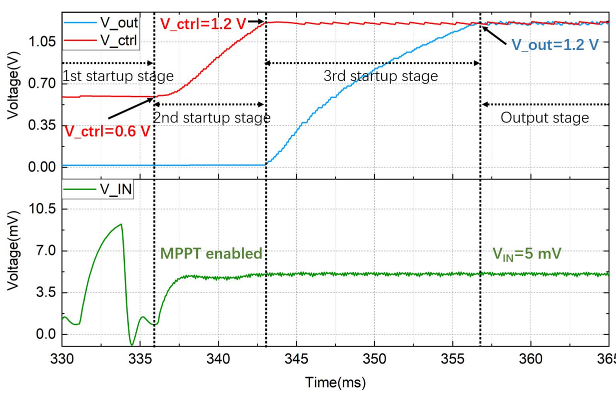
TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

	2012 [5][1]	2018 [6][1]	2019 [8][1]	2021 [7][1]	This work[2]
Process	0.13 μm	65 nm	0.18 μm	0.18 μm	**0.18 μm**
Architecture	Transformer	Boost	Transformer	Boost	**Boost**
V_out	2 V	1.1 V	1.2 V	1.2 V	**1.2 V**
Peak efficiency	61%	74.9%	81.5%	80%	**74.9%**
Min. V_{TEG} for cold-start	40 mV	40 mV	38 mV	50 mV	**10 mV**
Efficiency @ Min. V_{TEG}	32% @ 40 mV	12% @ 40 mV	32% @ 38 mV	58% @ 50 mV	**63.9% @ 10 mV**

[1] The cited results in the references are all measurement results.
[2] This work uses pre-layout simulation results.



(a)



(b)

Fig. 7. Startup waveform at V_{TEG}=10 mV. (a) Full waveform from the cold state to the normal operation state. (b) Zoomed-in waveform showing the details at the second and third startup stage.

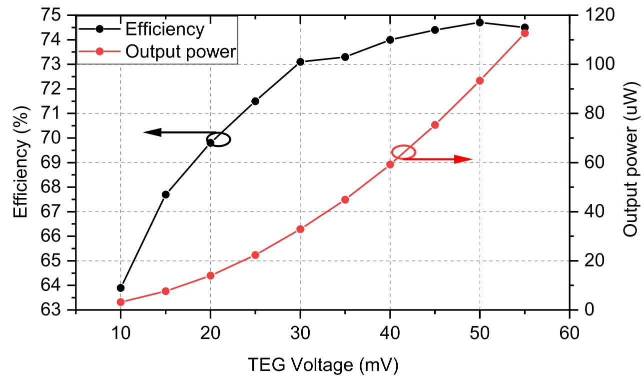


Fig. 8. Simulated efficiency and output power versus V_{TEG}.

there is no active power consumption in the circuit. The low switching frequency and high voltage drop on the PMOS diode impede the rising speed of V_ctrl. As V_ctrl goes over 600 mV, the system enters the second startup stage, as shown in Fig. 7(b). The PEG starter is blocked in the following stages. All the control circuits are enabled, and the system clock is replaced by the signal generated by the internal oscillator. The MPPT is also enabled, which stabilizes the input voltage of the inductor, V_{IN}, at half of the TEG voltage. The MPPT maximizes the extractable power from the TEG source and reduces the time spent in this stage. Once V_ctrl reaches 1.2 V, it stops increasing and is regulated by the ON-OFF control of ZCS block. During the third startup stage, the output voltage V_out keeps rising until it reaches 1.2 V. Eventually, in the output stage, the output port is stabilized at 1.2 V.

Fig. 8 depicts the simulated energy harvesting efficiency and output power versus V_{TEG}. The efficiency is calculated by dividing the maximum harvested power from the TEG source by the ideal input power ($V_{TEG}^2/4R_{TEG}$). The peak efficiency is achieved at 74.9% with V_{TEG} = 50 mV. It is noticeable that, even at ultra-low input TEG voltage at 10 mV, the proposed system can still achieve 63.9% efficiency.

The performance of proposed TEG system is compared with the state-of-the-art works in Table I. This design pushes the minimum cold-startup voltage to a level of 10 mV while others remain at around 40 mV. Meanwhile, the efficiency at the lowest V_{TEG} is also improved significantly to 63.9%.

V. Conclusion

This paper presents a thermoelectric energy harvesting system assisted by a PEG startup circuit. The VCO and MPPT circuit dynamically control the switching frequency and duty cycle by sensing V_{TEG}. The ZCS block tracks the optimal ON time for PMOS to maximize the energy conversion. A minimum startup voltage of 10 mV is achieved with an energy harvesting efficiency of 63.9% thanks to the PEG startup block. The peak efficiency is 74.9%, achieved with 50 mV TEG voltage.

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