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DOI
10.1109/TPEL.2021.3130677

Publication date
2022

Document Version
Accepted author manuscript

Published in
IEEE Transactions on Power Electronics

A Carrier-based Two-Phase-Clamped DPWM Strategy With Zero-Sequence Voltage Injection for Three-Phase Quasi-Two-Stage Buck-Type Rectifiers

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***Abstract*—A three-phase buck-type rectifier features a step-down ac-dc conversion function, which is considered as a prominent solution for electric vehicles chargers and telecommunication systems integrated to the grid above 380 V line-to-line. However, traditional solutions for those applications employ cascaded architectures with an ac-dc Boost-type stage and a dc-dc Buck-type stage which may suffer from high switching losses and large dc-link capacitor volume. To relieve this issue, a straightforward carrier-based two-phase clamped DPWM strategy with generalized zero-sequence voltage injection is proposed in this work for the commonly employed cascaded circuit. This method can stop the switching actions in the front-end stage during two-thirds of the grid period, which can yield to the best switching loss reduction. The operation of the front-and back-end converter stages become highly coupled to each other, which reduces the size requirement of capacitor in the dc-link. Therefore the equivalent circuit behaves as a quasi-two-stage buck-type rectifier allowing an enhancement of the system power density by improving power conversion efficiency and by reducing the volume of passive components and heatsink. The proposed carrier-based two-phase clamped DPWM strategy is described, analyzed, validated, and compared with different PWM methods on PLECS based simulation and a 5 kW prototype.**

***Index Terms*—Carrier-based, discontinuous pulsewidth modulation (DPWM), zero-sequence voltage injection, buck-type rectifier.**

I. Introduction

THREE-PHASE buck-type rectifiers feature a step-down function widely employed in industrial applications, such as electric vehicle (EV) batteries charging systems, data centers, and power supplies for telecommunications, where the 480 or 380 V (line-to-line rms voltage) grid voltage can be stepped down to 250-450 V dc [1]–[4]. In practice, two-stage power converters are normally used to allow the power conversion from the three-phase ac grid to a dc bus with lower voltage, which consist of a front-end boost-type rectifier providing 650 ... 800 V dc with a large capacitance in the dc-link, and a subsequent step-down dc-dc converter.

In order to achieve a smaller filter size and higher power efficiency for buck-type rectifiers, a wide variety of interesting solutions have been proposed on single-stage circuit topologies and their corresponding modulation strategies [5]–[15]. A three-phase six-switch buck-type PFC rectifier is studied in [5], and an ultra high efficiency can be achieved in comparison with other three-phase rectifier systems. The three-phase buck-type SWISS rectifier is introduced in [6], [7], which can be a favorable solution for EV battery charger systems. A new modulation concept for the uni- and bidirectional SWISS rectifier is discussed in [8] to improve the current distortions at the grid voltage sector boundaries. To reduce the input current and voltage ripples of the traditional SWISS rectifier, an interleaved SWISS rectifier is presented in [9], [12]. The delta-type current-source rectifier is designed in [10] to reduce the conduction loss in traditional current-source rectifiers [11], [13]. Although single-stage buck-type rectifiers are able to realize the voltage step-down directly, some technologies may suffer from a more complex modulation operating logic requiring overlap-time between the semiconductor bridge because of the impressed output current [8], [9], [11], [16]. Several circuit technologies of single-stage buck-type rectifiers will display limited power factor range [5]–[10]. Recently, with the promotion of commercial wide band gap semiconductor devices, i.e., Silicon Carbide (SiC), the losses for the conventional two-stage solution of such buck-type rectifier systems can be reduced significantly [17]–[19]. Therefore, a conventional two-stage rectifier circuit (c.f. **Fig. 1**) turns to be favored in practice due to simpler modulation operating logic and wider power factor range, where the front-end converter comprises a three-phase three-wire two-level six-switch voltage source rectifier (2L-VSR), which inherent features low complexity and low cost, and the back-end circuit works as a dc-dc buck-type converter, as shown in **Fig. 1**.

To further improve the power density, several advanced modulation strategies have been studied for the front-end circuit of **Fig. 1**, where two-phases in the ac side are clamped, and no dc-link voltage control is needed, leading to a very small capacitance requirement in the dc-link [20]–[28]. Such a circuit with low dc-link capacitance is called three-phase quasi-two-stage buck-type rectifier in this paper. One-phase modulation or two-phase clamped discontinuous pulsewidth modulation (DPWM) has been previously investigated in [20]–

Manuscript received March 09, 2021; revised June 01, 2021, August 01, 2021, and September 27, 2021 ; accepted November 22, 2021. This work was supported by the National Natural Science Foundation of China under Grant No. 51577118. (*Corresponding author: Yong Wang.*)

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[23] for motor drives or solar power generation systems, where only one phase-leg out of three phase legs in the ac-dc power conversion stage performs the switching actions at the same time, and the converter with such a modulation can be called as electrolytic capacitorless PWM converter. A comprehensive analysis in harmonic distortion and switching losses, and experimental validation of the two-phase clamped DPWM has been performed for EV traction inverters in [24]. In [25], the two-phase clamped DPWM has been applied in the fast dc-type EV charger, and a look-up table has been provided to implement such a modulation. Two-stage three-phase dc-ac buck-boost converters with synergetically controlled two-phase clamped DPWM are well-studied in [26], [27], in which a wider dc voltage can be achieved for the battery charger system. This converter functionality under regular and irregular grid conditions has been discussed in [28] as well. It is found that two-phase clamped DPWM can yield to the best switching loss reduction in any known DPWM strategies for the front-end ac-dc circuit, i.e., the ones described in [17], [29]–[32]. Another similar operations as the two-phase clamped DPWM but with different topology, e.g., Vienna-type front-end circuit [33], delta-switch-type front-end circuit [13], and series-resonant-type back-end circuit [34], have been proposed. However, for all previously studied two-phase clamped DPWM strategies, the modulation operations for front- and back-end stages are independent, and the relationship with traditional modulation techniques (space-vector-based and carrier-based PWM techniques) is unclear. Additionally, the literature works lack a comprehensive performance comparison in both front- and back-end circuits among different PWM methods over the whole power factor (PF) range, i.e., PF = 1 ... -1.

To fill these gaps, a new straight-forward carrier-based two-phase-clamped DPWM strategy with generalized zero-sequence voltage injection is proposed in this paper, where the back-end dc-dc stage can be regarded as the fourth phase-leg of the three-phase quasi-two-stage buck-type rectifier. Herein, the modulation signals are determined by the reference voltage and the zero-sequence voltage, and the equivalent relationship with the space-vector implementation and the duty cycle expression implementation are clarified. With such an approach, it is easy to carry out systematic analysis of performance characteristics about the modulator over the whole PF range in terms of switching losses, current ripples, and common-mode voltage (CMV) based on the universal theoretical model in [29], [32], [35]. To the best of the authors' knowledge, there is no literature work that has developed such a straight-forward carrier-based DPWM approach with generalized zero-sequence injection into the grid-connected rectifiers applications with two-phase-clamped functionality.

This paper contributes into the following points:

- A carrier-based two-phase-clamped DPWM strategy with generalized zero-sequence voltage injection is proposed.
- Theoretical basis of the proposed strategy and the relationship with different implementations are clarified.
- Comprehensive analysis of different performance characteristics over the whole PF range for the two-phase-clamped DPWM strategy in both front- and back-end stages is given. This includes a detailed derivation and analysis of the semiconductor switching loss and filter current ripple functions, and generated common-mode voltage, among others.
- The benchmarking of different PWM strategies for the grid-connected quasi-two-stage buck-type rectifiers in theory, simulations and experiments is performed.

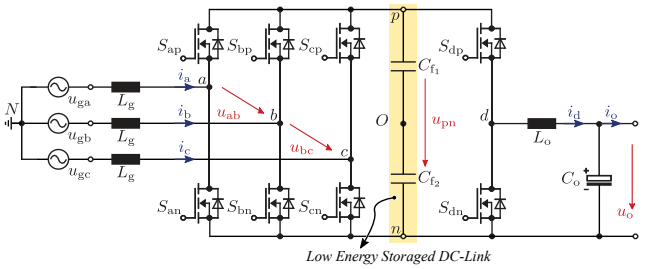

Fig. 1. Circuit topology for three-phase quasi-two-stage buck-type rectifier.

The rest of this paper is organized as follows. In Section II, the detailed principle of the studied carrier-based two-phase-clamped DPWM strategy with zero-sequence voltage injection is illustrated and its relationship with other PWM implementations is clarified. In Section III, performance characteristics in terms of switching losses, current ripples, and CMV are investigated mathematically and compared with other classical PWM methods with constant dc-link voltage. Finally, in Section IV, the key parameters of the prototype are designed and the studied carrier-based two-phase clamped DPWM strategy is evaluated and benchmarked against other traditional PWM methods with constant dc-link voltage in both simulation and a 5 kW, 400 V dc output prototype.

II. Working Principle of the Studied Two-Phase Clamped DPWM Strategy

The circuit topology for the studied three-phase quasi-two-stage buck-type rectifier is depicted in **Fig. 1**. As previously discussed, the front- and back-end circuits are connected to each other through a dc-link with low energy storage capability, which makes the operation of both circuits highly coupled to each other. Herein, the front-end ac-dc stage is composed of six active switches, $S_{\mathrm{abc,p/n}}$, and the back-end dc-dc stage is structured by another two active switches, $S_{\mathrm{d,p/n}}$, which is connected with the front-end stage via the dc-link capacitors, $C_{\mathrm{f_1,f_2}}$; u_{pn} is the dc-link voltage; u_{gabc} and i_{abc} are the grid input voltage and current, respectively; L_{g} represents the the ac phase inductors; i_{d} is the phase current for the back-end Buck circuit; u_{o} and i_{o} are the output voltage and current of the system; L_{o} is the output inductor, and C_{o} is the output capacitor. To make the two-phase clamped DPWM strategy valid over each fundamental period, two-phases with maximum voltage magnitude should be always clamped. Assuming no voltage drop across the circuit components and a symmetric ac voltage, the output voltage u_{o} of the studied three-phase quasi-two-stage buck-type rectifier should be adjusted to values starting from zero to:

$$u_{\mathrm{o}} \leq u_{\mathrm{pn,min}} = \frac{3}{2} U_{\mathrm{m}} \tag{1}$$

where, U_{m} is the magnitude of the grid phase voltage.

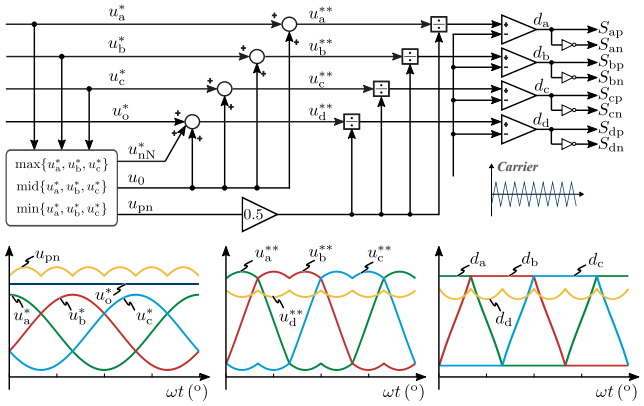

Fig. 2. Block diagram of the carrier-based PWM modulator and the simplified illustration of the studied PWM method.

A. Carrier-based two-phase-clamped DPWM strategy with zero-sequence voltage injection

Assuming that the operating condition is balanced and symmetrical, the reference voltages (u_{a}^*, u_{b}^*, and u_{c}^*) for the front-end ac-dc stage can be expressed as:

$$\begin{cases} u_{\mathrm{a}}^* = U_{\mathrm{m}}^* \cos \omega t \\ u_{\mathrm{b}}^* = U_{\mathrm{m}}^* \cos\left(\omega t - 2\pi/3\right) \\ u_{\mathrm{c}}^* = U_{\mathrm{m}}^* \cos\left(\omega t + 2\pi/3\right) \end{cases} \tag{2}$$

where ω is the phase angle speed, and U_{m}^* is the magnitude of the reference voltages. After that, the dc-link voltage can be decided by:

$$u_{\mathrm{pn}} = u_{\mathrm{pN}} - u_{\mathrm{nN}} \tag{3}$$

It is noted that in the three-phase two-level ac-dc converter, only the phase leg with the maximum or minimum references can be clamped, otherwise, it will cause the problem of over-modulation in another phase and affect the waveform quality [36]. Therefore, u_{pN} and u_{nN} are uniquely determined, i.e., $u_{\mathrm{pN}} = \max\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\}$ and $u_{\mathrm{nN}} = \min\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\}$, and there is no need to control u_{pn} to get the desired shape.

Thereafter, the reference voltage for the back-end dc-dc stage with the reference output voltage, u_{o}^*, is defined as:

$$u_{\mathrm{d}}^* = u_{\mathrm{o}}^* + u_{\mathrm{nN}} = u_{\mathrm{o}}^* + \min\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\} \tag{4}$$

The zero-sequence voltage of the modulation voltage of the studied method can be determined by:

$$\begin{aligned} u_0 = u_{\mathrm{NO}}^* &= u_{\mathrm{Nn}}^* + u_{\mathrm{nO}}^* = -\min\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\} - \frac{1}{2}u_{\mathrm{pn}} \\ &= -\frac{1}{2}\left(\max\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\} + \min\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\}\right) \\ &= \frac{1}{2}\mathrm{mid}\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\} \end{aligned} \tag{5}$$

Finally, the modulation waveforms u_{a}^{**}, u_{b}^{**}, u_{c}^{**}, and u_{d}^* of the studied carrier-based two-phase-clamped DPWM strategy with zero-sequence voltage injection can be obtained to compare with the PWM triangular carriers:

$$\begin{cases} u_{\mathrm{a}}^{**} = u_{\mathrm{a}}^* + u_0 = U_{\mathrm{m}}^* \cos(\omega t) + u_0 \\ u_{\mathrm{b}}^{**} = u_{\mathrm{b}}^* + u_0 = U_{\mathrm{m}}^* \cos(\omega t - 2\pi/3) + u_0 \\ u_{\mathrm{c}}^{**} = u_{\mathrm{c}}^* + u_0 = U_{\mathrm{m}}^* \cos(\omega t + 2\pi/3) + u_0 \\ u_{\mathrm{d}}^{**} = u_{\mathrm{d}}^* + u_0 = u_{\mathrm{o}}^* + \min\{u_{\mathrm{a}}^*, u_{\mathrm{b}}^*, u_{\mathrm{c}}^*\} + u_0 \end{cases} \tag{6}$$

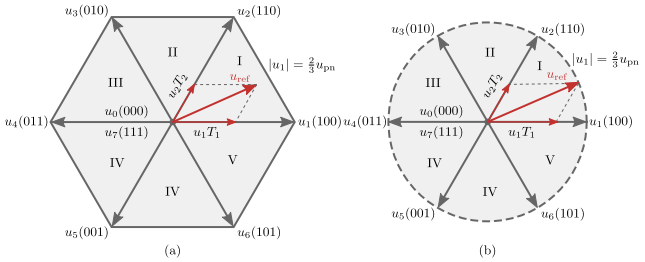

Fig. 3. The space-vector diagram for (a) the traditional PWM methods, (b) the studied two-phase-clamped DPWM.

The block diagram of the implementation of the studied carrier-based PWM modulator and its simplified illustration are presented in **Fig. 2**. It is found that the modulation waveforms u_{a}^{**}, u_{b}^{**}, u_{c}^{**} of the two-phase-clamped DPWM strategy in the front-end stage are exactly the same as the ones for the conventional SVPWM [29]. With the injection of the zero-sequence voltage, the studied two-phase clamped DPWM method can be similarly realized by the modern digital signal processing (DSP) with enhanced pulse width modulator (ePWM) units as other PWM methods, where the modulation signals are loaded into compare registers per phase directly and compared with inner counters to generate the switching signals, S_{a}, S_{b}, S_{c}, and S_{d}.

B. Space-vector modulation concept for the studied two-phase-clamped DPWM strategy

In traditional space-vector modulation for two-stage ac-dc converters, the dc-link voltage is normally kept fixed or constant, and thus the boundary of the space-vector diagram is a hexagon, as shown in **Fig. 3**(a). To synthesize a sinusoidal ac voltage output, as an example in Sector I, the space vector u_{ref} of the sampled reference voltage is synthesized by using the two nearest active voltage vectors u_1(100) and u_2 (110) and zero voltage vector u_0(000) or u_7(111) in one switching period T_s. It is noted that the zero voltage vector is indispensable to compensate the remaining time in one switching period. If both u_0(000) and u_7(111) are used, no phase-leg can be clamped, and these modulations are known as continuous PWM, while, if either u_0(000) or u_7(111) are utilized, only one phase-leg is clamped, which are called discontinuous PWM.

To realize the two-phase-clamped DPWM [20]–[23], as the example presented in **Fig. 3**(b), the execution time of the two nearest active voltage vectors u_1(100) and u_2 (110), i.e., T_1 and T_2, should satisfy the following equations:

$$\begin{cases} u_{\mathrm{ref}} T_{\mathrm{s}} = u_1 T_1 + u_2 T_2 \\ T_1 = \dfrac{\sqrt{3}|u_{\mathrm{ref}}|\left(\sqrt{3}\cos\omega t + \sin\omega t\right)}{2u_{\mathrm{pn}}} T_{\mathrm{s}} \\ T_2 = \dfrac{\sqrt{3}|u_{\mathrm{ref}}|\sin\omega t}{u_{\mathrm{pn}}} T_{\mathrm{s}} \end{cases} \tag{7}$$

Since neither u_0(000) nor u_7(111) can be selected to construct the reference voltage, u_{ref}, $T_1 + T_2 = T_{\mathrm{s}}$, and the relationship between u_{ref} and u_{pn} can be derived:

$$u_{\mathrm{pn}} = \left(\frac{3}{2}\cos\omega t + \frac{\sqrt{3}}{2}\sin\omega t\right)|u_{\mathrm{ref}}| \tag{8}$$

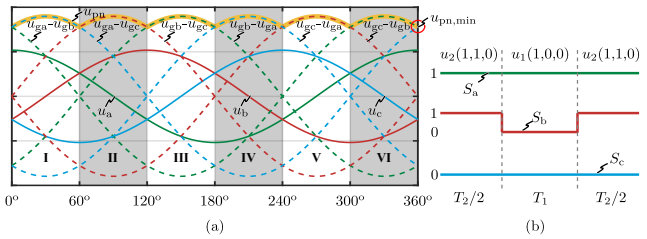

Fig. 4. Sectors definition and switching sequence for the two-phase clamped DPWM, (a) sectors definition, (b) switching sequence in Sector I.

Therefore, with the variable dc-link voltage controlled by the back-end dc-dc circuit, a sinusoidal ac voltage output in the front-end ac-dc circuit can be obtained without any zero voltage vector, i.e., two phase-legs are clamped at any instant either high (positive dc-rail) or low (negative dc-rail).

C. Relationship between space-vector-based and carrier-based PWM implementation

Taking Sector I as an example, i.e., $0^{\rm o} \le \varphi \le 60^{\rm o}$ in **Fig. 4**(a), (8) can also be expressed as:

$$u_{\rm pn} = U_{\rm m}^* \cos\omega t - U_{\rm m}^* \cos(\omega t + 2\pi/3) = u_{\rm a}^* - u_{\rm c}^*, \quad (9)$$

which is exactly the same as:

$$u_{\rm pn} = \max\{u_{\rm a}^*, u_{\rm b}^*, u_{\rm c}^*\} - \min\{u_{\rm a}^*, u_{\rm b}^*, u_{\rm c}^*\} \quad (10)$$

Moreover, as seen in **Fig. 4**(b), phase b is the only phase that is kept switching, whose duty cycle $d_{\rm b}$ is:

$$d_{\rm b} = \frac{T_2}{T_{\rm s}} = \frac{\sqrt{3}|u_{\rm ref}|\sin\omega t}{u_{\rm pn}}. \quad (11)$$

Then, the modulation wave for phase b with the triangular carrier wave can be calculated by:

$$\begin{aligned} u_{\rm b}^{**} &= \frac{1}{2}u_{\rm pn}\,(2d_{\rm b}-1) = (\frac{3\sqrt{3}}{4}\sin\omega t - \frac{3}{2}\cos\omega t)|u_{\rm ref}| \\ &= \frac{3}{2}U_{\rm m}^*\cos(\omega t - 2\pi/3) = u_{\rm b}^* + 0.5u_{\rm b}^* = u_{\rm b}^* + u_0. \end{aligned} \quad (12)$$

The result derived based on the space-vector modulation concept is exactly the same as the one defined in (6). This conclusion as well as the same expression of $u_{\rm pn}$ obtained in Sector I can be generalized to the other sectors. Consequently, these two different implementations of two-phase clamped DPWM strategy are inherently equivalent.

III. Analytical Comparison of Performance Characteristics

The analytical models of the modulator performance in terms of switching losses, current distortion, and CMV in the quasi-two-stage buck-type rectifier with the studied two-phase-clamped DPWM, the conventional SVPWM and the DPWM methods summarized in [37] are discussed in this section. For the traditional SVPWM and DPWM, the dc-link voltage is considered constant, which is set as $u_{\rm pn} = \sqrt{3}U_{\rm m}$. To comprehensively evaluate the performance of the modulator, the power factor angle, φ, range $0^{\rm o} \le \varphi \le 180^{\rm o}$, and the modulation index, $M = u_{\rm o}/U_{\rm m}$, range $0 \le M \le 1.5$, are used. It is assumed: a sinusoidal ac current shape; a constant dc voltage; no voltage drop and losses across the filter inductors, i.e., $U_{\rm m}^* \approx U_{\rm m}$; and a switching frequency $f_{\rm s}$ being much larger than the grid frequency $f_{\rm g}$, i.e., $f_{\rm s} \gg f_{\rm g}$.

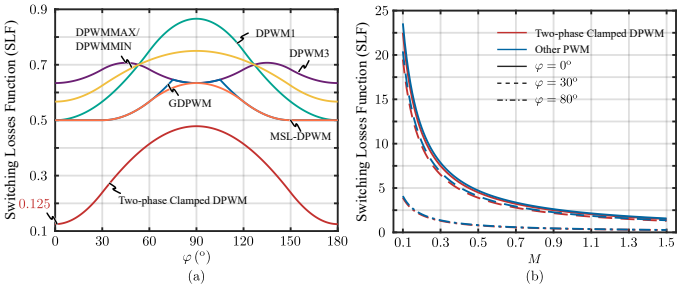

Fig. 5. Switching losses function (SLF) comparison for (a) front-end ac-dc stage, (b) back-end dc-dc stage.

A. Switching losses function or SLF

For the theoretical calculation of the switching losses, each phase current ($i_{\rm a}$, $i_{\rm b}$, $i_{\rm c}$ and $i_{\rm d}$) can be expressed as:

$$\begin{cases} i_{\rm a} &= I_{\rm m}\cos(\omega t - \varphi) \\ i_{\rm b} &= I_{\rm m}\cos(\omega t - 2\pi/3 - \varphi) \\ i_{\rm c} &= I_{\rm m}\cos(\omega t + 2\pi/3 - \varphi) \\ i_{\rm d} &= \dfrac{3U_{\rm m}I_{\rm m}}{2u_{\rm o}}\cos\varphi = \dfrac{3I_{\rm m}}{2M}\cos\varphi \end{cases} \quad (13)$$

After that, the average switching power loss for the device in phase x ($x \in \{a, b, c\}$) over a fundamental period can be defined as:

$$P_{{\rm sw\_}x} = \frac{1}{2\pi U_{\rm b}} f_s E_{\rm on,off,rr} \int_0^{2\pi} u_{\rm pn}(\omega t) I_x(\omega t)\,{\rm d}\omega t \quad (14)$$

where $E_{\rm on,off,rr}$ represents a lumped switching losses per commutation for a specified dc voltage and output current; $U_{\rm b}$ is the data-sheet reference voltage; f_s represents the constant switching frequency of the devices; $I_x(\omega t)$ equals zero in the intervals where no switching occurs and equals to the absolute value of the corresponding phase current $|i_x(\omega t)|$ otherwise. Normalizing the total switching losses $P_{\rm sw}$ to P_0, the switching loss function (SLF) of different modulators for the quasi-two-stage buck-type rectifier studied in this paper can be found as:

$$P_0 = \frac{2\sqrt{3}U_{\rm m}I_{\rm m}}{\pi U_{\rm b}} f_s E_{\rm on,off,rr} \quad (15)$$

$$\text{SLF}_{\rm ac} = \frac{P_{\rm sw_{a/b/c}}}{P_0} \quad (16)$$

$$\text{SLF}_{\rm dc} = \frac{P_{\rm sw_d}}{P_0} \quad (17)$$

Applying (14) to (17), the SLF for the two-phase-clamped DPWM in the front-end ac-dc stage can be obtained as in (18). The SLF for continuous PWM methods is 1, and that for other PWM methods in the front-end with a constant dc-link voltage can be found in [29]–[32]. The SLF for the two-phase-

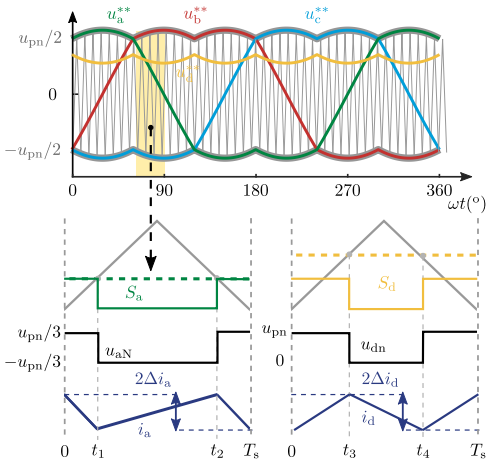

Fig. 6. Illustration of the switching sequence and current ripple of $i_{\rm a}$ and $i_{\rm d}$.

clamped DPWM and other PWM methods with a constant dc-link voltage in the back-end can be derived as in (19).

$$\mathrm{SLF_{ac}} = \begin{cases} \dfrac{\cos\varphi}{8} + \dfrac{\varphi\sin\varphi}{2} & 0 \le \varphi < \frac{\pi}{6} \\ \dfrac{(2\pi+3\sqrt{3})\sin\varphi}{24} & \frac{\pi}{6} \le \varphi < \frac{5\pi}{6} \\ -\dfrac{\cos\varphi}{8} + \dfrac{(\pi-\varphi)\sin\varphi}{2} & \frac{5\pi}{6} \le \varphi \le \pi \end{cases} \tag{18}$$

$$\mathrm{SLF_{dc}} = \begin{cases} \dfrac{9}{4M}|\cos\varphi| & \text{Studied DPWM} \\ \dfrac{3\pi}{4M}|\cos\varphi| & \text{Other PWM} \end{cases} \tag{19}$$

The comparisons of SLF for different PWM methods in both the front- and back-end stages are shown in **Fig. 5**. The SLF in the front-end stage is dependent on the power factor angle, φ, while that in the back-end stage varies with the modulation index, M. As seen in **Fig. 5**(a), the application of two-phase-clamped DPWM in the front-end stage can remarkably reduce the switching losses, i.e., it is able to reduce 75% of the losses found in the MSL-DPWM in [30] at unity power factor, which yields to the best switching loss reduction in any known DPWM strategies. Since the grid voltage and dc-link voltage is fixed, the SLF in the front-end stage is independent of M. In **Fig. 5**(b), the SLF of the two-phase-clamped DPWM is still lower than other PWM strategies with any M at the back-end dc-dc stage, because the average value of its dc-link voltage is smaller than that of the other strategies. With $|\cos(\varphi)|$ reduced, the SLF in the back-end stage is decreased accordingly. As **Fig. 5** indicates, the studied two-phase clamped DPWM method can achieve the minimum switching losses over the whole φ and M range in the quasi-two-stage system, which will lead to a simplified thermal management with low cost, improved efficiency, and higher power density of the converter.

B. Current Ripple function or CRF

The winding and core losses of the filter inductor are depending on the current ripple. Therefore, the output current ripple determined by the selected modulator gives an indication about the magnetic losses. To demonstrate the performance of

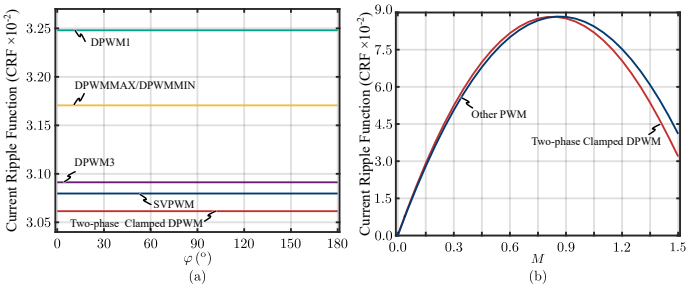

Fig. 7. Current ripple function (SLF) comparison at varied M for (a) front-end ac-dc stage, (b) back-end dc-dc stage.

the current ripple, the mathematical formulation can be derived from the terminal pulse voltage and current waveforms shown in Fig. 6, where the phase a is selected to represent the current performance in the front-end stage. The time intervals t_1 - t_4 can be obtained from the PWM period T_s and the modulation waveforms $u_{\rm a}^{**}$ and $u_{\rm d}^{**}$. For example, t_1 and t_3 in Fig. 6 are:

$$t_1 = \frac{2u_{\rm a}^{**}/u_{\rm pn}+1}{4}T_s \tag{20}$$

$$t_3 = \frac{2u_{\rm d}^{**}/u_{\rm pn}+1}{4}T_s \tag{21}$$

Then, the squared RMS value of the current ripple of $i_{\rm a}$ and $i_{\rm d}$ can be expressed as:

$$\Delta I_{\rm a,rms}^2 = \frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{T_s}\int_0^{T_s}\Delta i_{\rm a}^2 {\rm d}\tau\right){\rm d}\omega t \tag{22}$$

$$\Delta I_{\rm d,rms}^2 = \frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{T_s}\int_0^{T_s}\Delta i_{\rm d}^2 {\rm d}\tau\right){\rm d}\omega t \tag{23}$$

where the deviations of $\Delta i_{\rm b}$ and $\Delta i_{\rm d}$ are:

$$\Delta i_{\rm a} = i_{\rm b} - i_{\rm b,avg} = \frac{1}{L_{\rm g}}\int (u_{\rm ga} - u_{\rm aN})\,{\rm d}t \tag{24}$$

$$\Delta i_{\rm d} = i_{\rm d} - i_{\rm d,avg} = \frac{1}{L_{\rm o}}\int (u_{\rm dn} - u_{\rm o})\,{\rm d}t \tag{25}$$

By normalizing the squared RMS value of the current ripple $\Delta I_{\rm a,rms}^2$ and $\Delta I_{\rm d,rms}^2$ to ΔI_0^2 in (26):

$$\Delta I_0^2 = \frac{T_s^2 U_{\rm dc}^2}{2\pi L^2}, \tag{26}$$

the current ripple function (CRF) for $i_{\rm a}$ and $i_{\rm d}$ can be calculated as:

$$\mathrm{CRF}_{i_{\rm a}} = \sqrt{\frac{\Delta I_{\rm a,rms}^2}{\Delta I_0^2}} \tag{27}$$

$$\mathrm{CRF}_{i_{\rm d}} = \sqrt{\frac{\Delta I_{\rm d,rms}^2}{\Delta I_0^2}} \tag{28}$$

The comparisons of CRF for different PWM methods in both front- and back-end stages are shown in **Fig. 7**. The CRF in the front-end stage is independent of φ and M, because the modulation index in the front-end stage, from $u_{\rm abc}^*$ to $u_{\rm pn}$, is fixed, while that in the back-end stage varies with modulation index, M. As seen in **Fig. 7**(a), the application of two-phase-clamped DPWM in the front-end stage has the best current ripple performance as well in any known PWM strategies. In **Fig. 7**(b), the CRF of the two-phase-clamped DPWM is still

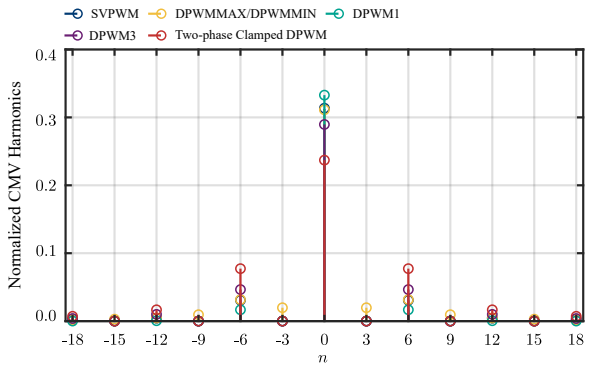

Fig. 8. Normalized CMV harmonics within the 1st carrier frequency.

TABLE I
INTEGRATION LIMITS FOR DOUBLE FOURIER INTEGRAL.

Sector	$y_s(i)$	$y_e(i)$	$x_r(i)$	$x_f(i)$
I	0	$\frac{\pi}{3}$	$-\pi$	π
II	$\frac{\pi}{3}$	$\frac{2\pi}{3}$	$\frac{-\pi(\sin\omega t+\sqrt{3}\cos\omega t)}{2\sin\omega t}$	$\frac{\pi(\sin\omega t+\sqrt{3}\cos\omega t)}{2\sin\omega t}$
III	$\frac{2\pi}{3}$	π	0	0
IV	π	$\frac{4\pi}{3}$	0	0
V	$\frac{4\pi}{3}$	$\frac{5\pi}{3}$	$\frac{-\pi(\sin\omega t-\sqrt{3}\cos\omega t)}{2\sin\omega t}$	$\frac{\pi(\sin\omega t-\sqrt{3}\cos\omega t)}{2\sin\omega t}$
VI	$\frac{5\pi}{3}$	2π	$-\pi$	π

higher than other PWM strategies at low M, but turns to be smaller at high M.

C. Common-mode Voltage

Common-mode voltage (CMV) of the quasi-two-stage system is generally defined as the potential difference from the grid star point to the negative terminal of the output voltage ($u_{\rm Nn}$ in **Fig. 1**) as expressed in (29):

$$u_{\rm cmv} = u_{\rm NO} + \frac{u_{\rm pn}}{2} = \frac{u_{\rm ao}+u_{\rm bo}+u_{\rm co}}{3} + \frac{u_{\rm pn}}{2}. \quad (29)$$

As discussed in Section II-B, since there is no zero voltage vector used in the two-phase clamped DPWM, the peak value of $u_{\rm NO}$ can be reduced from $\pm u_{\rm pn}/2$ to $\pm u_{\rm pn}/6$ in every switching period $T_{\rm s}$, which yields the same effect as the reduced-CMV PWM methods studied in [17].

To further theoretically analyze the spectrum of CMV, the double Fourier integral analysis is introduced. In general terms, the harmonic component of the phase-leg output voltage $C_{\rm mn}$ under given carrier index variable m (of the carrier frequency f_c) and fundamental index variable n (of the modulating frequency f_o) is given as:

$$C_{\rm mn} = \frac{1}{2\pi^2}\sum_{i=1}^{6}\int_{y_s(i)}^{y_e(i)}\int_{x_r(i)}^{x_f(i)} u_{\rm pn}(y)e^{j(mx+ny)}{\rm d}x{\rm d}y \quad (30)$$

Assuming $u_{\rm pn}$ only has dc and sixth-fundamental-frequency component, then, the high-frequency harmonic components of $u_{\rm cmv}$ can be expressed as:

$$u_{\rm cmv} = \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} C_{\rm mn}\times\cos(m\omega_c t + n\omega_o t) \quad (31)$$
$$n = 3p, p = 0, 1, 2\cdots$$

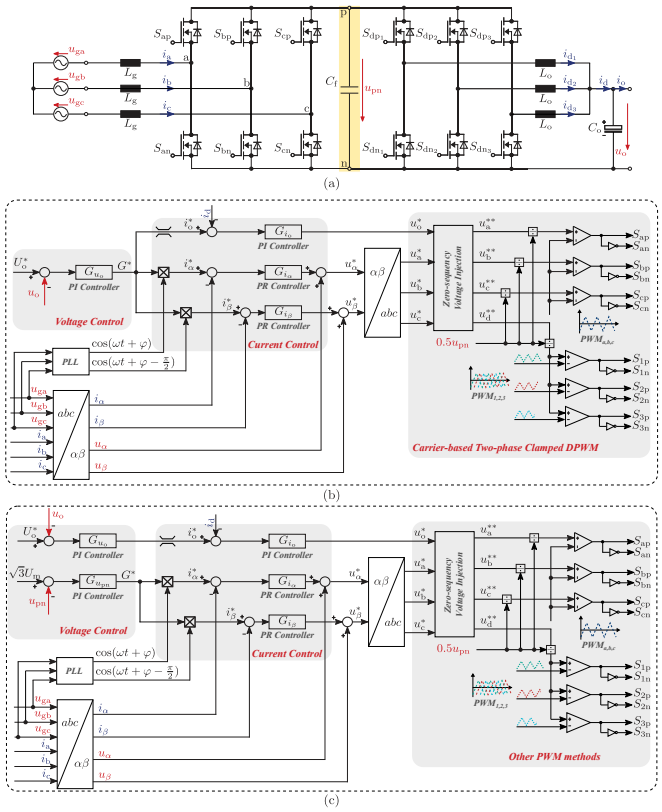

Fig. 9. Overall control block diagram of the three-phase quasi-two-stage buck-type rectifier, (a) circuit topology, (b) with two-phase clamping DPWM strategy, (c) with other PWM strategies.

TABLE II
SPECIFICATIONS OF THE EVALUATED THREE-PHASE QUASI-TWO-STAGE BUCK-TYPE RECTIFIER.

Variables	Parameters	Value
$P_{\rm o}$	Rated power	5 kW
$U_{\rm m}$	Grid voltage	311 V
ω	Grid angular frequency	$2\pi\times 50$ rad/s
$f_{\rm s}$	switching frequency	36 kHz

where $y_s(i)$, $y_e(i)$, $x_r(i)$, and $x_f(i)$ are the outer and inner double Fourier integral limits, which are listed in **Table. I**. $\omega_c = 2\pi f_c$ is the carrier angular frequency, and $\omega_o = 2\pi f_o$ is the fundamental angular frequency.

Following the aforementioned calculations, the normalized CMV harmonics (to $U_{\rm m}$) of different PWM methods within the 1st carrier frequency, i.e., $m = 1$, are shown in **Fig. 8**. Only the triple harmonic components of the fundamental exist in the CMV harmonics. It can be found that the maximum CMV harmonic of the two-phase clamped DPWM method is the lowest among the different methods. Since the resonant frequency of the common-mode circuit is close to its carrier frequency for grid-connection applications [38], the studied two-phase clamped DPWM will bring about a lower ground leakage current in practice as well.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To validate the effectiveness of the studied carrier-based two-phase-clamped DPWM strategy, simulations and exper-

TABLE III
VALUE OF FILTER INDUCTORS AND CAPACITORS FOR THE THREE-PHASE QUASI-TWO-STAGE BUCK-TYPE RECTIFIER.

Variables	Parameters	Value
$L_{\rm g}$	Grid inductor	720 μH
$L_{\rm o}$	Output inductor	450 μH
$C_{\rm o}$	Output capacitor	280 μF
$C_{\rm f}$	DC-link capacitor (with studied PWM)	5 μF
$C_{\rm f}$	DC-link capacitor (with other PWM)	360 μF

imental tests are conducted and compared with different PWM methods on the three-phase quasi-two-stage buck-type rectifier. Firstly, a PLECS based simulation is carried out. Thereafter, the studied DPWM method is operated on a digital-control hardware platform with the DSP from Texas Instruments, TMS320F28379D. In both simulation and experiment, SiC MOSFETs from CREE C3M0120090J [39] are used. The main specifications for the three-phase quasi-two-stage buck-type rectifier are listed in **Table. II**.

The studied topology circuit of the three-phase quasi-two-stage buck-type rectifier and its corresponding control blocks implemented in this section are shown in **Fig. 9**. Herein, the back-end circuit is operated as a three-channel PWM interleaved dc-dc Buck converter. This feature will enhance the loss distribution among the semiconductors or better current shared between the parallel circuits than the hard-paralleling of semiconductors, and it will cancel out the high frequency harmonics in both output voltage and current. It is noted that to keep a constant dc-link voltage for other PWM methods, a larger dc-link capacitor and an additional dc-link voltage controller are needed, as shown in **Fig. 9**(c). Since DPWMMAX and DPWMMIN methods have the same performance in switching losses, current distortion, and CMV, only DPWMMAX method is studied in this section.

A. Key Parameters Design

The current ripple flowing through $L_{\rm o}$ is defined as:

$$\Delta i_{L_{\rm o},{\rm pp}} = \frac{u_{\rm pn}-u_{\rm o}}{L_{\rm o}f_s}\frac{u_{\rm o}}{u_{\rm pn}} = \frac{u_{\rm o}}{L_{\rm o}f_s}\left(1-\frac{u_{\rm o}}{u_{\rm pn}}\right) \tag{32}$$

$$\Delta i_{L_{\rm o},{\rm pp},{\rm max}} = \frac{u_{\rm o}}{L_{\rm o}f_s}\left(1-\frac{u_{\rm o}}{u_{\rm pn,max}}\right) \tag{33}$$

$$\Delta i_{\rm o,pp,max} = \frac{\Delta i_{L_{\rm o},{\rm pp},{\rm max}}}{N}. \tag{34}$$

where N is the number of paralleled interleaved buck converters and $\Delta i_{L_{\rm o},{\rm pp},{\rm max}}$ is the maximum current ripple across $L_{\rm o}$. Therefore, the inductance value of $L_{\rm o}$ can then be selected according to:

$$L_{\rm o} \geq \frac{u_{\rm o}}{\Delta i_{L_{\rm o},{\rm pp},{\rm max}}f_s}\left(1-\frac{u_{\rm o}}{u_{\rm pn,max}}\right). \tag{35}$$

Similarly, taking the phase a as an example, the current ripple across $L_{\rm g}$ is given by:

$$\Delta i_{L_{\rm g},{\rm pp}} = \frac{u_{\rm aN}-u_{\rm ga}}{L_{\rm g}f_s} \tag{36}$$

$$\Delta i_{L_{\rm g},{\rm pp},{\rm max}} = \Delta i_{L_{\rm g},{\rm pp}}\Big|_{u_{\rm ga}=0} = \frac{u_{\rm pn,max}}{6L_{\rm g}f_s} \tag{37}$$

Accordingly, the inductance value of $L_{\rm g}$ can then be selected:

$$L_{\rm g} \geq \frac{u_{\rm pn,max}}{6\Delta i_{L_{\rm g},{\rm pp},{\rm max}}f_s}. \tag{38}$$

It is noted that herein the filter inductor designs are based on the maximum current ripple requirement [40], and the proposed expressions are similar to all studied PWM methods and the main difference is found in the reference value of $u_{\rm pn,max}$. If the harmonic distortion for grid-compliance is considered for a high-order filter at the ac side, e.g., LCL filter, the local RMS current ripple method can be calculated [41], and the impact of the PWM methods on the converter-side inductor design can be referenced to **Fig. 7**, where the two-phase clamped DPWM strategy requires the minimum filter demand.

The maximum peak-to-peak high-frequency voltage ripple across the output capacitor $C_{\rm o}$, $\Delta u_{C_{\rm o},{\rm pp},{\rm max}}$, occurs when the output current ripple is the maximum, which is determined by:

$$\Delta u_{C_{\rm o},{\rm pp},{\rm max}} = \frac{\frac{1}{2Nf_{\rm s}}\cdot\frac{1}{2}\Delta i_{\rm o,pp,max}}{2C_{\rm o}} = \frac{\Delta i_{L_{\rm o},{\rm pp},{\rm max}}}{8C_{\rm o}f_{\rm s}N^2}. \tag{39}$$

Thereafter, the output capacitor $C_{\rm o}$ can be decided:

$$C_{\rm o} \geq \frac{\Delta i_{L_{\rm o},{\rm pp},{\rm max}}}{8f_{\rm s}N^2\Delta u_{C_{\rm o},{\rm pp},{\rm max}}}. \tag{40}$$

The worst peak-to-peak voltage ripple across the dc-link capacitor $C_{\rm f}$, $\Delta u_{C_{\rm f},{\rm pp},{\rm max}}$, occurs when assuming that there is no current passing though the back-end stage:

$$\Delta u_{C_{\rm f},{\rm pp}} = \frac{P_{\rm o}}{u_{\rm pn}}\frac{1}{f_{\rm s}C_{\rm f}}\left(1-\frac{u_{\rm o}}{u_{\rm pn}}\right) \tag{41}$$

$$\Delta u_{C_{\rm f},{\rm pp},{\rm max}} = \frac{P_{\rm o}}{f_{\rm s}C_{\rm f}}\left(\frac{1}{u_{\rm pn,max}}-\frac{u_{\rm o}}{u_{\rm pn,max}^2}\right). \tag{42}$$

Hence, the dc-link capacitor $C_{\rm f}$ can be obtained as:

$$C_{\rm f} \geq \frac{P_{\rm o}}{f_{\rm s}\Delta u_{C_{\rm f},{\rm pp},{\rm max}}}\left(\frac{1}{u_{\rm pn,max}}-\frac{u_{\rm o}}{u_{\rm pn,max}^2}\right). \tag{43}$$

In particular, for the two-phase clamped DPWM strategy, the resonant frequency of the $L_{\rm o}-C_{\rm f}$ filter should be 10 times higher than the frequency of the six-pulse shaped dc-link voltage, i.e., $6f_{\rm g}$, to avoid an additional resonance suppressing control [42]. Under such a condition, $C_{\rm f}$ has an upper bound:

$$\frac{1}{2\pi\sqrt{L_{\rm o}C_{\rm f}}} \geq 10\cdot 6f_{\rm g} \tag{44}$$

$$C_{\rm f} \leq \frac{1}{14400L_{\rm o}f_{\rm g}^2} \tag{45}$$

Different PWM strategies impact less on $C_{\rm o}$ because their requirements of $\Delta u_{C_{\rm o},{\rm pp},{\rm max}}$ are the same. However, two-phase clamped DPWM strategy allows a lager $\Delta u_{C_{\rm f},{\rm pp},{\rm max}}$ in the dc-link, while the other PWM strategies must have very low $\Delta u_{C_{\rm f},{\rm pp},{\rm max}}$ to keep the ac current sinusoidal. Consequently, the resulting dc link capacitance value in $C_{\rm f}$ for the two-phase clamped DPWM strategy will be much smaller.

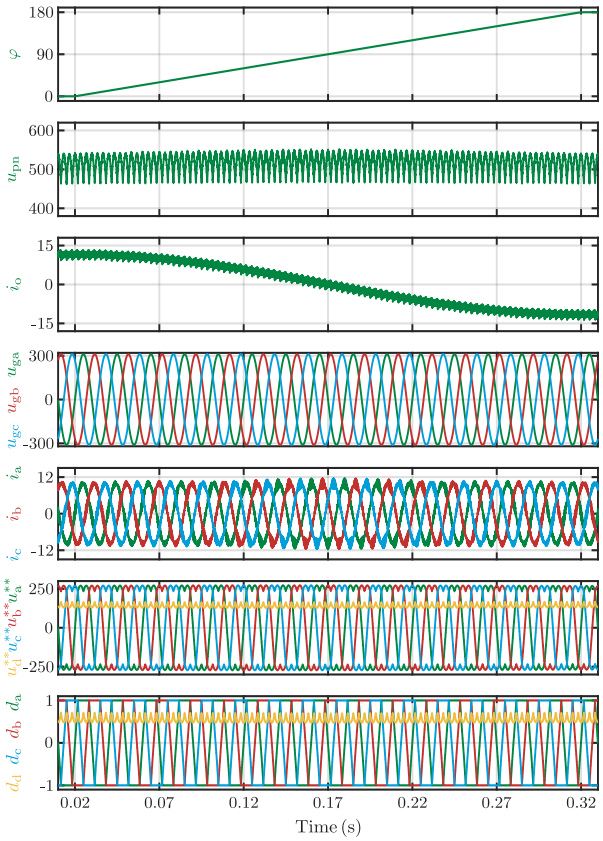

Fig. 10. Simulation waveforms of the dc-link voltage $u_{\rm pn}$, output current $i_{\rm o}$, ac voltages $u_{\rm gabc}$, ac currents $i_{\rm abc}$, modulation waveforms $u^{**}_{\rm abcd}$ and three phase duty cycles $d_{\rm abcd}$ with φ increased from $0^{\rm o}$ at $t = 0.02\,{\rm s}$ to $180^{\rm o}$ at $t = 0.32\,{\rm s}$, when using the two-phase clamped DPWM method.

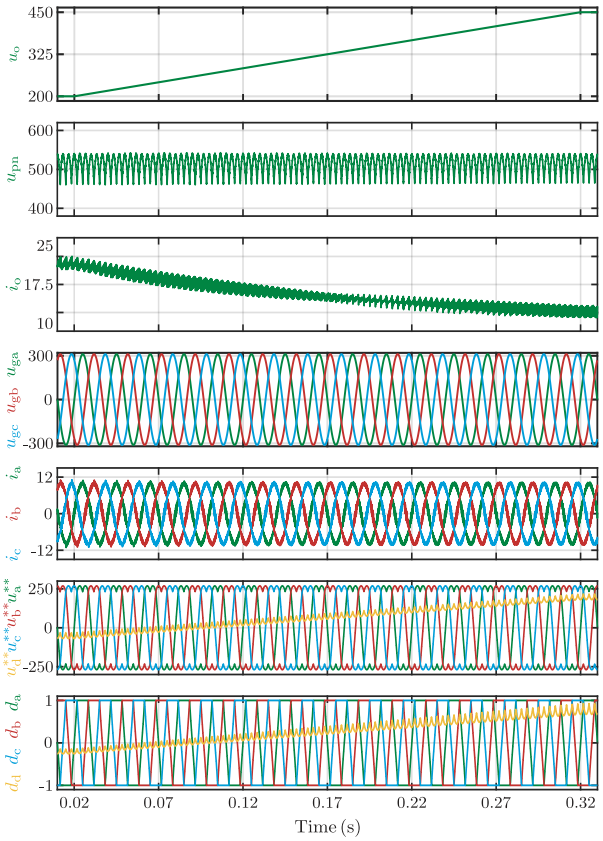

Fig. 11. Simulation waveforms of the dc-link voltage $u_{\rm pn}$, output current $i_{\rm o}$, ac voltages $u_{\rm gabc}$, ac currents $i_{\rm abc}$, modulation waveforms $u^{**}_{\rm abcd}$ and duty cycles $d_{\rm abcd}$ with the output voltage $u_{\rm o}$ increased from 200 V at $t = 0.02\,{\rm s}$ to 450 V at $t = 0.32\,{\rm s}$, when using the two-phase clamped DPWM method.

The design constraints of (35), (38), (40), (43), and (45) define a design space within the filter inductance or capacitance must be selected. In this section, setting

$$\Delta i_{L_{\rm g},{\rm pp},{\rm max}} \le 2 \cdot \frac{P_{\rm o}}{NU_{\rm o}} \tag{46}$$

$$\Delta i_{L_{\rm g},{\rm pp},{\rm max}} \le 40\% \cdot \frac{2P_{\rm o}}{3U_{\rm m}} \tag{47}$$

$$\Delta u_{C_{\rm o},{\rm pp},{\rm max}} \le 5\% \cdot U_{\rm o} \tag{48}$$

$$\Delta u_{C_{\rm f},{\rm pp},{\rm max}} \le \begin{cases} 20\% \cdot U_{\rm m} & \text{Studied DPWM} \\ 0.1\% \cdot U_{\rm m} & \text{other PWM} \end{cases}, \tag{49}$$

the filter inductance and the capacitance with enough margin are given in **Table. III**. Herein, lager $C_{\rm o}$ and $C_{\rm f}$ for the other conventional PWM methods are selected to make sure that a constant output and dc-link voltage can be obtained. A simple design guideline is provided in this section that was used to assemble the prototype, and to evaluate the effectiveness of the proposed carrier-based two-phase clamped DPWM strategy, and to finally benchmark all the studied PWM methods. If the three-phase quasi-two-stage buck-type rectifier is applied for industrial applications, specific standards are required to be met which may lead to a different passive filtering design.

B. Simulation results

Fig. 10 and **Fig. 11** show the simulation waveforms of the dc-link voltage $u_{\rm pn}$, output current $i_{\rm o}$, ac voltages $u_{\rm gabc}$, three phase currents $i_{\rm abc}$, modulation waveforms $u^{**}_{\rm abcd}$ and duty cycles $d_{\rm abcd}$ with φ increased from $0^{\rm o}$ at $t = 0.02\,{\rm s}$ to $180^{\rm o}$ at $t = 0.32\,{\rm s}$, and also with output voltage $u_{\rm o}$ increased from 200 V at $t = 0.02\,{\rm s}$ to 450 V at $t = 0.32\,{\rm s}$, respectively, when using the studied two-phase clamped DPWM strategy. To keep the power constant at 5 kVA, a dc voltage source is used and the magnitude value of the grid current $I_{\rm m}$ is controlled to be 10.71 A. It is evident that the implemented carrier-based two-phase clamped DPWM can adapt well with wide range of φ and $u_{\rm o}$, according to the analytical development in (2)-(6).

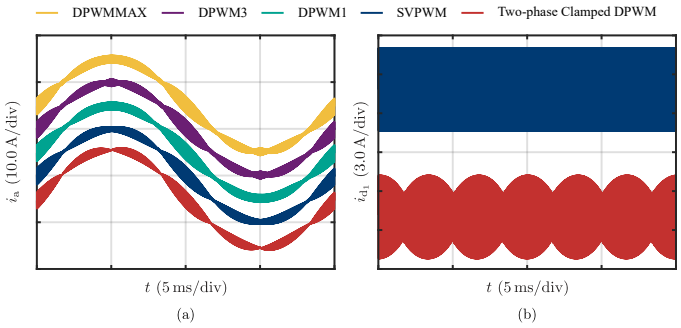

Fig. 12. Comparison of the ac and dc current in simulation among various PWM methods at $\varphi = 0^{\rm o}$, $u_o = 400\,{\rm V}$, (a) $i_{\rm a}$, (b) $i_{\rm d_1}$.

Fig. 12 compares the simulation results of $i_{\rm a}$ and $i_{\rm d_1}$ with various PWM methods at $\varphi = 0^{\rm o}$, $P = 5\,{\rm W}$. Since the back-end stage operates as a three-channel PWM interleaved dc-dc

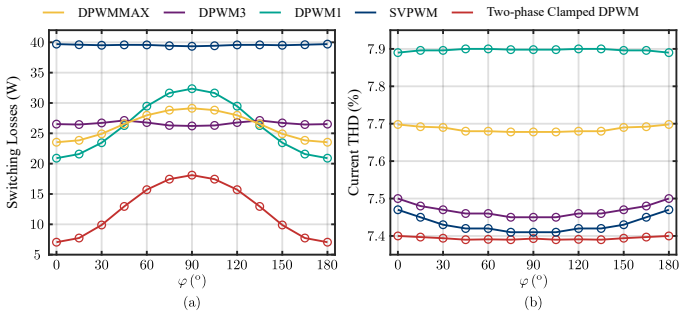

Fig. 13. Switching losses and current THD comparison at varied φ in simulation for the front-end ac-dc stage, (a) switching losses (b) current THD. Noted that due to the fact that only L filter is used at the ac side, and all harmonic components are considered in the analysis, the current THD observed in simulation is relatively high.

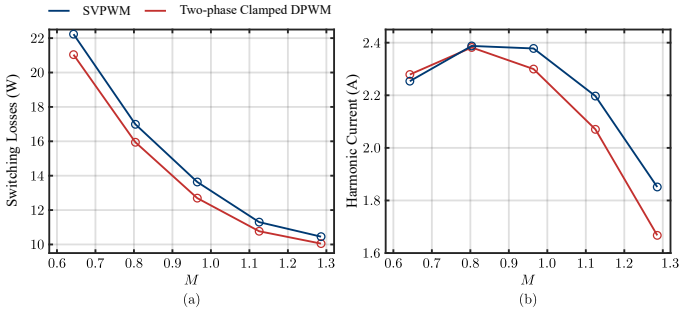

Fig. 14. Switching losses and harmonic current comparison at varied M in simulation for back-end dc-dc stage, (a) switching losses (b) harmonic current.

converter, the current ripple can not be truly reflected in the measured total output current i_{d}. Consequently, the current in a single output inductor L_{o}, i.e., $i_{\mathrm{d_1}}$ is plotted in **Fig. 12**(b) to represent i_{d}. By visual inspection, one can observe that the current ripple of i_{a} obtained with the two-phase clamped DPWM can be slightly lower than any of that obtained with other PWM methods. The current ripple of i_{d} with the studied DPWM strategy is not constant because the dc-link voltage u_{pn} is fluctuating, while the ripple with the SVPWM method is constant, which is the same in other DPWM methods.

To obtain a better insight and to validate the results of the theoretical analysis, the switching losses and the current total harmonic distortion (THD) of i_{a} in the front-end ac-dc stage for various PWM methods with different φ are compared in **Fig. 13**, while keeping $I_{\mathrm{m}} = 10.71\,\mathrm{A}$. The data-sheet value of E_{on} and E_{off} are used and built into the thermal model of the SiC MOSFET in the PLECS simulation. As expected, the switching loss performance of the studied two-phase clamped DPWM is the lowest than any other PWM methods, which can reduced nearly 87.5% switching losses compared to the SVPWM at the unity power factor. Moreover, the current THD of i_{a} does not change significantly with φ, and that of the studied two-phase clamped DPWM is the best as well, which matches the analysis in Section III-B. It is noted that due to the fact that only a L filter is used at the ac side, and all harmonic components are considered, the current THD observed in simulation is relatively high. The comparison of switching losses and harmonic current of the back-end stage for different PWM methods with different M are given in **Fig. 14**. Herein, only SVPWM is performed to represent all

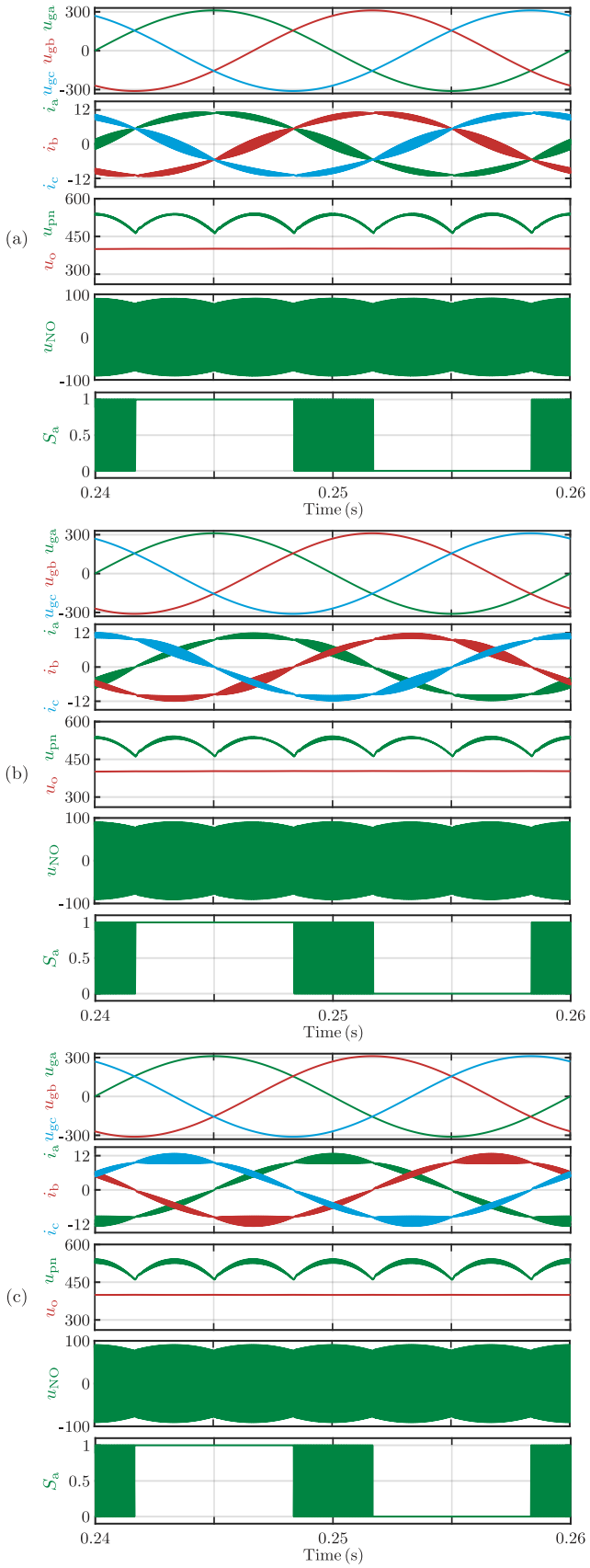

Fig. 15. Simulation results of the two-phase clamped DPWM with different operation mode, (a) $\varphi = 0^{\mathrm{o}}$ unity power factor rectifier mode, (b) $\varphi = 30^{\mathrm{o}}$ rectifier mode, (c) $\varphi = 90^{\mathrm{o}}$ STATCOM mode.

TABLE IV
COMPARISON OF CMV HARMONICS WITHIN THE 1st CARRIER FREQUENCY DETERMINED BY ANALYTICAL CALCULATIONS AND SIMULATIONS WITH THE TWO-PHASE CLAMPED DPWM.

n	Calculation	Simulation	Deviation (%)
-18	0.0071	0.0071	-0.4346
-12	0.0167	0.0166	-0.3393
-6	0.0772	0.0768	-0.5331
0	0.2371	0.2371	0.0060
6	0.0772	0.0776	0.4903
12	0.0167	0.0167	0.4859
18	0.0071	0.0071	0.1573

the PWM methods with constant dc-link voltage, and the harmonic current $I_{\rm h}$ is defined as [35]:

$$I_{\rm h} = \sqrt{I_{\rm rms}^2 - I_{\rm avg}^2} \tag{50}$$

where $I_{\rm avg}$ and $I_{\rm rms}$ are the average and rms value of $i_{\rm d}$. It can be found that the simulation results match well with the theoretical model in **Fig. 5**(b) and **Fig. 7**(b). The values of the CMV harmonics within the 1st carrier frequency calculated with the theoretical modelling are compared to the results obtained with the simulation, as listed in **Table. IV**. It shows a good accuracy of the CMV modelling built in Section III-C. Therefore, the effectiveness of the SLF, CRF, and CMV models in Section III has been proved.

Fig. 15 shows the simulation results of the steady-state operation of the three-phase quasi-two-stage buck-type rectifier with the two-phase clamped DPWM strategy at $u_{\rm o} = 400\,{\rm V}$ and $I_{\rm m} = 10.71\,{\rm A}$. Three specific cases are selected in **Fig. 15**. The first one is the unity power factor rectifier mode with resistive load where $\varphi = 0^{\rm o}$; the second one is the rectifier mode as well where $\varphi = 30^{\rm o}$; the last one is the STATCOM mode where $\varphi = 90^{\rm o}$ without dc resistive load. It can be seen that in all cases, the carrier-based two-phase clamped DPWM strategy works well with different operating mode. Two-thirds of the switching signal is clamped, while sinusoidal input ac currents are obtained. The peak value of $u_{\rm NO}$ is $\pm u_{\rm pn}/6$ featuring the characteristic of suppressing CMV.

Fig. 16 shows the simulation results of the transient responses of the three-phase quasi-two-stage buck-type rectifier with the two-phase clamped DPWM when load/current reference changed from no-load to full-load at $t = 0.1\,{\rm s}$ and full-load to no-load at $t = 0.13\,{\rm s}$. In all cases, i.e., the unity power factor rectifier, STATCOM and inverter modes, the two-phase clamped DPWM method performs well during the dynamics, where the switching signal is clamped at two-thirds of fundamental period as expected. It can be seen that in **Fig. 16**, there exists a voltage overshoot or undershoot at the load transient period. Since the capacitance for the quasi-two-stage structure is much lower than that for the conventional two-stage design, the voltage increment or decrement in the dc-link capacitor will be larger, which is about 8% higher than the maximum operating value. However, such voltage overshoot or undershoot can be confined within the safe operating area of the semiconductor devices that have to block this voltage. Additionally, the variations in the dc-link during

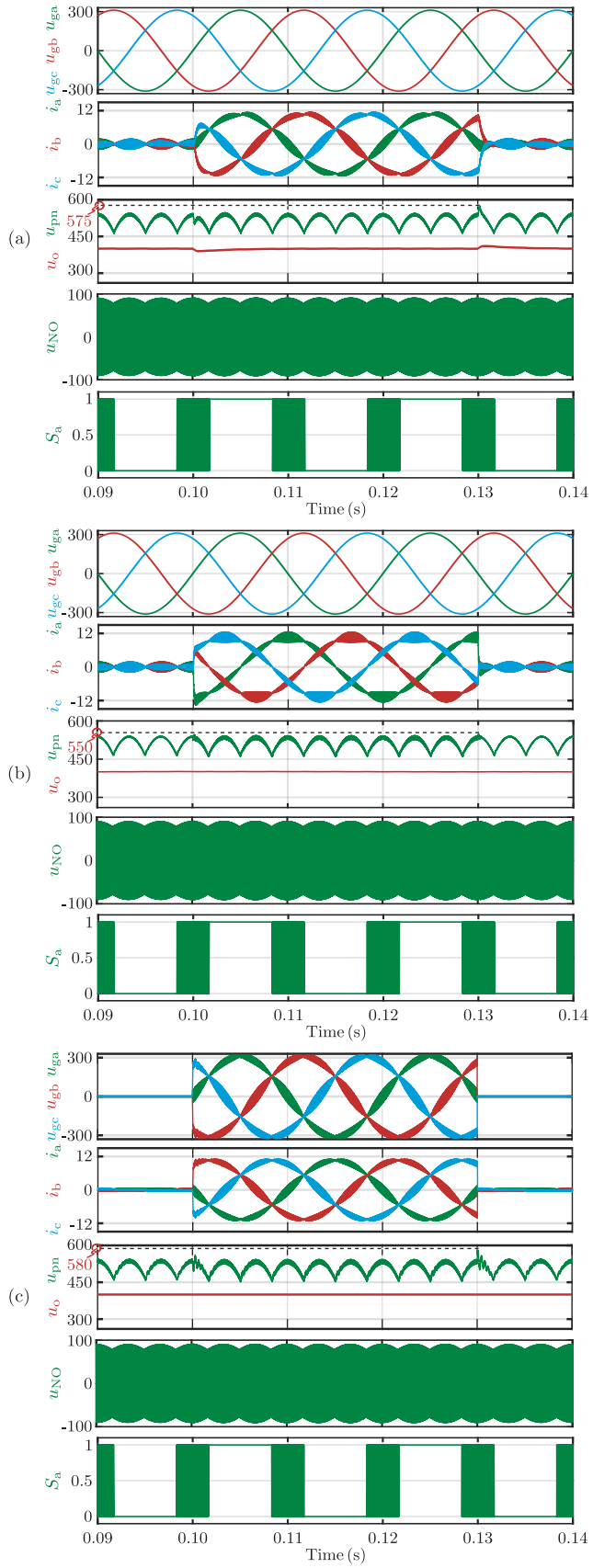

Fig. 16. Simulation results of the transient responses with the two-phase clamped DPWM when dc-side load/current reference step changed from no-load to full-load and full-load to no-load, (a) $\varphi = 0^{\rm o}$ unity power factor rectifier mode, (b) $\varphi = 90^{\rm o}$ STATCOM mode, (c) $\varphi = 180^{\rm o}$ inverter mode.

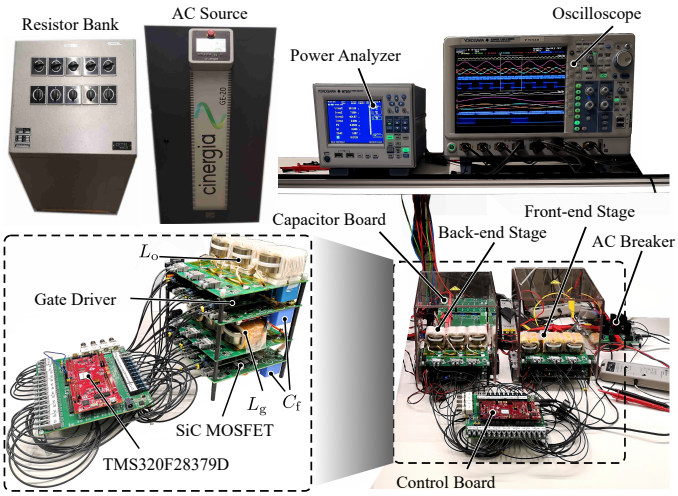

Fig. 17. Experimental setup.

transient can be relieved by slowing down the response time of the dynamic by reducing the bandwidth of the controllers.

C. Experimental results

A 5 kW prototype based on the power electronic circuit presented in **Fig. 9**(a) is built to further validate the feasibility and superiority of the proposed carrier-based two-phase clamped DPWM method. In experiments, the three-phase quasi-two-stage buck-type rectifier is operated in inverter, rectifier, and STATCOM modes working with different PWM methods. The experimental setup and the detailed photos for the constructed three-phase quasi-two-stage buck-type rectifier are shown in **Fig. 17**. The average dc voltage in all experimental cases is controlled at 400 V. All of the experimental waveforms are recorded by the oscilloscope YOKOGAYA DLM4058, and the current THD and power conversion efficiency of the converter are tested by the power analyzer YOKOGAYA WT500.

Fig. 18 shows the experimental results for the three-phase quasi-two-stage buck-type rectifier at steady state with the carrier-based zero-sequence voltage injection two-phase clamped PWM method in different operating modes. **Fig. 18**(a) and (b) are the experimental results at rectifier mode. In this case, an ac voltage source with $220\,\mathrm{V_{rms}}/50\,\mathrm{Hz}$ is used and a dc resistor bank is connected at the output port, where φ is set as 0^{o} and 30^{o} respectively. **Fig. 18**(c) is the experimental result at STATCOM mode. In this case, an ac voltage source with $220\,\mathrm{V_{rms}}/50\,\mathrm{Hz}$ is used and no load is connected to the dc-link, where φ is set to be 90^{o}. **Fig. 18**(d) is the experimental result at inverter mode. In this case, a dc source with 400 V output is used, where φ is set at 180^{o}. The experimental results demonstrate that the front-end ac currents i_{a}, i_{b}, and i_{c} can effectively follow the sinusoidal shape of the input ac voltages, while the dc-link voltage is variable, attesting the feasibility of the studied circuit and control method depicted in **Fig. 9**(b). It is clearly observed that in **Fig. 18**, at every moment, two-thirds of the cycle of S_a is clamped, either at high (positive dc-rail) or low (negative dc-rail), where no switching actions occurs. Additionally, at unity power factor rectifier mode, S_a is switched only at the lowest current magnitude which can reduce the switching losses

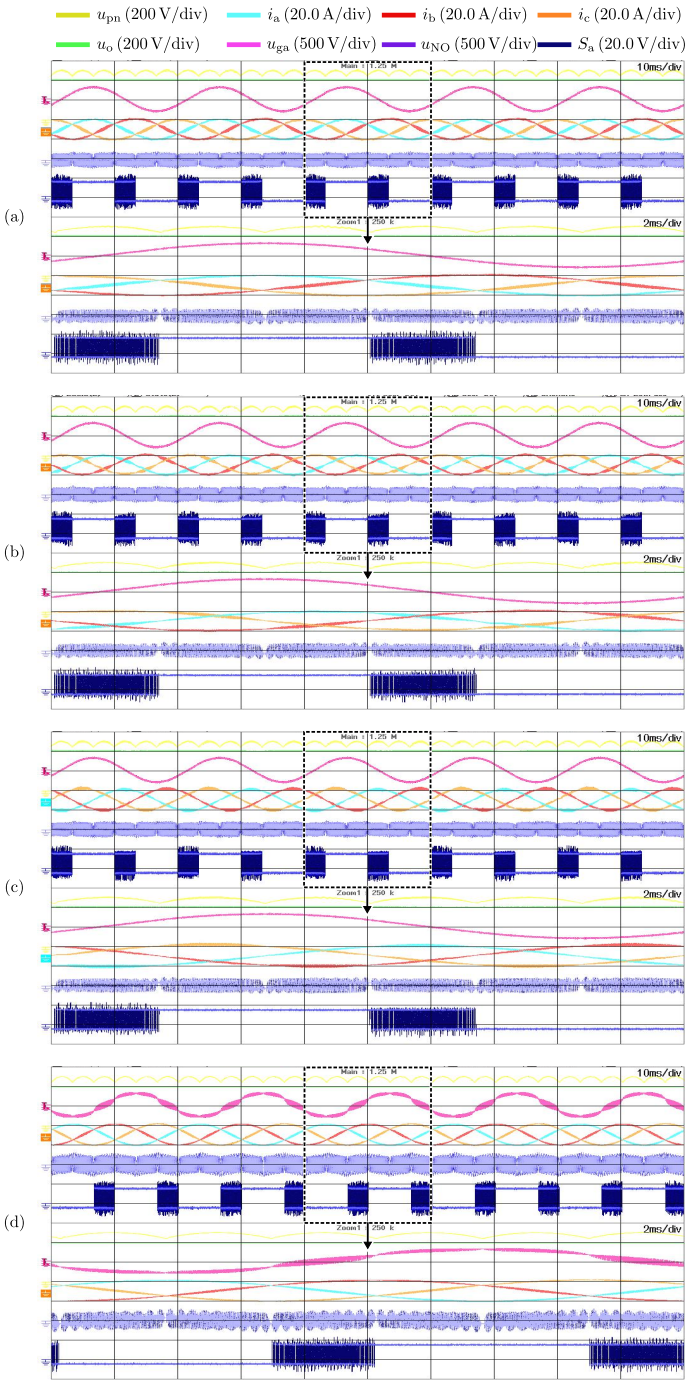

Fig. 18. Experimental results showing the steady states of the two-phase clamped DPWM at: (a) $\varphi = 0^{\mathrm{o}}$ unity power factor rectifier mode, (b) $\varphi = 30^{\mathrm{o}}$ rectifier mode, (c) $\varphi = 90^{\mathrm{o}}$ STATCOM mode, (d) $\varphi = 180^{\mathrm{o}}$ inverter mode. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

of the front-end stage considerably. All of the experimental cases show that the proposed straight-forward carrier-based two-phase clamped PWM method with zero-sequence voltage injection can adapt to the changes of the set phase angle φ and operating modes, which match well with the steady-state simulation results shown in **Fig. 15**.

Fig. 19 shows the transient-state experimental results for the three-phase quasi-two-stage buck-type rectifier with the proposed carrier-based two-phase clamped DPWM method.

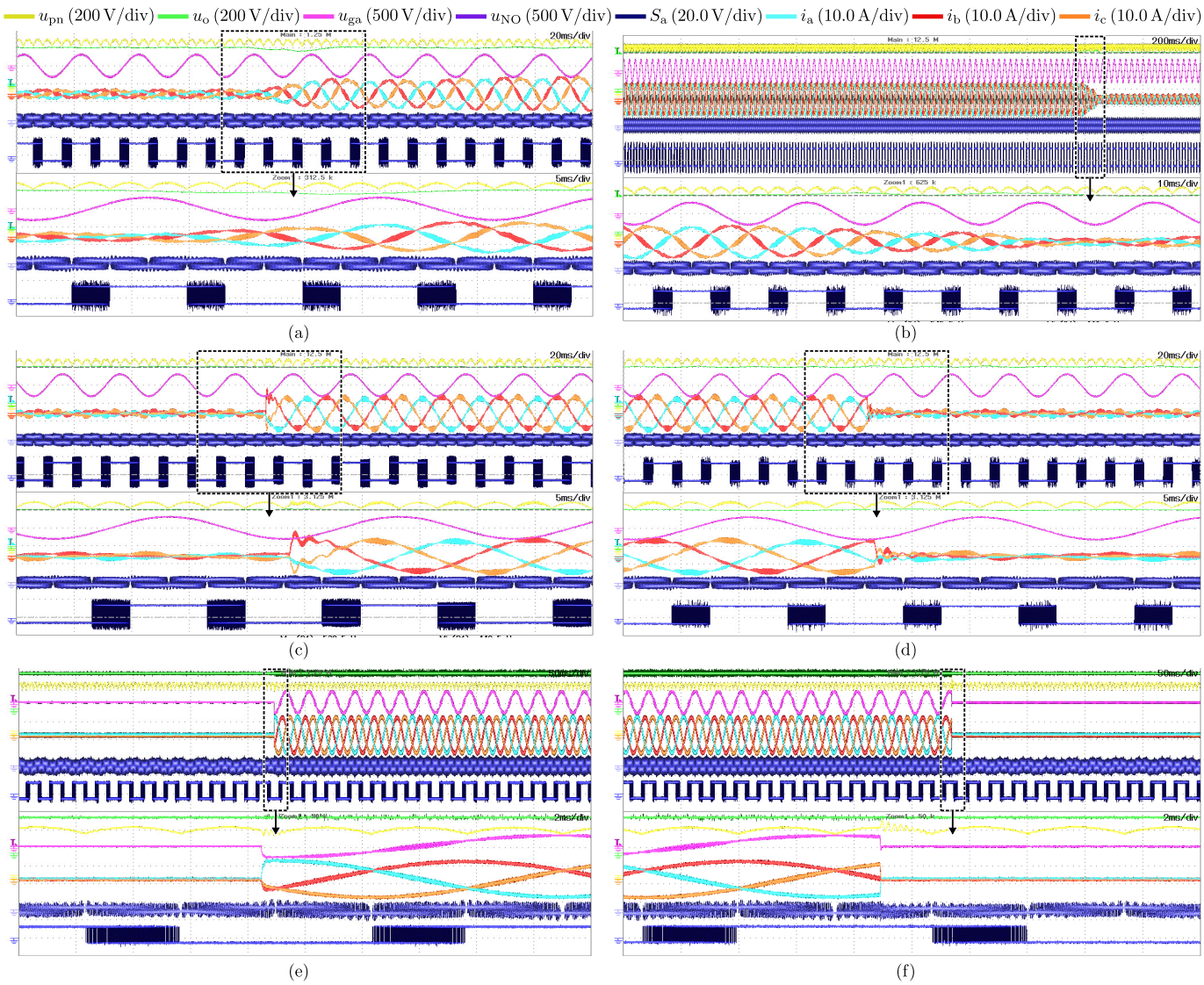

Fig. 19. Experimental results showing the transient states with two-phase clamped DPWM at: (a) $\varphi = 0^{o}$ unity power factor rectifier mode with load step changed from 30% to 80% full-load, (b) $\varphi = 0^{o}$ unity power factor rectifier mode with load step changed from 80% to 30% full-load, (c) $\varphi = 90^{o}$ STATCOM mode with current reference step change from 1 A to 9 A, (d) $\varphi = 90^{o}$ STATCOM mode with current reference step change from 9 A to 1 A, (e) $\varphi = 180^{o}$ inverter mode with load step changed from no-load to full-load, (f) $\varphi = 180^{o}$ inverter mode with load step changed from full-load to no-load. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

Fig. 19(a) and (b) are the experimental results at $\varphi = 0^{o}$ unity power factor rectifier mode with load step-up from 30% to 80% full-load and step-down from 80% to 30% full-load. It is noted that in this case, the dc-load change is achieved by switching 4 switches together on the resistor bank which is difficult to achieve a full synchronization of the value change, so that the dynamic transition time shown in experiments is not as short as that in the simulation. **Fig. 19**(c) and (d) are the experimental results at $\varphi = 90^{o}$ STATCOM mode with current reference step-up from 1 A to 9 A, and step-down from 9 A to 1 A, nearly 9%-85% full-load (reactive). **Fig. 19**(e) and (f) are the experimental results at $\varphi = 180^{o}$ inverter mode with load step-up from no-load to full-load, and step-down from full-load to no-load, which is controlled by the switching on/off the AC breaker. In all cases, the proposed carrier-based two-phase clamped DPWM method can still clamp the switching signal at two-thirds of the fundamental period, which meets the corresponding simulation results presented in **Fig. 16**. In **Fig. 19**(a) and (b), since the reaction time of the manual load-change is long, there is no noticeable inductor current overshoot/undershoot, as well as the dc capacitor voltage overshoot/undershoot at the transient instant. In **Fig. 19**(c) and (d), since the current reference is set via the communication, the current response is rapid. Additionally, the load-step change in **Fig. 19**(c) and (d) is nearly 9%-85% full-load (reactive), and thus inductor current distortion as well as the dc capacitor voltage overshoot/undershoot at the transient instant are more visible, but well within the safe operating area of the utilized semiconductor. In **Fig. 19**(e) and (f), it can be found that there is a nearly 50 V voltage overshoot in the dc-link at the load step-down transient, which matches the simulations in **Fig. 16**(c) and the overvoltage of 50 V is within

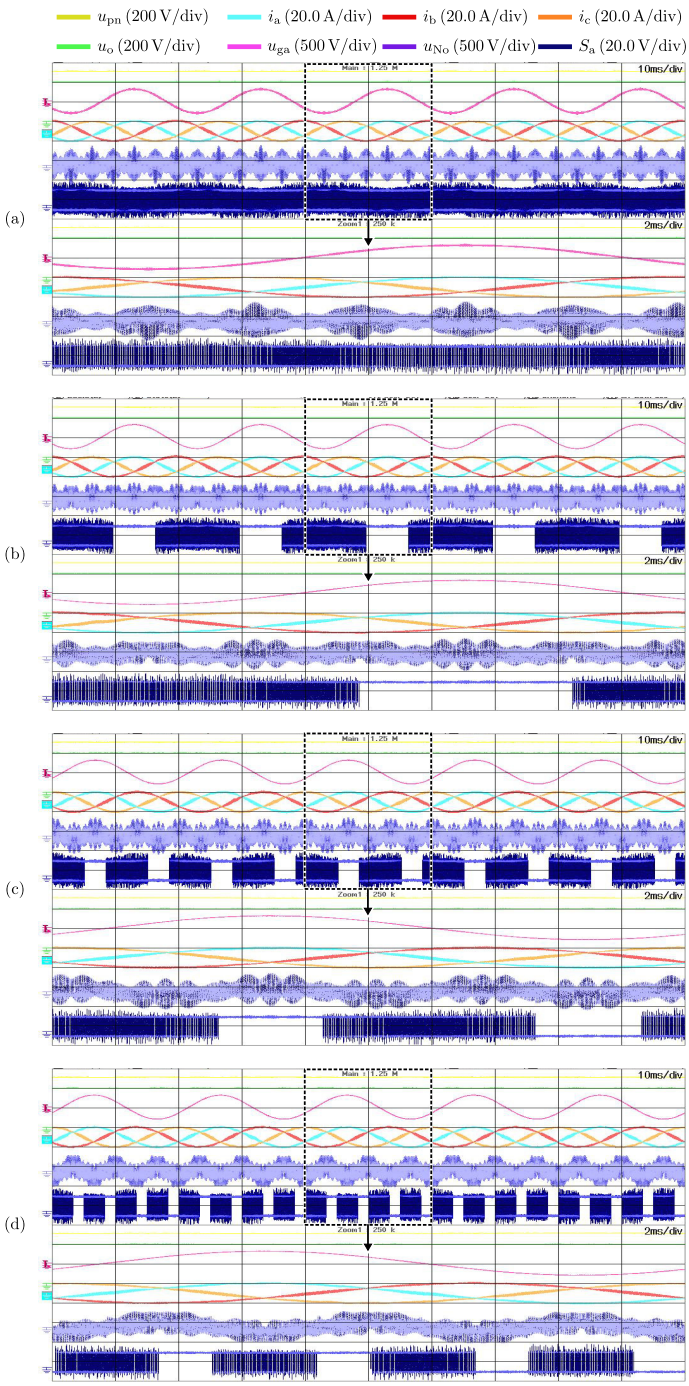

Fig. 20. Experimental results showing the steady states of other PWM methods with constant dc-link voltage in rectifier mode at $\varphi = 0^{\rm o}$: (a) with SVPWM, (b) with DPWMMAX, (c) with DPWM1, (d) with DPWM3. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

safe values because the MOSFETs used are 900V rated. Due to the lower dc-link capacitance in the dc-link, the voltage increment or decrement capacitor will be larger than that of the conventional two-stage design at the transient instant. The voltage overshoot/undershoot in the dc-link capacitor also deteriorates the performance of the current control loop and makes the inductor current distorted during transients.

Experimental results of the steady-state operation with other PWM methods following the control strategy depicted in

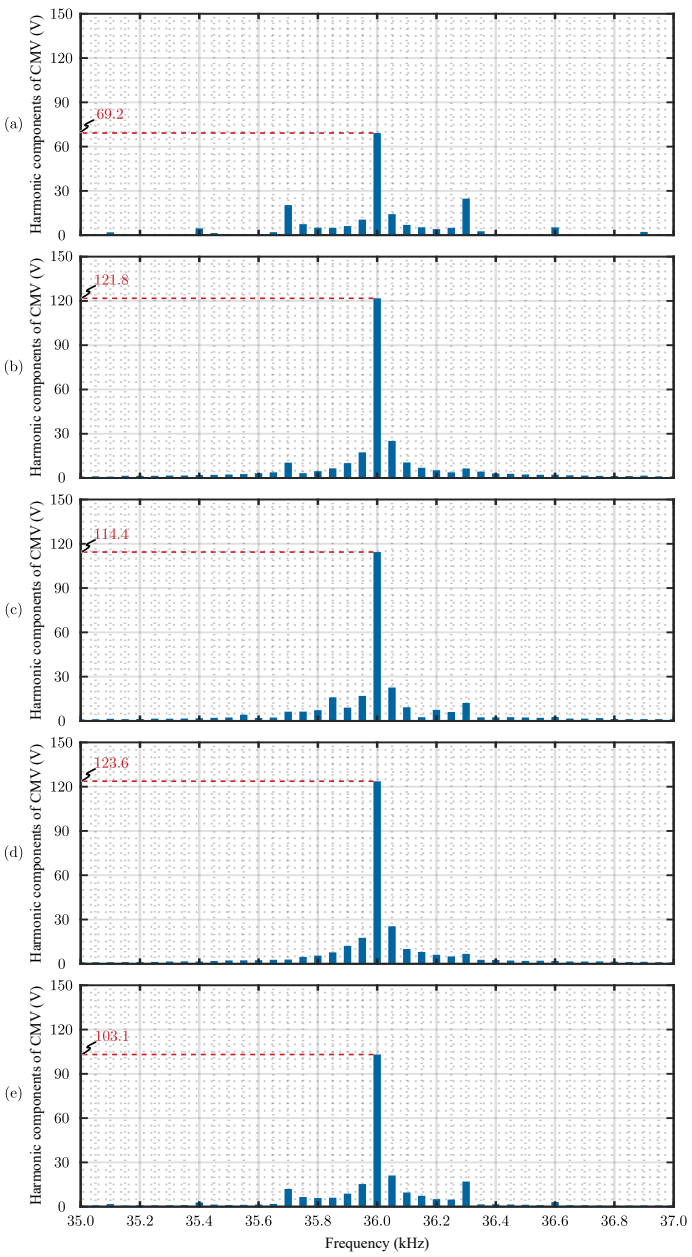

Fig. 21. Harmonic components of CMV: (a) with two-phase clamped DPWM, (b) with SVPWM, (c)with DPWMMAX, (d) with DPWM1, (e) with DPWM3.

Fig. 9(c) in rectifier mode at $\varphi = 0^{\rm o}$ are shown in **Fig. 20**. The three-phase circuit works as a true two-stage power conversion system working at $P = 5\,{\rm kW}$ with $220\,{\rm V_{rms}}/50\,{\rm Hz}$ ac source and $32\,\Omega$ dc resistive load. The output voltage can also be controlled at $400\,{\rm V}$ and the dc-link voltage is controlled constantly at $540\,{\rm V}$ with the other PWM methods, while effectively tracking the sinusoidal current reference. It can be seen that the clamped duration time of $S_{\rm a}$ for different DPWM methods in **Fig. 20** are much shorter than that for the two-phased clamped DPWM method, i.e., only one-thirds of the cycle of S_a.

The essential part of CMV, $u_{\rm NO}$ is also measured in the experiments, as seen in **Fig. 18** and **Fig. 20**. It can be found that the peak-to-peak value of $u_{\rm NO}$ with the two-phased clamped DPWM method is smaller than that of the others. To further study the CMV performance, CMV harmonic components of

TABLE V
COMPARISON OF THE MEASURED EXPERIMENTAL RESULTS.

Mode	φ	PWM	THD	ΔP	Efficiency
Rectifier	0°	SVPWM	2.62 %	115.5 W	97.56 %
		DPWMMAX	2.03 %	105.3 W	97.78 %
		DPWM1	3.40 %	104.2 W	97.79 %
		DPWM3	2.44 %	105.2 W	97.78 %
		Studied	2.55 %	**77.7 W**	**98.38 %**
	30°	SVPWM	2.33 %	108.9 W	97.22 %
		DPWMMAX	2.06 %	97.5 W	97.50 %
		DPWM1	3.41 %	99.3 W	97.46 %
		DPWM3	2.46 %	98.0 W	97.49 %
		Studied	2.52 %	**72.6 W**	**98.16 %**
STATCOM	90°	SVPWM	1.38 %	94.4 W	-
		DPWMMAX	1.71 %	83.6 W	-
		DPWM1	1.58 %	83.8 W	-
		DPWM3	1.67 %	84.2 W	-
		Studied	1.69 %	**63.2 W**	-
Inverter	180°	SVPWM	1.28 %	111.9 W	97.74 %
		DPWMMAX	1.42 %	102.1 W	97.95 %
		DPWM1	1.45 %	100.9 W	97.96 %
		DPWM3	1.34 %	102.6 W	97.94 %
		Studied	1.27 %	**69.1 W**	**98.61 %**

different PWM methods within the 1^{st} carrier frequency, are shown in **Fig. 21**. The result is calculated by the MATLAB 2020a with the data collected from the oscilloscope. The experimental results measured at inverter mode are used. As it can be seen, the maximum harmonic component of the two-phased clamped DPWM is the lowest, as predicted in the theoretical analysis.

Table. V shows the current THD, power losses, and the efficiency of the two converters stage three-phase rectifier working with SVPWM, DPWMMAX, DPWM1, DPWM3, and the studied quasi-two-stage rectifier operating with two-phase clamped DPWM for different φ. The load is changed at different φ to make the magnitude value of the grid current I_{m} constant at 10.71 A. The total power losses $\Delta P = P_{\text{in}} - P_{\text{out}}$, current THD, and the power efficiency (from $220\,\text{V}_{\text{ac}}$ to $400\,\text{V}_{\text{dc}}$) are measured by the power analyzer YOKOGAWA WT500. The difference between the real power flowing into the converter and the one flowing out of the converter can be regarded as an estimation of the total losses in the converter, including the switching devices, passive components, and PCB/cable connections. For STATCOM mode, the output active power is zero, and thus the measured input active power represents the circuit losses. As shown in **Table. V**, with the two-phase clamped DPWM, the power efficiency and power losses of the converter can be improved remarkably compared to the commonly employed PWM methods with constant dc-link voltage. The current THD of the two-phase clamped DPWM is close to that of the SVPWM. Since only the harmonics components below the 50^{th} order are considered in the power analyzer, the measured current THD results are lower than the ones obtained from the simulation results in **Fig. 13**(b). Moreover, the role of the voltage and current controllers have a much greater impact on current THD than the PWM strategy in experiments. Different PWM methods

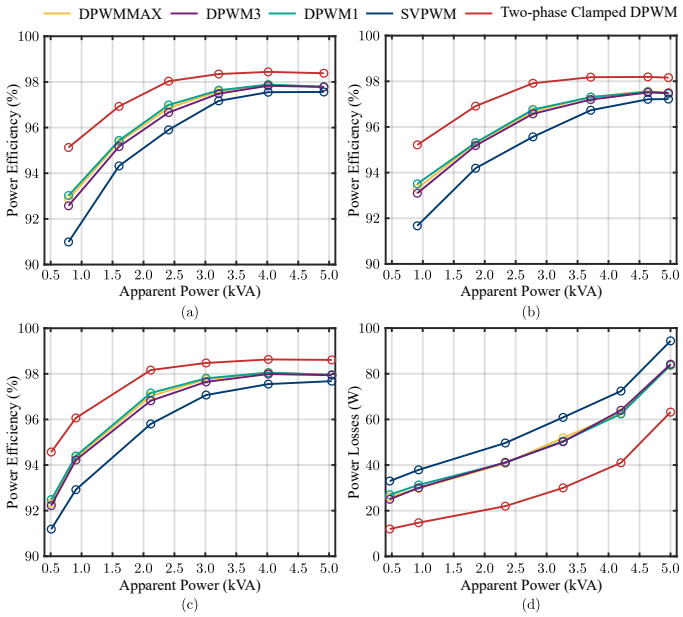

Fig. 22. Power efficiency and power losses comparison at different operating modes: (a) $\varphi = 0^{\text{o}}$ unity power factor rectifier mode, (b) $\varphi = 30^{\text{o}}$ rectifier mode, (c) $\varphi = 180^{\text{o}}$ inverter mode, (d) $\varphi = 90^{\text{o}}$ STATCOM mode.

resulting in different low frequency harmonics will influence the performance of the controllers. This effect is hard to be detected in the simulation, because the sampling delay and other non-ideal factors that influence the control bandwidth do not exist in the simulation. Therefore, the effect of the PWM method on current ripple can not be well presented in the measured current THD results.

Fig. 22 shows the power efficiency and power losses comparison among different PWM methods at different operating modes. In STATCOM mode, the measured input active power is regarded as an estimation of the total losses in the converter, as presented in **Fig. 22**(d). It can be seen that, with traditional DPWM methods, the power efficiency and losses of the converter can be improved relative to the SVPWM method, and with the two-phase clamped DPWM, the advantage can be further increased leading to the highest efficiency or the lowest power losses in the three-phase quasi-two-stage buck-type rectifier.

All in all, the presented experimental cases have shown that a remarkable reduction on power losses and common-mode voltage with the two-phase clamped DPWM method is possible in the three-phase quasi-two-stage buck-type rectifier. This confirms the superiority of this modulation method when compared to other traditional PWM strategies with constant dc-link voltage. Therefore, the validity and advantages of this DPWM strategy implemented with the proposed straight-forward carrier-based zero-sequence voltage injection method are verified.

V. CONCLUSION

This work has proposed a straight-forward carrier-based two-phase-clamped DPWM strategy with generalized zero-sequence voltage injection for the three-phase quasi-two-stage buck-type rectifiers. The modulation waveforms of the proposed DPWM strategy in the front-end stage is exactly the

same as the ones of conventional SVPWM method, but the dc-link voltage is variable which allows a low energy storage between the two cascaded converters. The principle of the two-phase-clamped DPWM strategy from both carrier-based PWM and space vector concepts have been explained in detail. The mathematical models have been built and shown that the presented strategy has the best switching losses, current distortion, and common-mode voltage performance over other suitable PWM methods within all power factor angle range. Both simulations and experimental results have been used to verify the effectiveness of the studied modulation method, and to prove the correctness of the presented theoretical analysis. It is found that in the experiments, the highest power efficiency or the lowest power losses can be obtained by the studied PWM method in comparison with other modulation methods, and the performance of common-mode voltage can also be improved.

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