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Temperature dependent trap characterisation and modelling of silicon carbide MOS capacitor

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Abstract

Due to the deficient passivation of the interface between silicon carbide and silicon dioxide, the defect-induced capture and release of trapped charges triggered by external Bias Temperature Stress (BTS) leads to parameter shifts and degraded device performance. This study models the trap-induced transient current in silicon carbide metal-oxide-semiconductor capacitors, providing insight into how capacitance and conductance change during C-V measurements under conditions of high temperature, varied frequency, and varied applied voltage.

1. Introduction

The utilisation of wide bandgap semiconductors has significantly propelled the advancement of power electronics. Among these, silicon carbide (SiC) stands out as a prominent material, due to its remarkable physical properties such as high operating temperatures and thermal conductivity [1]. The enhanced physical properties enable a diverse range of potential applications: (1) high-temperature scenarios, such as energy conversion and embedded generators [2]–[4] and (2) high power density applications: aircraft applications, uninterrupted power supply system and power converter [5]–[7]. However, reliability issues have emerged as a crucial concern, posing limitations on its commercialisation. One critical concern originates from the insufficient passivation of carbon-related defects, resulting in a high density of traps near the SiO_2/SiC interface [8]. These near-interface traps, positioned close to the interface where they readily interact with external energy sources, are considered the primary source of reliability problems for SiC devices, such as parameter shifting as active traps undergo charging and discharging processes.

The capture and release of trapped charges induced by external Bias Temperature Stress (BTS) contribute to Bias Temperature Instability (BTI). Effectively using SiC in integrated circuits and power devices necessitates the need to understand the SiO_2/SiC interface. However, the mechanisms governing the transport of trapped charges and the associated parameter shifts at elevated temperatures in SiC devices remain unclear. While studies have reported on parameter drift and characterisations under high-temperature conditions [9]–[11], the specifics of charge transport and the capture/release processes of defects remain ambiguous.

In this work, the charge transportation under high-temperature C-V measurements is analysed. Afterwards, the characterisation and evaluation of the defects are performed to evaluate the quality of the gate oxide layer. In addition, the time constant of trapped charges and their temperature response are investigated.

2. Trap induced conduction

A. Device under tests and experimental setup

The devices under test (DUTs) utilised in this study are silicon carbide metal-oxide-semiconductor capacitors (SiC MOSCAPs), fabricated on 350 μm thick 4-inch 4H-SiC wafers. These wafers feature a 9 μm nitrogen-processed epitaxial layer with a concentration of $5 \times 10^{14}\,\mathrm{cm}^{-3}$. Doping is carried out via ion implantation, involving nitrogen (N^+) doping with a concentration of $5 \times 10^{15}\,\mathrm{cm}^{-3}$ and aluminium (Al^+) doping with a concentration of $10^{16}\,\mathrm{cm}^{-3}$. The activation of these dopants is achieved through annealing at 1700 °C for 30 minutes in an argon atmosphere. Furthermore, a 50 nm thick gate oxide layer is grown, followed by a 60-minute nitric oxide annealing at 1300 °C aimed at reducing the interfacial trap density. Subsequently, circular poly-silicon is deposited as the gate, with NiAl and TiAl applied for n-type and p-type contacts, respectively. Fig. 1 illustrates the cross-section of the under-test MOSCAPs.

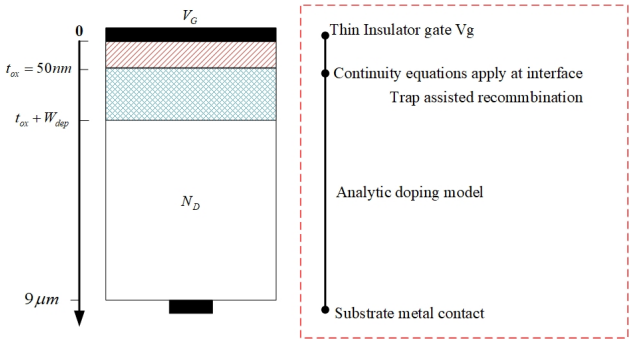

Figure 1. Left: cross-section of tested vertical MOSCAP, with gate oxide thickness, depletion region (depletion mode) and epitaxial layer illustrated. Right: the 1-D model used for calculation.

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The C-V measurements are conducted for electrical characterisation and to assess the response of trapped charges. The testing setup involves a cascade probe station combined with a Keysight 4294A impedance analyser for high-frequency tests. The input signal consists of a DC sweeping signal with a small sinusoidal AC component superimposed, allowing for adjustable signal frequencies. For quasi-static C-V measurements, a semiconductor device analyser B1500A is employed, applying a DC ramp signal with sufficient duration at each step. The V_{gs} is swept from -20 V to +20 V to make sure the device transitions sufficiently from deep depletion to accumulation.

B. Charge current relate to the interfacial traps

This section presents a comprehensive analysis of charge transportation and trap-induced transient current under C-V measurement. The model framework is built upon the following assumptions: (1) the capture and release of charges by the traps occur instantaneously, and (2) each trap is assumed to have the capacity to capture only one charge at a time.

The rate of capture $r_{n,c}$ for an electron to be captured is determined by the electron concentration at the interface n_0 and the density of empty trap states,

$$r_{n,c} = c_n n(1-f)D_{it} \tag{1}$$

where c_n denotes the capture cross-section, D_{it} stands for the trap density, and f represents the occupancy probability of a certain trap considering Fermi statistics.

$$f = [1 + \frac{g_d N_c}{N_d} exp(\frac{E-E_c}{kT})]^{-1} \tag{2}$$

where g_d denotes the electrons' ground-state degeneracy, N_c represents the available states at the conduction band edge, N_d is the ionised doping concentration, E_c signifies the conduction band edge, K represents Boltzmann constant and T is the absolute temperature.

Similarly, the emission rate $r_{n,e}$ characterises the transmission of emitted charges from occupied defect centres to the conduction band, is defined by:

$$r_{n,e} = e_n f D_{it} \tag{3}$$

Here, e_n is the emission cross-section.

The charge interaction due to capture and emission results in a detectable net electron current density i_n,

$$i_n = qD_{it}[c_n n(1-f) - e_n f] \tag{4}$$

During C-V measurement, a sinusoidal small signal is superimposed with a linear sweeping signal,

$$V_{app} = V_{lin} + \upsilon_{ac} exp(j\omega t) \tag{5}$$

This combined signal leads to a response in the electron concentration n and occupancy probability f. Each of these parameters can be decomposed into:

$$f = f_{lin} + \Delta f; \quad n = n_{lin} + \Delta n \tag{6}$$

where f_{lin} and n_{lin} are occupancy probability and electron concentration controlled by gate sweeping bias. Δf and Δn represents the variation caused by sinusoidal signal.

Considering thermal equilibrium when $V_{app} = 0$, the current $i_n = 0$, which gives the identity:

$$c_n n_{lin}(1-f_{lin}) = e_n f_{lin} \tag{7}$$

This will be applied to eliminate the emission cross-section e_n, and now the transient current density can be expressed by capture cross-section only:

$$i_n = qD_{it}c_n[\Delta n(1-f_{lin}) - n_{lin}\frac{\Delta f}{f_{lin}}] \tag{8}$$

The following will calculate the variation Δn and Δf. The electron concentration at the interface is determined by doping concentration $n = N_d$ and surface potential (band bending at surface) φ_s: $n = N_d \exp(q\varphi_s/kT)$. The variation Δn is due to the surface potential variation under the AC signal, which can be expressed as,

$$\Delta n = \frac{q}{kT}\Delta\varphi_s n \tag{9}$$

where $\Delta\varphi_s$ represents variation of surface potential.

The Fermi statistic defined occupancy probability f is also influenced by the sinusoidal signal, $\Delta f = f_x \exp(j\omega t)$. The Δf is time dependent,

$$\frac{\Delta f}{\Delta t} = j\omega\Delta f \tag{10}$$

This equation directly links the time-varied term Δf and i_n. Since the transient current originates from the dynamic occupancy of the traps, it is reasonable to rewrite the transient current i_n in equation (8) in terms of the variation in time, we obtain:

$$i_n = qD_{it}\frac{\Delta f}{\Delta t} \tag{11}$$

Equation (8) describes the microscopic behaviour for single electron, whereas equation (11) operates at macro level. The variation Δf can be determined by solving,

$$j\omega\Delta f = c_n[\Delta n_0(1-f_{lin}) - n_{lin}\frac{\Delta f}{f_{lin}}] \tag{12}$$

Substituting Δn and Δf back to equation (8) gives the final results,

$$i_n = \frac{q^2 D_{it}}{kT}(1-f_{lin})(\frac{1}{j\omega f_{lin}} + \frac{1}{c_n n_{lin}})^{-1}\Delta\varphi_s \tag{13}$$

The current is influenced by both gate bias and temperature, which jointly regulate the occupancy frequency and electron concentration.

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3. Discussion

A. Trap induced capacitance and energy loss

The transient current serves as an indicator of defects and is sensitive to the frequency and amplitude of the applied signal. To eliminate the influence of small signal amplitude, we define the trap-induced admittance $Y_n = i_n / \Delta\varphi_s$, which can be further split into conductance and capacitance part, is expressed as,

$$C_{it} = \frac{q^2 D_{it}}{kT}(1 - f_{lin})\left(\frac{1}{f_{lin}} + \frac{\omega^2 f_{lin}}{c_n^2 n_{lin}^2}\right)^{-1} \quad (14)$$

$$G_{it} = \frac{q^2 D_{it}}{kT}(1 - f_{lin})\left(\frac{1}{c_n n_{lin}} + \frac{c_n n_{lin}}{\omega^2 f_{lin}^2}\right)^{-1} \quad (15)$$

The trap-induced capacitance, reflecting the charge-holding capability of the defects under certain frequencies and temperatures, can be decomposed into an intrinsic part and a frequency-dependent part. The frequency-dependent component significantly decreases as the signal frequency increases because the trapped charges cannot keep pace with the applied signal. The intrinsic part is determined by physical properties such as the doping concentration determining the occupancy frequency and the fabrication processes determining D_{it}.

The C_{it} is the additional capacitance due to the charging and discharging with respect to the applied signals. Experimental evidence of traps manifests the frequency response of the trapped charges. The MOSCAPs in Fig. 1 were tested, sweeping from -20V to +20V at room temperature. As illustrated in Fig. 2, the high-frequency curve has less capacitance than that of the quasi-static curve, particularly in deep depletion region. In this region, electron concentration is primarily governed by the doping concentration. This discrepancy arises because, in quasi-static conditions, the trapped charges have sufficient time to settle, contributing more to C_{it}. In an ideal scenario, only the intrinsic part of capacitance remains as the applied frequency approaches zero. However, under the high-frequency signal, the trapped charges are unable to track the rapid changes, resulting in the depletion capacitance.

The trap-induced capacitance C_{it} exhibits a direct proportionality to the trap density and an inverse relationship with temperature. As temperature increases, the C_{it} decreases due to enhanced electron capture. Referring to equation (1), the capture rate escalates at elevated temperatures owing to the increased electron concentration at the interface and the reduction in occupancy probability (as indicated by $\partial f / \partial T < 0$). This observation implies that the increased number of empty states at higher temperatures promotes recombination, thereby intensifying the interaction between the conduction band and defects, and consequently accelerating device degradation. The temperature dependence of capacitance in depletion is observed when measuring the high-frequency C-V from room temperature to 200°C, as illustrated in Fig. 3. As the temperature increases, the decrease in capacitance indicates the release of trapped electrons from interfacial defects. However, the observed decrease in accumulation capacitance with increased temperature is attributed to the increase in contact resistance [13]. Furthermore, it is noteworthy that the absolute value of the threshold voltage (V_{th}) has a negative temperature coefficient.

The trap-induced conductance G_{it} reflects the energy dissipation during charge transport from the defect to the SiC lattice. As depicted in Fig. 4, when a negative signal is applied, the Fermi level bends downwards, releasing trapped charges (shaded area) from defect states at the interface compared with majority charge carriers in SiC.

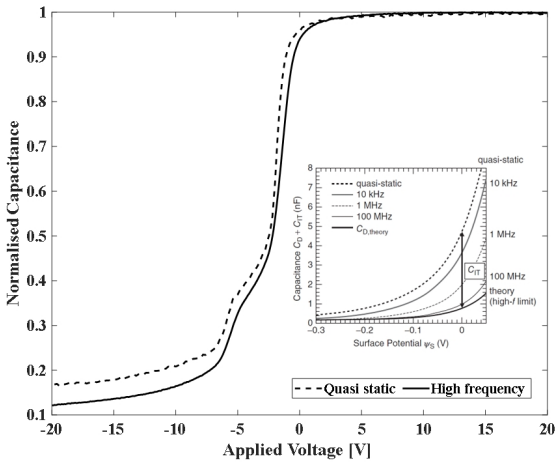

Figure 2. The measured capacitance from high frequency (1 MHz) to quasi-static at room temperature, and the "sketch out" is observed. The inset is reproduced from [12], where the $C_{D,theorey}$ represents the theoretical depletion capacitance only, when frequency approaches infinite.

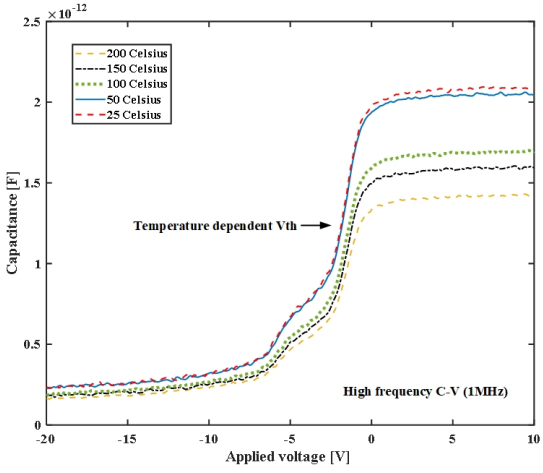

Figure 3. High-frequency C-V characteristics of n-well substrate MOSCAP from room temperature to 200°C. The "sketch out" is observable in early depletion and the diversity in deep depletion capacitance decreases. The series resistance increases at elevated temperatures, causing a decreasing accumulation capacitance.

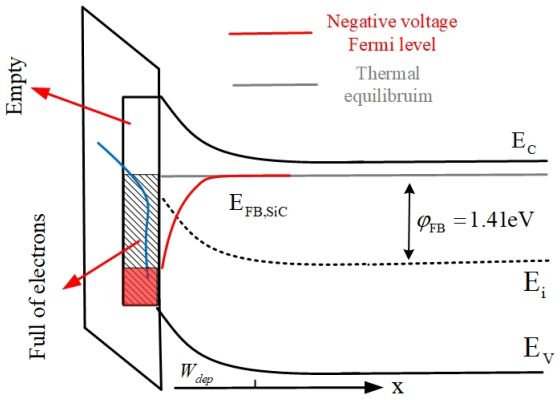

Figure 4. Band diagram of n-well substrate MOSCAP. The shaded area illustrates trap states filled with electrons, and the blue curve represents the exponentially distributed trap density.

Due to the mismatch of the time constant, the trapped charges with higher energy lag behind. With a sufficiently prolonged negative signal, these released electrons traverse from defect sites to the SiC lattice, eventually stabilising and aligning with the average electron energy in the substrate. Throughout this process, electrons decelerate and lose energy due to Coulomb collisions, thereby energy dissipation that heats the SiC lattice. However, when the frequency of the applied signal is too high, the released electrons may not have sufficient time to travel from the defects to the SiC lattice, leading to diminished energy dissipation. The frequency-dependent terms in G_{it} in equation (15) monotonically increase as ω increases, wherein higher conductance is equivalent to reduced energy losses.

B. Time constant of trapped charges

Based on the previous analysis, the time constant of the trapped charges governs the frequency response of the tested conductance and capacitance. Specifically, the trapped charges can only respond to signals with frequencies $\omega < 1/\tau_{it}$, where τ_{it} represents the interface trap time constant. The time constant is jointly determined by the occupancy probability f_{lin} and electron concentration n_{lin},

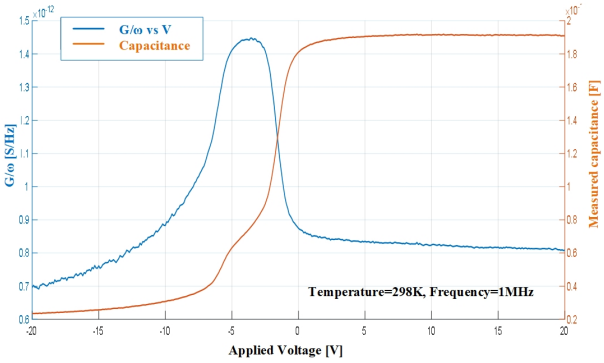

Figure 5. G_p/ω and capacitance plot as a function of applied voltage, measured at room temperature under 1MHz.

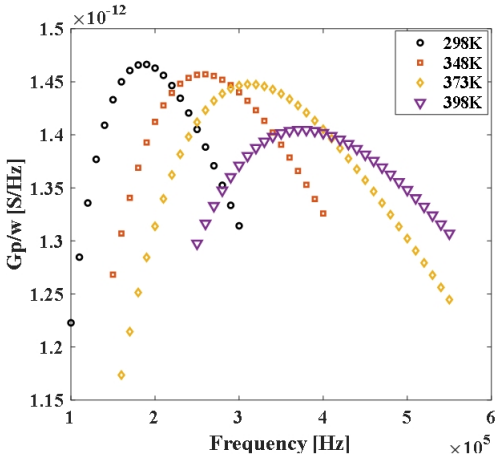

Figure 6. G_p/ω plot as a function of ω from 25 °C to 125 °C. The time constant and density of traps are available from the local maximum of the curves.

and both are controlled by gate bias:

$$\tau_{it} = \frac{f_{lin}}{c_n n_{lin}} \tag{16}$$

It characterises the average time required for a trapped charge to settle and stabilise within the SiC lattice. It is worthwhile to note that the τ_{it} remain unchanged in the deep depletion region, as the electron concentration n_{lin} is primarily determined by doping concentration at the edge of the space charge region, and the change in the occupancy probability f_{lin} is negligible small.

The time constant was characterised and extracted by measuring the G_p/ω plot under a specific frequency as a function of V_{app}, as illustrated in Fig. 5. This procedure was repeated across multiple frequencies, ranging from 100kHz to 1MHz, resulting in a G_p/ω plot as a function of ω, shown in Fig. 6. The maximum point on this plot contains crucial device information, indicating both the trap density D_{it} on the y-axis and the corresponding time constant τ_{it} at that temperature on the x-axis. By conducting these measurements at various temperatures, the variations of τ_{it} and D_{it} as functions of temperature were determined.

Fig 7 illustrates the time constant of the trapped charges as a function of temperature and applied voltages. These time constants were extracted from the G_p/ω plot at various temperatures. Changes in external temperature induce variations in the time constant, leading to diverse responses from the traps under different conditions. As temperature increases, the occupancy probability decreases exponentially, as described by equation (6). Consequently, trapped charges have a shorter time to stabilise at higher temperatures. Moreover, more trapped charges activated at higher temperatures can follow higher frequencies, leading to an increase in the number of empty trap centres. This phenomenon supports the reduced capacitance observed in Fig. 3. In addition, it is also worthwhile to find in Fig 7

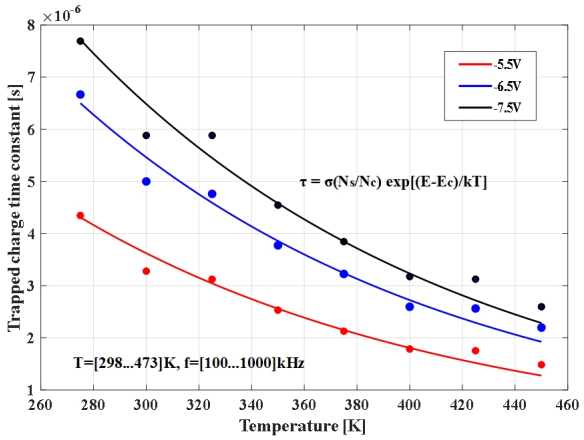

Figure 7. Time constant plot as a function of temperature and gate bias from room temperature to 200°C. Exponential fit is applied.

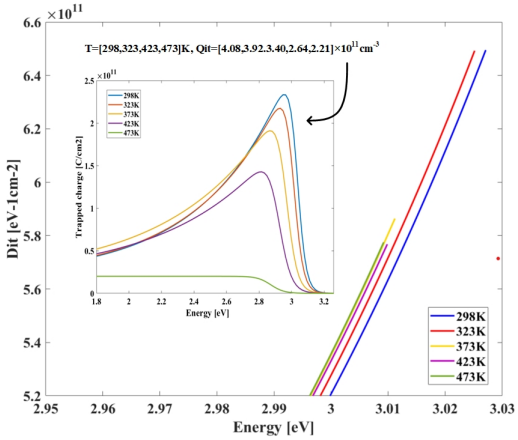

Figure 8. Temperature relation of trapped charges and trap density from 298K to 473K. The trap density is from the conductance method [15].

that at more negative gate bias, the electron density at the interface drops dramatically, resulting in an increase in the time constant. In depletion, the occupancy probability exponentially increases, whereas the electron concentration slightly increases, thus leading to an increase in τ_{it}, especially at the start of depletion. However, in deep depletion, time constant remains unchanged since the n_{lin} is sorely determined by doping concentration and occupancy probability f_{lin} also approaches to zero.

C. Trap characterisation

The temperature dependence of the trap density is illustrated in Fig. 8. Elevated temperatures alter the trap state density by modifying the separation of bonds, leading to a reduction in the density of traps near the conduction band edge [14]. These traps are more prone to interacting with electrons in the conduction band and are thus more active. The trap state density at energy level E follows an exponential form with temperature-dependent parameters D_{edge}, and temperature-independent D_{it0}, representing deep states that are less easily activated [14]:

$$D_{it}(E) = D_{it0} + D_{edge}\, exp(-\frac{E_C - E}{\sigma}) \qquad (17)$$

where E_C represents the conduction band edge and σ accounts for band tail decay energy.

The inset within Fig. 8 depicts the temperature dependence of the density of trapped charges, Q_{it}, calculated by integrating the occupancy frequency f and trap state density D_{it}. The expression for Q_{it} is given by:

$$Q_{it}(E,T) = -q\int_{E_i}^{E_C} D_{it}(E)\, f(E,T)\, dE \qquad (18)$$

where E_i is the midband energy level. From 298K to 473K, the trapped charge concentration varies from $4.08 \times 10^{11}\text{cm}^{-3}$ to $2.21 \times 10^{11}\text{cm}^{-3}$. At elevated temperatures, the concentration of trapped charges decreases significantly, particularly for charges located near the conduction band edge. This reduction occurs because the trapped charges receive sufficient energy to escape from the traps, and the interaction between the traps and the SiC lattice is intensified.

4. Conclusions

This study aims to provide a comprehensive understanding of trap characterisation and trap-induced parameter variations under high temperatures. The circular MOSCAPs were measured and characterised, with the experimental results supporting the derived conclusions. Specifically, the findings indicate that the trap-induced capacitance, representing the electron-holding ability for a trap, decreases with increasing temperature and signal frequency. However, this phenomenon is reduced in deep depletion, as the electric field suppresses the capture and release of trapped charges.

Moreover, trap-induced conductance characterises the energy dissipation during the charge transportation from defect centres to the SiC lattice. Elevated temperature reduces the conductance due to increased lattice vibrations and enhanced scattering. Additionally, at increased frequency, the traps travel a shorter path, leading to reduced energy loss. Furthermore, the trap state density decreases at elevated temperatures due to the separation of bonds. The trapped charge concentration reduces since the enhanced capture and release of charge carriers provide sufficient energy to escape to the conduction band, leaving unoccupied trap states alone.

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