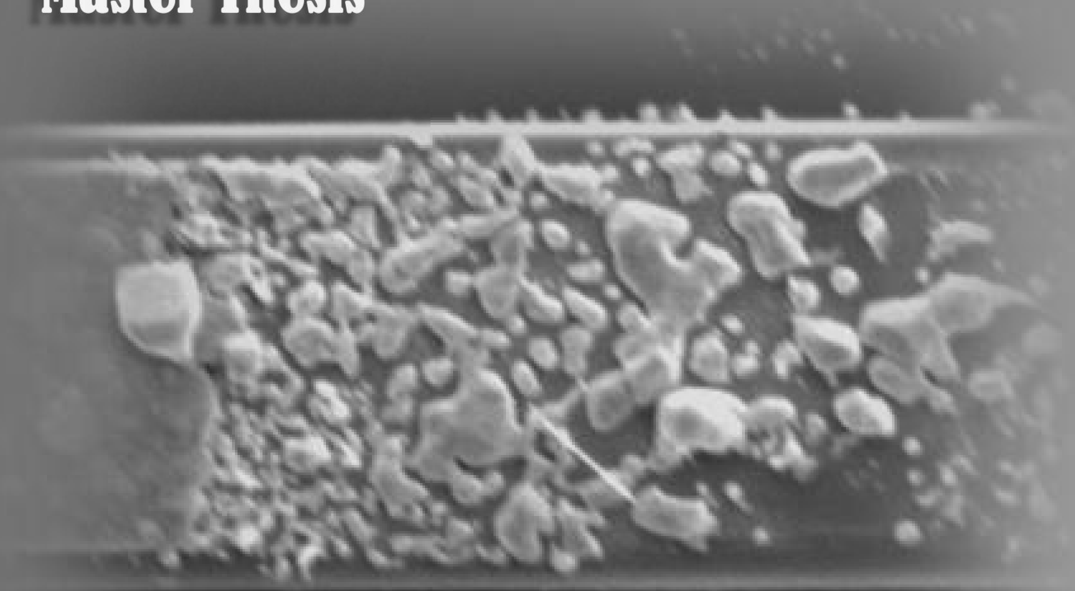
Effects of Varying Annealing Temperatures on the Microstructure and Electromigration Performance of Copper Interconnects

Yixin Yan

Master Thesis



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Effects of Varying Annealing Temperatures on the Microstructure and Electromigration Performance of Copper Interconnects

By

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Abstract

In the semiconductor industry, the ongoing demand for the miniaturization of electronic devices has significantly increased the number of components integrated into a single wafer. Consequently, the dimensions of interconnects in integrated circuits (ICs) must be minimized to connect more transistors. This trend inevitably leads to a substantial rise in current density within the interconnects, posing a major reliability challenge known as electromigration (EM). EM can result in further reliability issues, ultimately causing device failure. Extensive research has been conducted over the past decades to mitigate the impact of EM.

This study focuses on copper (Cu) interconnects, investigating the effect of annealing on their microstructure and the resulting impact on resistivity, with particular emphasis on how the microstructure influences EM. Additionally, the progress of attempting to forming Cu nanotwins via electroplating to resist EM is briefly investigated. Sputtered Cu was annealed at temperatures of 300°C, 400°C, 500°C, and 700°C, and the resulting microstructural variations were characterized by using EBSD. The findings reveal a progressive strengthening of the (111) texture in Cu film and an increase in grain size with higher annealing temperatures. Additionally, a notable decrease in grain boundary length was observed as the annealing temperature increased, correlating with reduced resistivity across the annealed samples. Moreover, the study highlights a elimination of defects and strain within the Cu films with increasing annealing temperatures.

Furthermore, EM measurements were conducted using accelerated tests under conditions of high current stress and high temperature. The variations in the microstructure of Cu films were described, and the correlation between EM mechanisms and microstructural parameters was discussed. To quantify the progress of EM, the drift velocity for each sample was calculated, revealing a trend of slower drift velocities with increasing annealing temperatures. This work provides a unique opportunity to investigate the impact of annealing on the microstructure of Cu

interconnects and to study how these changes influence EM performance. The findings contribute to a deeper understanding of EM and enhanced reliability prediction in electronic devices.

Keywords: electromigration, copper interconnects, microstructure, annealing.

1. Introduction

1.1 Electromigration

Electromigration (EM) is a phenomenon of mass transport due to the momentum transfer of electrons and metal ions that occurs in the conductor under the action of high current density. This process causes ions to gradually migrate in the direction opposite to the electric field, leading to the depletion of atoms at the cathode side to form voids, and accumulation of atoms at the anode side to form hillocks, as shown in Figure 1. The formation of voids and hillocks can ultimately result in open circuit and short circuit within electronic devices, eventually lead to failure.

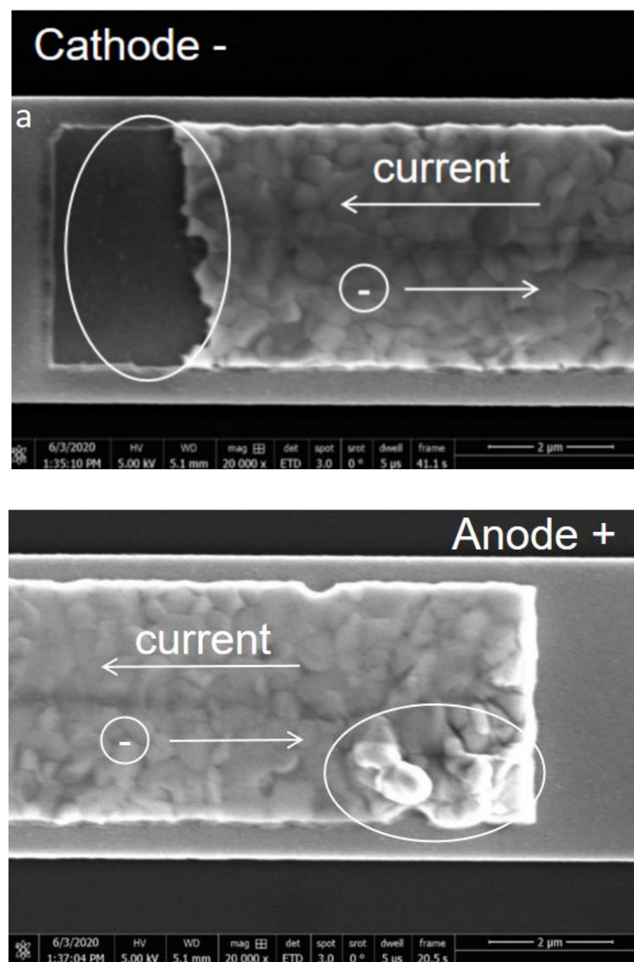


Figure 1. SEM image of formation of (a) voids and (b) hillocks in EM.

The EM phenomenon was first observed by Geradin during the study of molten alloys of lead-tin and mercury-sodium in 1861 [1]. In 1959, the first systematic study on EM was reported by Fiks [2]. Soon after, in 1961, Huntington et al. [3] proposed the concept of ‘electron wind’ force, concluding that the EM process is induced by this driving force, which is generated by the momentum transfer between conduction electrons and metal ions in the crystal lattice. Since the concept of EM was formally proposed, people were aware of the great threat of EM to the development of integrated circuits (ICs). Consequently, studies on the EM degradation of metals such as Au, Cu, Al, Ag and their alloys flourished in the late 1960s.

Nowadays, due to the demand for further device miniaturization in the semiconductor industry, the shrinkage of transistors is required in ICs. As a result, the narrowing of metal interconnects, which are crucial for connecting these transistors and other electrical elements (as illustrated in Figure 2a), is also required. Modern ICs can feature over a dozen layers of interconnects, as shown in Figure 2b, with line widths of each interconnect reaching the order of 10nm for the initial few metal layers [4]. Such small-size components result in a significant increase in current density within the interconnects. Hence, EM becomes a more serious reliability issue today due to the surge in current density in the interconnects. In order to eliminate the EM-induced issues that arise with the development of IC technology, extensive research has been conducted over the past few decades.

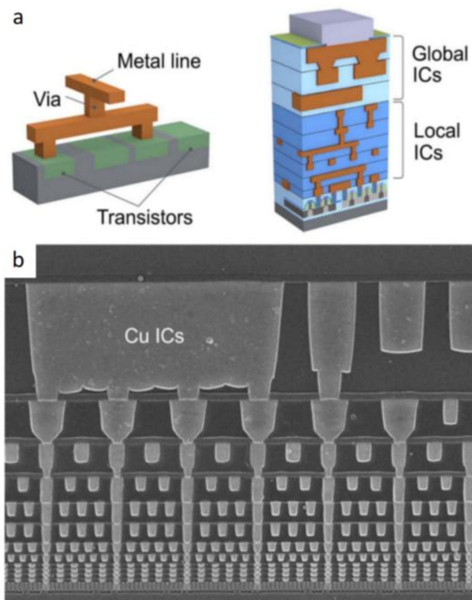


Figure 2. Schematic of (a) structure of an IC and (b) SEM section of an Intel Broadwell architecture IC with interconnects. [4]

1.2 EM in Cu interconnects

The study of EM on Cu can be traced back to the the late 1950s [5]. Nevertheless, it has been a long time remained only of academic interest with little association with reliability in ICs. Until 1990, the number of EM-related publications has increased remarkably, and research on Cu-based EM also emerged at this time [6]. During this period, however, studies on Al still accounted for the majority as shown in Figure 3.

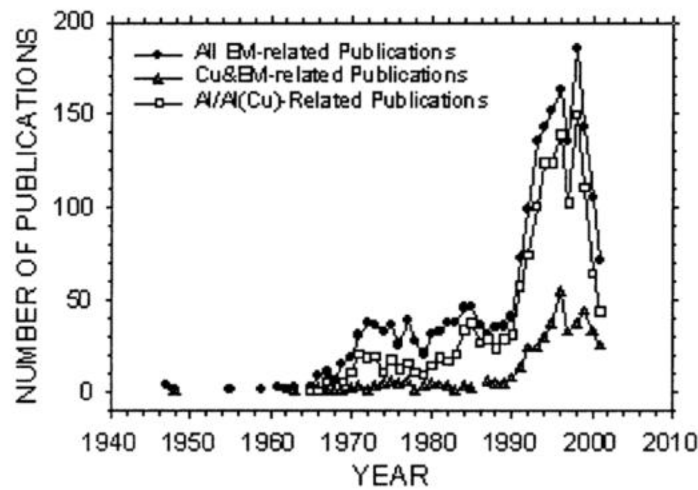


Figure 3. Evolution of EM-related or interconnect-related publications. [6]

In the late 1990s, Al-based metallization was found to no longer fulfil the needs of ultra-large-scale integration (ULSI) interconnects. Hence, research focus shifted gradually towards Cu due to its higher electrical conductivity and higher thermal stability attributed to its higher melting point compared to Al. More importantly, Cu has been reported to exhibit higher EM resistance in comparison with Al [7]. Studies have shown that the activation energy for bulk and grain boundary diffusion of Cu is much larger than that of Al, while the activation energy for interface diffusion is comparable between the two [8], as shown in Table 1. It further indicates Cu is less susceptible to mass transport than Al due to its higher activation energy for most

diffusion paths. Interestingly, it was reported that the choice of deposition technology can influence the activation energy, with chemical vapor deposition (CVD) Cu layers exhibiting smaller activation energies compared to physical vapor deposition (PVD) Cu layers [9].

Metallization	Activation energy (eV) for various diffusion paths			
	Bulk	Grain boundary	Surface	Interface (typical)
Al	1.4	0.6	NA	?
Al/Cu (alloy)	1.2	0.7	NA	0.9–1.0
Cu	2.1	1.2	0.7	0.8–1.2

Table 1. The activation energy for various diffusion paths for Al, Cu and Al/Cu alloy. [8]

Current interconnect technology is primarily driven by Cu/low dielectric constant technology, known as the dual damascene process [10]. Despite the widespread use of this process, several challenges still exist, one of which is EM. Unlike Al, Cu cannot spontaneously form a dense oxide layer with oxygen to resist diffusion and corrosion. However, this issue with Cu can be effectively suppressed by incorporating appropriate barrier layers. These interconnect barriers are deposited both before and after Cu deposition, named respectively as the underlying diffusion barrier and capping layer. They play a crucial role in enhancing the EM resistance and mean time to failure (MTTF) of the interconnect. Ta/TaN and Al2O3 are considered as effective barrier materials [11,12].

As the central focus of this work, the microstructure has a great influence on the EM performance of Cu. Factors such as grain size, grain distribution, grain boundary angle and grain orientation can significantly affect the EM performance. Experimental evidence has demonstrated that Cu with a (111) texture exhibits superior EM resistance [13]. Rapid thermal annealing (RTA) treatment has been reported to be a means to enhance texture quality [14]. At high annealing temperature, Cu with near-bamboo and even bamboo structure can be obtained when the line width/grain size ratio is small, reducing the diffusion paths and consequently enhancing EM performance [15]. Additionally, several reports have shown that Cu with a

nanotwinned structure can suppress the effects of EM [16]. Furthermore, it has been observed that voids formation primarily occurs at large grain boundary angles, further suggesting that microstructure plays an important role in localized EM in Cu interconnects [15].

1.3 Objectives and Goals

Nowadays, EM effects on Cu interconnects have aroused more attention than ever because EM has become one of the major concerns for the reliability of advanced ICs due to the demand of narrowing on-chip interconnects. Cu as one of the most commonly used interconnect materials so far, has been confirmed that its EM performance strongly depends on the microstructure. Therefore, a systematic study on microstructure of Cu plays a crucial role for its EM reliability. From a microstructural perspective, the primary research questions are:

- How does thermal annealing at different temperatures alter the Cu microstructure, and how does this alteration affect Cu resistivity?
- How does the change in Cu microstructure impact EM performance?

Additionally, the side research question is:

- Can nanotwinned Cu be produced via electrodeposition method?

In this work, a platform to conduct EM testing at the micro-level will be built and the effect of different microstructural factors of Cu such as grain size, grain orientation will be investigated. The microsturtcure of Cu interconnect will be altered by thermal annealing. In addition, the electron backscatter diffraction (EBSD) technique will be primarily carried out to characterize the change of Cu microstructure during the EM process. This work aims to provide part of the theoretical support for our group to systematically establish the multi-physics EM failure modeling on Cu, which can shed more light on the understanding of EM and reliability prediction.

1.4 Outline

In this study, the influence of different annealing temperatures on the microstructure of Cu interconnects, along with the electromigration (EM) performance corresponding to each annealing temperature, is examined. The thesis is composed of five main chapters, each with a brief introduction outlined as follows:

Chapter 2 provides a foundational understanding of EM, detailing its mechanisms and how it operates. This chapter specifically delves into the impact of microstructure, while briefly introducing other relevant contributing factors.

Chapter 3 offers a comprehensive review of experimental methods, including relevant measurement and characterization techniques utilized throughout this research.

Chapter 4 presents a comparative analysis of Cu microstructures at different annealing temperatures through integrating theoretical insights with experimental findings.

Chapter 5 focuses on the analysis of EM performance corresponding to each Cu microstructure affected by varying annealing temperatures after EM test.

Chapter 6 is a comprehensive summary of the study synthesizing the experimental results and discussion, and an outlook for future work is given in this chapter.

2. Theory

2.1 Concept of Electromigration

Electromigration (EM) is a a phenomenon in which metal atoms migrate through electron flow in a conductor under the influence of high current density. When the current flows through a conductor, individual metal ions within it experience two opposing forces: the direct force (F_{direct}) and the 'electron wind' force (F_{wind}), as illustrated in Figure 4.

The direct force, also known as the electric field force, is produced by the applied electric field in the conductor and operates in the direction opposite to the flow of electrons. On the other side, the 'electron wind' force is caused by the momentum exchange between the electrons and metal ions. This force acts in the direction of the current flow and plays a significant role in driving the EM phenomenon.

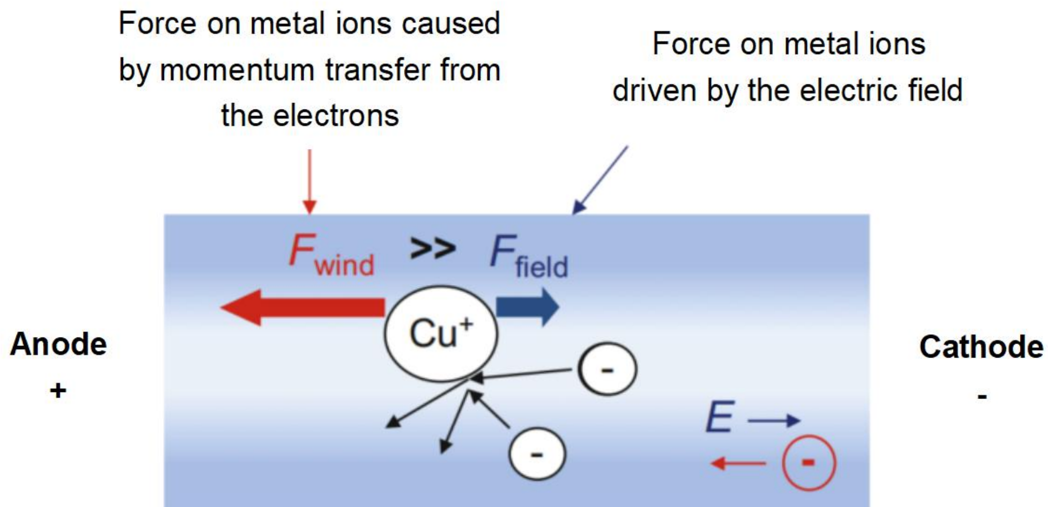


Figure 4. Schematic of two opposing microscopic forces on a metal ion [17]

Hence, the force generating EM can be expressed by the resultant of 'electron wind' force and 'direct force' [18]

$$\vec{F}_{em} = \vec{F}_{wind} + \vec{F}_{d} \quad (1)$$

where the 'electron wind' force is given by

$$\vec{F}_{wind} = -\frac{n_e e\tau}{n_d \tau_i}\vec{E} = -\frac{n_e \rho_d}{n_d \rho} e\vec{E} \quad (2)$$

It is defined by the electron density n_e, defect density n_d, and the relaxation time τ of the electrons, incorporating all scattering mechanisms. This formula is based on electron scattering by defects (or impurities) and the resulting momentum transferred to the defect. It is assumed that the electron transfers all of its momentum in a collision with a defect, so the momentum transferred per defect is equal to $-n_e eE\tau/n_d$, where e is the elementary charge and E is the applied electric field. In a transport lifetime τ_i, the momentum transferred per unit time can be calculated as formulated above, representing the 'electron wind' force. This formula can also be expressed by ρ and ρ_d, which are the total resistivity of the metal interconnect and the resistivity contribution from the defects in the metallization.

On the other hand, the direct force is given by

$$\vec{F}_d = Z_d^* |e| \vec{E} \quad (3)$$

where Z_d^* is a parameter related to the valence of the metal atom. If there is no scattering process, Z_d^* is equal to the valence number (Z) of the metal atom.

Therefore, the net EM force can be written as

$$\vec{F}_{em} = \left(Z_d^* - Z\left[\frac{\rho_d}{n_d}\right]\left[\frac{N}{\rho}\right]\right) \cdot |e| \cdot \vec{E} \quad (4)$$

where N is the atomic density equal to n_e/Z, and this formula can be simplified as

$$\vec{F}_{em} = Z^* \cdot |e| \cdot \vec{E} = Z^* \cdot |e| \cdot \rho \cdot \vec{j} \quad (5)$$

where

$$Z^* = Z_d^* - Z\left[\frac{\rho_d}{n_d}\right]\left[\frac{N}{\rho}\right] \quad (6)$$

and it is known as ‘effective charge number’ and is a parameter indicating the extent to which electrons interact with metal ions.

Hence, the EM drift velocity can be obtained by the Nernst-Einstein equation

$$\vec{v}_d = D\frac{\vec{F}_{em}}{k_B T} \quad (7)$$

where D is the atomic diffusion coefficient and is expressed by

$$D = D_0 exp\left(-\frac{E_a}{k_B T}\right) \quad (8)$$

and D_0 is the maximal diffusion coefficient at infinite temperature, E_a is the activation energy for diffusion, k_B is the Boltzmann’s constant and T is the temperature. By substituting F_{em} and D into the equation of v_d, it can be expressed as

$$\vec{v}_d = \frac{D_0}{k_B T}|e| \cdot \rho \cdot Z^* \cdot \vec{j} exp\left(-\frac{E_a}{k_B T}\right) \quad (9)$$

where j is the current density in the conductor and $E = j \cdot \rho$. As a result, the driving force for atoms (or vacancies) to diffuse in the interconnect is strongly dependent on numerous factors according to the obtained formula. The drift velocity can be obtained experimentally by measuring the area of depletion at the cathode and the time for the EM test. Once v_d is determined, the activation energy for EM can also be calculated. Equation (9) can be re-written as follows,

$$\ln\left(\frac{\vec{v}_d T}{\vec{j} exp}\right) = \ln\left(\frac{D_0}{k_B}|e| \cdot \rho \cdot Z^*\right) - \frac{E_a}{k_B T} \quad (10)$$

From Equation (10), the activation energy for EM can be determined by measuring the drift velocity at various temperatures. This approach provides a straightforward and effective means of assessing mass transport resulting from EM and is particularly suitable for the Blech test structure.

2.2 Mechanism of EM

As stated above, the primary driving force for the EM process is the 'electron wind' force. Generally, the mechanism of this mass transport phenomenon can be described by different diffusion paths. This section will also provide a brief introduction to other factors that can influence EM.

2.2.1 Diffusion Paths

The fundamental concept of this mechanism is based on the existence of various diffusion paths for vacancies and metal atoms, with the "electron wind" force serving as the only driving force for mass transport. This approach can be characterized by factors such as path type (e.g., grain boundary, surface, interface), path width, path thickness, activation energy, and more.

Combining all types of diffusion paths, the EM drift velocity can be expressed as

$$\vec{v}_d = \frac{D_{eff}(T)}{k_B T} \cdot \left(Z_{eff}^* \cdot |e| \cdot \rho \cdot j\right) \quad (11)$$

where

$$D_{eff} \cdot Z_{eff}^* = D_b Z_b^* f_b + D_d Z_d^* f_d + D_i Z_i^* f_i + D_s Z_s^* f_s + D_{gb} Z_{gb}^* f_{gb} \quad (12)$$

And D_{eff} is the effective diffusivity, Z_{eff}^* is the effective charge number, and the subscripts in this formula represent as follows

- $b \equiv bulk$
- $d \equiv defect$
- $i \equiv interface\ (if\ it\ exists\ in\ the\ particular\ interconnect)$
- $s \equiv surface\ (if\ it\ exists)$
- $gb \equiv grain\ boundary$

and f denotes the fraction of atoms diffusing through each given path. Among these paths, the ‘bulk’ are assumed negligible at the temperatures of interest (< 400 C°) in comparison with others. Hence, the grain boundary, surface and interface pathways

dominate in the EM, as shown in Figure 5.

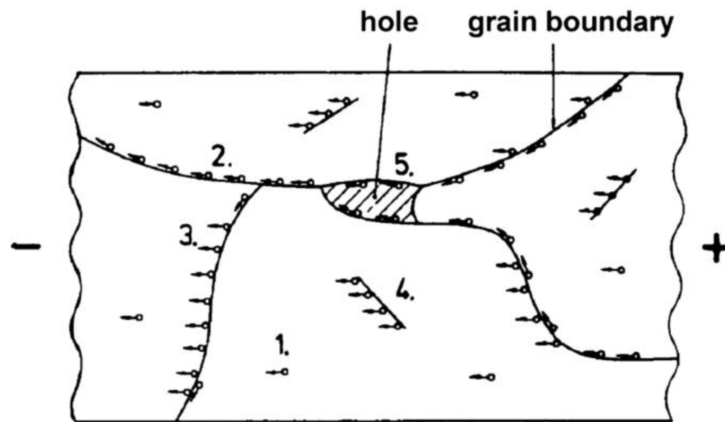


Figure 5. Diffusion paths: 1, bulk; 2, grain boundary; 3, grain/bulk; 4, defect; 5, surface. [19]

It's noteworthy that the dominant diffusion path in different interconnect materials can vary, which can be assessed by examining the activation energy values obtained from experiments. Generally, in cases where multiple diffusion paths exist within an interconnect, one of them typically dominates the EM process at a specific temperature.

2.2.2 Other Driving Forces

In addition to the 'electron wind' force, other driving forces significantly impact the electromigration (EM) characteristics. These forces, arising from various physical causes such as stress gradient, temperature gradient, and gradients of atom concentration, play crucial roles in the EM process, as shown in Figure 6.

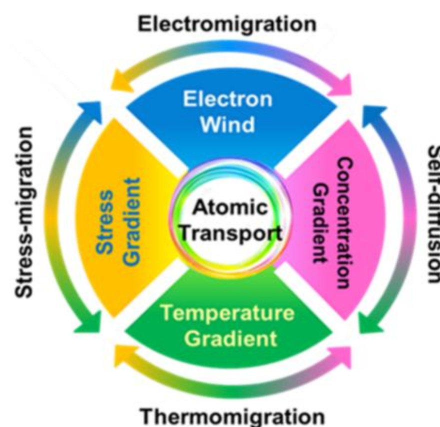


Figure 6. Interrelations among electromigration, thermo-migration, self-diffusion, and stress-induced migration. [20]

2.2.2.1 Stress gradient induced driving force (SGIDF)

It was verified that the SGIDF acts as a potential driving force during EM, which can even rival the 'electron wind' force [21]. in general, there are two sources of stress gradient in the EM process. One of these stems from the thermal mismatch between the metallization material and the surrounding material resulting in non-uniform stress distribution. The other stems from the EM-induced non-uniform stress in the interconnect, which is also known as back flow stress.

During the EM process, when SGIDF and 'electron wind' force are equal and opposite in direction, the mass transport will terminate. Since the stress gradient caused by EM is related to the interconnect length, there is a critical length below which EM does not occur. Although the hypothesis of back flow is still being questioned [22], it well interprets the Blech length effect in EM.

Besides, the SGIDF induced by thermal mismatch also plays an important role in the EM process. It was believed that void initiation is due to the thermo-mechanical stress gradient while diffusion of atoms are driven by the 'electron wind' force. Moreover, it was reported that the EM lifetime can be significantly improved by reducing the processing temperature, wh`ich is attributed to the reduction of the tensile stress gradient present in the interconnect [23].

It can be predicted that such stress-induced driving force tends to occur in regions of non-uniform distribution of temperature and complex geometry, as well as at junctions of dissimilar materials.

2.2.2.2 Temperature gradient induced driving force (TGIDF)

Atoms have a tendency to move from regions of higher temperature to regions of lower temperature, thus generating atomic flow which in turn creates driving force.

Similarly to SGIDF, it was verified that TGIDF cannot be ignored as it's also comparable to the 'electron wind' force.

There are numerous sources for temperature gradient to appear, and one of the most common is the temperature gradient caused by Joule heating. With the formation of voids during EM, there is an increase of local Joule heating thus producing a larger temperature gradient. It is also prone to have non-uniform temperature distribution at some structural connections in the interconnect. The regions that have thickness/width variation can be certainly sources of temperature gradient.

It was found that the EM failure always occurred at the region near the maximum temperature gradient [24,25]. Moreover, it was reported that with the reduction of temperature gradients, the EM lifetime was obviously longer than before [26]. Since TGIDF has a strong relation to the temperature gradient, the design and geometry of interconnect are essential for optimizing the EM performance.

2.2.2.3 Atomic concentration induced driving force (ACIDF)

Atomic concentration gradient occurs when one region has a higher concentration of particles than another. Particles have a tendency to diffuse from regions of higher concentration to regions of lower concentration, which is also known as self-diffsuion. It was reported that atomic concentration gradient migration is an important factor that has a large influence on the EM evolution induced, which can not be ignored [27]. A study shows that in the absence of mechanical stress under un-passivated condition (i.e. without barrier layer) for the metals, atomic concentration gradient can be the only balancing force against 'electron wind' force in EM development. However, when mechanical stress was present, stress migration played a dominant role in resisting EM [28]. It was also found that the atom concentration depends on the atomic concentration gradient and the stress gradient of the structure greatly [27].

2.3 Factors Affecting EM

Due to numerous sources for EM, as outlined in the previous section, there are many factors that can result in EM failure of Cu. These factors include microstructure, interface, barrier material, and temperature. While microstructure is the primary focus of this study and will be elaborated upon, the other factors will be briefly discussed.

2.3.1 Microstructure

The microstructure of the Cu interconnect has a significant influence on EM performance. As mentioned in previous section, it is concluded that the microstructure can be characterized by grain size, grain distribution, grain boundary angle and the grain orientation. There are several types of basic lattice structures in metallic interconnects, including polycrystalline, near-bamboo, bamboo, amorphous and monocrystalline structures as shown in Figure 7. They all have very different microstructure characteristics. Among them, amorphous and monocrystallin state can only be achieved in extreme conditions for metals, so they are out of scope of this work.

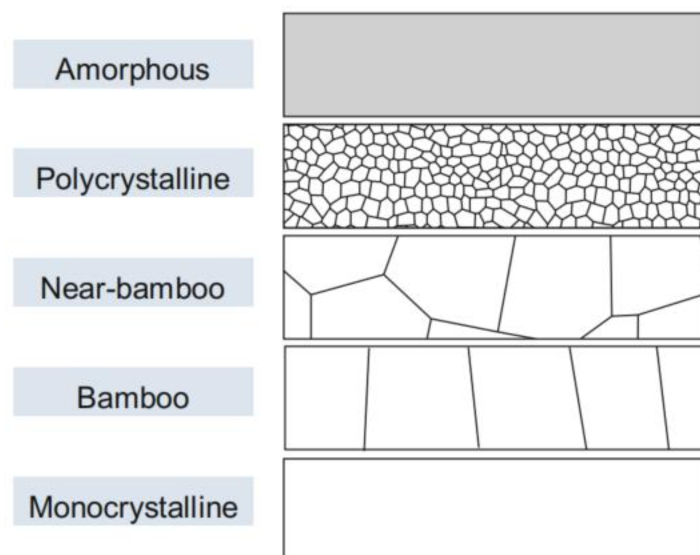


Figure 7. Schematic of different types of lattice structures in metal. [17]

The most common type of structures occurred in interconnects is polycrystalline. They generally have relatively smaller grain size and more grain boundaries, thus providing more diffusion paths for atomic flow and is prone for EM to occur. Near-bamboo or bamboo structures have larger grain size and fewer grain boundaries, thereby significantly reducing the diffusion paths for Cu atoms and being more resistant to EM. EM failure tends to occur adjacent to the region where mass is easily accumulated or depleted. A well-known structural inhomogeneity that can leads to mass accumulation and depletion is called triple points, which are points where grain boundaries branch off as shown in Figure 8. Bamboo structure is very resistant to EM since no triple point appeared in it.

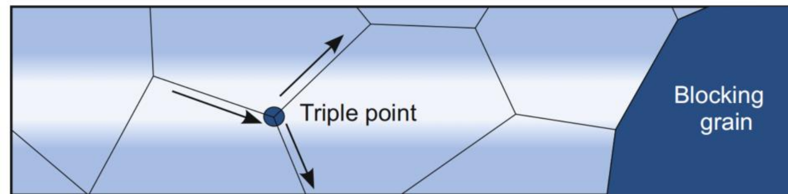


Figure 8. Schematic of tripe points in grain boundaries. [17]

Near-bamboo and bamboo structure can be obtained by means of annealing [14]. Temperature and line width/grain size ratio play an important role in this process. Only if the ratio is small enough can a bamboo structure be obtained at an elevated annealing temperature, as illustrated in Figure 9. Annealing not only enhances EM resistance from the perspective of grain size, it can also improve EM life-time by increasing (111) grain orientation in Cu [29]. Cu as face-centred-cubic (FCC) structured metal, (111) oriented plane is the closely packed plane thus possessing the lowest surface energy, which is desirable in resisting EM.

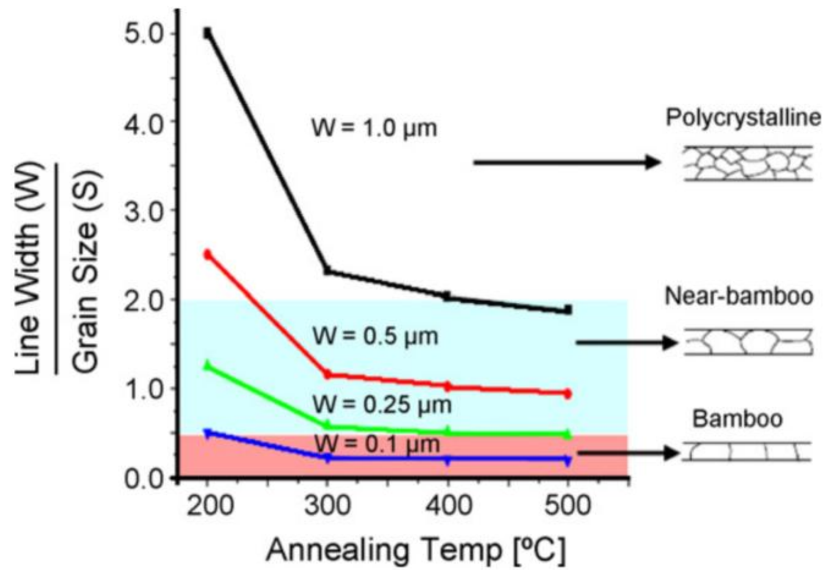


Figure 9. Grain structures of the electroplated Cu with annealing temperature for different line widths. [14]

Twin boundary is a unique grain boundary whose lattice structures are mirror images of each other in the plane of the boundary as shown in Figure 10a . A more detailed microscopic image of twin boundaries observed by HRTEM is presented in Figure 10b.

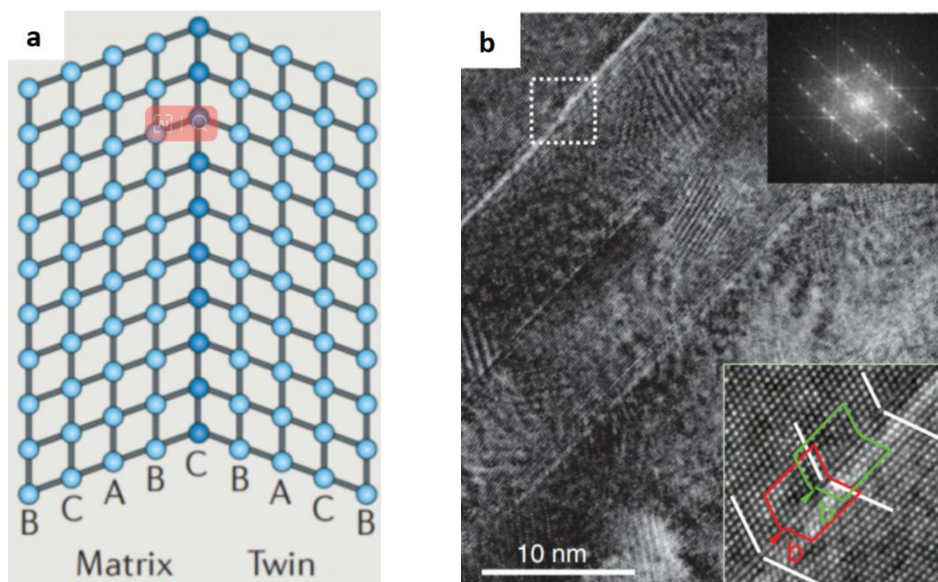


Figure 10. (a) Schematic of lattice structure of twin boundary [30]. (b) HRTEM image of lattice structure of twin boundary [31].

The mircorstructure can be also effected by different deposition techniques, seed layers, barrier materials types, and film thickness. It was reported that the electroplated Cu has two times EM lifetime than Cu grown by CVD [13]. The types of barrier materials also have effect on the microstrcuture. The grain size distributions for different barrier materials including SiN, TaN, Ta, TaSiN and CVD TaSiN are present in Figure 11. In addition, the grain size was found to increase both with increase in film thickness and line width [32,33].

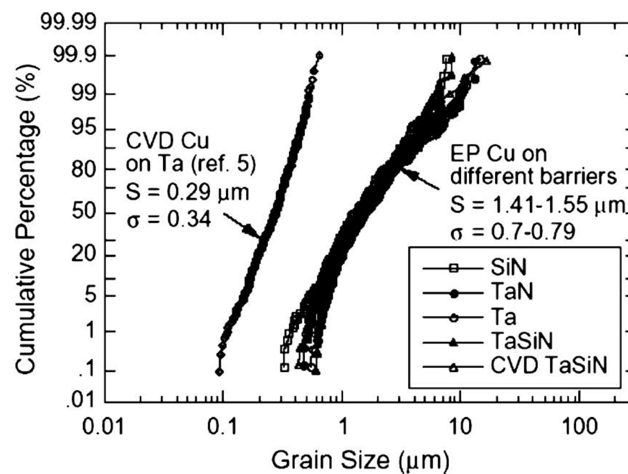


Figure 11. Grain size distribution of electroplated Cu with various barriers. [34]

Noteworthy, different metals may fail in different ways due to their diverse microstructure. As Cu and Al demonstrated in Table 1, they have various dominant diffusion modes due to the discrepancy in activation energy.

2.3.2 Interface

From the perspective of activation energy, the interface between metals and other surrounding materials can be a fast diffusion path for EM process, especially for Cu in damascene interconnects [35]. The main reason for the EM produced by interface is that defects can be generated when removing redundant Cu from the top of the wafer (i.e. chemical mechanical polishing (CMP) process), thus promoting the occurrence of EM. Hence, improving interface characteristics is an effective way to suppress EM in interconnects.

In general, there are two ways to improve interface characteristics, which are surface treatment and adding different capping layers.

A very commonly used surface treatment is called plasma treatment, which uses plasma ions to remove native oxides on the metal surface through redox reactions. It has been reported that H_2, He and NH_3 can be used in plasma treatment [36-38].

Adding a capping layer, such as SiN and SiC, also shows a good results on improving EM performance [39]. Such capping layers improve the adhesion properties of the interconnect surface, and a tightly bonded interface can simply slow down the diffusion of atoms, thus hindering the occurrence of EM. It was also reported the Cu line covered with Ta/TaN, SiN_x, and $SiC_xN_yH_z$ layers has a better EM lifetime and the activation en increases from 0.87eV to 1.4eV [40,41].

2.3.3 Barrier Materials

For Al and Cu based interconnection system, barrier layers, also known as metal liner, play a very important role in improvement of EM performance. In damascene process, it is deposited between metal and dielectric, and between via and underlying metal layer as shown in Figure 12.

At high temperature, Cu tends to diffuse into surrounding silicon and silicon oxide, which can lead to degradation of Cu and formation of a copper silicide layer with low conductivity. Barrier layers are able to effectively hinder such phenomenon and block surface diffusion. Moreover, the barrier layers can contribute to the current flow and acts as an electrical contact between the vias and the metal layer.

A study has been performed to compare the barrier performance among Ta, TaN and TiN in Cu metallization. It was found that Ta shows the best EM performance and lowest electrical resistance while TaN has better stability with Cu at high temperature and better step coverage capability [42,43].

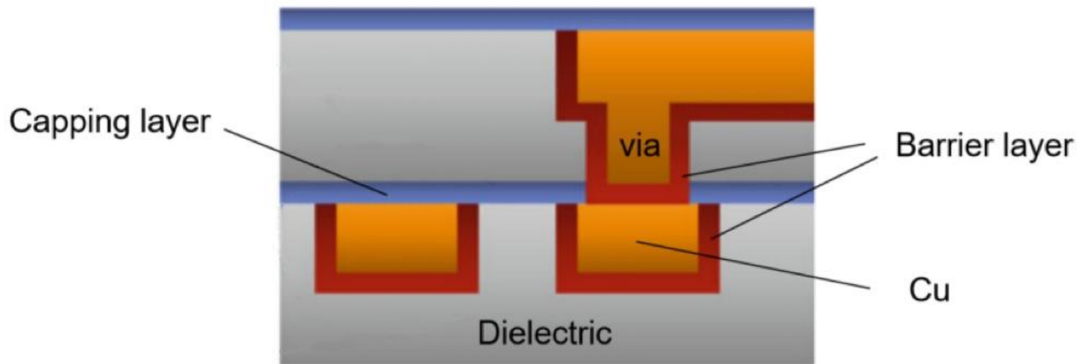


Figure 12. Schematics of cross-section of Cu tracks with surrounding barrier layers. [17]

2.3.4 Other Factors

2.3.4.1 Current crowding effect

The current density is not uniform in different regions of the conductor. When atoms are in a region with higher current density, the atomic transport speed will be faster, thus leading to EM. Especially some regions with large-angled corners (e.g. right-angled corners) are prone to the current crowding effect and the current density can be very high. Therefore, the current crowded zone is always found in the via structure used in the Damascene process, which has steps with large angles as shown in Figure 13.

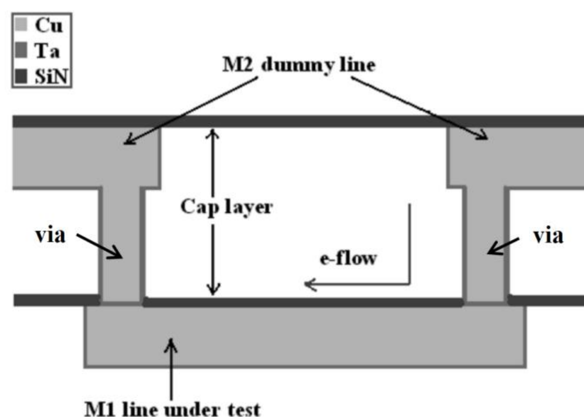


Figure 13. Cross sectional schematic of via structure. [44]

In a current crowded zone, the temperature distribution can be non-uniform because the current and temperature are related to each other in an electrical conductor. Such non-uniform temperature distribution can result in stress gradient due to thermal mismatch and temperature gradient, which both have been shown previously to be the driving force for EM.

2.3.4.2 High frequency effect

The current density in an interconnect can be non-uniform at high frequencies. The current tends to flow near the interconnect surface, which will make the current density to increase at the outer regions of the wire and the effective cross sectional area of the interconnect is decreased, so this phenomenon is also called skin effect. Hence, excessive current density is known to cause EM occurrence.

3. Experimental

3.1 Fabrication Process

The provided wafer is a single-side polished p-type wafer with a thickness of 525um, featuring a 300nm SiO_2 layer serving as an isolation layer. Positioned above the SiO_2 is a 300nm titanium nitride (TiN) layer deposited to act as a conducting layer. The purpose of the TiN layer is to enhance adhesion between the Cu interconnect and the substrate and to prevent Cu diffusion into the SiO_2 layer. During the electromigration (EM) test, the current passes through the TiN layer before reaching the Cu interconnect. To establish a robust and efficient contact interface between TiN and Cu interconnect, a hot sputtering etch (HSE) process is applied to remove the oxide on the wafer surface before Cu deposition. Subsequently, a 200nm thick Cu film is sputtered onto the TiN layer. The comprehensive schematic of this structure is represented in Figure 14.

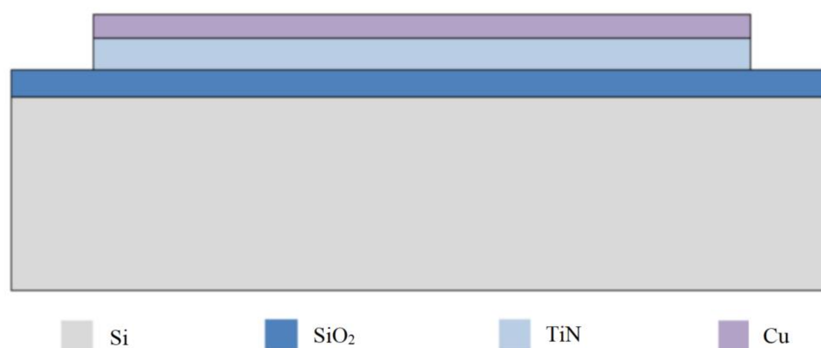


Figure 14. Schematic side view of the wafer structure.

3.1.1 Photolithography

Photolithography is a technique to construct thin film with desired patterns on a substrate with high precision. In this work, the photolithography process is composed of three primary steps: coating, exposure and development. Initially, the wafer is coated with AZ ECI 3027 photoresist by spin coating. Subsequently, the coated wafer undergoes a softbake at 100°C for approximately 60s. After the softbake, the wafer is exposed using the ASML PAS 5500/80 wafer stepper to create patterns. The

comprehensive pattern design on the mask is shown in Figure 15. Immediately following the exposure, a post-exposure bake is conducted at 120°C for around 60s. Finally, the wafer is developed using the AZ 726 MIF developer at room temperature.

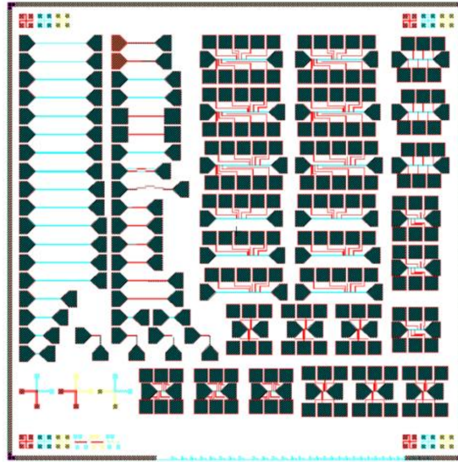


Figure 15. Schematic of the designed pattern on the mask for exposure.

3.1.2 Test Structure

In this study, Blech structure serves as the test structure, where the interconnects are directly deposited on a thin redundant layer TiN, as shown in Figure 16a. Redundant layers, usually with relatively higher resistivity, connect to external contact pads. The layout of the structure is shown in Figure 16b, which is composed of five identical Cu lines with dimensions of 100μm in length and 5μm in width. When electric current passes through the structure, it preferentially flows through each Cu line due to its lower resistivity compared to TiN, facilitating EM to occur. This is also called a drift structure because the movement of the material induced by EM is visible from above. This simplifies the observation of voids and hillocks that form following the electromigration test, thus enabling the measurement of the physical drift rate.

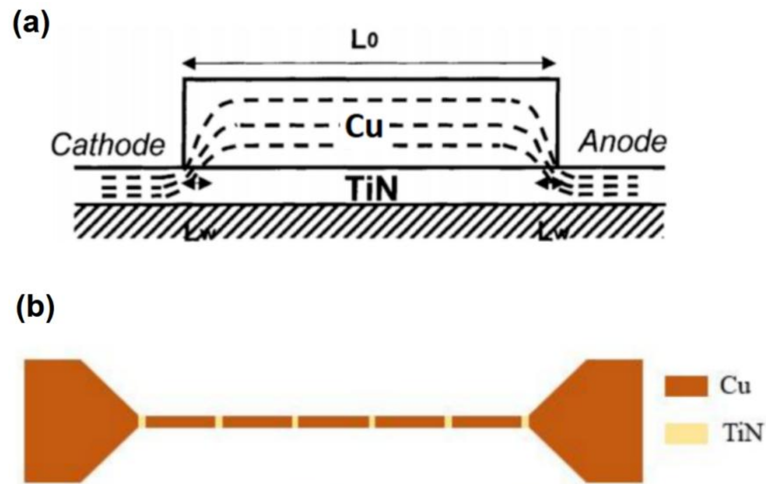


Figure 16. Schematic of (a) side view of Blech structure [45] and (b) test unit for EM test.

3.1.3 Etching

Etching is a process that selectively removes material in the unmasked region after photoresist development to form the required pattern. Generally, etching methods can be categorized into dry etching and wet etching. Dry etching is typically an anisotropic process utilizing accelerating ions to physically etch the target materials. This method offers advantages such as achieving precise cuts and highly anisotropic profiles. However, it has low etch-selectivity between different materials and can cause subsurface damage. In contrast, wet etching is an isotropic process that employs liquid chemicals or etchants to remove target materials. Wet etching can be highly selective to other materials, is relatively inexpensive, and simple to use. However, it suffers from poor directional etch selectivity and less accuracy compared to dry etching.

In this study, to construct the desired structure, dry etching was utilized for TiN to achieve a precise profile, while wet etching was employed for Cu due to the limited etching selectivity of TiN.

3.1.4 Sputtering

Sputtering is a physical vapor deposition (PVD) technique widely applied in the semiconductor industry for thin film fabrication. The process involves the

acceleration of high-energy argon ions by applying voltage, leading them to bombard the target material in a vacuum chamber. This bombardment causes the atoms or molecules of the target material to be ejected and deposit onto the substrate, forming a thin film.

In this work, the target materials are TiN and Cu successively. Radio frequency (RF) sputtering was employed for the deposition of both the TiN layer and the Cu film. Prior to the deposition of copper, HSE was performed to remove the thin oxide layer on the TiN. This step was essential for enhancing the adhesion between the TiN layer and the Cu film. The final product of the sputtered Cu is shown in Figure 17.

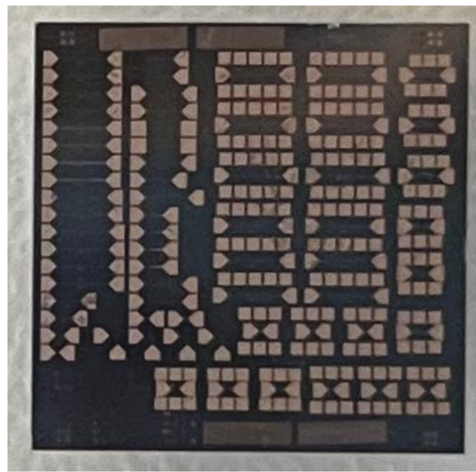


Figure 17. Schematic of the final product of the sputtered Cu film.

3.1.5 Annealing

Annealing is a heat treatment process that involves heating a material to a specific temperature and holding it at that temperature for a certain period, followed by slow cooling. The purpose of annealing for this work is to modify the microstructural properties of Cu interconnect. In this study, Cu samples were annealed in a vacuum chamber with N_2 and H_2 at 300℃, 400℃, 500℃, 600℃ and 700℃ for 1 hour . Subsequently, the heat source was turned off and the samples were cooled slowly in the furnace.

3.1.6 Electroplating

Electroplating is a technique used to deposit a layer of metal onto a substrate through the reduction of cations of that metal by applying an electric current. It can be broadly categorized into two types: direct current (DC) and pulse electrodeposition (PED). PED is the primary method employed in producing Cu nanotwin structures. This method includes cycling between on-time (t_{on}) and off-time (t_{off}), where t_{on} and t_{off} represents the duration of power being on and off in each cycle, respectively. The ratio of t_{on} to the total period in each cycle is referred to as the duty cycle. Adjusting the duty cycle plays an essential role in influencing the outcomes of electroplating.

In this study, electroplating was conducted using the Meco Mecoplater Copper MEMS in the EKL cleanroom. As in previous processes, a TiN layer and a Cu film were deposited on SiO_2 without etching, and the Cu film served as a seed layer. Subsequently, electrodeposition was performed at room temperature. The plating bath comprised $CuSO_4 \cdot 5H_2O$ and H_2SO_4 as the main constituents, with additional additives such as HCl, Cu8510A, and Cu8510C. The applied voltage during the on-time (t_{on}) was set at 0.4V, with an off-time (t_{off}) fixed at 0.04s (seconds). To optimize the formation of nanotwinned structures, various values of ton were adjusted from 0.2 to 1s, in increments of 0.2s. Following the plating process, the samples were rinsed in deionized water and dried. Subsequently, they were immersed in acetone to remove any remaining photoresist, followed by additional rinsing and drying. This procedure ensured the cleanliness and proper preparation of the samples for further analysis.

3.2 Electromigration (EM) Test

To expedite the slow EM process, an accelerated test is conducted by manipulating temperature and current density to promote the occurrence of failure. Prior to testing, the sample is placed into a vacuum box called NEXTRON micro probe station (MPS), as shown in Figure 18. The tungsten-based probes connected to a power source are employed to apply current to the Cu interconnect, while the plate in the middle can heat the sample with a control via computer commands.

The experiments are carried out at a temperature of 250°C and a loading current density of $2.7\times10^6 A/cm^2$, each lasting for a duration of 5 hours. For each sample, four cycles of testing are performed on each sample, resulting in a cumulative application of 20 hours of testing. After each test, the samples are characterized by SEM to observe any EM-related variations. Throughout the measurements, the sample voltage and temperature variation were continuously monitored and recorded in real-time, with a sampling frequency of 20s per reading.

Figure 18. Schematic of the internal structure of the NEXTRON micro probe station (MPS).

3.3 Characterization Techniques

3.3.1 Scanning Electron Microscope

The Scanning Electron Microscope (SEM) employs a focused beam of electrons to scan the sample, providing detailed information about surface topography and composition through the interactions between the electron beam and the atoms in the sample. SEM is widely recognized as an indispensable analytical tool for characterizing microelectronic structures.

In this study, SEM was utilized to observe and record the EM process occurring on Cu films. The electron beam energy was set at 5 or 10kV, with a spot size setting at “Spot 3”, and the working distance was adjusted between 5 and 10mm to ensure accurate imaging. Additionally, SEM can be coupled with Electron Backscatter Diffraction (EBSD) and Energy Dispersive X-ray Spectroscopy (EDS) to give comprehensive insights into the microstructural and compositional characteristics of the samples.

3.3.2 Energy-dispersive X-ray Spectroscopy

Energy-dispersive X-ray spectroscopy (EDS) relies on an interaction of some source of X-ray excitation and a sample to perform elemental analysis and chemical characterization on the sample. It is usually used in combination with SEM, TEM, etc. It can be used to qualitatively analyze the elements present in the sample and identify the concentration of each element.

3.3.3 Electron Backscatter Diffraction

Electron Backscatter Diffraction（EBSD）is a technique that allows crystallographic orientations, misorientations, texture trends and grain boundary types to be characterized and quantified on a sub-micron scale in the Scanning Electron Microscope (SEM). It uses the accelerated electron beam to strikes a steeply inclined crystalline sample, and produces backscattered electrons, which are diffracted by the surface crystal structure and carry the information of the orientation of the grains on the surface of the sample into the detector. It can give orientation mapping of the sample, which capture the diffraction pattern and analyze crystallographic orientation relationships. From EBSD map the grain orientation and average grain size of detected area can be obtained.

In this work, EBSD analysis was conducted using the SEM XL30 SFEG equipped with an EBSD system featuring an EDAX DigiView-5 camera. Given that the primary objective of this study is to observe the surface variations of Cu stripes, a low-energy electron beam (5kV) was used for SEM imaging. For EDS, high-energy electron beams at 15kV were used to provide element analysis. During EBSD measurements,

the electron beam energy was set at 20kV, with a spot size of 3μm. EBSD mapping was performed with a fine step size of 0.03μm to ensure detailed and accurate observations of the microstructural features. Additionally, the sample was tilted to an angle of 70° with a work distance of around 13 to 15mm to obtain high-quality diffraction patterns. After characterization, data acquired from EBSD were processed using OIM Analysis 8.3 software.

3.3.4 Probe Station

To measure the resistivity of the annealed samples, a Cascade Summit 12000 probe station was employed, as illustrated in Figure 19. The sample is placed at the center of the chuck and secured using the vacuum system integrated into the chuck. Subsequently, the chuck is loaded into the chamber and positioned beneath the probe system, which provides voltage through settings configured in the computer software. By adjusting the positions of both the chuck stage and the probe stage, the probes can be accurately placed on the designated areas of the sample for measurement. An optical microscope, Mitutoyo FS-60, is mounted on the mounting block with a hole that allows the lens to go through for obervation. The measurement setup is connected to a Keysight B1500A semiconductor parameter analyzer, which is used to acquire data such as the I-V characteristics of the sample, facilitating the analysis of the annealed Cu samples.

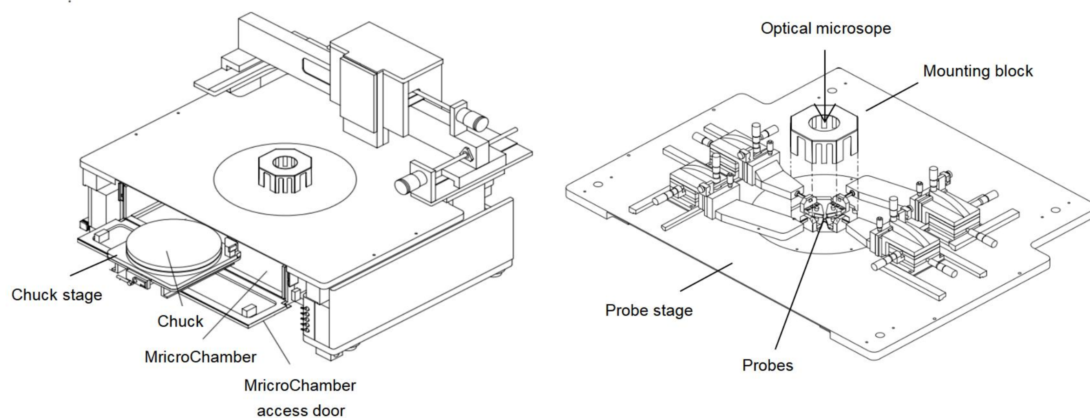


Figure 19. Schematic of Cascade Summit 12000 probe station.

4. Effects of Annealing Temperature on Microstructure

In this section, the influence of annealing at temperatures of 300℃, 400℃, 500℃, and 700℃ on the microstructure of Cu interconnects is systematically investigated. Due to the exclusive use of sputtering for producing annealed samples, electroplated samples were excluded from this analysis. Furthermore, owing to time constraints and limited success in forming Cu nanotwins via electrodeposition, the results of the electrodeposition process are detailed in Appendix A.

As mentioned in Section 3.1.2, each sample contains five identical Cu lines. In this work, three of these lines were selected for analysis. Due to space constraints, the detailed analysis of one representative line is presented in the main content, while the figures of the other lines is included in the Appendix B. The SEM images for samples annealed at each temperature are shown in Figure 20.

It is important to note that the sample annealed at 600℃ is not suitable for this study as it exhibits significant void formation on the surface of the Cu interconnect, likely due to dewetting caused by the elevated annealing temperature. This phenomenon prevents subsequent EBSD analysis. The dewetting phenomenon is further discussed in Section 5.1. Although dewetting also occurred in the sample annealed at 700℃, the structure was not severely deformed and could still be characterized by EBSD. Since all samples were derived from the same wafer and annealed under identical conditions with only the temperature varying, this anomaly could be attributed to external factors such as fabrication and processing errors, though the exact cause remains unknown.

The microstructure of the interconnect is critical in determining its electromigration (EM) reliability. This investigation delves into the effects of annealing on grain orientation, grain size, grain boundary angle, and defect-related parameters to provide a comprehensive understanding of the microstructural factors influencing EM performance.

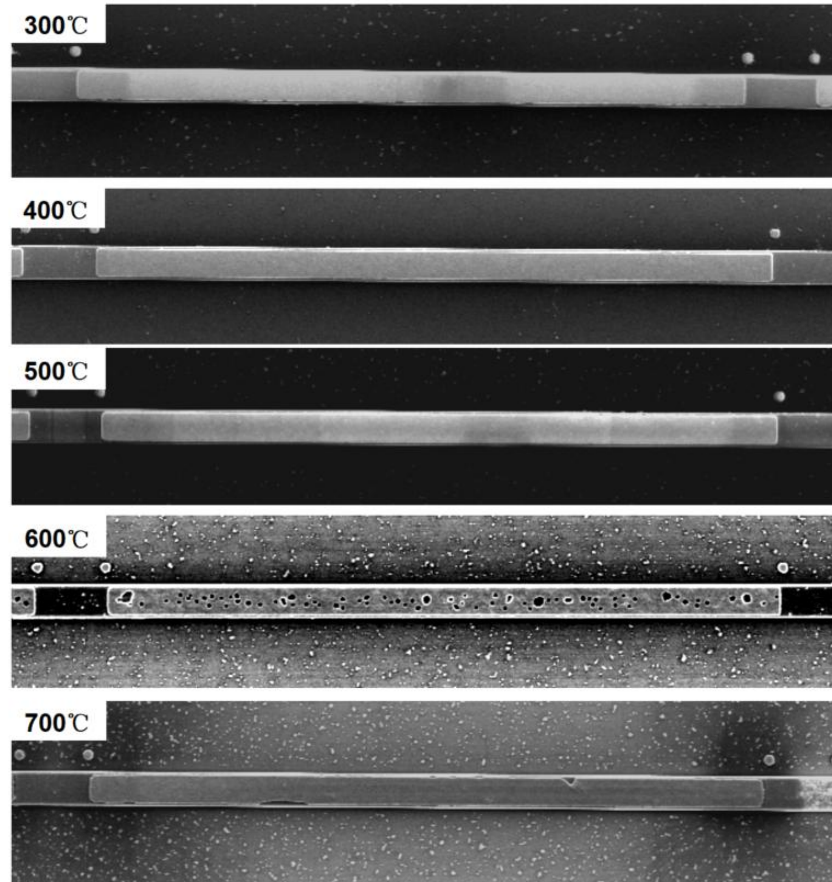


Figure 20. SEM images of samples annealed at 300°C, 400°C, 500°C, 600°C and 700°C.

4.1 Grain Orientation

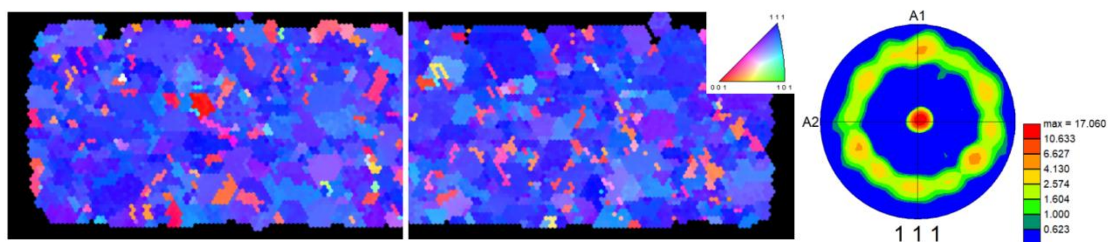
The inverse pole figures (IPFs) indicating textures of the three samples are illustrated in Figure 21, accompanied by pole figures that further confirm their predominant grain orientation. A color legend is provided in each figure, which represents the orientation distribution through a color-coded pattern.

At 300°C, the annealed sample is predominantly (111) textured. Nevertheless, a substantial number of grains with other textures, such as (001) represented by the red regions, are observed randomly distributed across the sample. For sample annealed at 400°C, with the maintained dominance of the (111) texture, a reduction in randomly oriented grains is observed. However, various textures other than (111) are still scattered throughout the sample. As the annealing temperature reaches 500°C, the

texture distribution becomes more uniform, with a stronger (111) texture emerging. Additionally, other textures with small areas, which sporadically appeared in the sample annealed at 300℃ and 400℃, is remarkably decreased. With further elevation of annealing temperature to 700℃, the Cu film exhibits a strong (111) texture with fewer occurrences of other textures such as (001).

The pole figures on the right of each plot further indicate that the dominant texture for all different samples is (111), with sharp (111) textures evident in all plots. These pole figures represent stereographic projections of the (111) crystallographic plane normal orientation distributions, with the center of the plots representing the position normal to the sample surface. The color scale with values beside the pole figures is known as multiples of uniform density (MUD). This MUD number is one measure of the texture strength in an EBSD pole figure, with higher values indicating stronger alignment [46]. Interestingly, from 300℃ to 500℃, the distributions of the (111) texture for these samples change only slightly, as indicated by the maximum MUD value shown in each pole figure. A stronger (111) texture is observed when the annealing temperature reaches 700°C. This outcome suggests that the density of the (111) texture increases slightly as the annealing temperature rises, and the uniformity of its distribution improves. Although not highly pronounced, this result is consistent with previous findings suggesting that higher annealing temperatures can enhance preferential grain orientation in Section 2.3.1.

(a) 300℃



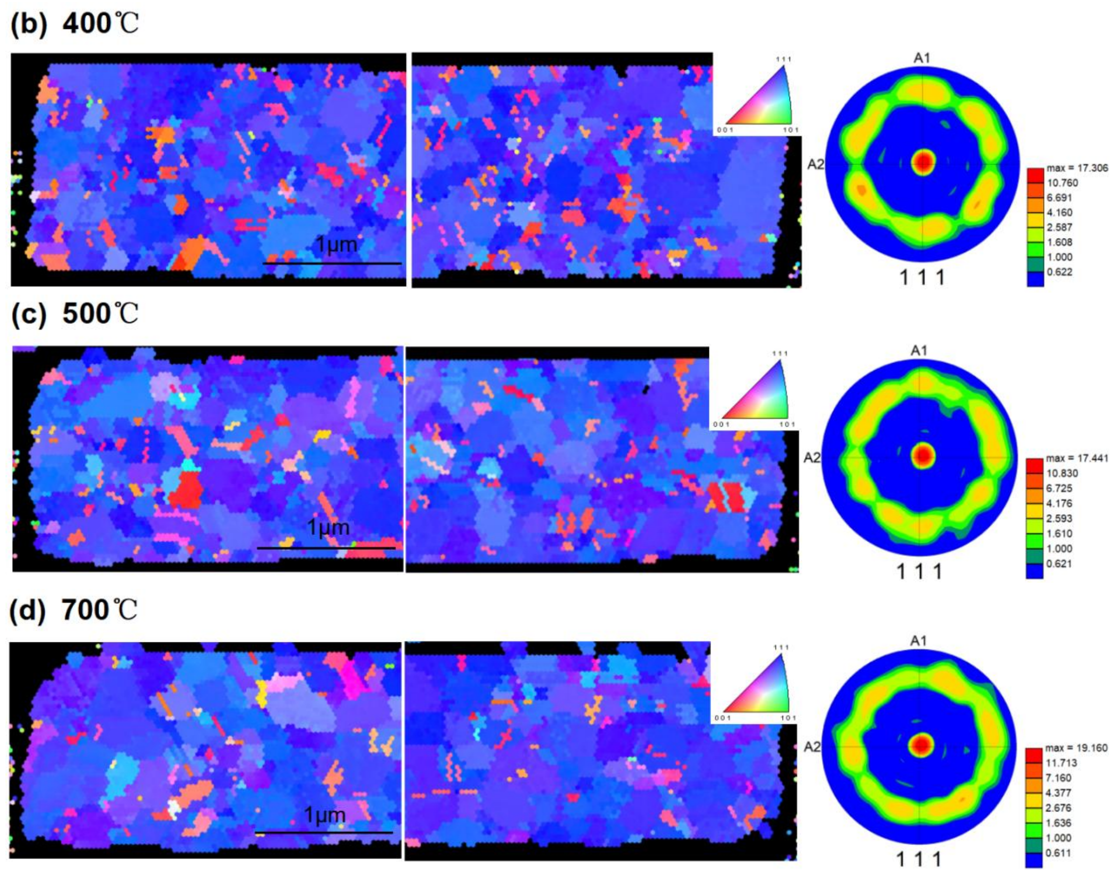


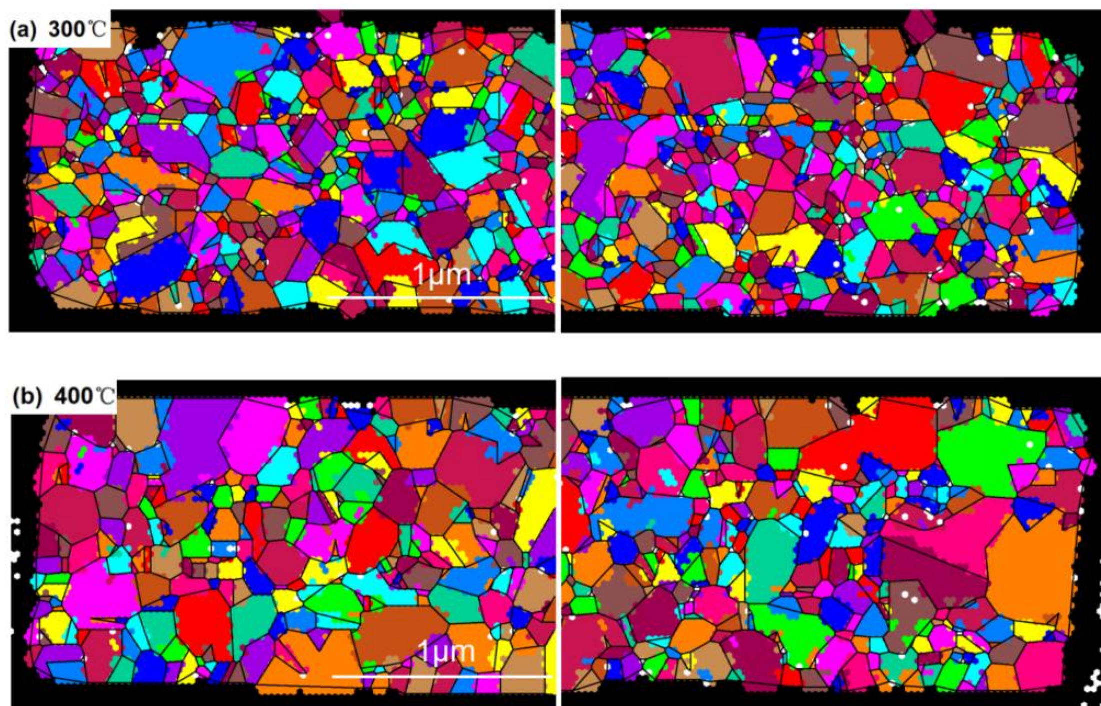
Figure 21. Schematic of inverse pole figures (IPFs) and pole figures (PFs) of samples annealed at (a) 300°C, (b) 400°C, (c) 500°C and (d) 700°C.

4.2 Grain Size and Distribution

The grain structures of the samples at different temperatures are presented in Figure 22. Each color-coded area represents an individual grain as generated by the OIM software, with a general grain tolerance angle set at a default value of 5°. White areas indicate unindexed points, typically considered part of grain boundaries. With the increase in annealing temperature, the grains are observed to grow larger, and the grain size distribution becomes more uniform. This observation is consistent with the understanding that annealing provides thermal energy for grain growth, facilitated by grain boundary migration toward the centers of curvature [47]. The average grain sizes calculated by the OIM software for samples annealed at 300°C, 400°C, 500°C, and 700°C are 0.145μm, 0.188μm, 0.199μm, and 0.246μm, respectively, indicating a

clear increasing trend.

In Figure 23, the comparison of grain size distributions is presented. At 300°C, the sample exhibits a predominant grain size peak around 0.05μm, representing more than 20% of the total area fraction, with a gradual decrease as grain size increases. Upon annealing at 400°C, the grain size distribution appears more uniform compared to 300°C, with a peak at approximately 0.14μm, accounting for 12% of the fraction. Similarly, at 500°C, the peak occurs at 0.11μm with fractions around 13%. Notably, samples annealed at 400°C and 500°C show minimal change in grain size, maintaining peaks at nearly the same position. At 700°C, the grain size distribution exhibits a Poisson distribution with a downward-facing opening. Moreover, both samples annealed at 500°C and 700°C contain grains exceeding 0.5μm in diameter, a phenomenon absent in the lower temperature annealed samples. This analysis indicates significant grain growth at higher annealing temperatures, and the Cu film has undergone deformation due to the elevated temperature.



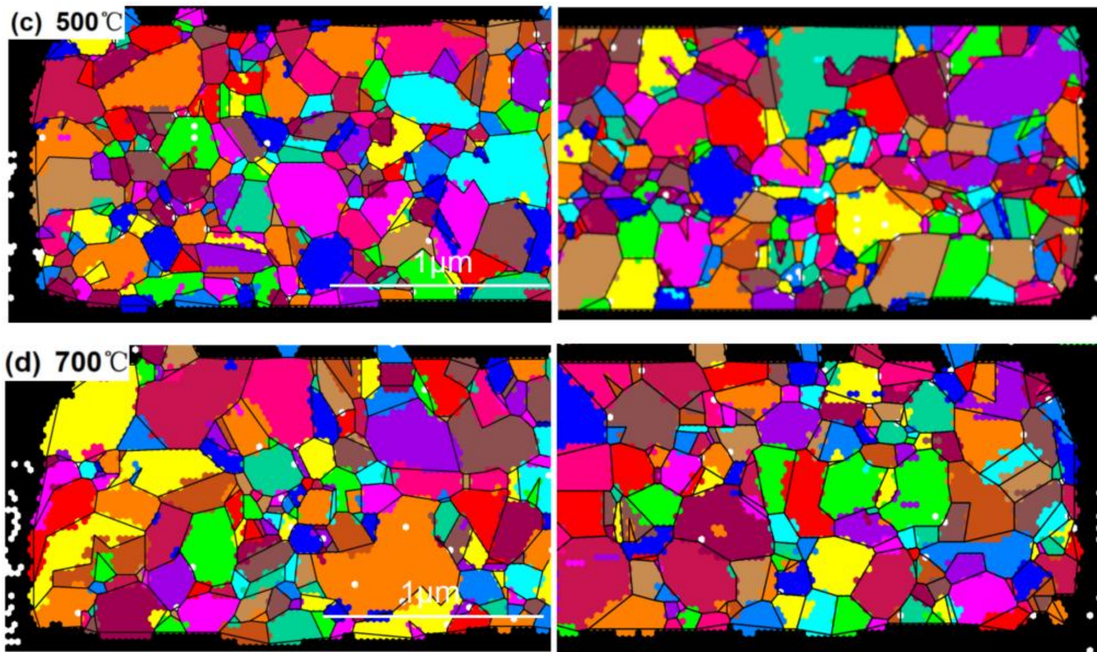


Figure 22. Schematic of grain mappings of samples annealed at (a) 300°C, (b) 400°C, (c) 500°C and (d) 700°C.

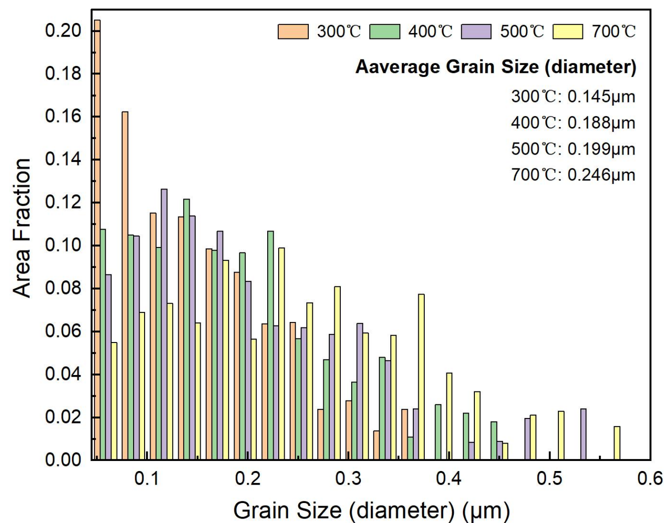


Figure 23. Schematic of grain image and grain size distribution of samples annealed at 300°C, 400°C, 500°C and 700°C.

4.3 Grain Boundary and Misorientation Angle

This section focuses on the characterization of grain boundaries and misorientation angles. Grain boundaries were identified using a threshold angle of 5°, with

boundaries exhibiting misorientation angles below 5° classified as subgrain boundaries [48]. These subgrains, represented by yellow lines, are observed to be distributed within grains, particularly within larger grains. Generally, grain boundaries can be classified into low angle boundaries (LABs) and high angle boundaries (HABs), defined by the misorientation angle between two crystal grains being less than and more than 15°, respectively [48]. Figure 24 depicts both types of grain boundaries for each sample, with LABs shown in red and yellow lines and HABs in blue lines. The corresponding lengths and fractions of each type of grain boundary are summarized in Table 2. The data reveal that the total grain boundary length decreases almost linearly with increasing annealing temperature, indicating a reduction in the number of grain boundaries. This trend aligns with the observed growth in grain size and the attainment of a more uniform grain distribution through annealing. Notably, despite the decrease in both HAB and LAB lengths, the fraction of HABs decreases by approximately 10%, while the fraction of LABs increases by around 18%. The increase in LABs contributes to a more stable structure of the Cu film due to their lower surface energy and diffusivity, as smaller misorientation angles lead to more coherent interfaces between grain boundaries. This result suggests that varied annealing temperatures impact the ratio of HABs to LABs and tend to lower the system's energy by decreasing the number of HABs.

The detailed misorientation angle distribution is presented in Figure 25. As the annealing temperature increases, there is a noticeable increase in the proportion of the smallest misorientation angles. It is noteworthy that the number of twin boundaries, characterized by a 60° misorientation angle, constitutes a significant portion of the fraction and also increases with the annealing temperature. This observation suggests that higher annealing temperatures enhance resistance to EM, partially due to the increased presence of twin boundaries.

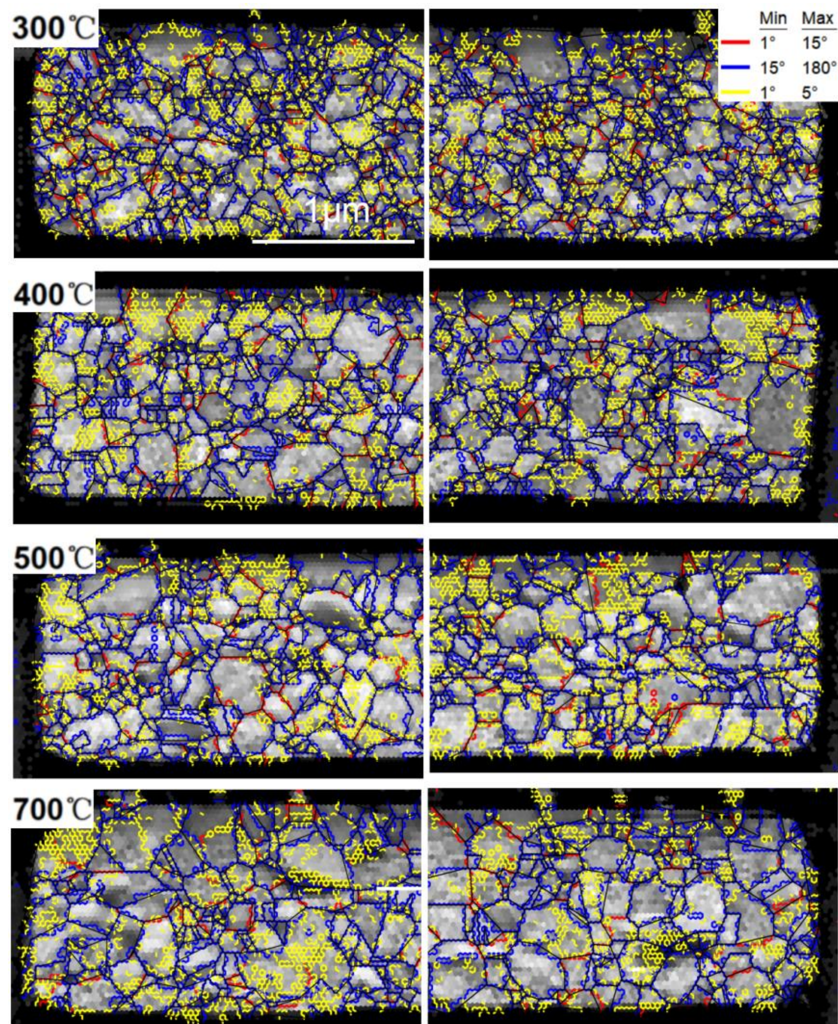


Figure 24. Schematic of ratio of high boundary angle and low boundary angle of samples annealed at 300°C, 400°C, 500°C and 700°C.

	High angle (15 - 180°)		**Low angle (1-15°)**		**Total length**
	length (μm)	Fraction	length (μm)	Fraction	length (μm)
300°C	83.89	0.642	46.628	0.358	130.518
400°C	72.048	0.634	41.578	0.366	113.626
500°C	59.585	0.585	42.365	0.415	101.95
700°C	46.08	0.579	33.418	0.421	79.498

Table 2. The length and fraction of HAB and LAB of samples annealed at 300°C, 400°C, 500°C and 700°C.

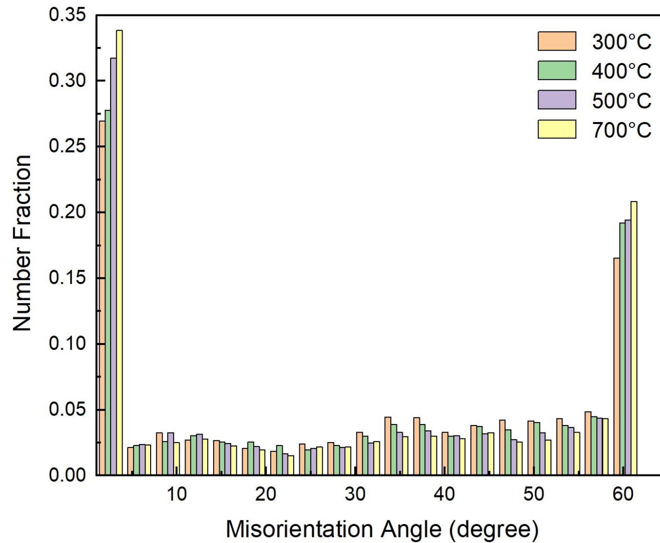


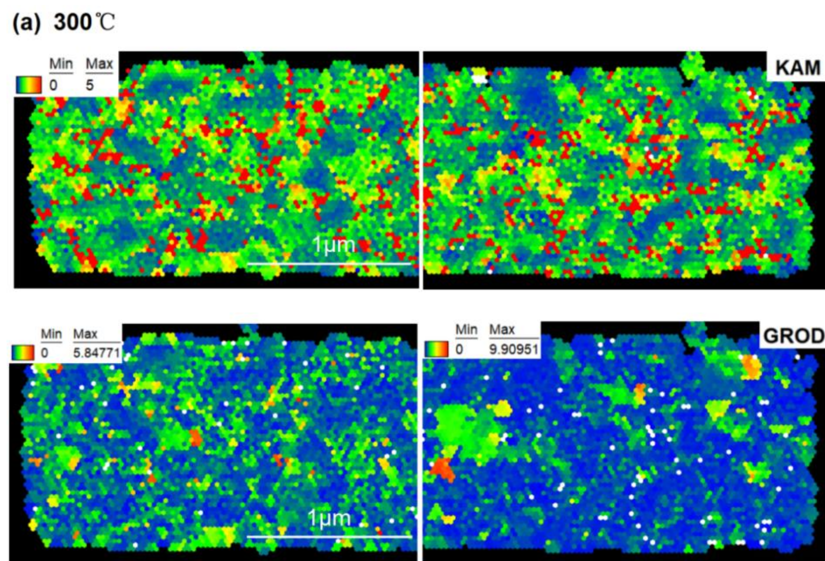
Figure 25. Schematic of misorientation angle distribution of samples annealed at 300℃, 400℃, 500℃ and 700℃.

4.4 Kernel Average Misorientation (KAM) and Grain Reference Orientation Deviation (GROD)

The Kernel Average Misorientation (KAM) is employed to describe the local misorientation (LM), defined as the average misorientation between a specified point and all its neighboring points. KAM values are commonly utilized to quantify variations in local misorientation induced by geometrically necessary dislocations (GNDs) and strain within the material [49]. On the other hand, the Grain Reference Orientation Deviation (GROD) provides an intra-grain misorientation map referenced to the average misorientation of a given point within the grain and all points belonging to that grain. The GROD parameter usually serves to quantify the recrystallization process and highlight localized changes in the material structure [50]. The KAM maps, featuring a gradient color range up to the 2nd neighbor with a 5° threshold angle, and the GROD map with a gradient color range are depicted in Figure 26. Regarding the KAM, it is evident that a considerable number of regions exhibit high KAM values at an annealing temperature of 300℃. Notably, these high KAM areas tend to appear around small grains, which may be attributed to the

increased presence of triple points in these regions. For the sample annealed at 400℃, a significant reduction in the occurrence of high KAM areas is observed, indicating potentially fewer defects and smaller stress within the sample. As the annealing temperature increases to 500℃ and 700℃, high KAM values further decrease, and the gradients appear to be more uniform. However, there is little change between these two temperatures, likely suggesting that the effects of annealing, such as defect and strain elimination, may have reached saturation within this temperature range. This outcome implies a decrease in defects and strain within the analyzed region as the annealing temperature increases within a specific range.

As observed in the GROD maps, the maximum value of the average misorientation characterized by GROD gradually decreases from 300℃ to 700℃, further indicating a reduction in defects and strain with increasing annealing temperature. Notably, relatively higher GROD values are observed in regions with larger grains, which may seem counterintuitive. This suggests that numerous misorientations are present within these large grains, likely due to the existence of a significant number of subgrains, as represented by yellow lines shown in Section 4.1.3, leading to higher GROD values. Moreover, the GROD values do not exhibit significant changes across different annealing temperatures. As the GROD value is primarily sensitive to factors such as localized deformation, this could imply that the samples analyzed do not exhibit substantial variation in this aspect across the annealing temperature range studied.



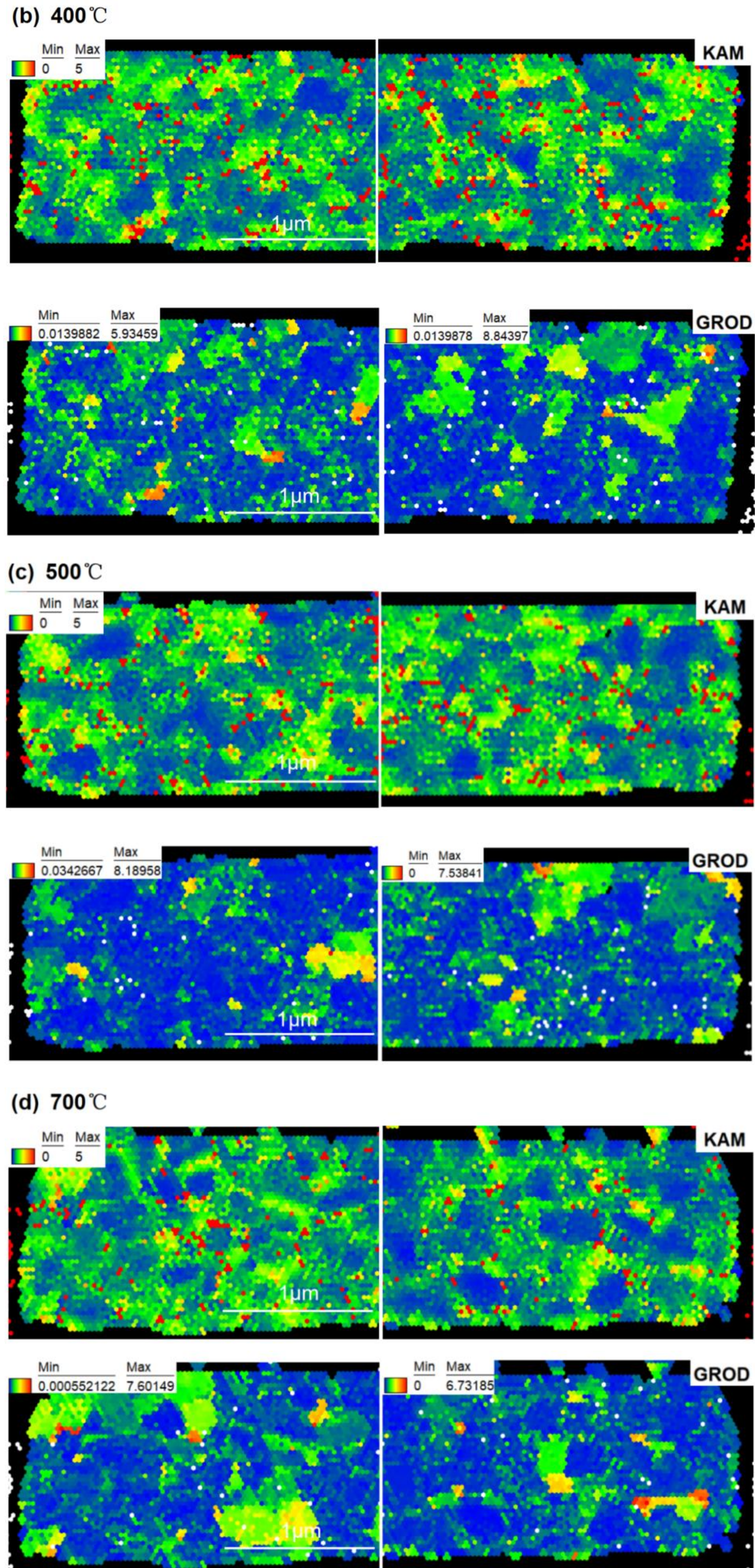


Figure 26. Schematic of KAM and GROD images of samples annealed at (a) 300℃, (b) 400℃, (c) 500℃ and (d) 700℃.

4.5 Resistivity Measurement

It has been reported that microstructure variations caused by annealing significantly impact the resistivity of Cu films, as both grain size and grain boundaries play crucial roles. The resistivity can increase due to electron scattering at the line sidewalls and electron reflection at grain boundaries [51]. Resistivity is a material property that quantifies the electrical resistance of a conductor with a specific unit cross-sectional area and unit length. For this study, as the Cu samples consist of thin-film Blech structures, the Van der Pauw method, which is a well-established technique for measuring the sheet resistivity of thin films, was employed. This method, first introduced by Leo Van der Pauw in 1958 [52], uses four probes placed on four identical contact pads of the sample, as illustrated in Figure 27. The current is passed through adjacent probes (A to B, B to C, C to D, or D to A), while the voltage is measured across the remaining probes (C to D, D to A, A to B, or B to C). The sheet resistance can then be calculated using Van der Pauw's formula:

$$R_s = \frac{\pi}{ln(2)} \cdot \frac{V_{CD}}{I_{AB}} \quad (12)$$

where I_{AB} is the current flowing through the adjacent probes, V_{CD} is the voltage measured across the remaining probes, R_{sheet} is the sheet resistance. The resistivity then can be subsequently calculated by:

$$\rho = R_s \cdot t \quad (13)$$

Where ρ is the resistivity and t is the thickness of the thin film.

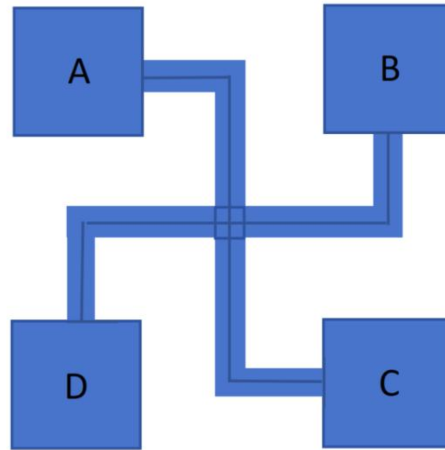
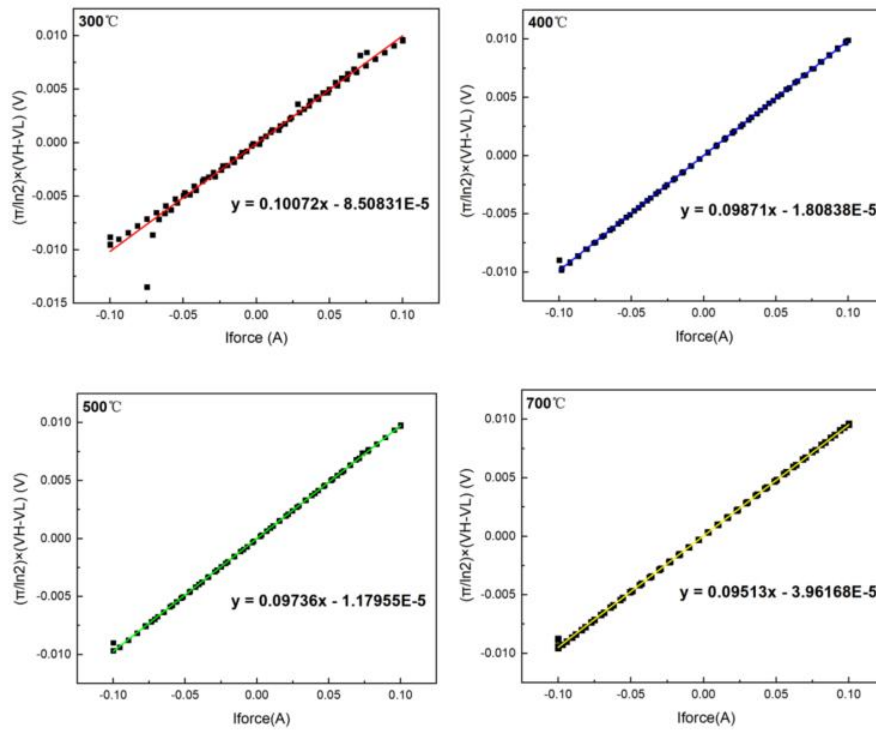


Figure 27. Schematic of the Van der Pauw measurement test structure.

In this study, the I-V curves for calculating sheet resistance and the resulting resistivity for samples annealed at various temperatures are presented in Figure 28. It is observed that the resistivity of the Cu film decreases with increasing annealing temperature, exhibiting an almost linear relationship. This finding aligns with previous results indicating that the resistivity of Cu films decreases with longer duration and higher annealing temperatures [51]. As discussed previously, annealing promotes grain growth and reduces grain boundary length. Grain boundaries pose significant obstacles to electron motion as the crystal lattice orientation differs on either side of the grain boundary relative to the wave vector of the incoming electron [53]. Therefore, a larger grain size results in fewer grain boundaries in the crystalline material, consequently decreasing resistivity.

(a)



(b)

	Sheet Resistance (Ω)	Resistivity (Ωm)
300°C	0.10072	2.0144×10^{-8}
400°C	0.09871	1.9742×10^{-8}
500°C	0.09736	1.9472×10^{-8}
700°C	0.09513	1.9026×10^{-8}

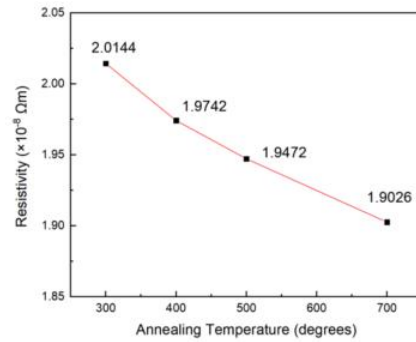


Figure 28. Schematic of (a) I-V curve for calculating sheet resistance, and (b) resistivity of samples annealed at 300°C, 400°C, 500°C and 700°C.

In Chapter 4, the results demonstrate a progressive enhancement of the (111) texture in Cu films, accompanied by an increase in grain size and a more uniform grain distribution as the annealing temperature rises. Additionally, a notable decrease in grain boundary length was observed with higher annealing temperatures, which correlates with reduced resistivity in the annealed samples. The fraction of HABs decreased while that of LABs increased, indicating enhanced microstructural stability at elevated annealing temperatures. Furthermore, defects and strain within the Cu films were found to diminish with increasing annealing temperatures, contributing to improved overall microstructural integrity.

5. Electromigration (EM) Test

The electromigration (EM) test was conducted on samples annealed at 300℃, 400℃, and 500℃, with each cycle lasting 5 hours, totaling 4 cycles of 20 hours. Similar to Section 4, only the selected representative line for each sample is analyzed in detail here, while the figures for the other lines are included in Appendix C. The sample annealed at 700℃ was excluded from this analysis due to significant dewetting observed on the contact pads, as illustrated in Figure 29, which resulted in electrical conduction failure within the Cu line.

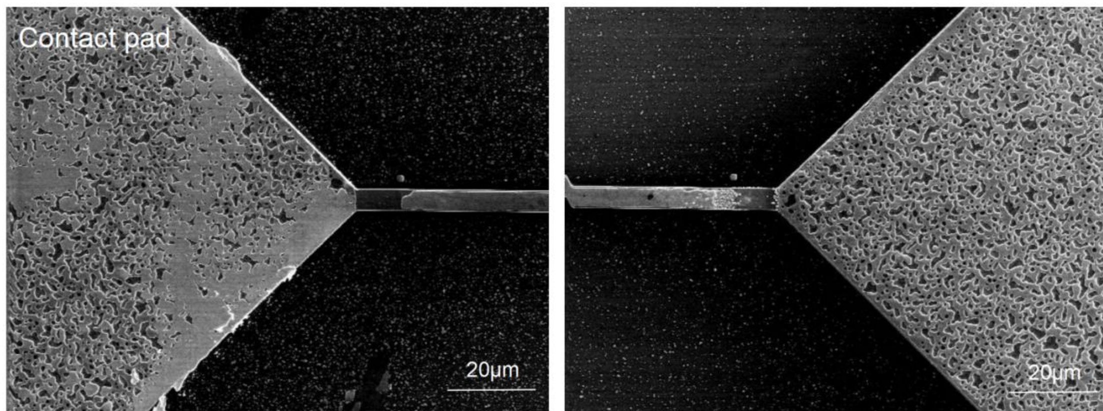


Figure 29. SEM images of contact pads on both sides of the sample annealed at 700℃.

In this section, the same microstructural parameters studied in Section 4 in terms of grain orientation, grain size, grain boundary angle, and defect-related parameters are investigated after the EM test. Additionally, the EM velocity, which quantifies the EM process, is calculated for each sample.

5.1 Effects of Microstructural Variation on EM Performance

Figure 30 presents the SEM images of the samples annealed at 300℃, 400℃, and 500℃, captured at 5-hour intervals during the EM test. EM is visible due to the formation of voids at the cathode. A consistent trend is observed across all figures, indicating a decrease in the area of void formation at the cathode as the annealing

temperature increases.

It is observed that a small hillock appeared at the edge of the Cu stripe for the sample annealed at 300°C after 5 hours of EM test. Notably, there was no significant change observed during the intermediate 10-hour EM test. However, when the test duration reached 20 hours, numerous hillocks appeared on the sample surface at the anode. In contrast, voids began to appear at the cathode when the EM test time reached 15 hours. Before the 10-hour measurement, only a few small voids had formed. Interestingly, the voids that appeared earlier did not expand further, while new voids formed in other locations, including the bulk region rather than just the edges. When the test time exceeded 15 hours, a significant amount of Cu migrated from the cathode. However, the migration was not complete, as some of the Cu film remained at the cathode, indicating a non-uniform transfer of Cu atoms.

When the annealing temperature increased to 400°C, a similar phenomenon was observed at both the anode and cathode. Hillocks became visible at the anode only after 15 hours, and between 10 and 15 hours, non-uniform migration also appeared at the cathode, spreading from the cathode to the anode along the stripe as time progressed. However, the migration rate was slower than the sample annealed at 300°C. Besides, both the 300°C and 400°C annealed samples exhibited a structure where numerous granular particles remained on the TiN surface after 15 hours. This phenomenon will be discussed in detail later.

At an annealing temperature of 500°C, EM was observed to be effectively suppressed. Noticeable voids appeared only after 15 hours, and the area of voids was much smaller compared to the previous two samples. Unlike the sample annealed at 300°C, where new voids formed at other locations, the original voids in the samples annealed at 400°C and 500°C expanded at the cathode. This phenomenon could be attributed to the enhanced stability of the bulk structure resulting from the higher annealing temperature.

Despite the fact that EM appears to initiate at the edge of the cathode, while the mass migration does not always proceed directly from the cathode to the anode. A small portion of atoms have a trend of migrating from the cathode toward the TiN surface

nearby, and numerous isolated particles have been observed at the cathode and attached on the TiN surface near the cathode. Additionally, a significant number of small voids have been detected at the edge of the anode for each sample when EM time reaches 20 hours, particularly in samples annealed at 300℃ and 400℃, indicating there is depletion of atoms at the anode. These phenomena, namely the formation of isolated particles and migration opposite to the expected direction of EM, are likely attributable to the effects of dewetting and thermomigration (TM).

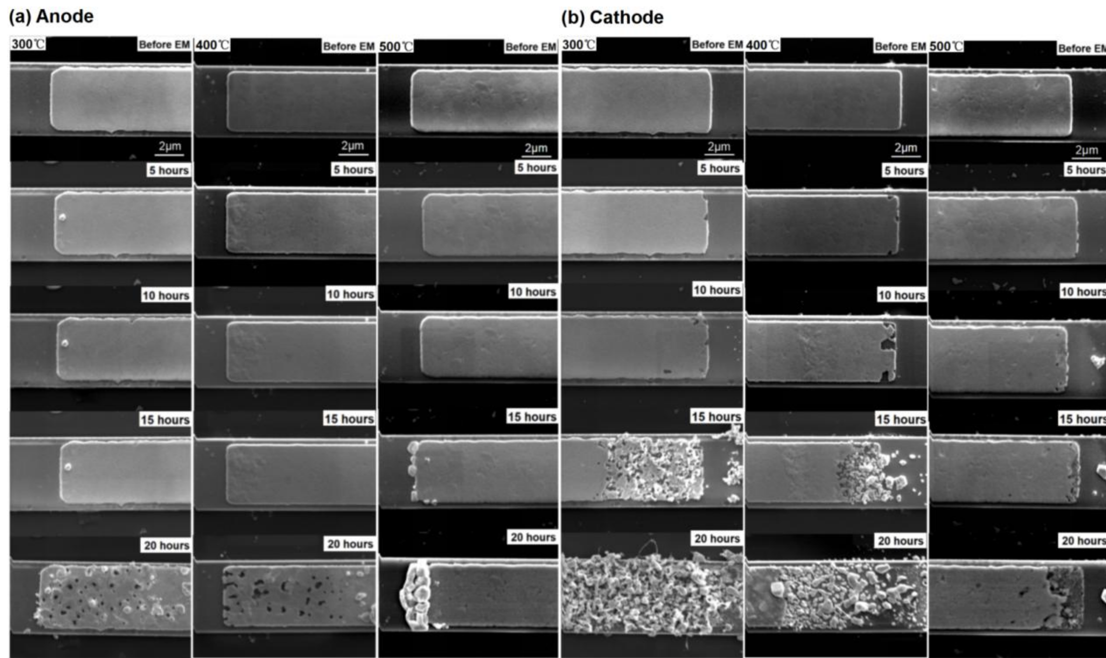


Figure 30. Images of (a) anode side and (b) cathode side of Cu interconnect annealed at 300℃, 400℃ and 500℃ before and after EM for 5, 10, 15 and 20 hours.

Dewetting is a process wherein a thin film breaks down into isolated islands through agglomeration at elevated temperatures, driven by surface energy minimization of the film. Solid films are typically metastable or unstable in their as-deposited state [54]. Furthermore, it has been reported that annealing can exacerbate this instability, causing the continuous film to rupture as surface energy increases [54].

In this study, all the Cu films were deposited through sputtering, which can result in limited atomic motion and the formation of nonequilibrium structures. As shown in Figure 31, dewetting was observed exclusively at the cathode of each Cu film, where dewetted Cu particles formed around the film edge and adhered to the TiN layer. This

phenomenon could be attributed to the Joule heating generated by the oxide layer between the Cu and TiN layer, as current density is significantly higher in regions near the oxide with high resistivity, as reported by Zhang et al [55]. Despite the pretreatment of removing the oxide layer before sputtering the Cu film, the samples were continuously exposed to the atmosphere during multiple separate EM tests, leading to inevitable oxidation as the EM test progressed.

Dewetting generally initiates from hole formation, which serves as a small perturbation and a necessary precursor to dewetting [54]. This initiation is closely associated with EM due to the formation of voids, which promotes the occurrence of dewetting. Furthermore, grain boundaries play a crucial role in dewetting for polycrystalline films, indicating a strong correlation with microstructure. Hole formation is most likely to occur at high-energy grain boundaries, such as high-angle boundaries with large misorientation [54]. It has been reported that triple points are particularly vulnerable to hole formation since the depth of the groove between grain boundaries at tripe points is deeper than in other regions [56]. Therefore, holes would first form at triple points created by grain boundaries with high energies.

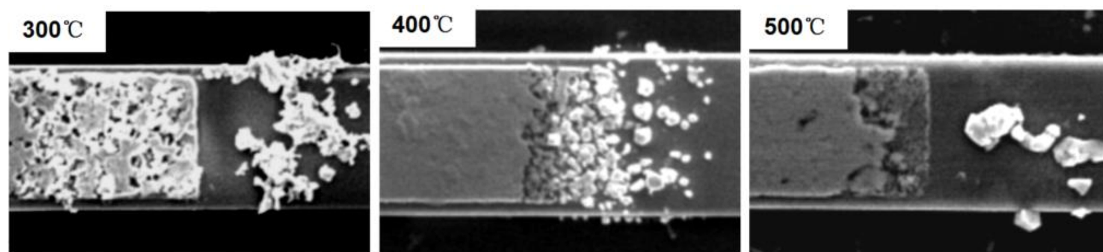
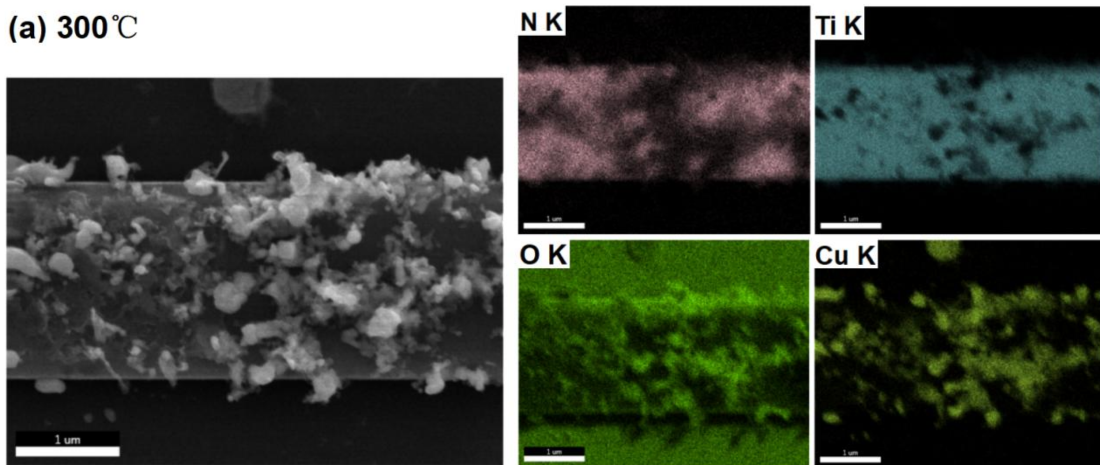
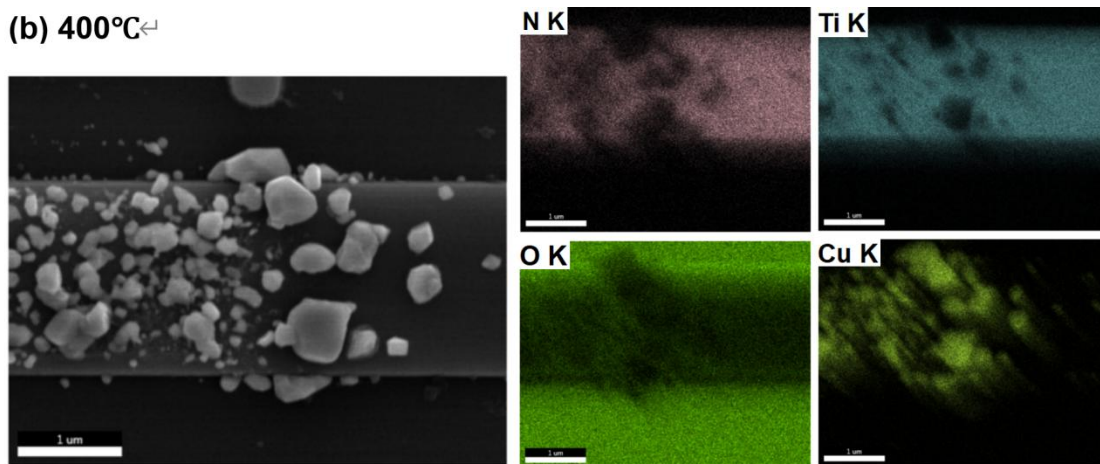


Figure 31. Schematic of dewetting occurred during EM test for samples annealed at 300°C, 400°C and 500°C.

In addition to the formation of isolated particles, particles were also observed on the surface of the TiN layer near the cathode for all samples, as illustrated on the right side of each image in Figure 31. To clarify the mechanism underlying this abnormal phenomenon, EDS was conducted to characterize the composition of these particles, as shown in Figure 32. The EDS results reveal that the particles lying on the TiN surface are composed of Cu, indicating that Cu atoms have migrated from the film to

the substrate. These Cu atoms are likely sourced from the cathode of the Cu film, although a detailed discussion of this is beyond the scope of this work. Moreover, it is observed from all figures, particularly in Figure 36a, that the presence of oxygen in the depletion zone of Cu confirms that oxidation occurred during the measurement process. This observation is significant as it corroborates the hypothesis that oxidation occurs throughout the experimental procedure, likely leading to the formation of an oxide layer between the Cu film and the TiN layer as voids in Cu become significant.





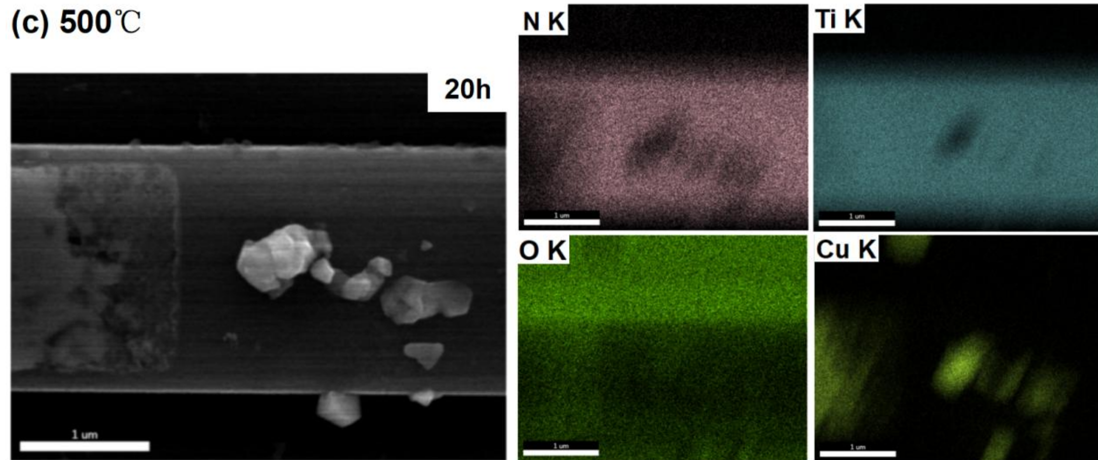


Figure 32. EDS images of particles appeared on the TiN layer and the surrounding elements for samples annealed at (a) 300°C, (b) 400°C and (c) 500°C.

TM is a type of mass migration driven by temperature gradients, as discussed in Section 2.2.2.2. Areas subjected to high current density can generate thermal effects such as Joule heting, which significantly impacts regions where defects form. It has been reported that hot spots are created by the formation of voids due to EM as the current density near the voids increases, which thus generates temperature gradients [57]. At the cathode, the growth of voids resulting from EM can lead to poor adhesion between the Cu film and the TiN layer, resulting in increased resistance in this area. This process gives rise to further temperature gradients due to current density heterogeneity and facilitates additional mass transport via TM.

However, a depletion zone is also observed at the anode, as shown in Figure 33. Voids form at the edge of the anode, and hillocks appear in the bulk region. This anomalous phenomenon was also observed by Nalla et al. [57], who reported that mass transport occurred at both sides of the Cu interconnect and migrated towards the center of the film in a Blech test structure. It was reported that hot spots can be created due to current crowding at the edges of the Cu film, especially where there are corners or tortuous conductors. Hence, temperature gradients are generated between both edges and the middle region of the Cu film, resulting in the observed mass transport from the anode to the central region of the Cu film. Similarly to the cathode, the formation of voids further decreases the adhesion of the interface between the metal film and the

substrate, and inversely increases the current density in the vicinity, accelerating the failure of Cu interconnects. Notably, the mass transport at the cathode was significantly higher than at the anode, which can be attributed to the fact that EM still serves as the predominant mechanism for atom migration. It is reasonable to assume that the coupling effects of EM and TM facilitated atom migration at the cathode, while only TM was operative at the anode.

Interestingly, TM does not appear in the sample annealed at 500℃. Only hillocks were observed at the anode after a 20-hour EM test, suggesting that EM could be the sole mechanism driving mass migration, or that the effect of TM is too weak to be observed. This could be attributed to the more stable microstructure that the sample possesses at this higher annealing temperature. However, distinguishing the extent of TM's influence in samples annealed at 300℃ and 400℃ is challenging. While it is anticipated that annealing improves TM resistance, this remains a topic of debate. The effect of annealing on TM has not been extensively studied, indicating a need for further research in this area to clarify these mechanisms and their interactions.

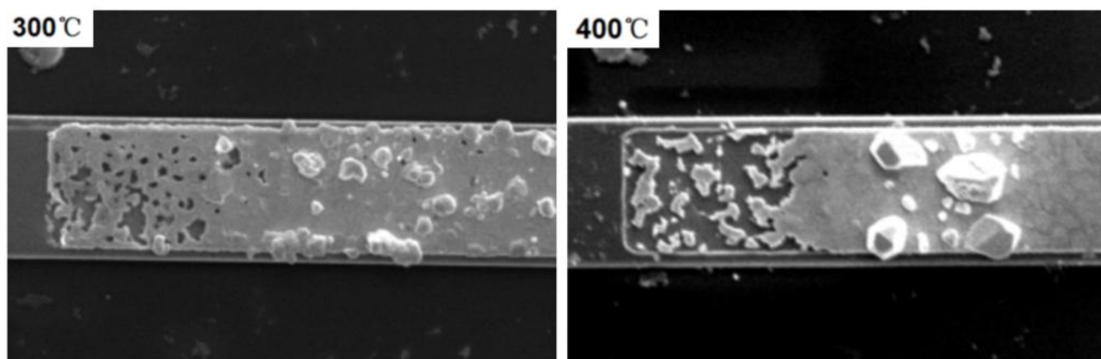


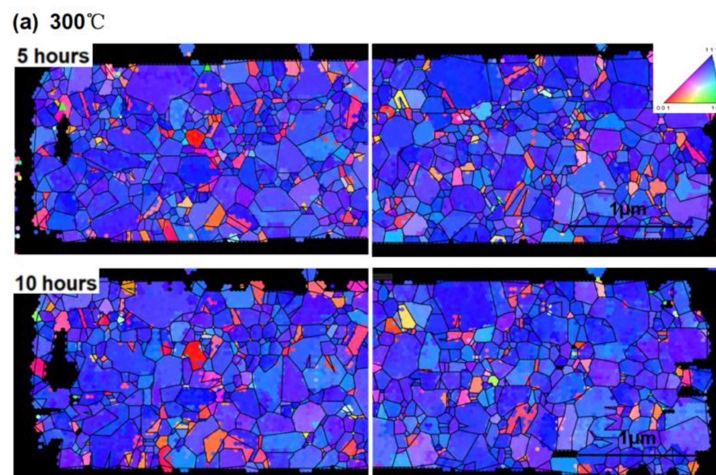
Figure 33. SEM images of thermomigration occurred at the anode as EM test reached 20 hours for samples annealed at 300℃ and 400℃.

Figure 34 presents the inverse pole figure (IPF) and grain images for each sample annealed differently after 5 and 10 hours. Due to fewer voids nucleating in the sample annealed at 500℃, a longer EM test duration of 15 hours was selected to allow more atoms to migrate and reveal variations in the microstructure. The images on the left side represent the anode, while those on the right side represent the cathode. The

black lines represent the reconstructed grain boundaries generated by OIM software, overlapping with the IPF image, and each enclosed region represents a grain. The black area at the anode indicates where the hillocks are located, which cannot be identified by EBSD.

Comparing the IPF and grain images before and after the EM test, it is evident that both grain orientation and grain size exhibit minimal changes during EM at the bulk region. Even after 10 hours, when voids became apparent, the size and orientation of grains that did not migrate remained almost unchanged. Despite the limited area characterized and potential errors in EBSD operation, such as drift, it can be reasonably inferred that the diffusion of atoms does not significantly influence the other grains as they migrate along the stripe.

By examining the locations where voids are generated, it becomes evident that voids tend to initiate at corners of the stripe and regions where small grains cluster. As mentioned previously, corners with large angles likely experience higher current density, known as the current crowding effect, making them more susceptible to EM. In regions where small grains aggregate, the number of triple points significantly increases, providing numerous paths for atoms to diffuse. Moreover, hillocks also seem to be prone to generate at regions with small grains. However, as the annealing temperature increases, the grain size of the Cu interconnect becomes larger. Consequently, the small-grain-induced effect is inferred to be inhibited due to the decrease in diffusion paths available for atoms.



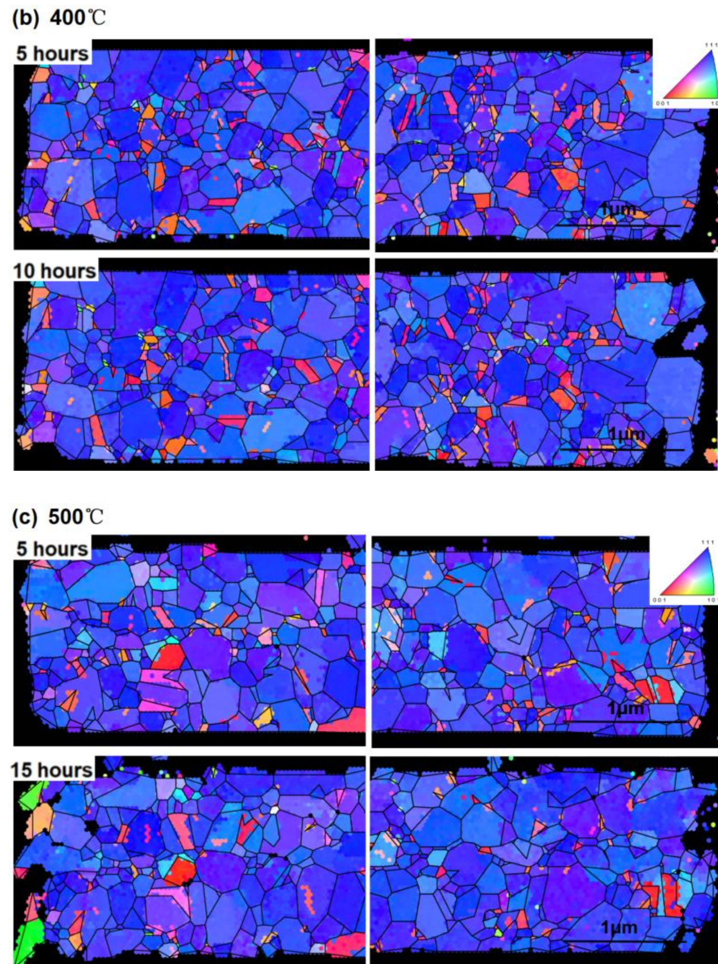


Figure 34. Schematic of inverse pole figures and grain images of samples annealed at (a) 300°C, (b) 400°C and (c) 500°C at different stages of time.

Figure 35 presents the change in grain size distribution before and after the EM test. The average grain size varied only within a small range before and after EM, consistent with the previous observation that grain size exhibit minimal variation during EM. Despite small fluctuations in the average grain size, an overall trend indicates a slight increase as the EM test duration extends. Especially for the sample annealed at 500°C, when the EM test reached 15 hours, the average grain size increased by approximately 0.02μm, which is one order of magnitude larger than that of other two samples. This is likely attributed to the 5-hour longer EM test duration for the sample annealed at 500°C, allowing for slight grain growth due to the continuous application of high temperature.

Additionally, the peak of the largest grain size for each sample increased with longer

EM test duration, indicating grain growth as the EM test progressed. However, this increase is not as pronounced for samples annealed at 300°C and 400°C, which are theoretically more susceptible to high ambient temperatures. Therefore, while recrystallization during the EM test could influence the variation, it does not appear to be the only factor. Given that EM predominantly occurs in regions with small grains, the small grains are depleted while the larger grains, which are in a more stable state, remain unchanged. Consequently, the average grain size could increase slightly. Apart from minor recrystallization and the depletion of small grains, EM appears to cause no significant changes in grains or in the overall grain size distribution.

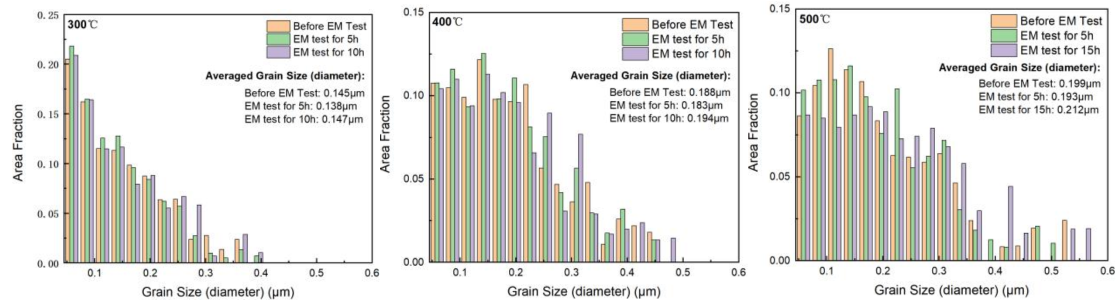


Figure 35. Schematic of grain size distribution of samples annealed at 300°C, 400°C and 500°C at different stages of time.

The variation in misorientation angle distribution for each sample is shown in Figure 36. Overall, the data indicates an increase in the number of small misorientation angles below 5°, while a decrease in the number of twin boundaries following significant EM. This phenomenon suggests that the number of subgrains increased during EM, a trend that is more pronounced in samples annealed at higher temperatures. However, the fraction of grains with moderate misorientation angles does not show significant variation.

Notably, as indicated by the green bar in each figure, only slight changes are observed in the early stages of EM, while significant changes in misorientation angle distribution appear after prolonged EM test duration. This may suggest that misorientation variation could be accelerated at a critical point during the EM test, which needs further investigation in future studies.

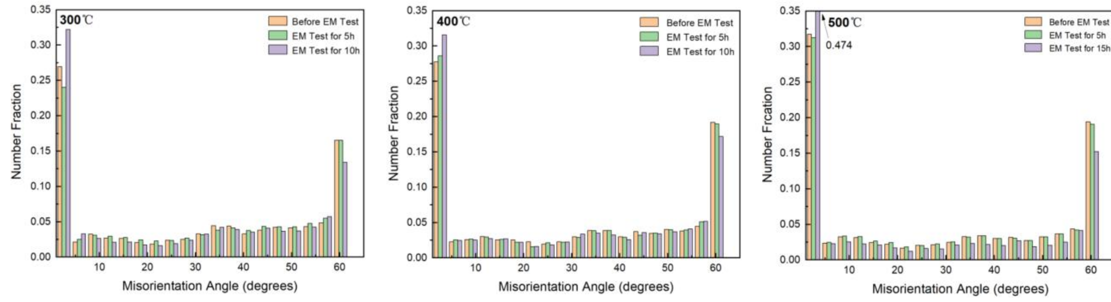


Figure 36. Schematic of misorientation angle distribution of samples annealed at 300°C, 400°C and 500°C at different stages of time.

The boundary angle distribution figures, overlapped with SEM images, are shown in Figure 37. The grain boundary angles are categorized into four groups ranging from 0°to 90°, with each color representing a specific range of angles as indicated at the top of the figure. The black areas highlighted represent voids formed during EM.

It can be observed that, regardless of the annealing temperature, voids consistently appear in regions with high-angle boundaries (HABs), particularly close to the blue lines (30° to 60°). A smaller portion of voids is found near the green lines (60° to 90°), although this range accounts for a very small fraction. As previously indicated, voids tend to form in areas with small grains, but these small grains do not always coincide with HABs as shown in the figures. Additionally, some large grains are even surrounded by HABs. Therefore, despite the tendency for voids to form at HAB sites, there seems to be no clear correlation between grain boundary angle and small-grain-induced EM.

Table 3 presents the length and fraction of HABs and LABs after EM tests conducted for 5 hours, 10 hours, and similarly, 15 hours for the sample annealed at 500°C. The change in the total length of grain boundaries appears irregular at different time stages of the EM process, which could significantly depend on the area characterized by EBSD, as these areas can vary slightly with each measurement. Nevertheless, the overall trend still indicates a decrease in total length as the annealing temperature increases. Notably, as EM progresses, the fraction of HABs for all samples decreases, even becoming smaller than that of LABs for the sample annealed at 500°C. This

suggests that EM leads to a reduction in the fraction of HABs and a corresponding increase in LABs. This phenomenon can be explained by the depletion of grains located at HAB sites, indicating the susceptibility of HAB regions to EM-induced changes.

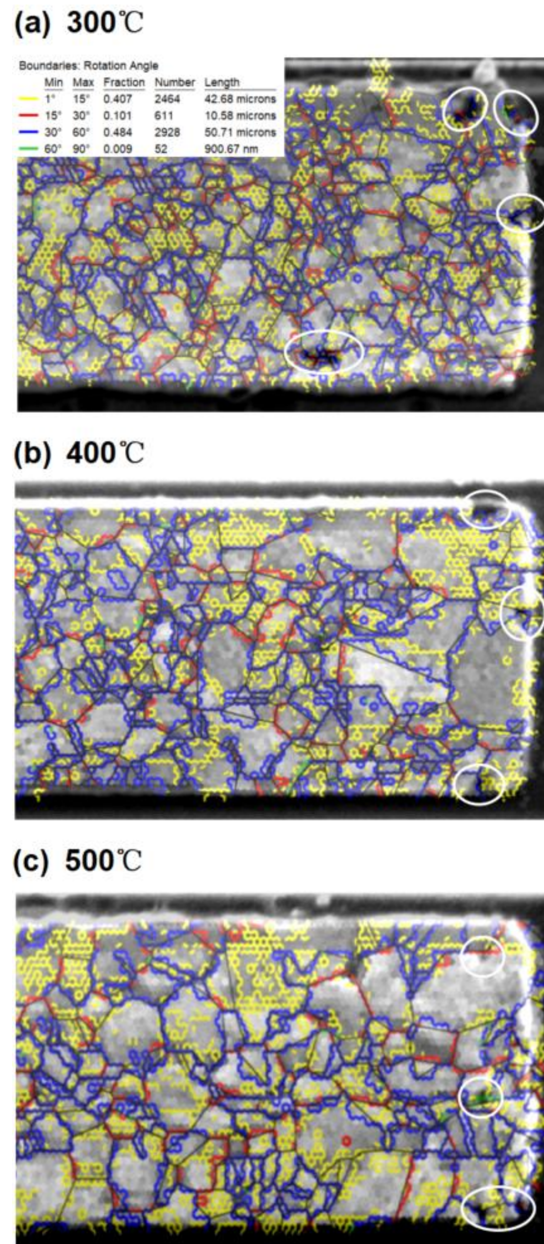


Figure 37. Schematic of grain boundary angle distribution overlapped with SEM images of samples annealed at (a) 300℃, (b) 400℃ and (c) 500℃ at different stages of time.

1st EM	High angle (15 - 180°)		Low angle (1-15°)		Total length
	length (µm)	Fraction	length (µm)	Fraction	length (µm)
300°C	80.002	0.665	40.552	0.335	120.554
400°C	66.848	0.621	40.875	0.379	107.723
500°C	58.1	0.585	41.54	0.415	99.64

2nd EM	High angle (15 - 180°)		Low angle (1-15°)		Total length
	length (µm)	Fraction	length (µm)	Fraction	length (µm)
300°C	86.263	0.589	60.295	0.411	146.558
400°C	62.063	0.599	41.473	0.401	103.536
500°C	45.038	0.445	56.918	0.555	101.956

Table 3. The length and fraction of HAB and LAB after EM test at different time stages for the samples annealed at 300°C, 400°C and 500°C.

Figure 38 presents the Kernel Average Misorientation (KAM) maps overlapped with SEM images and reconstructed grain boundaries for each sample after 10 hours and 20 hours of EM testing. This visualization facilitates understanding the relationship between EM occurrence and defect density. As indicated in the previous section, the KAM shows local misorientation represented by a color gradient. The black areas indicate voids formed on the sample surface, and the black lines represent grain boundaries.

In Figure 38a, the KAM map of the sample annealed at 300°C indicates that small voids not only initiate in regions with tiny grains but also form in areas exhibiting high local misorientation. This is particularly evident in the highlighted area after 10 hours of testing, located downward in the Cu stripe, where red points (indicating maximum local misorientation) are found to be clustered. Notably, it is observed that these red points seem to be strongly associated with tiny grains and consistently

appear near these regions. The EM test at 20 hours further confirms the strong correlation between void formation and local misorientation represented by the KAM value. Although the number of voids increases significantly, they tend to appear in regions near the red and green areas, while the blue areas remain almost unchanged. This suggests that voids are prone to nucleate in regions with high local misorientation, where defects are generally located. This observation implies that, for this sample, EM does not progress in the initially formed voids but rather in other locations with high misorientation.

As the annealing temperature increases to 400°C showing in Figure 38b, the influence of high-misorientation-induced EM appears to diminish. This could result from defect elimination due to the higher annealing temperature. Voids primarily nucleate at the edges with small grains rather than in the bulk region with high local misorientation. However, the blue areas in the figure remain intact, typically indicating regions with large grains possessing strong stability. After 20 hours, the depletion of atoms spreads inward along the Cu stripe, and isolated grains appear on the sample surface. It is noteworthy that these isolated grains align with the positions of the grains in the blue region. Furthermore, the depletion areas coincide well with the black lines representing grain boundaries. This phenomenon suggests that atoms surrounding the grain boundaries are more likely to migrate first, leaving the large grains isolated on the surface.

Figure 38c shows that EM also predominantly occurs at the grain boundaries as the annealing temperature reaches 500°C. After 10 hours of EM testing, only small voids appear, and they are primarily located at triple junctions. As the EM test progresses to 20 hours, more voids nucleate along the grain boundaries, and several granular grains become isolated.

In summary, the KAM analysis illustrates that mass migration is likely to occur in regions with high local misorientation for samples annealed at 300°C. It is reasonable to assume that defects could serve as diffusion paths in samples annealed at lower temperatures, although grain-boundary diffusion still predominates. However, at higher annealing temperatures such as 400°C and 500°C, grain boundaries become the

exclusive diffusion paths due to the reduction in defects.

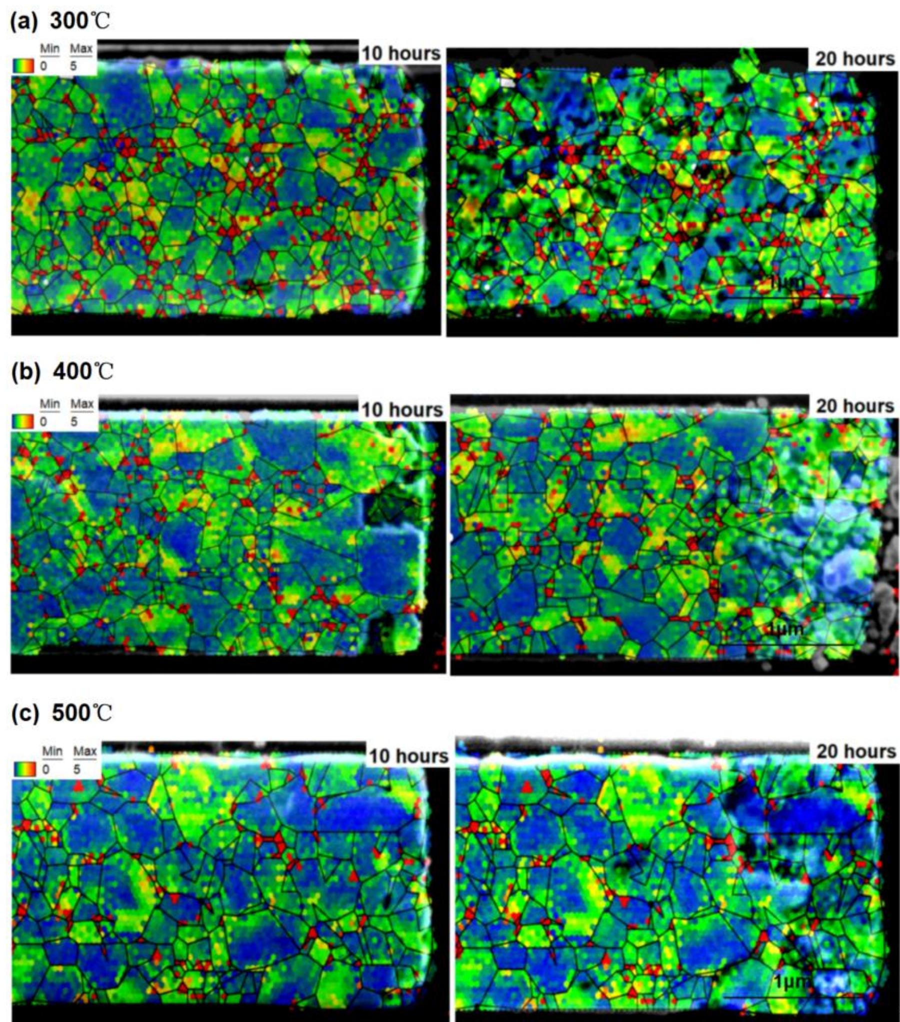


Figure 38. Schematic of KAM maps overlapped with SEM images of samples annealed at (a) 300℃, (b) 400℃ and (c) 500℃ at different time stages.

5.2 Drift Velocity

The atoms in Cu interconnect diffuse from the cathode to the anode, leading to a depletion of atoms at the cathode and, consequently, an accumulation of vacancies. The drift velocity can be defined as the ratio of the drift length to the drift time. The drift length can be approximately determined by the average length of voids appearing within the Cu interconnect.

In this study, the test conditions involve an applied current density of 27mA/m² at a temperature of 250°C. The areas selected for measuring the average length of voids are chosen at the final points where significant EM occurred. These time points are 20 hours for samples annealed at 300°C, 400°C, and 500°C. The comprehensive figures of each Cu line after EM and the measurements of drift length at the cathode are shown in Figure 39.

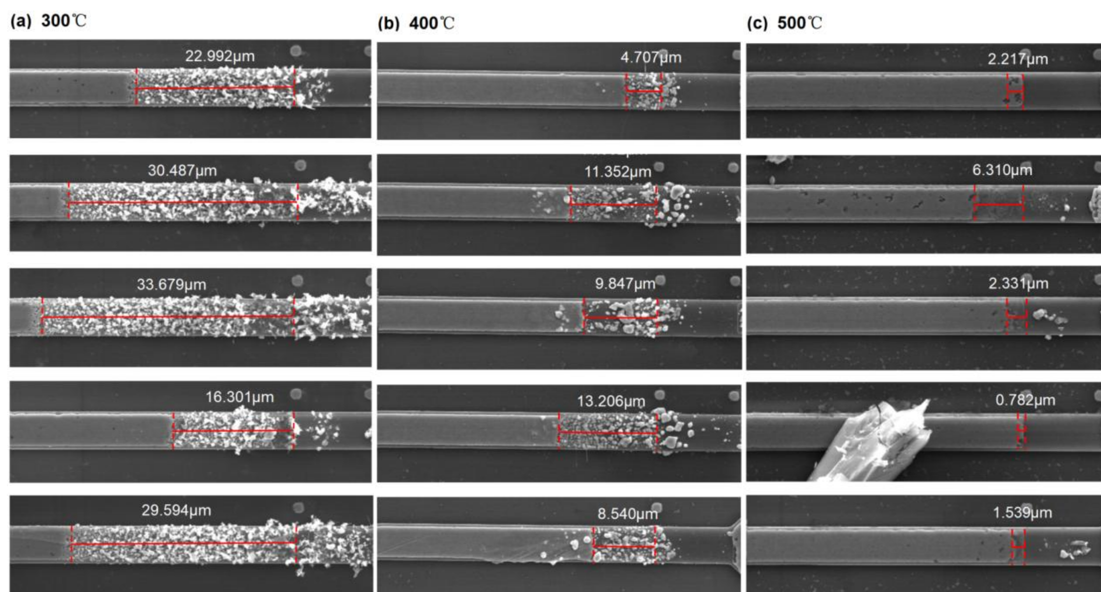


Figure 39. SEM images and drift length of Cu lines at the cathode annealed at (a) 300°C, (b) 400°C and (c) 500°C after 20 hours of EM test.

All the parameters used to calculate the averaged drift velocity are shown in Table 4. Despite the fact that the atoms in the depletion zone after the EM test do not completely migrate and some atoms even migrate in the opposite direction due to the influence of dewetting and thermomigration, the measured length is determined to be

the length from the original edge at the cathode to the region where migration terminates. Therefore, the averaged drift velocities for samples annealed at 300°C, 400°C, and 500°C are calculated to be 1.311μm/h, 0.476μm/h, and 0.132μm/h, respectively, with corresponding standard deviation values of 0.363, 0.161, and 0.107. There are five lines for each annealing temperature, and their average values and standard deviations are shown in Figure 40, demonstrating that higher annealing temperatures result in reduced drift velocities. It can be observed that the trend of drift velocity is not a linear decline with annealing temperature. As the annealing temperature increases, the variation in drift velocity becomes more gradual. However, to draw a definitive conclusion, further tests must be conducted under a wider range of annealing conditions.

Parameter / Temperature	**Drift time (hours)**	**Drift length (μm)**	**Drift velocity (μm/h)**	**Average (μm/h)**
300°C	20h	20.992	1.050	1.311
		30.487	1.524	
		33.679	1.684	
		16.301	0.815	
		29.594	1.480	
400°C		4.707	0.235	0.476
		11.352	0.568	
		9.847	0.492	
		13.206	0.660	
		8.540	0.427	
500°C		2.217	0.111	0.132
		6.310	0.316	
		2.331	0.117	
		0.782	0.039	
		1.539	0.077	

Table 4. Parameters for calculating the averaged drift velocity for samples annealed at 300℃, 400℃ and 500℃.

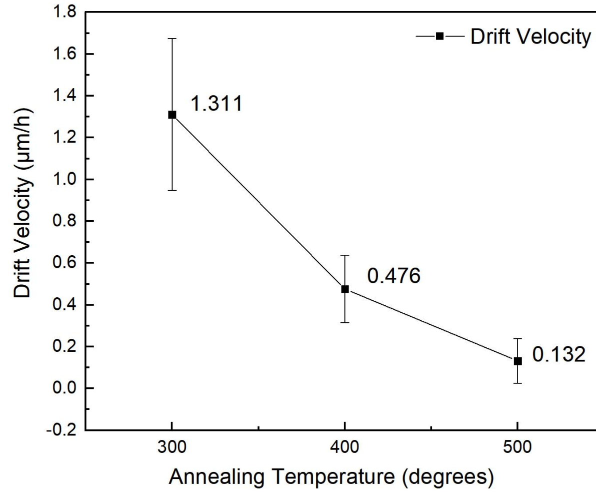


Figure 40. Schematic of variation of drift velocity for samples annealed at 300℃, 400℃ and 500℃.

In summary, Chapter 5 reveals the microstructural variations observed after the EM test. The findings indicate that the formation of voids and hillocks is suppressed as the annealing temperature increases. This suppression is quantified by the drift velocities of samples annealed at different annealing temperatures. Notably, grain orientation and grain size exhibit no significant change post-EM test. However, an increase in the fraction of small misorientation angles was observed, as voids tend to form at HAB sites, thereby reducing the number of HABs and increasing the number of LABs. Additionally, voids were found to preferentially initiate in regions with smaller grains, which feature more grain boundaries and triple junctions, and in areas with high KAM values. This suggests that grain boundaries and defects serve as effective diffusion paths for atom migration during EM process.

6. Conclusion and Recommendations

6.1 Conclusion

This study primarily focuses on the effect of different annealing temperatures on the microstructure of Cu interconnects and the resulting impact on their resistivity, as well as how microstructural variations influence electromigration (EM) performance. Additionally, attempts to form nanotwins in Cu through pulse electrodeposition are briefly introduced.

The sputtered Cu samples were annealed at 300°C, 400°C, 500°C, 600°C, and 700°C. Due to severe defects in the sample annealed at 600°C, it was not possible to characterize it using electron backscatter diffraction (EBSD), and thus it is excluded from this discussion. Various microstructural factors, including grain orientations, grain size and distribution, grain boundaries, misorientation angles, and KAM, were compared. For all annealed samples, the predominant texture was (111). With increasing annealing temperature, the Cu film exhibited a slightly stronger (111) texture. Furthermore, the grain size and uniformity of grain distribution both increased with annealing temperature. The average grain sizes for samples annealed at 300°C, 400°C, 500°C, and 700°C were measured to be 0.145μm, 0.188μm, 0.199μm, and 0.246μm, respectively.

As annealing promotes grain growth, the length of grain boundaries decreases. Besides the reduction in both numbers of high angle boundaries (HABs) and low angle boundaries (LABs), the fraction of HABs decreased while LABs increased, indicating enhanced microstructural stability. Notably, the fraction of twin boundaries increased with annealing temperature, which is typically regarded as beneficial for resisting EM. From the perspective of the dislocation-related parameter KAM, higher values of KAM were always found in samples annealed at lower temperatures, suggesting that defects and strain diminish with increasing annealing temperature. As the grain boundaries decrease, electron scattering and reflection at these boundaries also decrease, thereby reducing the resistivity of the Cu films.

Several settings for pulse electrodeposition were attempted to form Cu nanotwins. Cu films were formed with on-times of 0.2s, 0.4s, 0.6s, 0.8s, and 1s, with a fixed off-time of 0.04s. Cu was only plated on the wafer when the on-time reached 0.6s. Compared to sputtered Cu, the surface of the electroplated sample was too rough for EBSD characterization. As the on-time increased from 0.6s to 1s, the thickness of the Cu film also increased. Unfortunately, FIB images of the cross-sections of these electroplated Cu samples did not show nanotwinned features. The FIB cross-sections of the electroplated samples could be characterized by EBSD due to their sufficient smoothness; however, this was not pursued due to time constraints.

EM tests were carried out on samples annealed at 300°C, 400°C, and 500°C, while the sample annealed at 700°C was excluded because of severe dewetting at the contact pads which led to a loss of conductivity in the Cu line. It was observed that the rate of void formation caused by EM decreased with increasing annealing temperature. This was characterized by the drift velocity, with the results showing that drift velocity decreases with increasing annealing temperature, with values of 1.311μm/h, 0.476μm/h, and 0.132μm/h for each sample, respectively. This result aligns with previous reports indicating that annealing enhances EM resistance. As EM progressed, voids tended to form at corners of the Cu line and regions where small grains gathered due to current crowding effects and the large number of triple points. After the migration of atoms, the grain orientation of Cu films remained almost unchanged. However, the average grain size slightly increased, possibly due to grain growth from continuous exposure to elevated temperature, with smaller grains migrating before larger, more stable grains.

Additionally, analysis with OIM software showed that the fraction of HABs appeared to decrease while LABs increased. Although statistical errors might arise from the reduced characterized area as more voids formed, it can be confirmed that EM is prone to initiate around HAB sites. By overlaying grain boundary angle distribution figures with SEM images, voids were found to form at grains surrounded by HABs. Similarly, void formation occurred in regions with high KAM, coinciding with the fact that defects such as dislocations are more likely to be located in regions with

HABs and high local misorientation.

Notably, several voids initiated near regions with high KAM values in the sample annealed at 300°C, whereas EM in samples annealed at 400°C and 500°C primarily started from the edges of the Cu line and small grains. With prolonged EM test duration, atoms surrounding grain boundaries were observed to migrate, particularly in samples annealed at higher temperatures. This illustrates that defects can serve as diffusion paths in samples annealed at lower temperatures, while at higher annealing temperatures, grain boundaries become the dominant diffusion paths due to the reduction in defects.

When EM duration is excessively long, thermomigration and dewetting also occur, manifesting as voids at the anode and isolated Cu particles adhering to the TiN layer, which was not observed in samples annealed at 500°C. Dewetting is prone to occur at high-energy grain boundaries such as HABs, leading to void formation around these boundaries. This further supports the observation that EM is likely to occur at grain boundaries, particularly HABs.

6.2 Recommendations and Future Work

Due to time constraints, certain limitations in this study remain unresolved. Below, several key points are outlined for future research, which could provide a deeper insight into how the microstructure affects EM performance.

6.2.1 Exploration of Additional Annealing Parameters

The samples annealed at 600°C and 700°C were damaged due to excessive temperature. Future studies should explore more moderate temperature increments, such as 50°C, to investigate more continuous variations in the microstructure. Additionally, the impact of annealing duration on Cu microstructure should be examined, as the current study used a fixed annealing time for each sample.

6.2.2 Further Investigation of Electrodeposition

Given that the electrodeposition is conducted, further exploration of electrodeposition is necessary due to the significant differences in microstructure between electrodeposited Cu and sputtered Cu. Experimentation with various combinations of on-time and off-time (i.e., duty cycle) may facilitate the formation of Cu nanotwins. It is also worthwhile to attempt the direct current method, which has been reported to fabricate such structures. Although FIB imaging did not reveal nanotwinned structures, characterization using EBSD could determine if changes in microstructure occur as on-time varies.

6.2.3 Utilization of In-Situ SEM

In-situ Scanning Electron Microscopy (SEM) can be employed to monitor atomic migration and microstructural changes in real-time during electromigration tests. The results indicated significant variations due to different factors, including electromigration, dewetting, and thermomigration. However, the mechanisms behind these phenomena were only briefly interpreted. In-situ SEM, which can operate under conditions of high temperature and high current, would enable detailed observation and imaging of these variations during EM tests, thereby facilitating a more comprehensive understanding of each phenomenon's mechanism.

Based on the reviewed literature, various approaches can be used to modify the microstructure of Cu films. These include using different deposition techniques (such as electrodeposition, chemical vapor deposition, and other physical vapor deposition methods besides sputtering), altering the length and thickness of the Cu film. Future research should explore these and other methods to further understand and manipulate the microstructure of Cu interconnects.

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My incredible three-year journey at TU Delft has come to a close with the completion of this thesis. Originally a student of Materials Science and Engineering, I have acquired a wealth of knowledge and developed numerous skills in the microelectronics field within the ECTM group, equipping me to make meaningful contributions in my future career. I am forever grateful to TU Delft and to all those who have played an essential role in shaping the person I have become.

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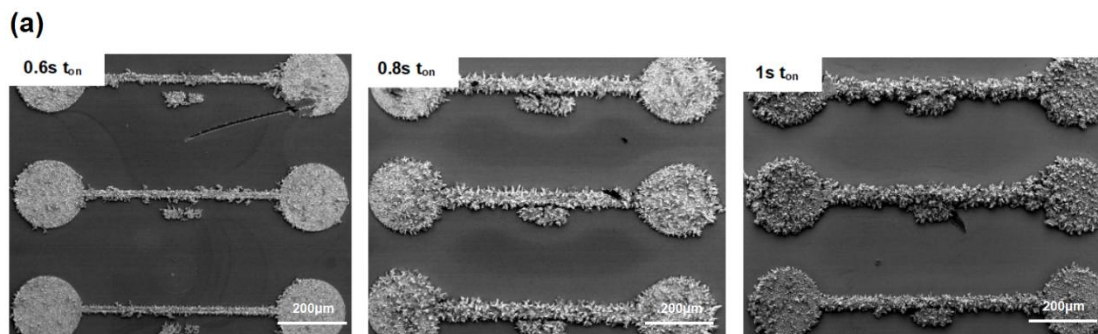
Appendix A

This section presents the results of Cu deposition achieved via pulse electrodeposition (PED). The applied voltage during the on-time (t_{on}) was set at 0.4 V, with ton ranging from 0.2s to 1s in increments of 0.2s. The off-time (t_{off}) was fixed at 0.04s. It was observed that at t_{on}=0.2s and 0.4s, the electrolyte completely etched the sample surface, making these conditions unsuitable for further analysis. This indicates that the critical t_{on} for effective Cu deposition is between 0.4s and 0.6s.

Figure A1a illustrates the surface morphology of the electroplated samples at t_{on} equals 0.6s, 0.8s, and 1s. A substantial presence of single-crystal-like Cu formations was observed on the surface, with growth characterized by significant irregularity and heterogeneity, resulting in a highly rough surface that is unsuitable for EBSD characterization.

The side views of the Cu lines, depicted in Figure A1b, reveal that the electroplated Cu exhibits the thinnest thickness at t_{on}=0.6s. As t_{on} increases to 0.8s, the Cu growth becomes thicker. When t_{on} reaches 1s, the thickness increases slightly but without significant variation. Due to the roughness of the Cu edges produced by PED, precise thickness measurements are challenging. However, the overall trend indicates an increase in thickness with longer t_{on}, which is consistent with the expectation that longer electroplating time results in more Cu deposition.

Figure A1c presents the measured particle sizes of several Cu grains on the surface of each sample. The data indicate that the sizes of Cu particles increase with t_{on}, suggesting that Cu particles tend to grow larger with extended t_{on}.



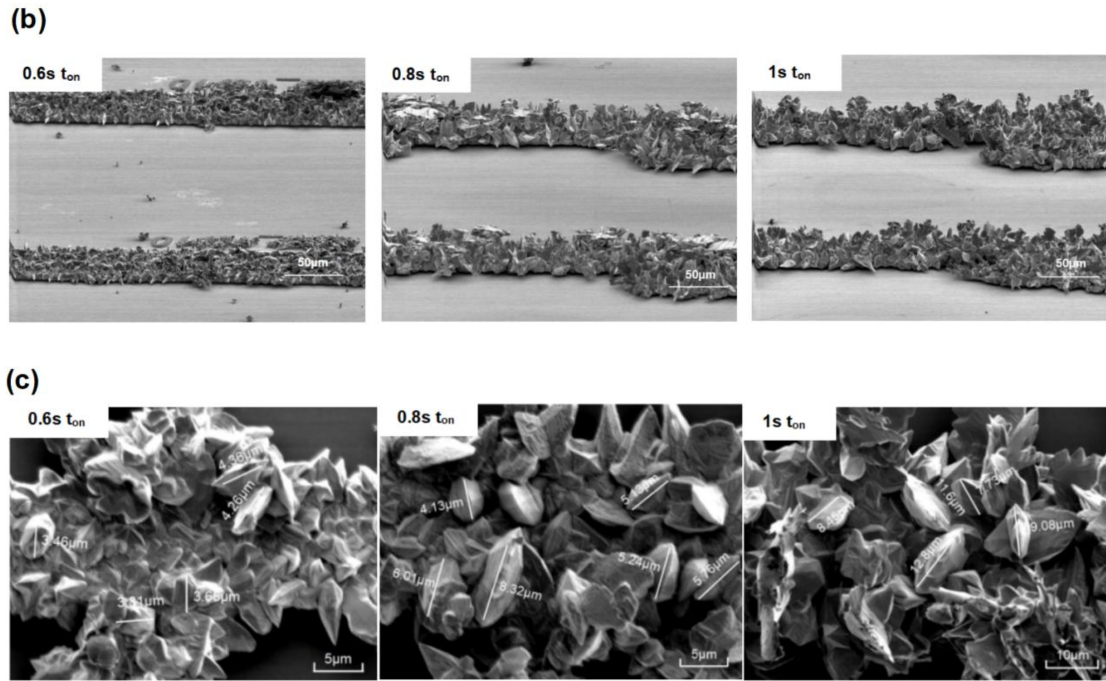


Figure A1. SEM images of (a) top view, (b) side view of electroplated Cu when t_{on} is 0.6s, 0.8s and 1s.

The cross-sectional focused ion beam (FIB) scanning ion images for each sample are presented in Figure A2. These images reveal that the grains at the bottom of the samples are smaller and exhibit more irregular shapes compared to those at the top. Notably, the anticipated nanotwinned features, such as columnar grains and the step-and-terrace structures, are absent in these samples.

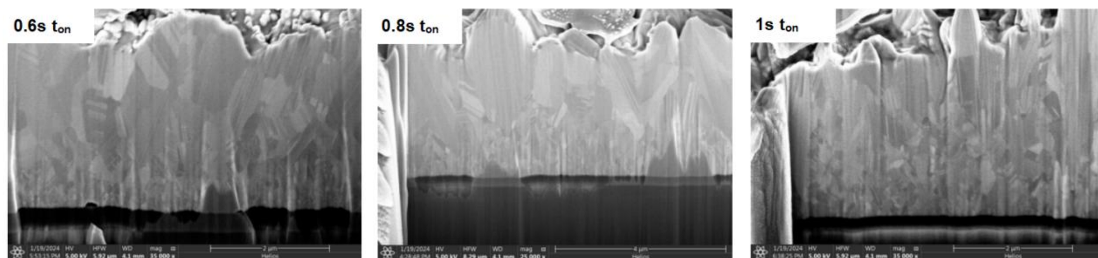
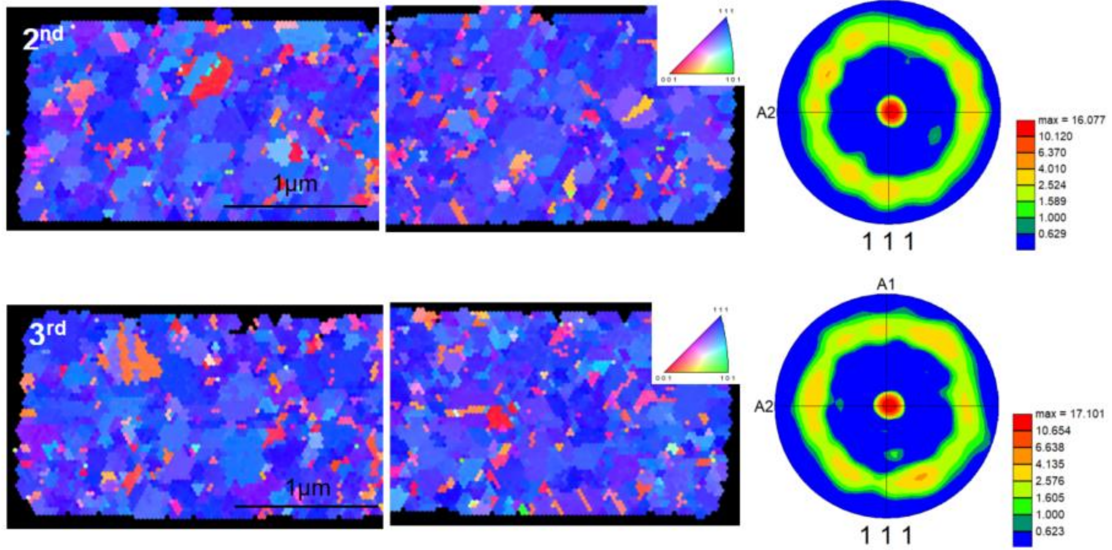


Figure A2. FIB images of electroplated Cu when t_{on} is 0.6s, 0.8s and 1s.

Appendix B

300℃



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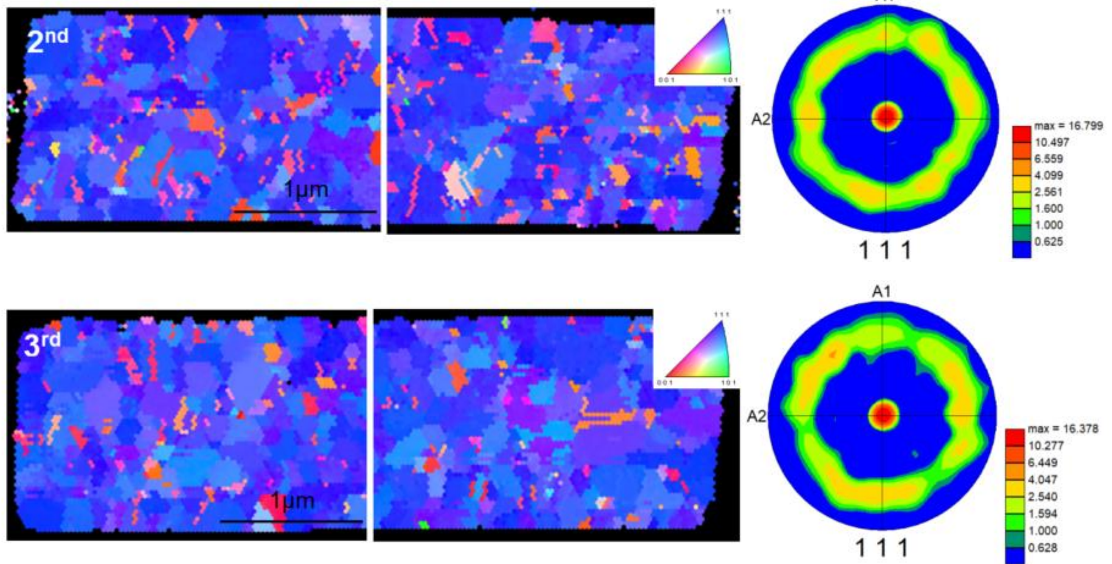
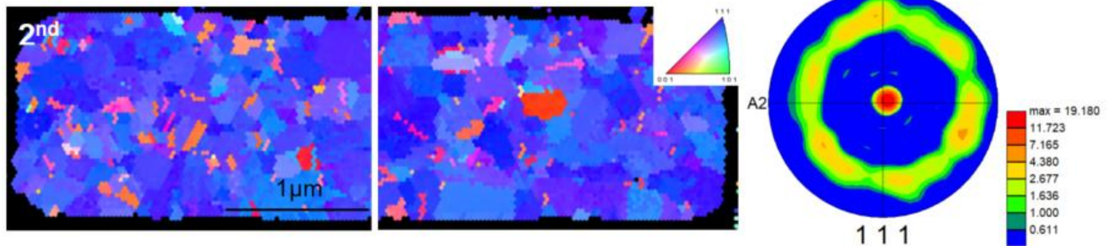


500℃



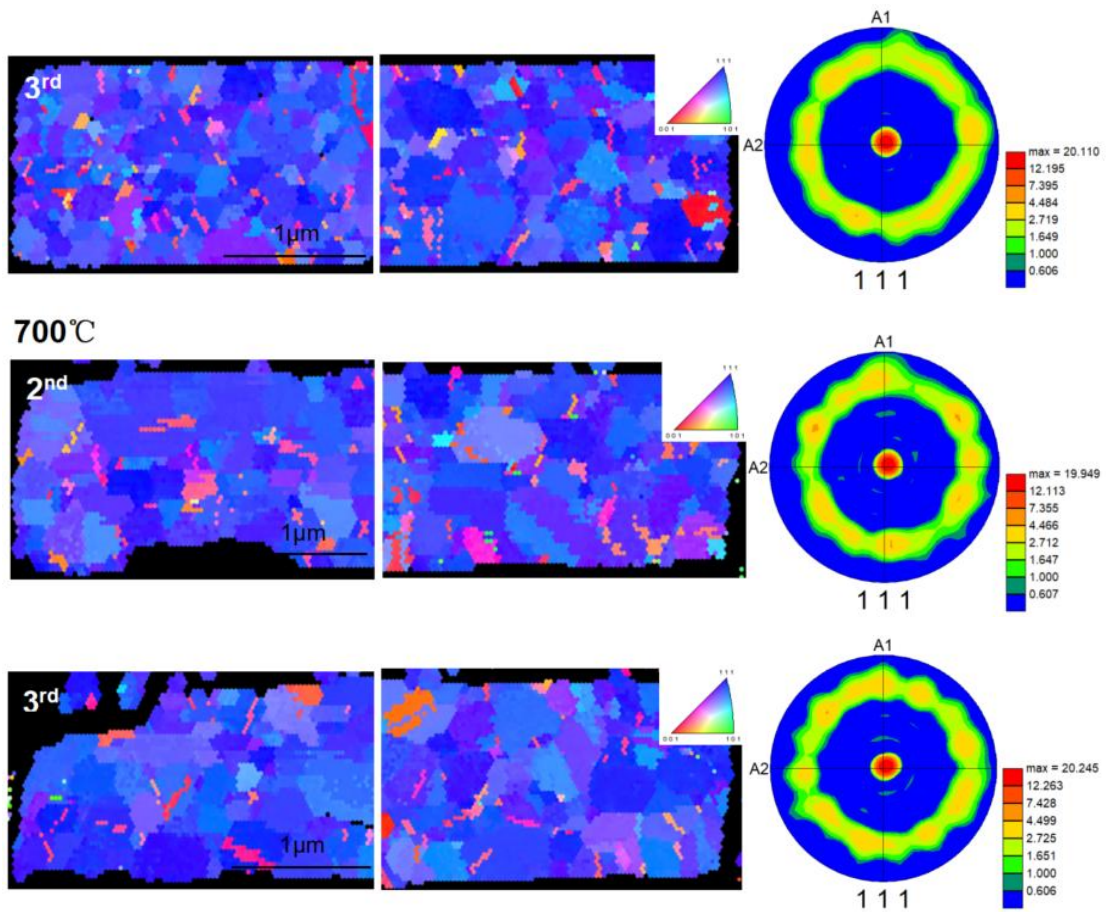
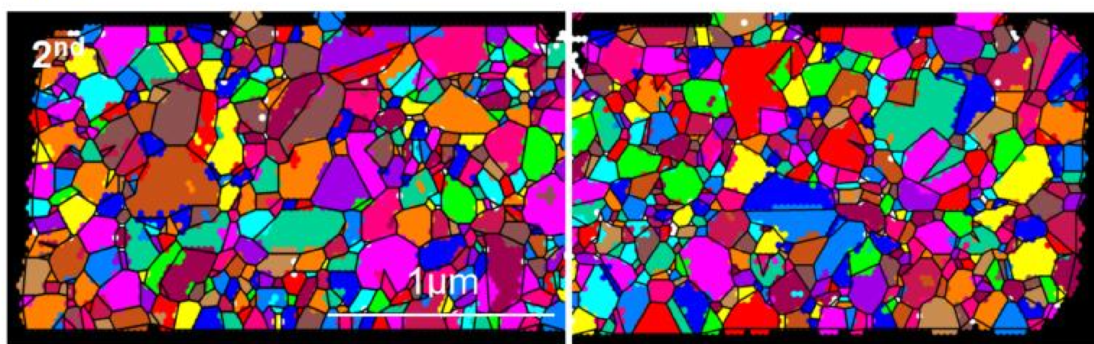
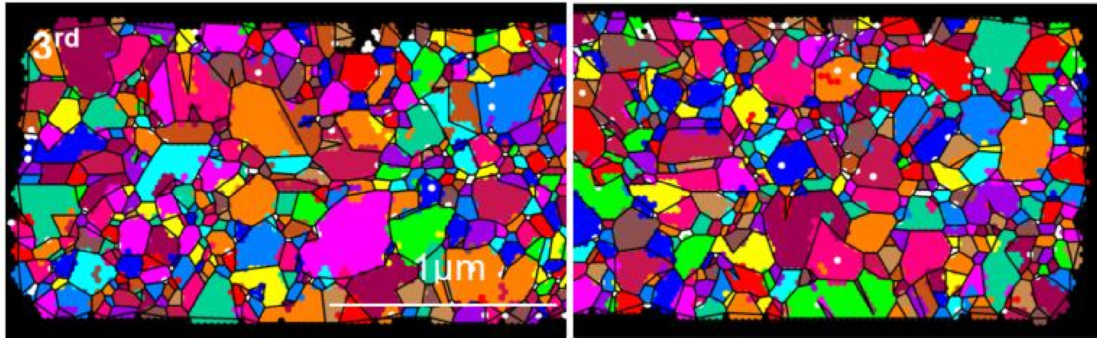


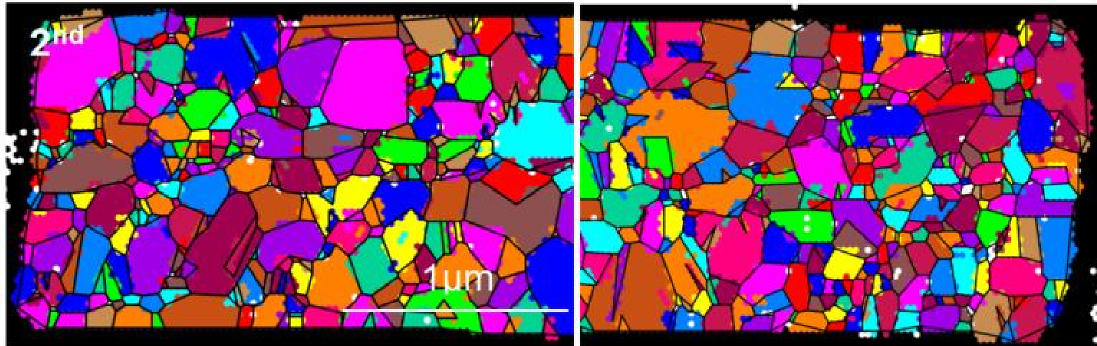
Figure B1. Schematic of inverse pole figures (IPF) for the two additional samples annealed at 300℃, 400℃, 500℃ and 700℃.

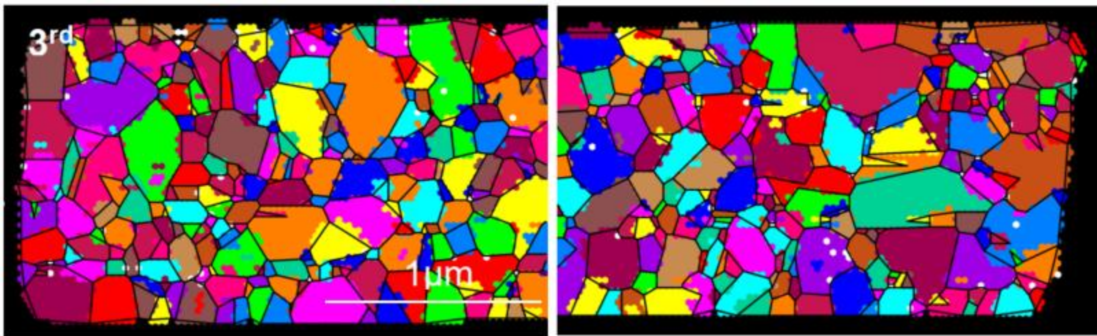
300℃



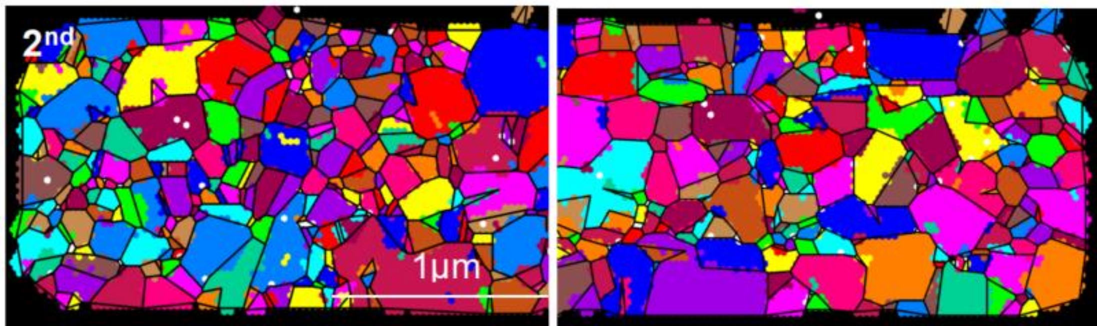


400℃





500℃



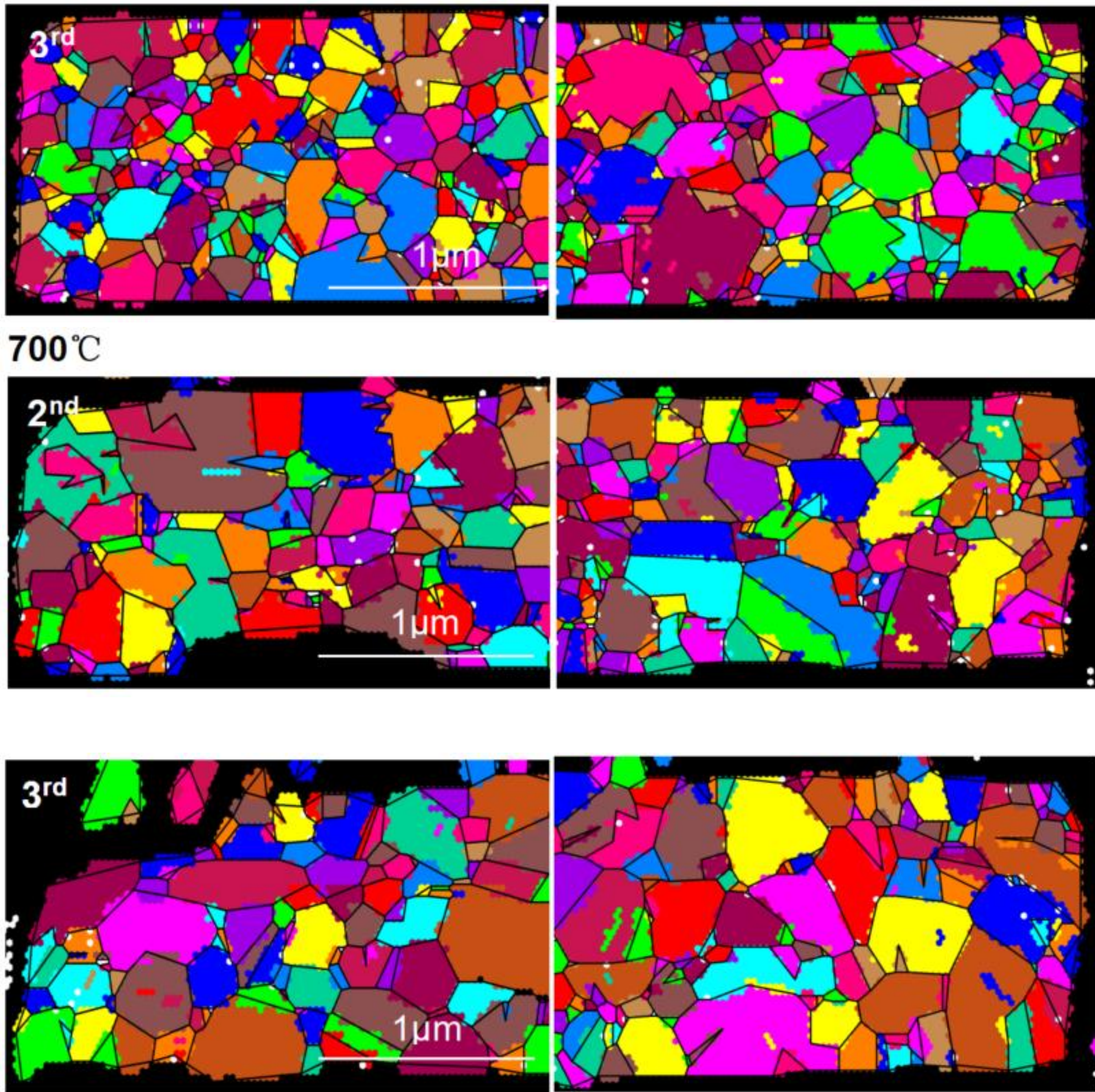
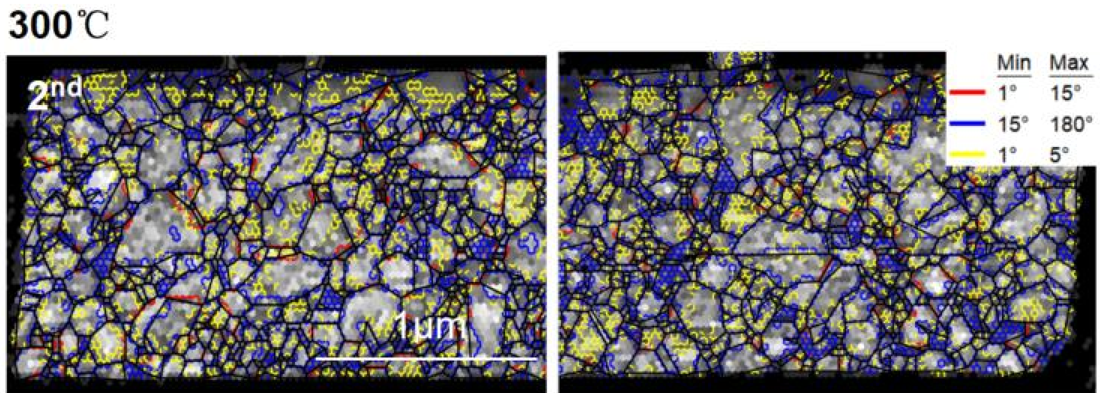
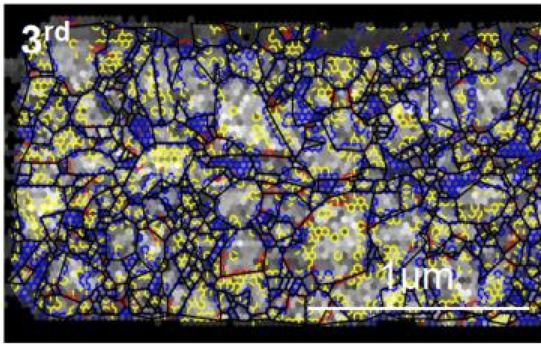
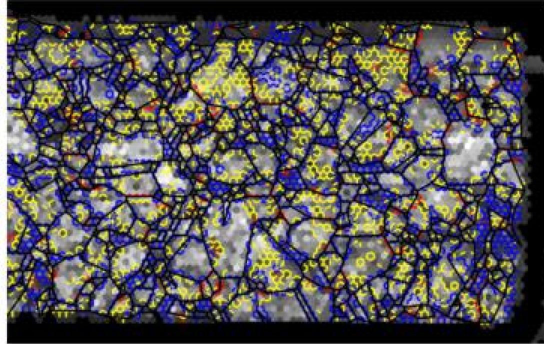


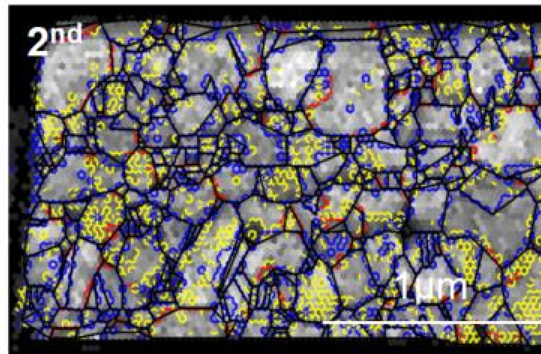
Figure B2. Schematic of grain mappings for the two additional samples annealed at 300℃, 400℃, 500℃ and 700℃.

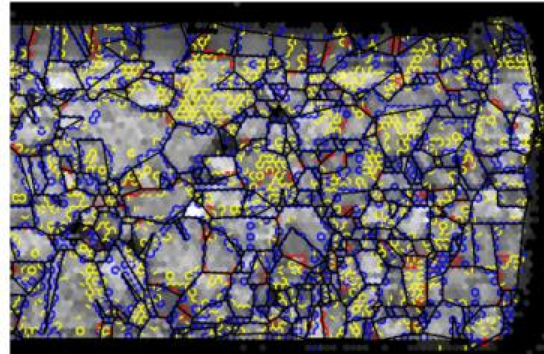


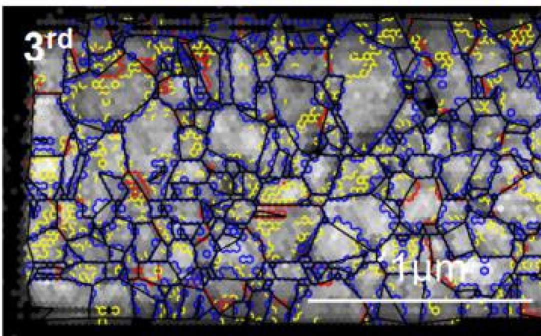


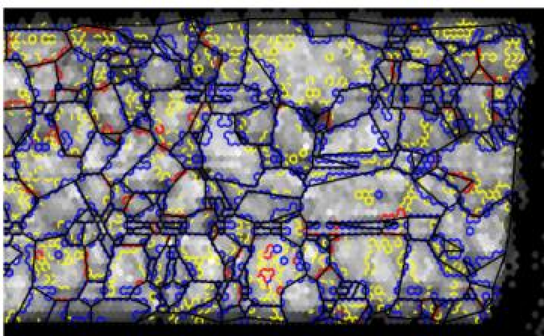


400℃









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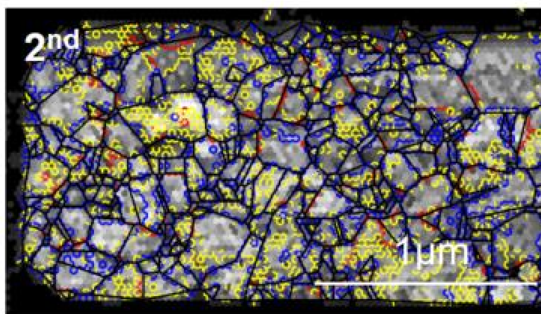
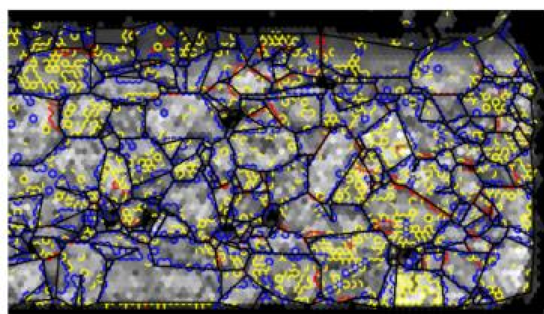
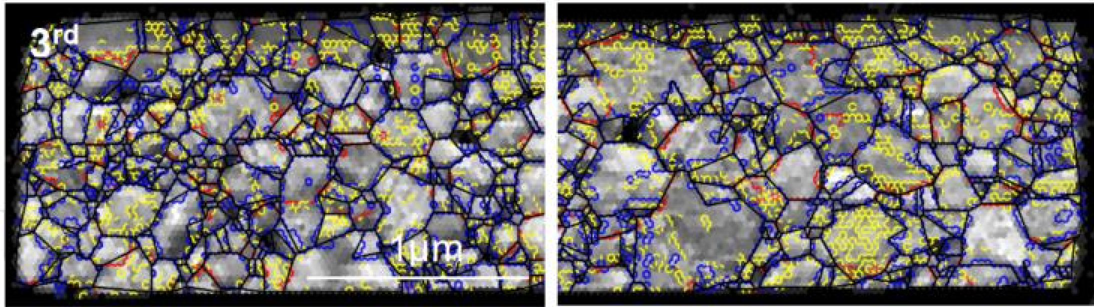
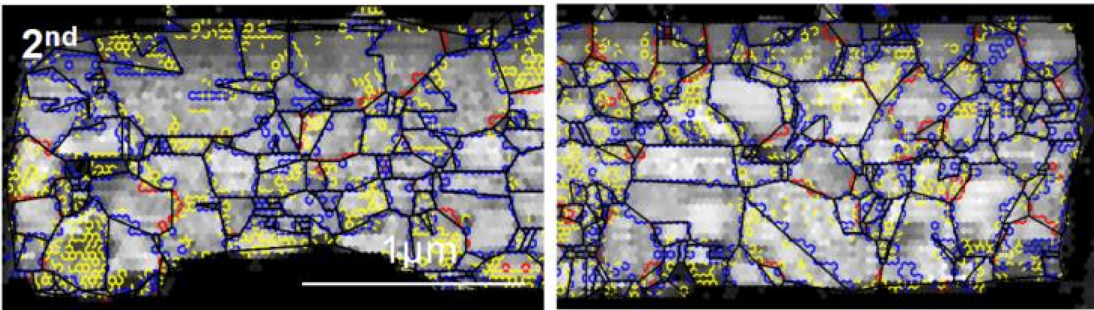






700℃



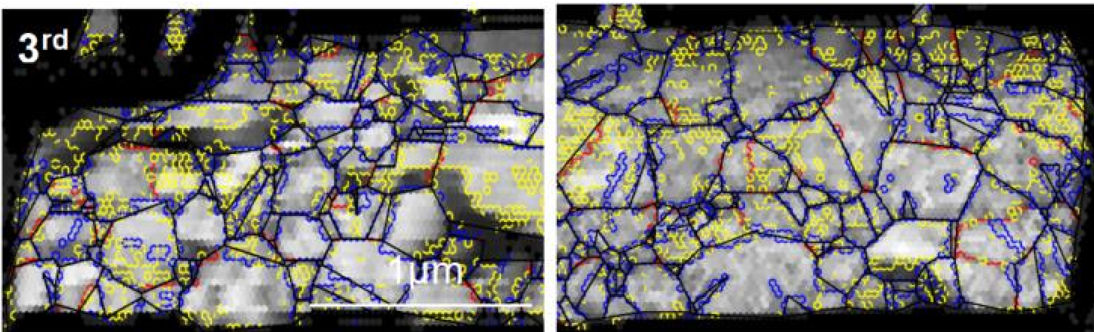
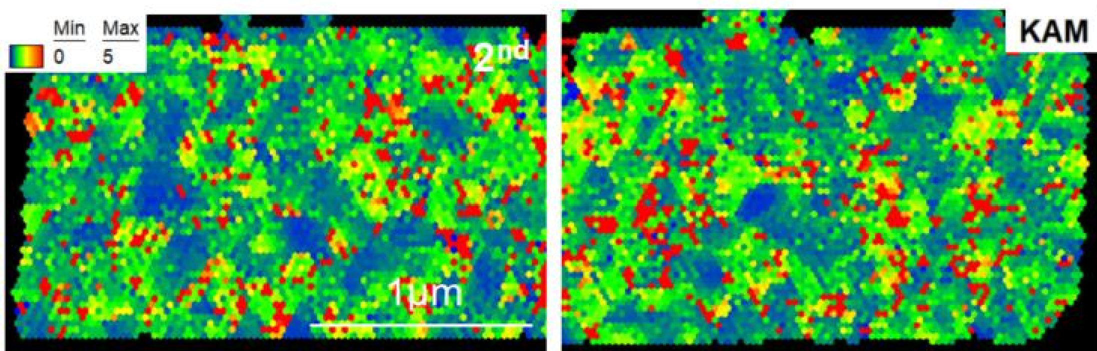
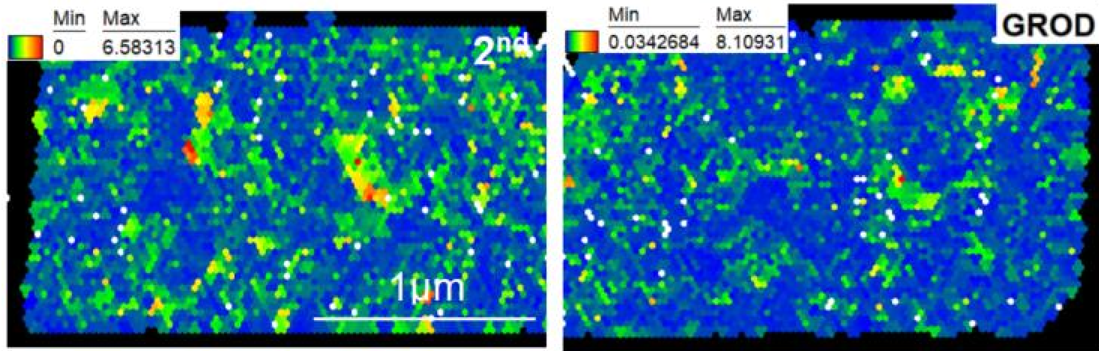
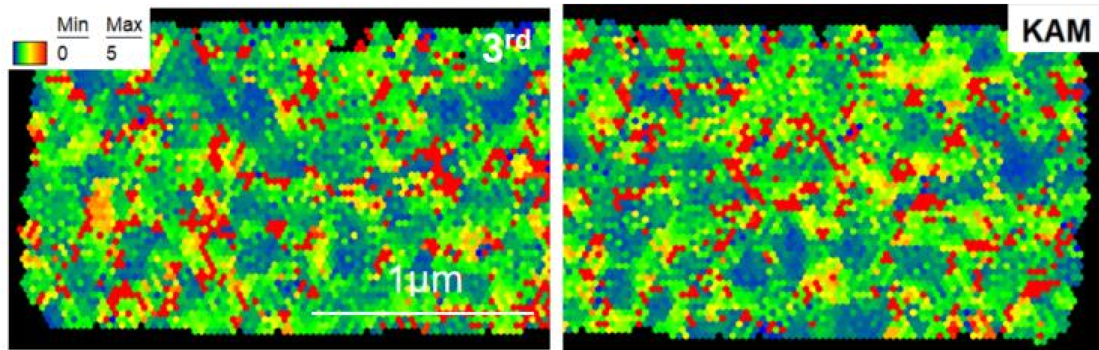


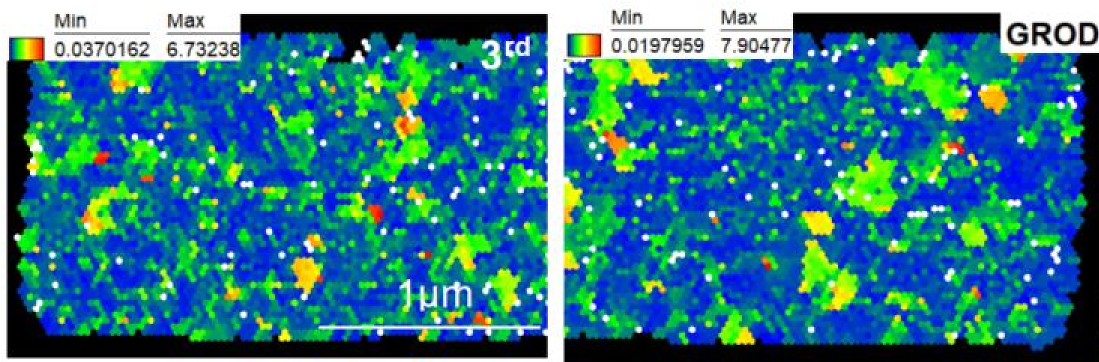
Figure B3. Schematic of the ratio of high angle boundaries (HABs) to low angle boundaries (LABs) for the two additional samples annealed at 300°C, 400°C, 500°C, and 700°C.

300℃

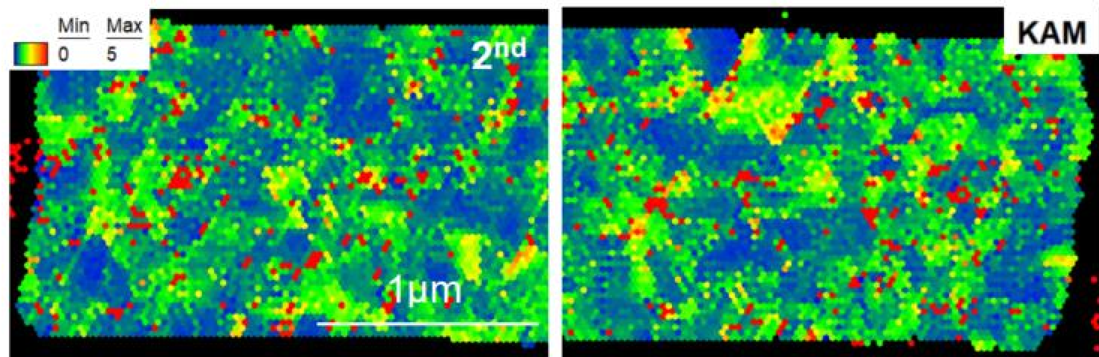


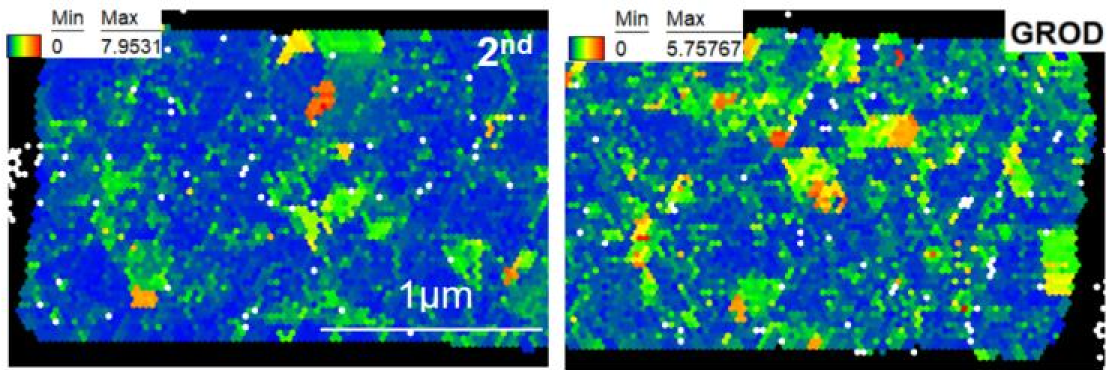


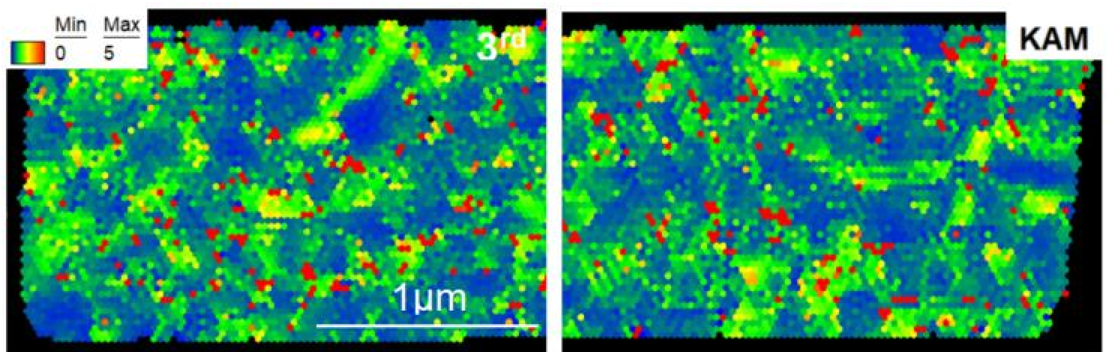


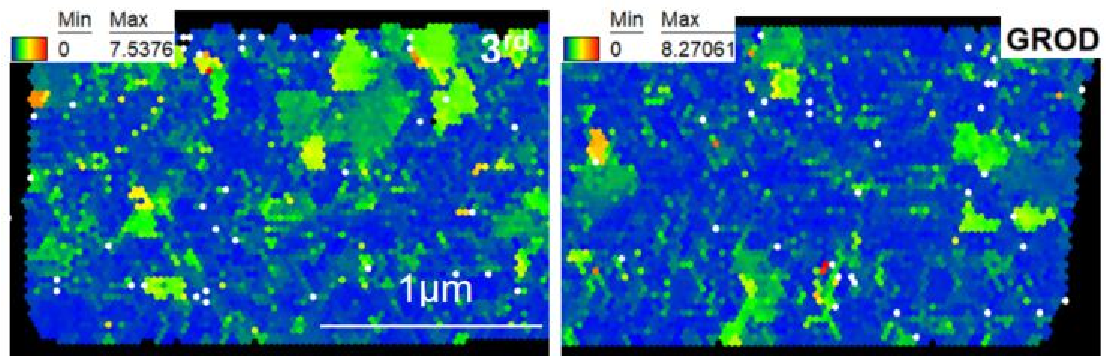


400℃

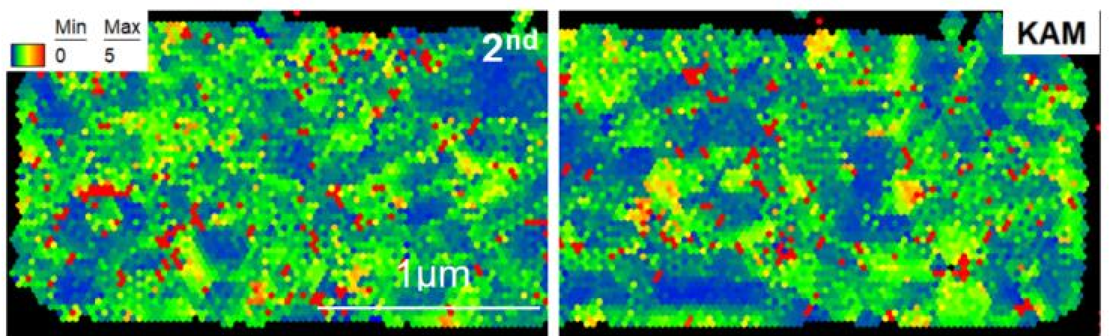


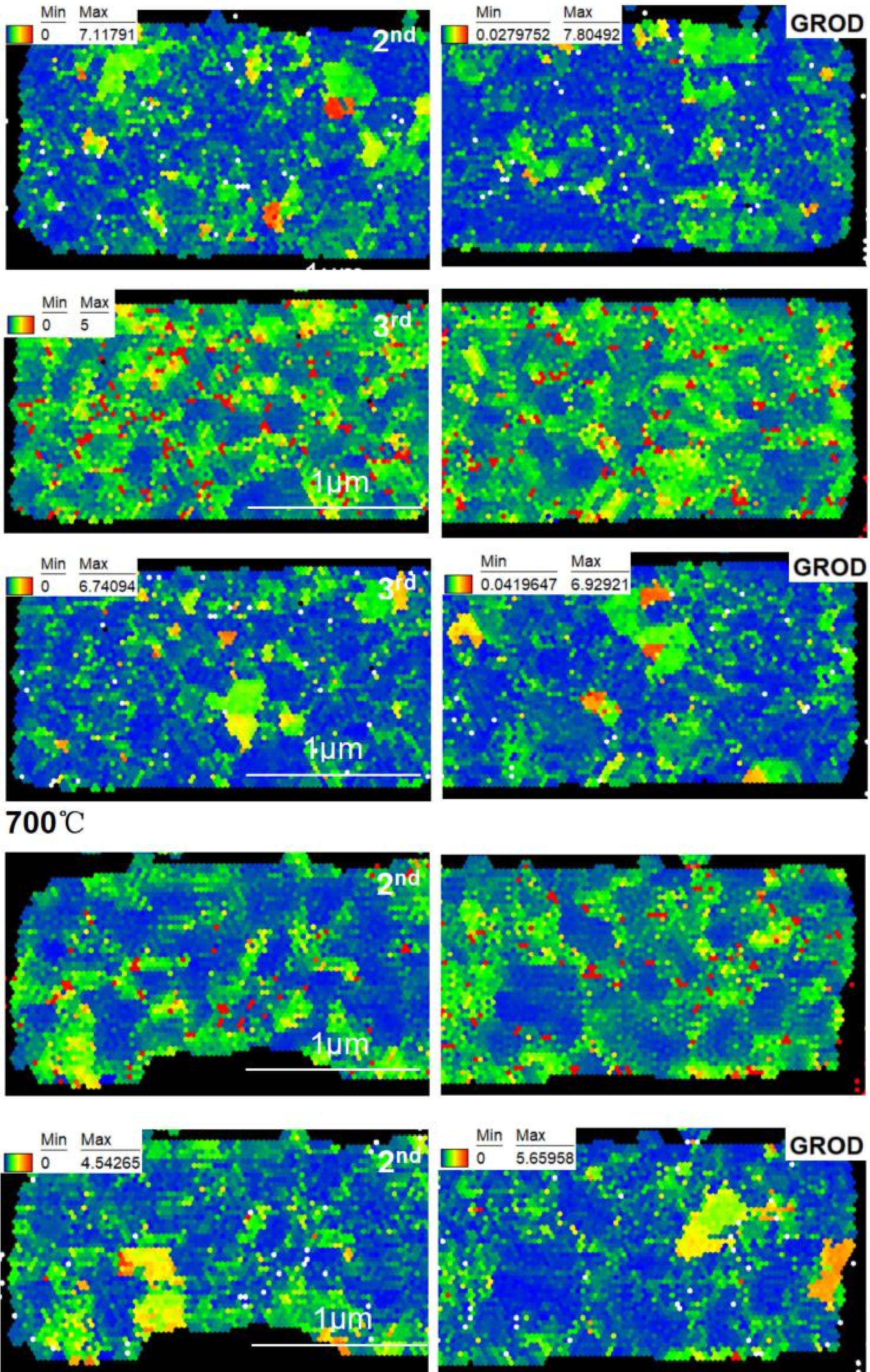






500℃





Min Max
0 7.11791
2nd
Min Max
0.0279752 7.80492
GROD
Min Max
0 5
3rd
1μm
Min Max
0 6.74094
3rd
1μm
Min Max
0.0419647 6.92921
GROD
700℃
2nd
1μm
Min Max
0 4.54265
2nd
1μm
Min Max
0 5.65958
GROD

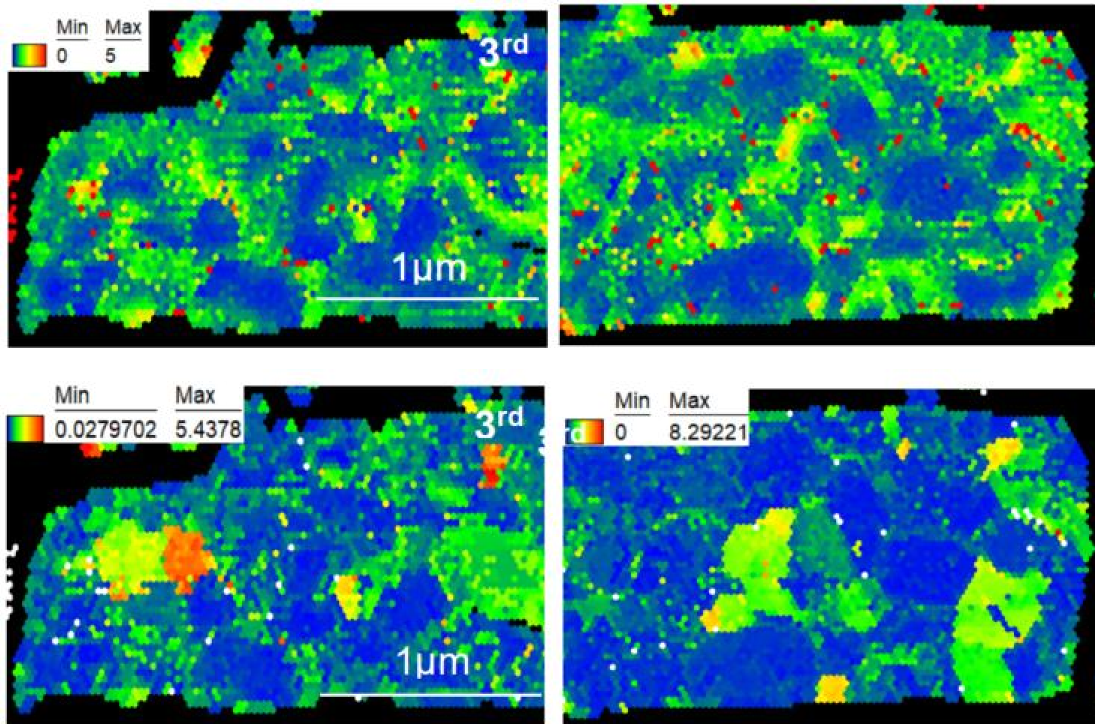
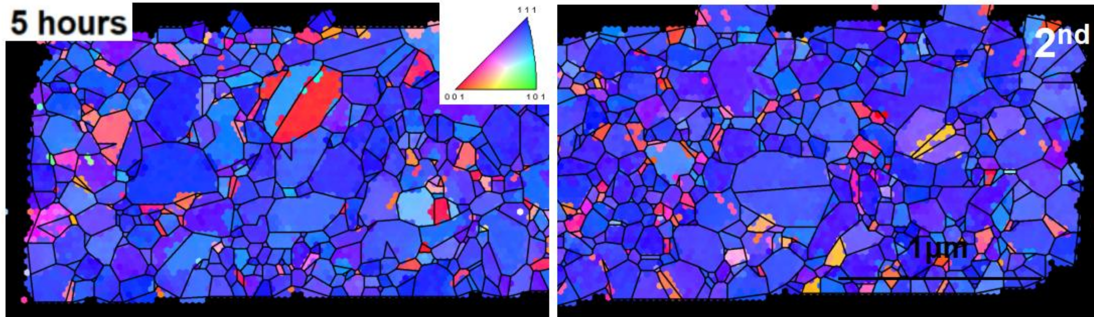
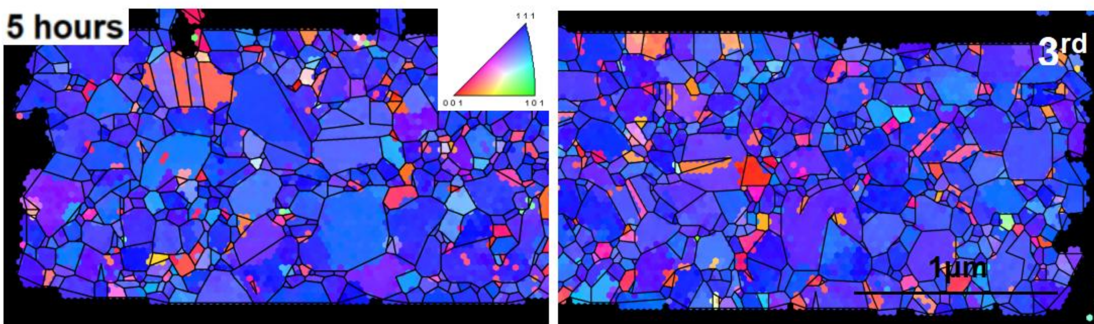


Figure B4. Schematic of Kernel Average Misorientation (KAM) image and Grain Reference Orientation Deviation (GROD) for the two additional samples annealed at 300℃, 400℃, 500℃ and 700℃.

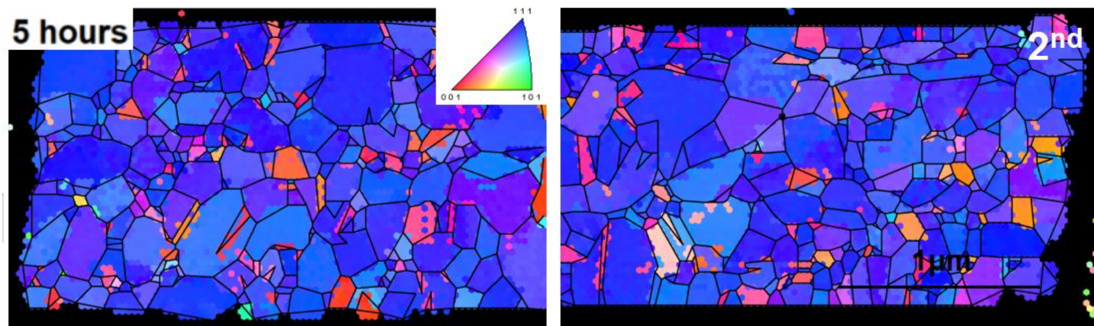
Appendix C

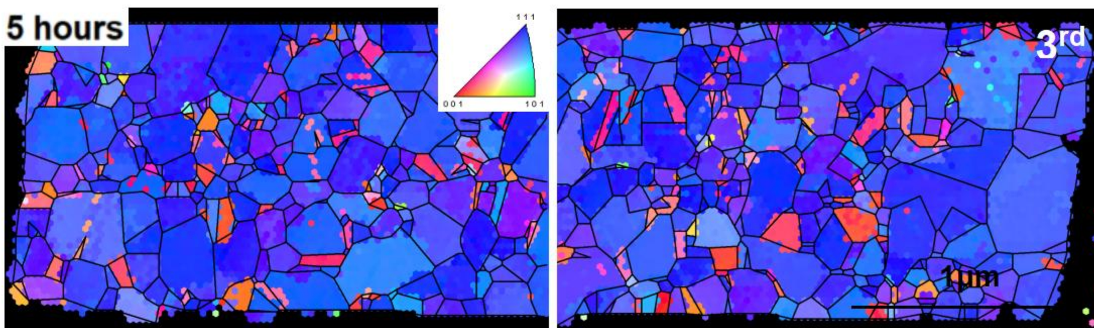
300℃





400℃





500℃

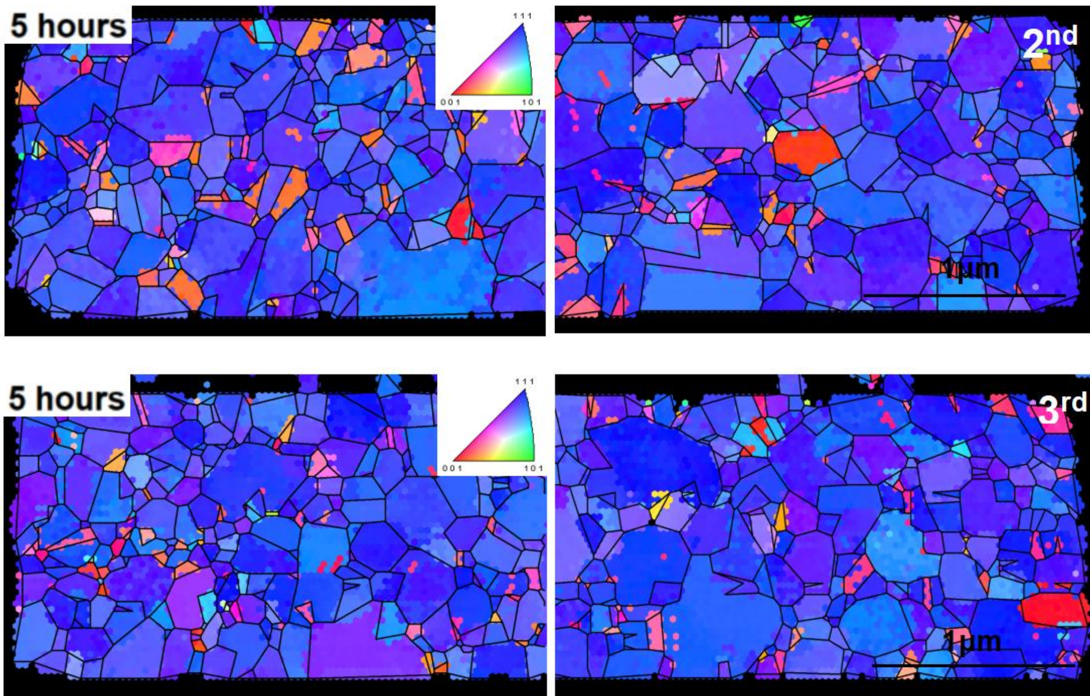
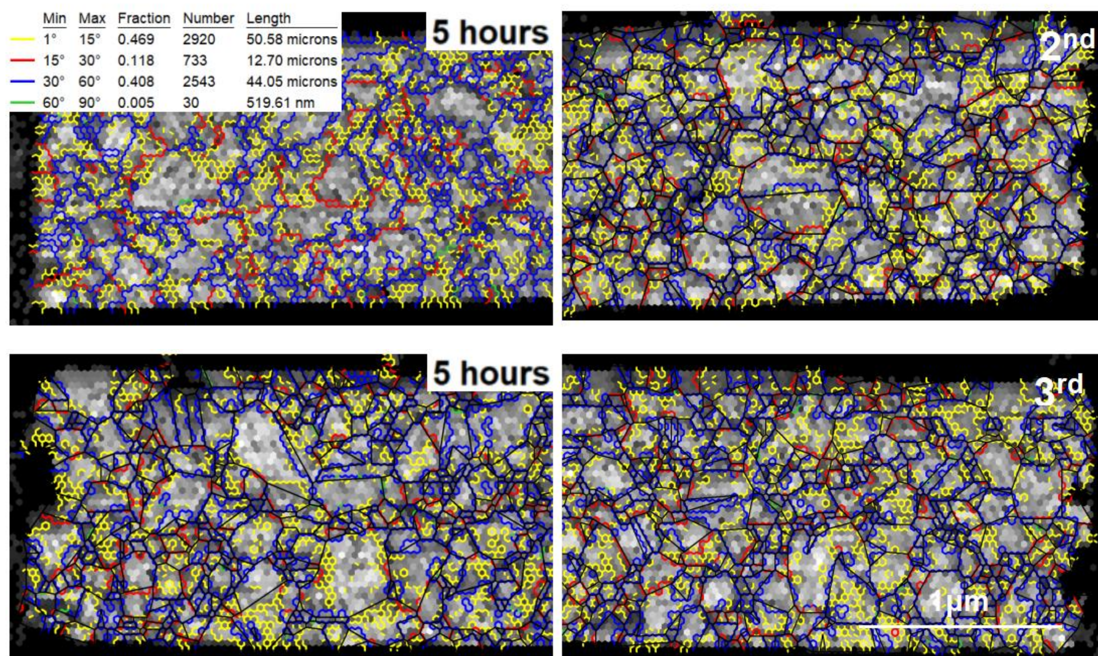
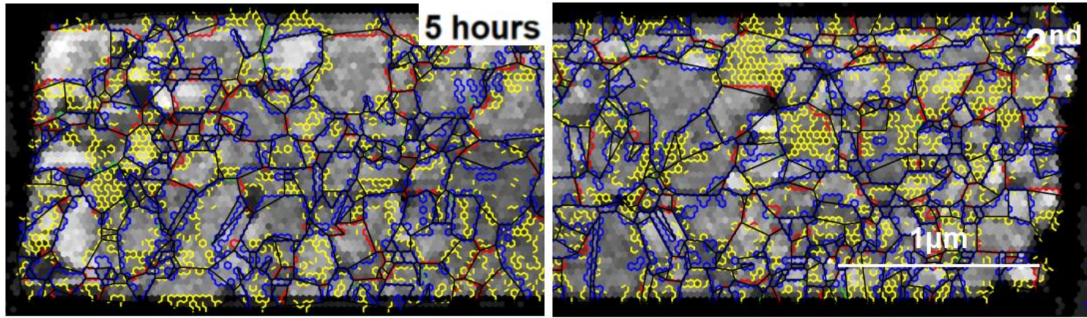


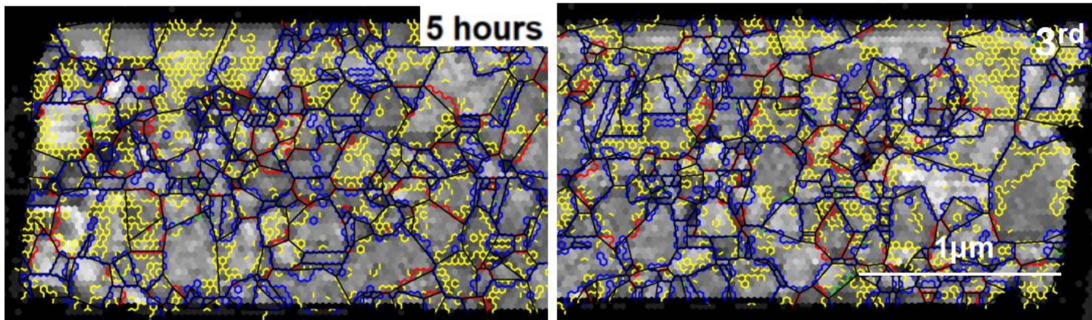
Figure C1. Schematic of inverse pole figure (IPF) and grain images for the two additional samples annealed at 300℃, 400℃ and 500℃ after an EM test duration of 5 hours.

300℃

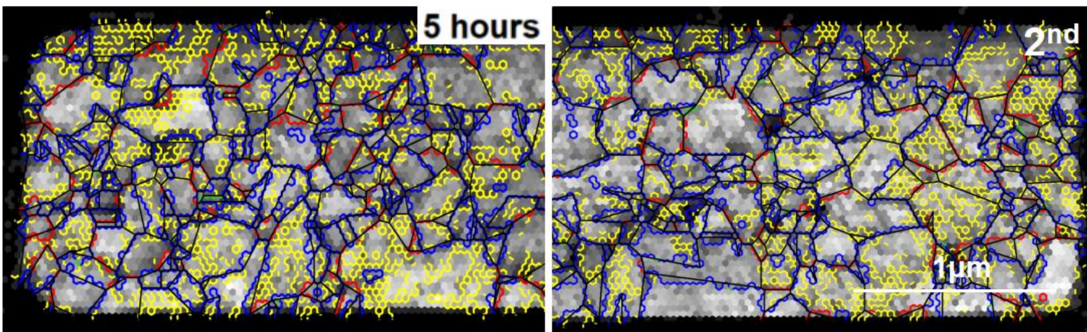


400℃





500℃



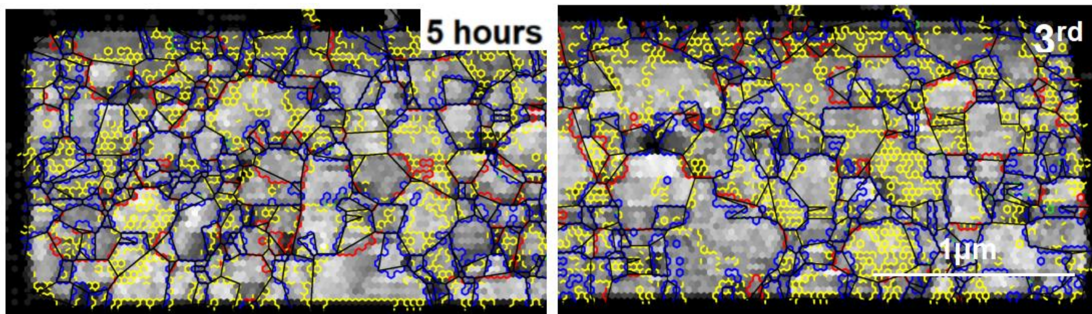
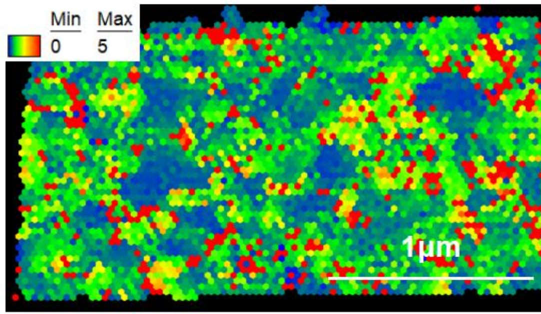
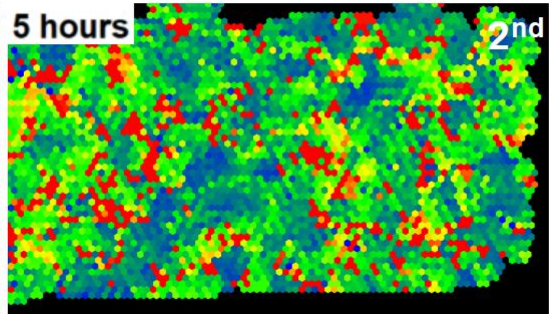
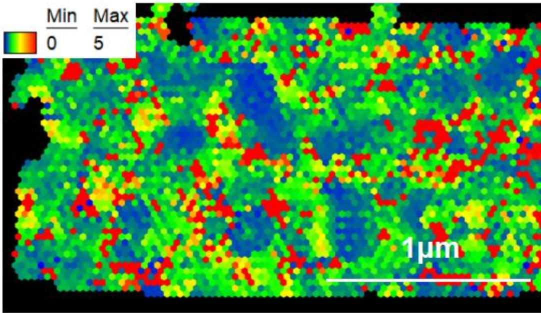


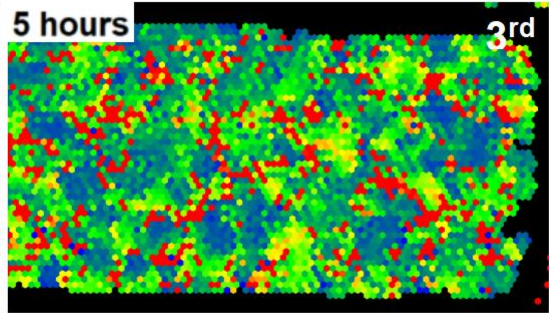
Figure C2. Schematic of grain boundaries with different intervals from 1 to 90° for the two additional samples annealed at 300℃, 400℃ and 500℃ after an EM test duration of 5 hours.

300℃

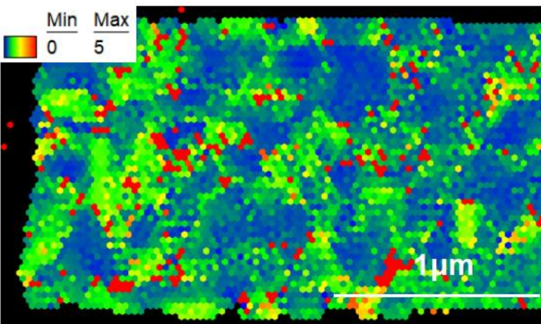


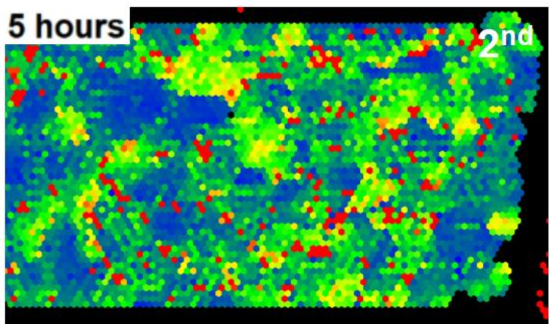


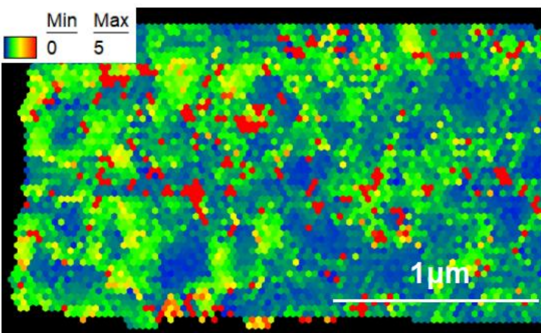


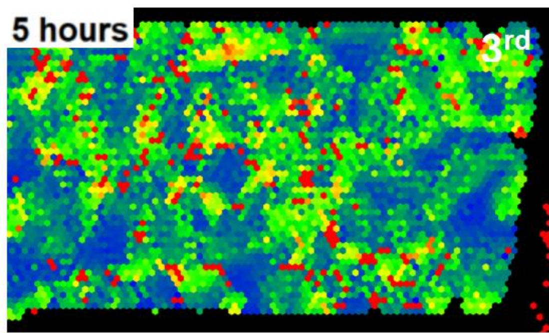


400℃









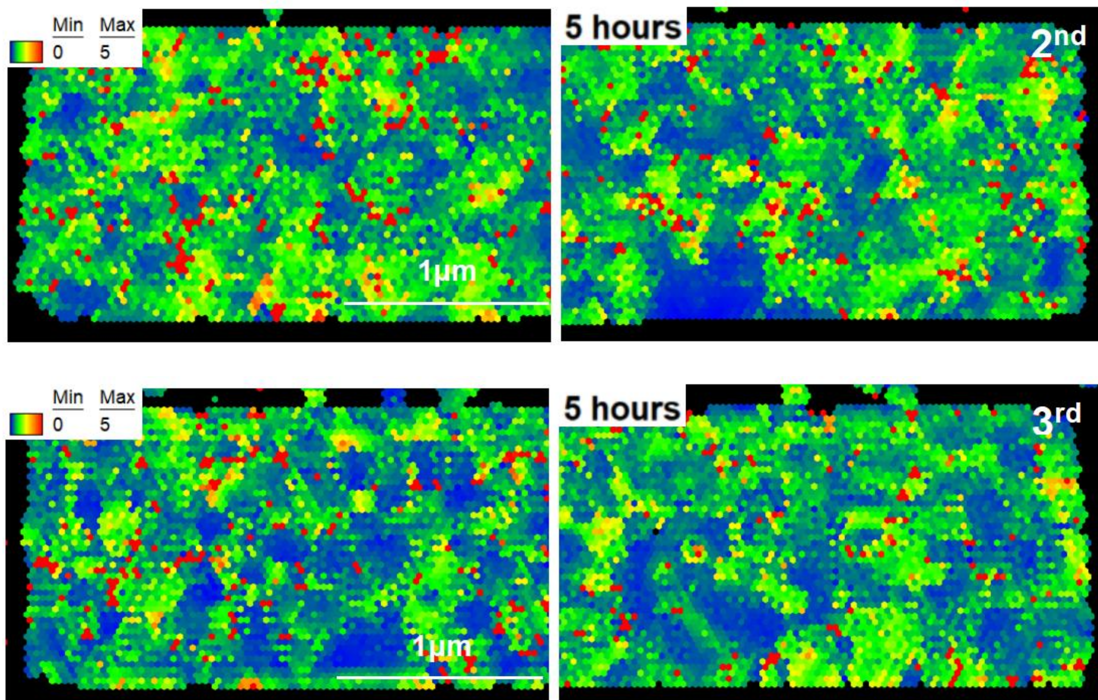


Figure C3. Schematic of Kernel Average Misorientation (KAM) for the two additional samples annealed at 300℃, 400℃ and 500℃ after an EM test duration of 5 hours.