Bachelor Graduation Project Thesis

RF Power Amplifier Efficiency Enhancement

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Executive summary

In this thesis, a new RF Power Amplifier design is proposed that targets for improving the efficiency profile of classical RF Amplifiers. This RF Power Amplifier is especially designed for modulation schemes that need a PA with high PAPR. The PA consists of two different stages that will be digitally controlled. One of these stages has an optimized efficiency profile for supporting input signals with nominal power and the other stage has an optimized efficiency profile for supporting input signals with peak power. The PA has been designed with GaN HEMT's which perform very well at high frequencies while delivering high power.

The PA has been designed to perform optimal for frequencies around 100 MHz. Measurements show that at peak power, which is 40 dBm for this amplifier design, the PA has an efficiency of 63.5%. At 6 dB power back-off, the PA has an efficiency of 65.5 %. The PA has a gain of approximately 20 dB at peak power level and approximately 18 dB at nominal power level. Furthermore the stability of the PA is optimized for the carrier frequency of the input signal. At 100 MHz the Rollet Stability Factor K is of magnitudes higher than unity which guarantees the stability of the circuit.

Furthermore a PCB has been developed to do some investigations in how this new PA design will perform in practice. Measurements on this PCB show that in power back-off a maximum efficiency of 63% can be reached. Results of the performance at peak power show that the efficiency reaches a maximum level of 37%. A possible reason for this is insufficient compression of undesired harmonics. Research is still done on why these results are not as expected and how to find a possible solution.

Acknowledgements

First of all we would like to thank our overall project supervisor prof.dr. Leo de Vreede to give us this opportunity to develop on state of the art technology of RF electronics. The proposal that this thesis will investigate we owe to him and we would like to acknowledge him for that. We also are pleased that we could borrow all the expensive hard- and software that was needed to develop this thesis.

Furthermore we would like to thank our daily supervisors Morteza Alavi and Marco Pelk for their fundamental support and continuous encouragement throughout the development of this thesis. Without their passionate participation and availability throughout this project, the development of this thesis would not been where it is at this point.

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List of Abbreviations

The following abbreviations are used throughout this document:

ADS	Advanced Design Software
CCA	Current Conduction Angle
DPA	Doherty Power Amplifiers
DPD	Digital Predistortion
ESL	Effective Series Inductance
ET	Envelope Tracking
FET	Field Effect Transistor
GND	Ground
$GaAs$	Gallium Arsenide
GaN	Gallium Nitride
$HEMT$	High Electron Mobility Transistor
I_D	Drain current
IMD	Intermodulation Distortion
$MIMO$	Multiple Input Multiple Output
$OFDM$	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAE	Power Added Efficiency
$PAPR$	Peak to Average Power Ratio
PCB	Printed Circuit Board
P_{DC}	The power delivered by DC sources
P_{in}	The input power of the PA
P_{out}	The output power of the PA
RF	Radio Frequency
R_L	Load impedance of the PA
$SISO$	Single Input Single Output
Si	Silicon
THD	Total Harmonic Distortion
V_{DD}	Supply Voltage at the Drain
V_{gs}	External AC signal applied to gate-source (e.g. RF signal)
V_{GS}	The DC bias voltage applied on gate-source
V_{TH}	Threshold Voltage
WPD	Wilkinson Power Divider

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Chapter 1

Introduction

1.1 Background

In current modern communication systems, the demand for data is ever growing. Research from Cisco [1] states that *"global mobile data traffic grew 63 percent in 2016"* and that *"almost half a billion (429 million) mobile devices and connections were added in 2016"*. Where normally bigger amounts of data were crucial to the development of communication systems, the amount of data nowadays is even more crucial to development of economical systems. With the introduction of new data-consuming concepts such as the Internet of Things, the amount of wireless data transport will keep exploring its limits. Current wireless users are served by 2G/3G/4G macro/micro-cell base stations that have still bounds on their data capacity, while the available spectrum for increasing this data capacity has become a scarce resource.

This increase in data-consumers combined with current power hungry technology will lead to an enormous amount of CO_2 emission due to wireless networking. Considering the fact that already today the CO_2 emission of wireless networking approximates that of all commercial airlines worldwide together [2], the amount of CO_2 that is emitted by only wireless networking will be a problem on its own in the future. To prevent future generations from any kind of disastrous consequences that this high number of CO_2 emission will have, drastic innovations are needed to reduce the energy consumption of future's communication network.

The new generation of mobile networks, Fifth-generation (5G), will try to overcome these problems by developing smart and efficient hardware that will make use of technologies such as MIMO/smart antenna techniques operating at high bandwidths [3]. These technological advancements and processes will however demand more energy. The second law of thermodynamics tells us that in all energy exchanges, if no energy is entering or leaving an isolated system, the total entropy of that system will always increase. To prevent this increase in entropy, the amount of energy that will be consumed must be used as efficient as possible. Therefore, 5G-network systems demand for energy-efficient technologies that will improve the overall efficiency of base cell stations.

1.2 Project Overview

In Figure 1.1 a basic overview of a transmitter system is given. In reality this system can be more complex but the fundamental components remain more or less the same. The crucial part w.r.t. the efficiency of this transmitter system is the RF Amplifier. The RF Amplifier is responsible for amplifying the signal up to a level where it can be transmitted into free space. This amplification requires a lot of energy since the signal at the input of the amplifier is of small magnitude while the signal that must be transmitted by the antenna must be of high magnitude to accomplish communication over great distances.

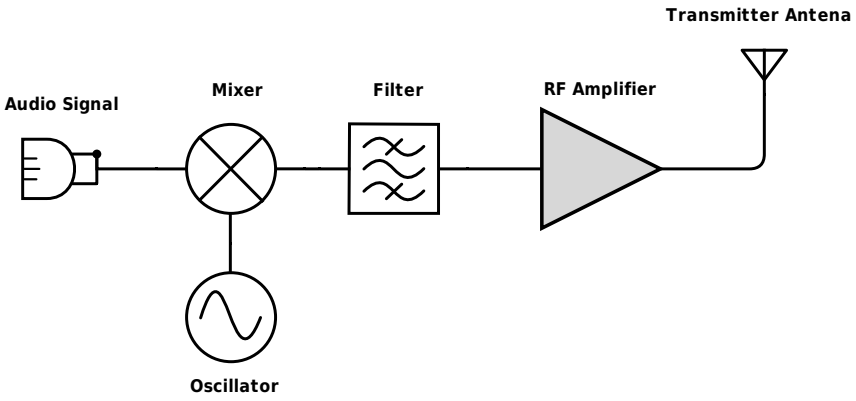


Figure 1.1: A basic overview of a transmitter system.

As has been explained, energy efficiency will play an important role in future communication systems. Therefore it should be clear that the RF Amplifier ideally would be a loss-less component with an overall efficiency of 100%. This is however a problem in contemporary RF Amplifier technologies. In Figure 1.2 it can be seen that when using a fixed supply voltage, more power is dissipated as heat as the envelope of the RF signal does not equal the supply voltage. Older modulation schemes such as FM have the capability to work at peak output power such that peak efficiency can be reached by using classical power amplifier topologies. The fact that these classical amplifier topologies only reach peak efficiency at peak output power is especially problematic for newer modulation techniques with a high Peak-To-Average Power Ratio (PAPR) such as OFDM. Since these modulation schemes operate more often at lower power-regions, newer power amplifier topologies are needed that can provide a reasonable efficiency even in power back-off.

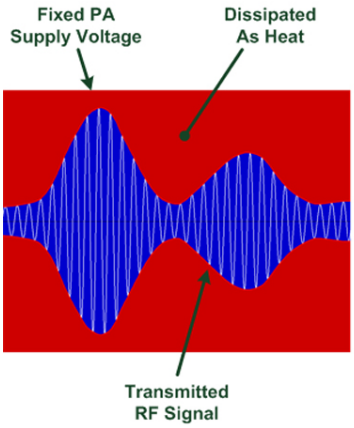


Figure 1.2: Using a fixed power supply voltage, a lot of power can be dissipated as heat

This thesis is part of a project that will investigate in a new PA topology that will try to enhance the efficiency for RF Amplifiers, especially when the PA is in power back-off region. The topology of this new PA concept which will be called **supply interpolating power amplifier** can be seen in Figure 1.3. Instead of using a fixed power supply, two different power supplies will be used to power two active devices in different operating regions. In effect this creates two amplifier stages that are either switched on or off based on the output power level of the system. One stage (main stage) will be used to amplify its input to a nominal power level while the other amplifier stage (peak stage) will amplify signals that would otherwise drive the main stage into compression. As such it will be expected that this new system shows two clear peaks in the efficiency curves, with the transition between the two stages further dictating how the efficiency curve looks around the switch point.

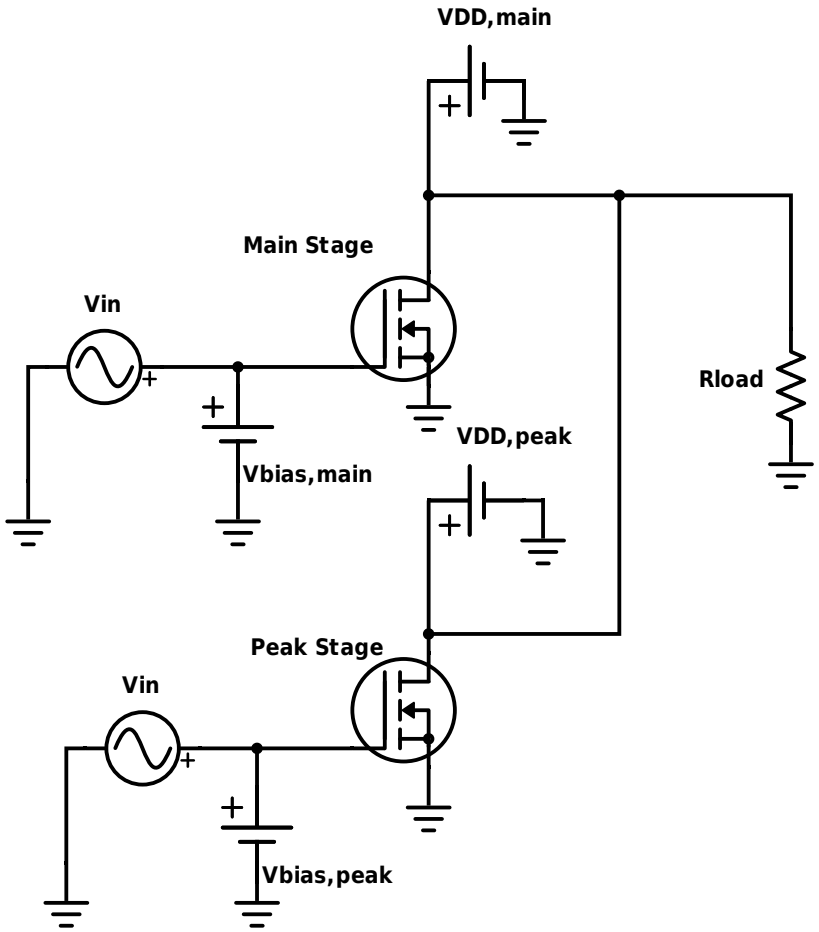


Figure 1.3: A basic overview of the supply interpolating power amplifier

The input to both of these stages will be controlled digitally such that it can adjust to the envelope of any RF input signal. Implementation of the system shown above can be done in two ways:

1. Variable Gain: The input of the system is switched from one amplifier stage to the other once a threshold in the input is reached while keeping the gate bias constant. The presence/absence of an input signal to the amplifier stages will determine whether the amplifier is on of off.

2. Variable Bias: The input signal is applied equally to both amplifier stages but the gate bias is changed depending on the envelope of the input signal such that the correct amplifier stage is on when needed.

The Bachelor Graduation Project is carried out by three teams of two people. The first two teams will aim to implement and design the two different PA implementations described above. The third team will provide the necessary digital control on the input signal and will come up with a testing setup in order to validate that the work done by the first two teams will adhere to the technical specifications. This thesis will aim to explain all the necessary design choices made in order to deliver a working system according to the **Variable Gain** implementation. Thus the definition of this project is:

> *"Design a RF amplifier, where the input signal is digitally controlled, that has improved efficiency in the power back-off region to support newer modulation schemes that need a PA with high PAPR."*

1.3 State-of-the-Art Analysis

As have been explained, when it comes down to RF Power Amplifiers, the main figure of merit in developing RF PAs is efficiency. A convenient way to get a better grip on different aspects of the PA is to calculate the Power Added Efficiency (PAE). This term gives a good insight in how much of the supply power is needed to convert the input power to the output power and can be calculated as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{supply}} * 100\%$$

In order to get a grasp of the current technological limits within the RF PA sector, a state-of-the-art analysis is done to identify topologies and methods that are being employed to help overcome the problem of a degraded efficiency in power back-off.

One of those techniques is using Doherty Power Amplifiers (DPA) and it can be shown that this technique can achieve a PAE greater than 67.08% [4]. DPA is using a concept called load modulation that can be achieved by combining two amplifiers. Despite the use of two amplifiers, the working principle of a DPA is not the same as that of the investigated architecture. The DPA will however be given more attention in Chapter 3 as its efficiency curve greatly resembles the one this research hopes to achieve.

Another common feature that is used to implement efficient RF Power Amplifiers is the practice of Envelope Tracking. The main principle is that the supplies adjust their outgoing power on the power the PA demands [5]. The envelope of the input signal is digitized such that it can be compared with the possible supply voltages in order to choose the optimal value. A larger range of available supply voltages will thus ensure a higher PAE in the system [6]. Results of using this technique show good efficiency profiles but their main constraint is that their bandwidth is limited or that their implementation is complicated and comes with a lot of costs [7]. ET is shown to be able to increase the PAE at 10 dB back-off power by 4.2% [8].

A second architecture used to raise the efficiency of RF amplifiers over a larger output power range is the class G amplifier. This amplifier class combines the use different voltage supply rails that can be used to supply the transistor based on the output power needed together with the typical class AB PAs in order to guarantee linearity of the system.In using class-G power amplifiers, the main culprit is that the switching of the supply voltage causes discontinuities in the gain and the phase of the modulated signal which in turn leads to a non-linear system and out-of-band emission. The gain or phase discontinuities can however be compensated by applying a dynamic gate bias modulation together with the class-G modulation, thereby making class-G operation of power amplifiers an even more viable option [9]. Class G amplifiers can reach efficiency of over 50% at 9 dB PAPR when amplifying a 20 MHz OFDM signal [10].

Lastly, there has been looked into the performance limits of the CGH40010F devices, that will be used throughout the project. Operating in class B, a PAE was measured of 69.2% at an operating frequency of 1.7 GHz with an associated gain of 14.9 dB [11].

1.4 Design Requirements

As explained above, the goal of the Bachelor Graduation Project is to design and verify a proof-of-concept of a new PA architecture that will aim to achieve a high efficiency at an output power range of 6 dB. In order to keep the scope of the project within reasonable bounds for the time allocated to finish it, a number of design objectives were set in order to maintain a clear understanding of what had to be done.

- Proper biasing of the drain and gate networks to ensure that the drain efficiency of the system as a whole is maximised.
- Choosing a proper threshold at the input power to switch between the two different amplifier stages such that main and peak amplifier can deliver a peak output power of 34 dBm and 40 dBm to a load of 50 Ω.
- The system should be unconditionally stable over a large frequency range in order to ensure no unwanted oscillations can occur.
- A prototype should be fabricated such that the design can be measured and verified.

Alongside these design objectives, a number of functional requirements and restrictions were placed on the project to ensure that it would be able to finish this research within the assigned time period. Contrary to state-of-the-art implementations, design of the variable gain interpolating supply amplifier will be done at a comparatively low operating frequency of 100 MHz. This operating frequency is chosen because it lies far below the cut-off frequency F_T of the transistor and as such displays high gain. As the focus is put on showing the desired efficiency curve, the process of linearising the circuit through methods such as DPD and design of matching networks fall outside of the initial scope of the project and will be deemed points for future research. Furthermore, the examining of unwanted harmonics in the output through methods such as THD and IMD will be deemed secondary objectives and will only be examined should time allow for it. Optimising of the switching profile between main and peak amplifier stages to further raise average efficiency will be deemed a secondary objective. Inputs to verify the design will also largely comprise of only single-tone inputs. The use of modulation schemes and two tone tests will be deemed points for further research. According to the state-of-the-art designs, the project objectives set and the restrictions put in place, a list of design specifications of the PA was made as listed below.

Table 1.1: Design Specifications of the Variable Gain interpolating Supply Amplifier

Parameter	Specification
Operating Frequency	100 MHz
Peak Output Power	10 W (40 dBm)
Gain	$\geq$ 20 dB
Maximum Gain Ripple	$\leq$ 2 dB
Peak Drain Efficiency at Main Stage	$\geq$ 60%
Peak Drain Efficiency at Peak Stage	$\geq$ 60%
PA Bandwith	10 kHz

1.5 Thesis Outline

This thesis focuses on the study, design and implementation of a new PA architecture that will achieve high drain efficiency even at output power back-off in order to aid in the efficiency amplification of high PAPR signals.

Chapter 2 will review the properties of the GaN HEMT devices used throughout the project to try and justify their usage for the purposes of this project. In Chapter 3, an introduction is given on power amplifiers to gain a clear understanding on the different ways that the biasing affects system efficiency and linearity. Alongside this, an effort is made to briefly describe the working principle of the Doherty Power Amplifier to show how the efficiency curve resembles the expected efficiency curve of the Variable Gain Interpolating Supply Amplifier. Chapter 4 aims to meticulously explain all steps and considerations made during the design process. This includes bias point selection, harmonic suppression, DC coupling and decoupling, switching between the two amplifier stages, combining network integration, stability analysis, and layout design.

The system's performance in regards to all the metrics explained is evaluated based on the simulations done throughout Chapter 4 and design specifications listed in Chapter 1.4. All simulation results that are shown have been done with software of the ADS tool. In Chapter 5 measurements done by the Measurement Group on the manufactured PCB are related back to the simulations done in Chapter 4 in order to verify the design. Lastly, Chapter 6 will give some conclusive arguments about the project as well as recommended points for future research w.r.t. the theory and results developed in this project.

Chapter 2

Introduction to HEMT

The provided CHG40010F transistors for the project are classed as HEMT transistors. HEMT stands for High Electron Mobility Transistor, which belongs to the class of FETs. FETs use an electronic field to vary the width of a channel along which charge carriers can flow. In contrast to the widely used MOSFETs, where a doped region functions as the channel, HEMTs employ a principle where two different materials with different band gaps are used for the channel. Figure 2.1 shows how the active devices are classed.

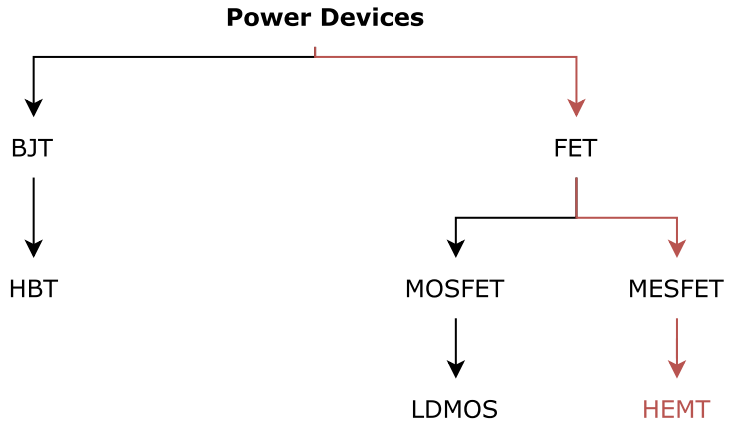


Figure 2.1: Classes of active devices.

The provided transistor is a GaN based transistor to fit the needs of the project. Where in the past active devices would usually be made of GaAs or Si, GaN provides a wide band gap, high breakdown voltage and high output power due to its electrical properties. The electrical properties of GaN against other common materials such as Si and GaAs are shown in Table 2.1.

As can be seen in Table 2.1, GaN maintains about the same electron and hole mobility as Si while the bandgap of GaN is almost three times as wide. Higher electron mobility will result in a lower knee voltage, the voltage required to turn on the channel of the transistor, thus resulting in lower losses and higher efficiencies.

A wider bandgap implies that more energy is needed for the electrons to traverse from the valence to the conduction band, as such the device can operate at a higher temperature and for the same reason it is also less prone to external noise sources. A higher operating temperature is highly preferred in the case of this project as the peak output power of 10W will result in relatively high temperatures. A wider

Table 2.1: Eletrical Properties of Active Device Compounds. [12]

Property	Si	GaAs	GaN
Electron mobility $[cm^2V^{-1}s^{-1}]$	1500	8500	1000
Hole mobility $[cm^2V^{-1}s^{-1}]$	450	400	350
Bandgap [eV]	1.12	1.42	3.2
Saturated Drift Velocity [10^7cm/s]	0.7	2.0	1.8
Thermal Conductivity [W/cm*°C]	1.4	0.45	1.7
Dielectric Constant	11.9	12.9	14

bandgap further implies a higher breakdown voltage of the device, which is preferable considering the high bias voltages and output waveforms applied to the drain of the device are relatively high. Lastly a higher bandgap in the material also results in a higher power density such that the transistor is able to output more power at a smaller size.

Furthermore, the thermal conductivity is an import property to look at. Since for this project's purposes the transistor will be outputting as much as 10W, the material's ability to easily disperse this heat and thus not increase the junction temperature is of great importance. The better dispersion of heat thus results is a more reliable operation at high output powers.

Chapter 3

Introduction to Power Amplifiers

Amplifiers have an essential role in RF circuits and are therefore widely researched to improve their performance and in effect that of the RF circuit. The basic working principle of the RF power amplifier is that a small input signal is amplified by converting power from a DC rail into RF output power which is shown in Figure 3.1.

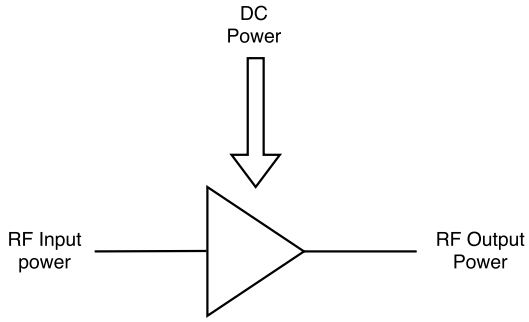


Figure 3.1: Working principle of the PA.

The conversion of DC power to RF power is characterised by the drain efficiency of the amplifier and is defined as:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{3.1}$$

As opposed to small signal amplifiers where the DC consumption is generally very low, in PAs the consumption of DC power is high and thus the drain efficiency of PAs is seen as one of the key parameters to designing a good amplifier. A more precise Figure of merit for PAs is the PAE.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{3.2}$$

The PAE takes into account the effect that the gain G of the amplifier has on the efficiency. By expanding equation 3.2 to equation 3.3, it can be shown that in PAs with a high gain, as is the case with the GaN HEMTs used throughout the project, the drain efficiency and PAE become equal.

$$PAE = \frac{P_{out}}{P_{DC}}(1 - \frac{1}{G}) = \eta(1 - \frac{1}{G}) \tag{3.3}$$

PAs can be classed as linear and non-linear PAs. The linear PAs have as main advantage that they are able to generate an output signal that is proportional to their input signal without adding a high amount of harmonic power in the output signal. Non-linear PAs introduce significantly more harmonic power in their output compared to their linear counterparts due to the fact that they operate at or near the cut-off region of the transistor. The main advantage of the non-linear PAs is that they are able to achieve a much higher efficiency. This does however come at a cost of a degraded output signal that is no longer proportional to the input signal due to the harmonics introduced.

Amplifier classes are mainly lumped into two basic groups. The first group, comprised of the more common class A, B, AB and C amplifiers are classed based on their bias points and in turn their output current conduction angle θ. The CCA defines the fraction of the RF input signal where a current is flowing through the transistor and thus dissipating power. The second group of amplifiers are the switching amplifier classes of D, E, F, G. These amplifier classes are characterised by their use of digital circuits and pulse width modulation signals to constantly switch the signal between ON and OFF driving the output into the transistors saturation and cut-off regions every time.

To gain a better understanding of the different classes while simultaneously maintaining a clear image of the classes, only the amplifiers of the biasing class will be discussed as the switching amplifier classes require a more in depth analysis of the harmonics introduced to be fully understood. Figure 3.2 shows the different classes of RF PAs.

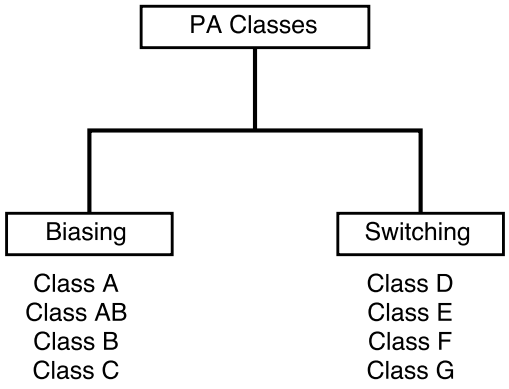


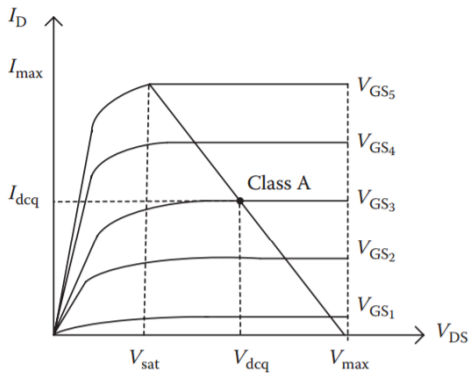
Figure 3.2: Different classes of PAs.

3.1 Class A Amplifier

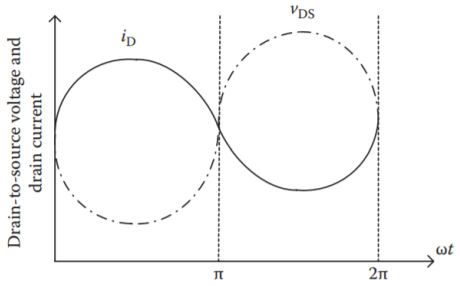
In class A, the amplifier is biased in between the cut-off and saturation regions such that class A amplifiers are linear amplifiers with a conduction angle θ of 360°. The conduction angle of 360° means that the transistor will be turned on and conducting over the whole output waveform.

A typical load line and V_{DS} and I_D waveforms are shown in Figure 3.3. Maximum efficiency for the class A power amplifiers can be calculated by realising that maximum efficiency happens when the drain voltage swings from 0V to $2V_{DC}$. The DC power is then defined by Equation 3.4:

$$P_{DC} = V_{DC} I_{DC} = \frac{V_{DC}^2}{R_L} \tag{3.4}$$



(a) Typical load line for class A PA.



(b) V_{DS} and I_D waveforms for class A PA.

Figure 3.3: Class A power amplifier characteristics. [13]

The RF output power is then defined by Equation 3.5:

$$P_{out} = \frac{1}{2}\frac{V_{DC}^2}{R_L} \tag{3.5}$$

Then from equations 3.1, 3.4 and 3.5, η_{max} can be calculated to be 50%. Because the transistor is conducting throughout the whole waveform, the maximum efficiency of class A amplifiers is the lowest out of all the amplifier classes. As such class A amplifiers are usually used in small signal amplifiers such as audio amplifiers where the total consumption of DC power is comparatively low and the need for a linear system is high.

3.2 Class B Amplifier

Dissipation of power in the transistor due to the 360° conduction angle in class A PAs greatly reduces RF output power and therefore efficiency. The dissipation of power in the active device can however be reduced by lowering the CCA. In class B PAs the active device is biased close to its cut-off region such that the transistor will only be turned on for none half cycle of the output waveform and as a result the CCA is lowered to 180°.

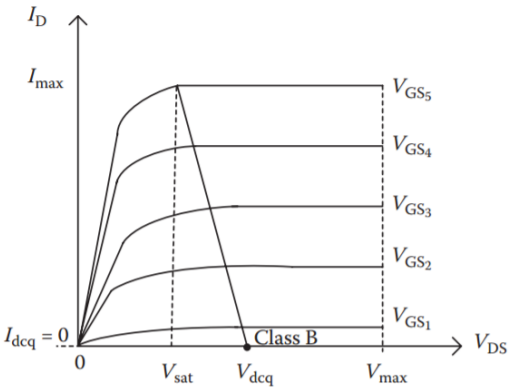
Typical load line and V_{DS} and I_D waveforms shown in Figure 3.4 show how a class B amplifier is biased and a result only outputs a current for half of the cycle.. Maximum efficiency for class B PAs occurs when the amplitude of the fundamental output voltage waveform V_m is equal to V_{DC}. Under this condition the DC power can be calculated to be [13]:

$$P_{DC} = V_{DC}I_{DC} = \frac{2}{\pi}I_m V_{DC} \tag{3.6}$$

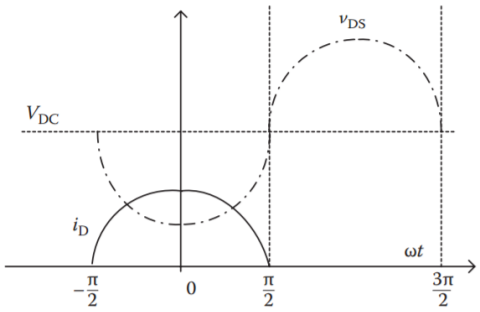
With I_m the amplitude of the fundamental output current waveform. The RF output power can be calculated as:

$$P_{out} = \frac{1}{2}V_m I_m = \frac{1}{2}V_{DC}I_m \tag{3.7}$$

From equations 3.1, 3.6 and 3.7 η_{max} can be calculated to be $\frac{\pi}{4}$ = 78.5%. Due to lower current conduction angle, maximum efficiency for class B amplifiers is greatly increased compared to class A amplifiers. Class B amplifiers do however show poor performance in regards to linearity due to the introduction of higher order harmonics. A currently existing method to improve linearity with class B amplifiers is to use two class B amplifiers simultaneously in a push-pull configuration. This type of configuration uses one



(a) Typical load line for class B PA.



(b) V_{DS} and I_D waveforms for class B PA.

Figure 3.4: Class B power amplifier characteristics. [13]

amplifier to source current through the available load while the other amplifier acts as a sink to the current from the load. [14]

3.3 Class AB Amplifier

Like explained before, in class B operation, linearity is sacrificed for amplifier efficiency. In cases where it is desirable to have an amplifier with better efficiency than in class A and better linearity than in class B, like in many RF applications, the class AB PA can be chosen as a good trade-off. In class AB PAs the conduction angle lies somewhere between 180° and 360° and thus the bias point for class AB power amplifiers has to be chosen somewhere in between that of the biasing points for class A and class B. As a result maximum efficiency of class AB amplifiers lies between 50% and 78.5%, depending on the bias point chosen. Typical V_{DS} and I_D waveforms for class AB amplifiers are shown in Figure 3.5

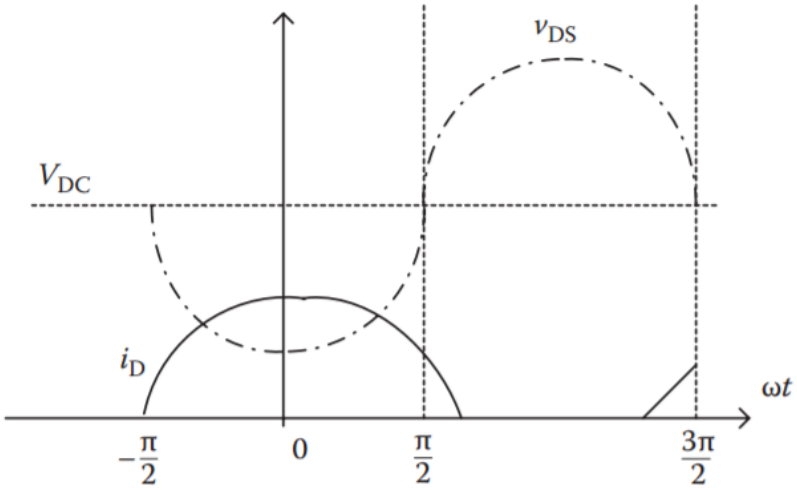


Figure 3.5: V_{DS} and I_D waveforms for class AB PA. [13]

3.4 Class C Amplifier

The classes discussed above are seen as linear amplifier classes where the phase and amplitude of the output signal is linearly related to that of the input signal. When efficiency becomes more important than linearity in the system, non-linear amplifiers such as class C, D, E and F can be used to increase efficiency. The conduction angle of class C power amplifiers lies below 180° which means that class C amplifiers overpower class B amplifiers in terms of efficiency. A conduction angle lower than 180° thus also means that the bias point for class C amplifiers lies below the cut-off region of the active device. Typical V_{DS} and I_D waveforms for class C amplifiers are shown in Figure 3.6

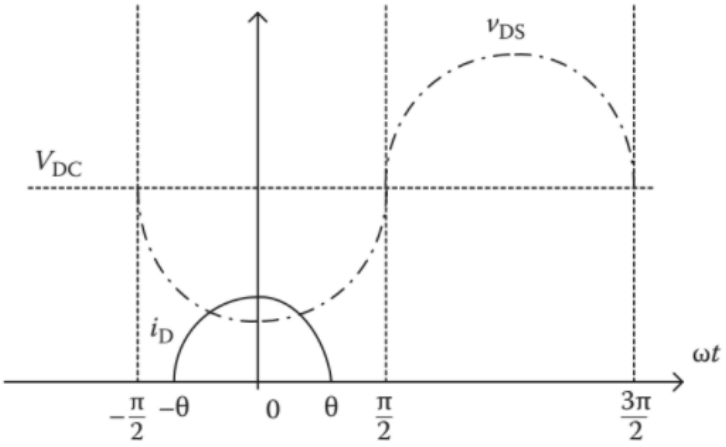


Figure 3.6: V_{DS} and I_D waveforms for class C PA. [13]

Maximum efficiency for class C amplifiers can be calculated by realising that the drain efficiency can also be calculated with the CCA [13]:

$$\eta = \frac{\theta - sin\theta}{4[sin(\theta/2) - (\theta/2)cos(\theta/2)]} \tag{3.8}$$

Equation 3.8 shows that 100% efficiency can be reached when θ is set to 0°. Reaching 100% efficiency using class C amplifiers is however not very feasible as the RF output power greatly decreases as the conduction angle reaches 0. Typical class C amplifiers usually provide an efficiency in the range of 75% to 80%.

3.5 Two stage power amplifier

As the main objective of this project was to prove how the concept of two stage amplifier can realise a high drain efficiency at lower output power. Since classical amplifiers lack in efficiency at a lower P_{out}, and new modulation schemes such as OFDM require the amplifiers to have a higher efficiency in the back-off region as these modulation schemes have a typical PAPR in the range of 6-12 dBm, we felt it was necessary to provide some background information on the working principle of the Doherty Power Amplifier (DPA). While its working principle differs from the proposed design for this project, the problem of a low efficiency in the back-off region is solved much like with our project.

3.5.1 Comparison to Doherty Power Amplifier

The basic working principle of the DPA can easily be explained as follows. Where in a class B amplifier the drain efficiency is dependent on the voltage swing of the output, the DPA seeks keep the maximum voltage swing over a certain range of the input, effectively maintaining maximum efficiency over the whole range of the input. $V_{out} = IR_{load}$ and as such when the input power is increased and thus also the current is increased, R_{load} should be lowered in order to keep the voltage swing constant. The concept of changing the load to keep V_{out} constant and thus maintain efficiency is called load modulation [15]. The load modulation in a DPA is achieved by combining two amplifiers called a main and auxiliary amplifier as shown in Figure 3.7.

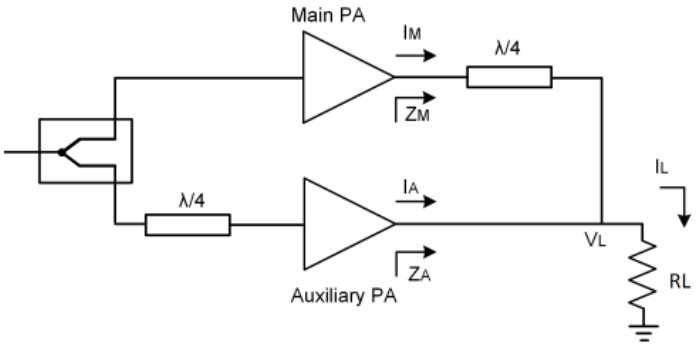


Figure 3.7: Doherty Power Amplifier.

In the DPA the impedances Z_M and Z_A are changed by the ratios of the currents I_A and I_M:

$$Z_M = \frac{Z_o^2}{R_L} - jZ_o\frac{I_A}{I_M} \tag{3.9}$$

$$Z_A = \frac{I_M R_L}{jI_A} \tag{3.10}$$

Equations 3.9 and 3.10 show that in order to have real impedances I_M and I_A should outphase each other by 90°. the λ/4 line is used to correct for this phase shift at the output. Figure 3.8 shows the efficiency curve of a DPA in the low power region where only the main amplifier is turned on and the Doherty region where both main and auxiliary amplifier are turned on to reach a static efficiency from the mid-low output that resembles the preferred outcome of this project.

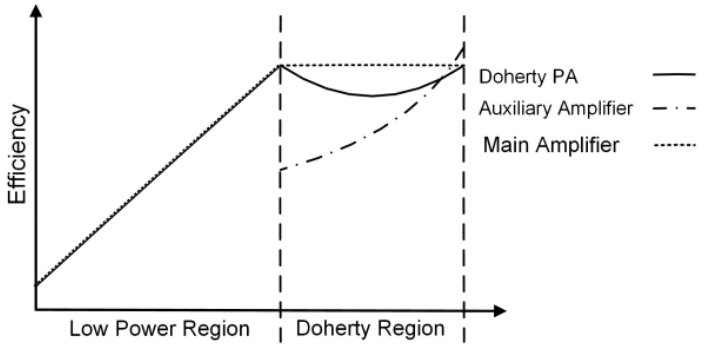


Figure 3.8: Doherty Power Amplifier efficiency curve.

Chapter 4

Power Amplifier Design and Simulations

The design of the RF Power Amplifier is done in simple but fundamental phases that in the end all add up to a understandable design process where all different aspects of the final RF Power Amplifier can be logically deduced from these design phases. This chapter will give deep insight in how all different components of the PA have been designed and how they do affect the behaviour of the amplifier. Different solutions that came up during the design with their will be explained. At the end of this chapter the final amplifier design is presented and considerations with respect to the layout that has been constructed according to this final design are worked out. In this chapter, the transistor that will deliver the peak power will be called *peak transistor* and the transistor that will deliver the nominal power power will be called *main transistor*.

4.1 DC Design for GaN HEMT

As has been explained in Chapter 3, the class of an amplifier (and therefore the characteristics) is determined by the bias voltage V_{GS}. The maximum output power that a transistor can deliver is determined by the drain voltage V_{DD}. It should be clear that these DC voltages must be properly determined to have a power amplifier that meets the design constraints.

4.1.1 Drain Bias Voltage

The final PA that is designed for this project should deliver a maximum power P_{max} of 10 W to R_L which will be a 50 Ω load. When a MOSFET is fully turned on, i.e. it's in saturation state, the maximum output power that it can deliver is determined by V_{DD}, the drain voltage. With these requirements, the value of V_{DD} of the peak transistor can be determined since this transistor will determine the maximum output power.

It can be shown that ideally the maximum drain efficiency is not dependent on V_{DD}. The drain efficiency is defined as $\eta_{drain} = \frac{P_{out}}{P_{DC}}$ where P_{DC} is defined as the power delivered by the drain. P_{DC} can be expressed as $V_{DD} \cdot I_{DC}$. While V_{DD} is known, finding an expression for I_{DC} requires some effort. When biasing the transistor in class B, the drain current will have a profile which ideally looks like Figure 4.1. Over a period of 2π, the transistor will conduct only for positive gate voltages, which will result in a sinus waveform on the interval $[0, \pi]$.

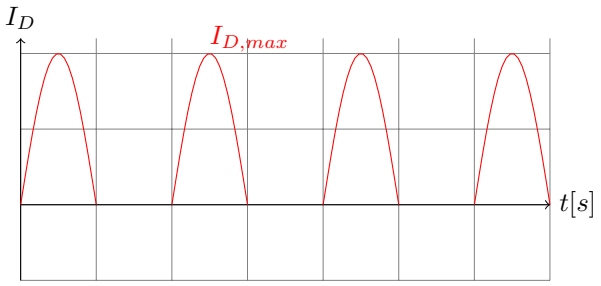


Figure 4.1: Drain current for transistor biased in class B.

The average DC current that needs to be delivered can be expressed in terms of $I_{D,max}$:

$$\begin{aligned} I_{DC} &= \frac{1}{2\pi}\int_0^{\pi} I_{D,max}\sin\,\theta\;\mathrm{d}\theta \\ &= \frac{I_{D,max}}{2\pi}\cdot -\cos\,\theta\Big|_0^{\pi} = \frac{I_{D,max}}{\pi} \end{aligned}$$

Therefore $P_{DC} = V_{DD}\cdot\frac{I_{D,max}}{\pi}$. The output power P_{out} can be expressed as $P_{out} = \frac{V_{DD}^2}{2\cdot R_L}$. The load resistance R_L can be expressed as the first harmonic of the output voltage divided by the first harmonic of the output current or in mathematical terms: $R_L = \frac{V_{out,1}}{I_{out,1}}$. For the maximum efficiency, the value of $V_{out,1}$ equals V_{DD}. The first harmonic of the output current can also be expressed in terms of $I_{D,max}$ in the same manner as has been shown for I_{DC}:

$$\begin{aligned} I_{out,1} &= \frac{1}{\pi}\int_0^{\pi} I_{D,max}\sin^2\,\theta\;\mathrm{d}\theta \\ &= \frac{I_{D,max}}{\pi}\cdot(\frac{1}{2}\theta - \frac{1}{4}\sin\,2\theta)\Big|_0^{\pi} = \frac{I_{D,max}}{2} \end{aligned}$$

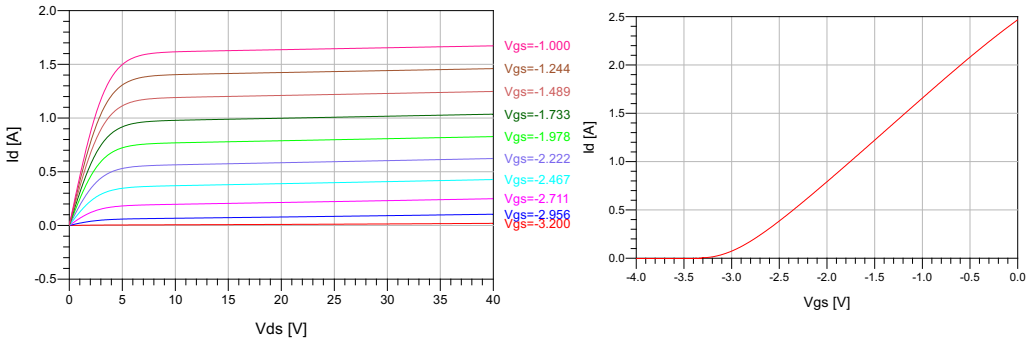
Therefore $R_L = \frac{2\cdot V_{DD}}{I_{D,max}}$ and substitution of R_L in P_{out} gives $\frac{1}{4}\cdot V_{DD}\cdot I_{D,max}$. The drain efficiency can now be expressed as:

$$\eta_{drain} = \frac{P_{out}}{P_{DC}} = \frac{\frac{1}{4}\cdot V_{DD}\cdot I_{D,max}}{V_{DD}\cdot\frac{I_{D,max}}{\pi}} = \frac{\pi}{4}$$

These derivations show that ideally the maximum drain efficiency is not dependent on V_{DD}. Therefore choosing a appropriate value for V_{DD} doesn't affect the maximum efficiency that can be achieved ideally. However, choosing a lower value for V_{DD} will result in a higher value for I_D to achieve the same power. Since the transistor acts as a resistive device, higher currents will have result to higher ohmic losses which is not desirable. But choosing a lower value for V_{DD} will also drive the transistor sooner in saturation which will improve the efficiency on the other hand. To find a good starting value for V_{DD}, Equation 3.5 can be solved for P_{out} = 10 W (40 dBm) and R_L = 50Ω which yields a value for $V_{DD,peak}$ of 31.6 V. One of the design constraints is that the main transistor will be used when the amplifier is in 6 dB back-off e.g. delivering 34 dBm. This is a quarter of the peak power that the peak transistor will deliver. For delivering a quarter power, $V_{DD,main}$ should be $\frac{1}{2}\cdot V_{DD,peak}$ = 15.8 V due to the quadrature relationship between power and voltage.

4.1.2 Gate Bias Voltage

Designing the amplifier properly means biasing the transistors properly. The amplitude of the bias voltage V_{GS} will determine the class of the amplifier and therefore the efficiency and linearity characteristics as has been explained in Chapter 3. Different biasing approaches can therefore lead to certain desired amplifier characteristics. To determine this bias voltage, some basic characteristics of the transistor have to be known. These characteristics can be seen in Figure 4.2. In Figure 4.2a the I_D vs V_{DS} curvatures are plotted from which the operation point can be determined. From Figure 4.2b it can be seen that the threshold voltage V_{TH} is ≈ -3.3 V.



(a) Plot of I_D vs V_{DS} curvatures for different values of V_{GS}

(b) Plot of I_D vs V_{GS} from where it can be seen that $V_{TH} \approx$ -3.3 V

Figure 4.2: Characteristics of the CGH40010F transistor.

Biasing the transistor in class A will not lead to the desired amplifier characteristics that this project aims for. From Figure 4.2a it can be seen that biasing the transistor in class A, thus setting V_{GS} far above the threshold voltage, means that the transistor is most of the time conducting even when no signal v_{gs} is applied and therefore is wasting a lot of power. A plot of the PAE can be seen in Figure 4.3. This efficiency has been achieved by setting V_{GS} for both transistors to a DC-value of -2.73 V. The maximum efficiency is around 40% which is close to the absolute maximum efficiency that class A can achieve which is around 50%.

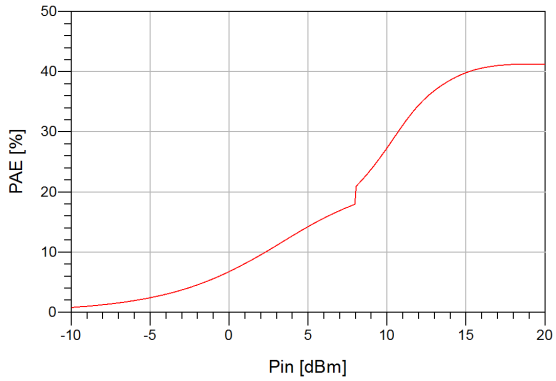


Figure 4.3: The PAE when biasing the transistor in class A

Setting V_{GS} to a value higher than V_{TH} will also introduce the problem of *reverse conduction*. In Figure 4.4 a very simplified version of the PA is shown. A signal is getting amplified by the peak stage while the main stage does not have any signal on the input. The amplified signal traverses ideally the green path. But it's also visible at the output of the main stage transistor which is indicated with the red path. Since this transistor is turned on because it's biased in class A, it conducts. Therefore the signal is also visible on the input of the main stage which is not desired because this will lower the efficiency. Reverse conduction will negatively impact the overall efficiency of the PA. Therefore class A is for sure not the right class to bias the transistor.

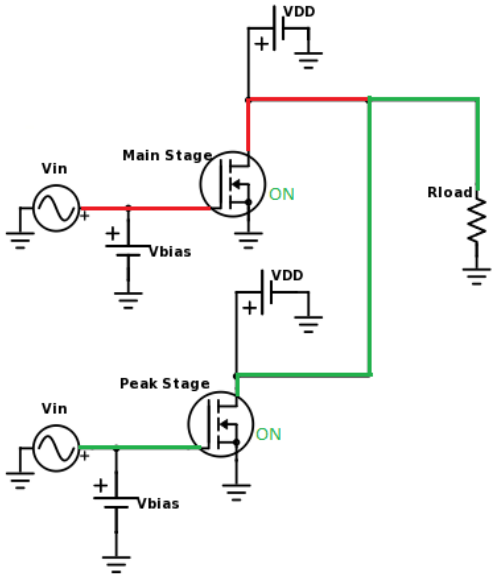


Figure 4.4: The PAE when biasing the transistor in class A

Class B or even class C are more power-efficient classes and are therefore good candidates to enhance the overall efficiency of the final PA. In both classes the transistor is normally turned off when no signal v_{gs} is applied. This has two main advantages:

1. Less power consumption since the transistor only conducts for 180° of the input signal and therefore won't conduct in quiescent state.

2. Better performance w.r.t. efficiency because there will be little reverse conduction since the transistor is turned off when no input signal is applied.

However class B and class C do also have their disadvantages such as bad linearity which negatively influence the gain profile of the amplifier and this has to be kept in mind when biasing in class B or C. Biasing the transistor in class B can be done by setting V_{GS} to a voltage which is close to V_{TH}. A sweep of different values for V_{GS} has been done to find out what the effect on linearity is. From Figure 4.5 it can be concluded that choosing a low value for V_{GS} will result in bad linearity characteristics.

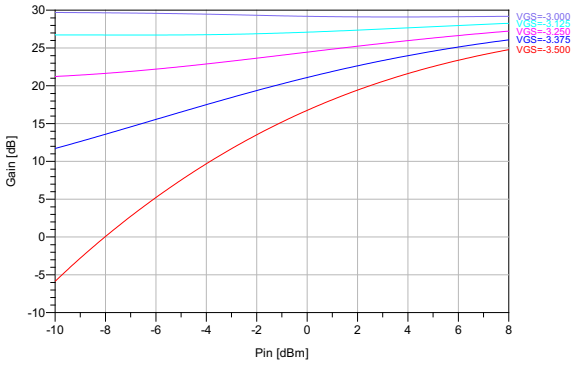


Figure 4.5: When sweeping V_{GS} different linearity characteristics can be achieved. These simulations have been performed with V_{DD} = 31.6 V on a single transistor stage

From these simulations, V_{GS} has been set to -3.20 V, which is resembled by the purple curve in Figure 4.5. At this operation point there is a relative stable gain compared to lower values. The problem of *reverse conduction* does also have less impact at this operation point because the transistor is almost off when no input signal is applied. To verify whether indeed this operation point will resemble a true class B operation, the drain current I_D has been plotted for both class A (V_{GS} = -2.73 V) and class B (V_{GS} = -3.20 V). In Figure 4.6 these results of simulating both classes can be seen. These results indeed verify that biasing in class B will result in a low quiescent current which is approximately 15 mA when V_{DD} = 31.6 V.

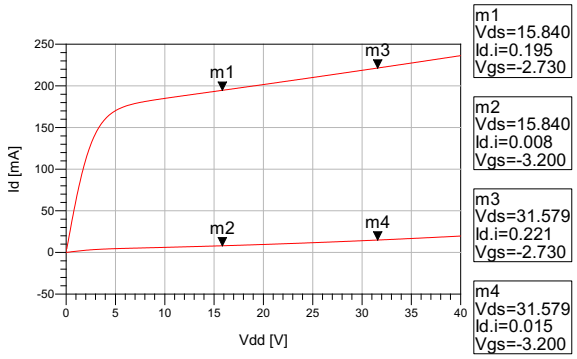


Figure 4.6: Simulations verify that a different quiescent current is obtained when biasing in different classes

The first simple design for the PA circuit can be seen in Figure 4.7. However this circuit is of course never applicable for AC signals, let alone high-frequency RF signals. In section 4.2 this basic circuit will be translated to a RF-applicable circuit that will try to meet the design constraints that are set for this project.

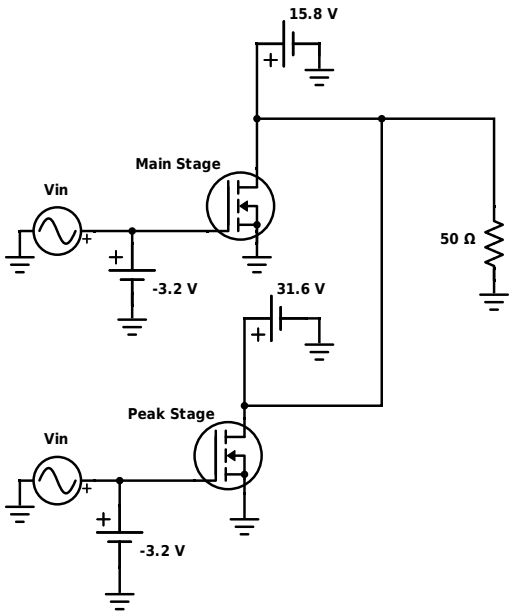


Figure 4.7: First circuit obtained by DC analysis of the transistor. This circuit is of course never applicable to RF signals.

4.2 Designing the PA for RF Application

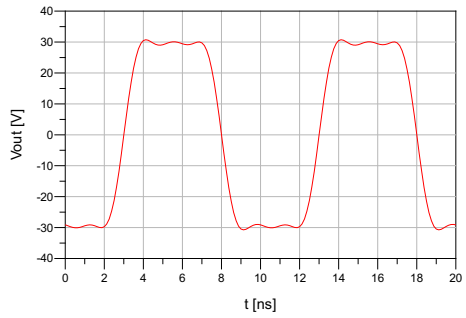
This section will aim to explain all the design choices made throughout the project in order for the supply interpolating amplifier to eventually meet the technical specifications listed in Section 1.4.

4.2.1 Output Power Correction

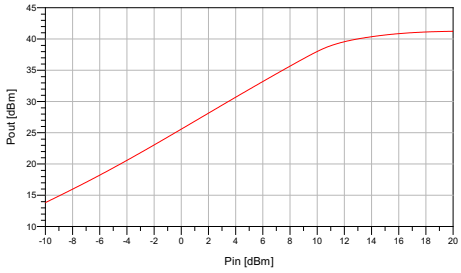
Up until now only DC analysis of the transistor has been performed through biasing. This small-signal analysis is an approximation and is only valid when the signals in the circuit are very small compared to the DC signals. For RF design, input signals can scale up to 20 dBm power, and small signal analysis is not valid anymore. Since the transistor is a non-linear device, it will introduce non-linearity in the signal that it's amplifying for large inputs signals. In Figure 4.8a the effects of non-linearity on the output signal can be seen. The signal is composed of different frequencies or harmonics, which are compressing the magnitude of the signal to the 31.6 voltage that V_{DD} can deliver. This leads however to problems when measuring the output power. The real output power P_{out} can be calculated with Equation 4.1

$$P_{out} = \frac{1}{2}\text{Re}(S) = \frac{1}{2}\text{Re}(I^*_{out,1}V_{out,1}) \tag{4.1}$$

From Equation 4.1 it can be seen that the fundamental tone of the V_{out} and I_{out} is taken to compute P_{out} since only the fundamental tone is the desired frequency. This output power is however higher than the transistor theoretically should deliver when simulating the PA. In Section 4.1.1 V_{DD} has been calculated to be 31.6 V to deliver a maximum of 40 dBm output power. Figure 4.8b shows however that the maximum output power is higher than 40 dBm. This is the effect of the harmonics that are compressing the output signal and forcing the fundamental frequency component to have a higher magnitude than 31.6 V



(a) The output voltage when P_{in} = 20 dBm. At this point the output signal is compressed because the transistor is saturating



(b) The output power for the main transistor stage e.g. V_{DD} = 31.6 V

Figure 4.8: Harmonics effecting the signal at the output of the amplifier resulting in a higher output power than calculated

There are two approaches that can solve this problem:

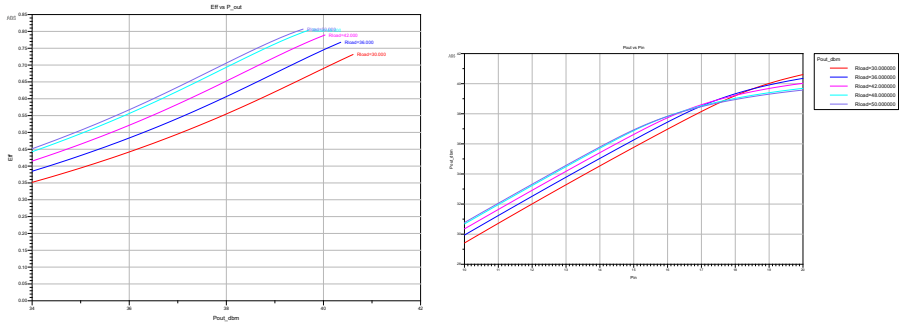
1. Only change V_{DD} : Changing V_{DD} to a lower value will result in a lower output signal and therefore will lower the output power to the desired 40 dBm.

2. Change V_{DD} and R_L: Changing the load that is visible from the perspective of the transistor will also fix the output power. First derive the V_{DD} which is needed to maintain 40 dBm and then calculate the load with $R_L = \frac{V_{DD}^2}{2*P_{out}}$.

As simply lowering the V_{DD} without changing R_L would quickly drive the peaking and main transistors into saturation before reaching their specified output powers of 34 dBm and 40 dBm, it has been chosen to lower both V_{DD} and R_L. In order to comply with [16], a $V_{DD,peak}$ of 28V was chosen with a

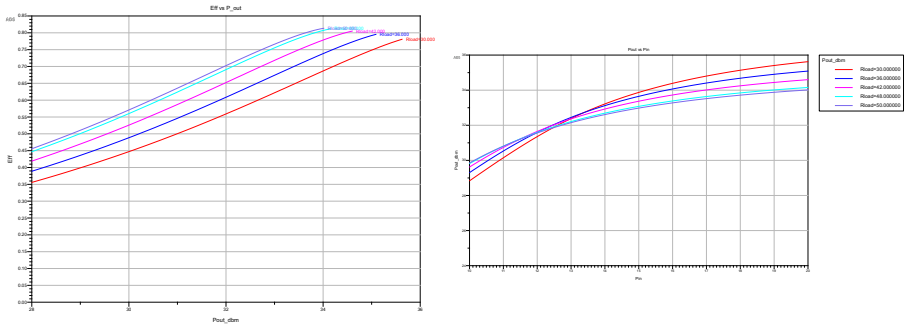
$V_{DD,main}$ of 14V. A lower V_{DD} is also beneficial due to the fact that the breakdown voltage of the device would be less easily reached at the drain. Keep in mind that due to the relatively low operating frequency, simply changing the load by putting a resistor in parallel with the 50Ω load is acceptable, thus no matching network is needed.

Figures 4.9 and 4.10 show the effect of changing the load impedance at V_{DD} = 28V and 14V respectively. Figures 4.9a and 4.10a show how the efficiency is affected by changing the load. A lower load resistance will need a higher current in order to supply the same output power. This higher current in turn dissipates more power in the active device when it is turned on. As a result the efficiency drops as the load resistance is lowered. Note that due to the increased current at the drain of the device, a new R_L must be chosen such that it does not surpass the device's current limit of 1.5A [16]. Despite the drawback of a lowered efficiency, Figures 4.9b and 4.10b show how a lower load resistance aids in delaying the input power at which the transistor saturates. Thus the required 34 dBm and 40 dBm peak output power for the main and peaking transistor is achieved much easier. As a good trade-off between efficiency and the amplifier not saturating before its peak output power is reached, a load resistance of 36Ω was chosen.



(a) Effect of changing R_L on efficiency. (b) Effect of changing R_L on P_{out}

Figure 4.9: Changing the load resistance R_L at V_{DD} = 28V.



(a) Effect of changing R_L on efficiency. (b) Effect of changing R_L on P_{out}

Figure 4.10: Changing the load resistance R_L at V_{DD} = 14V.

4.2.2 Controlling Harmonics

In order to DC couple the drain supply to the drain of the transistor, typically an infinitely large inductor (DC Feed) would be used in simulations [17]. The inductor poses as an infinitely high impedance to any AC signal while any DC signal treats the inductor as a short circuit. As an alternative to a high valued inductor in the drain bias, a λ/4-transmission line could be used. The main advantage of using a λ/4-transmission line over a high-valued inductor is that the transmission line will aid in reducing harmonic distortion in the output signal by filter out all even-order harmonics. The λ/4 line is thus used as short circuit λ/4 stub filter [18].

The λ/4 stub filter in the circuit works as follows: quarter wave transmission lines exhibit the behaviour that the impedance at one end of the line is the reciprocal of the impedance at the other end of it at the frequency where it is a quarter wavelength long. A half wave transmission line on the other hand exhibits the behaviour that the impedance at one end of the line is the same as the impedance at the other end of the line at the frequency where it is a half wavelength long. Due to the impedance of the voltage supply as seen by the transmission line is generally very low, ideally a short, the impedance at the other end is transformed to a high impedance (open circuit) for the quarter wave line while it is transformed to a low impedance (short circuit) for the half wave line. To any odd-order frequencies of 100 MHz, a quarter wave transmission line is seen while any even-order frequencies of 100 MHz see a half wave transmission line. As such the when λ/4-transmission line is tuned to the operating frequency of 100 MHz, any even order harmonics are filtered out of the output signal. Figure 4.11 shows the frequency contents of the output signal. This figure clearly shows the absence of any even order harmonics in the output signal and thus the short circuit stub works as expected. The only drawback when using a quarter wave line is the physical length it will take up in the PCB due to the relative low operating frequency. The wavelength in the line is equal to:

$$\lambda = \frac{c}{f \cdot \sqrt{\epsilon_r}} \tag{4.2}$$

Further efforts to also eliminate the odd order harmonics in the output signal can be made. One of the options we explored was the introduction of a open circuit quarter wave stub filter. This would however also filter out the fundamental frequency and is thus a very ineffective way of controlling harmonics introduced. A second option that was thought of was the introduction of series LC networks at the output at resonating frequencies tuned to the odd harmonics of 100 MHz. Functioning as notch filters they would provide low impedance paths to signals at their resonant frequency thus effectively providing us a way to filter out odd order harmonics. The introduction of these LC networks at the output would however require proper tuning such that they do not deteriorate the amplifier's efficiency. With the amount of harmonics that need to be filtered this would require a lot of time and quickly fall out of the scope of this project. The markers in Figure 4.11 do however show that the third order harmonic in the output is degraded by 28 dB compared to the fundamental component. This is within reasonable boundaries in order to allow for the absence of any output matching networks.

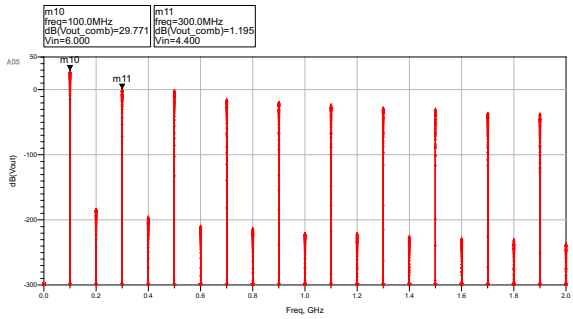


Figure 4.11: Frequency components of the output signal with λ/4 line added.

4.2.3 Input Impedance matching

To obtain maximum power transfer and to minimize the signal reflection at the input of PA, the input impedance of the PA should be matched with the characteristic impedance of the input source. Normally in RF applications and also in this project, the characteristic impedance of the input source is 50 Ω. Therefore a 50-Ω resistor should be placed in parallel at the input of the circuit to match the input impedance correctly. In Figure 4.12 the simulation results with and without the matching resistor can be seen. It can be seen that when not matched, the input impedance is varying a lot. From Equation 4.3 it can be seen that the voltage reflection coefficient is not zero when the load impedance Z_L , or input impedance of the PA in this case, deviates a lot from the characteristic impedance Z_0 of the input source. When Γ is not equal to zero, reflections will occur which is not desirable. Figure 4.12 shows however that the input is well matched, hence reflections are not likely to occur.

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.3}$$

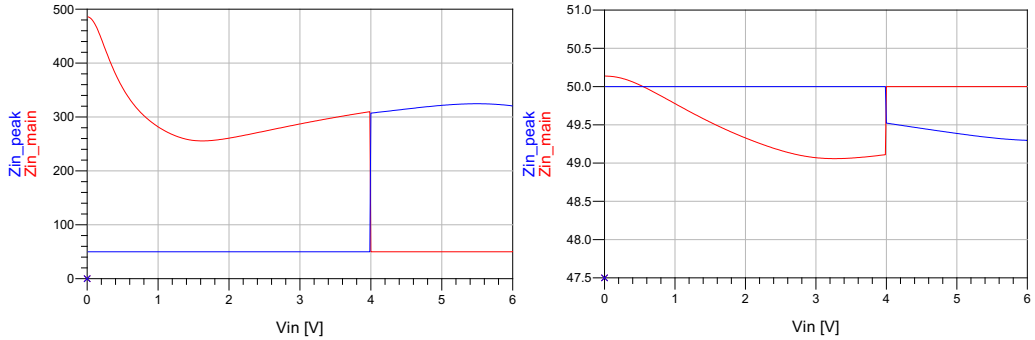


Figure 4.12: On the left: input impedance without matching resistor. On the right: input impedance with matching resistor. The red curves indicate the input impedance for the main transistor stage, the blue curves indicate the input impedance for the peak transistor stage

4.2.4 DC Coupling and Decoupling

Another main point to ensure that the prototype will function is the proper decoupling and coupling of DC and AC signals in the system. Coupling capacitors are used in the main line of the gate bias and drain are used to allow the high frequency signals to pass while it provides a large impedance to low frequency signals, especially DC. By using coupling capacitors in the circuit between different stages, the DC biasing points of the main and peaking transistors can be optimised such that they do not interfere with the RF signal. It has to be kept in mind that coupling capacitors will fulfill their role as long as there is enough capacitance and as such the precise value is not of importance. The only point of notice is that, as Figure 4.13 suggests, at high frequencies capacitors may start to act as inductors due to their dominant ESL. As such a component with a low ESL is preferred to drive the point at which the non-ideal capacitor starts to act like an inductor towards the higher frequency ranges.

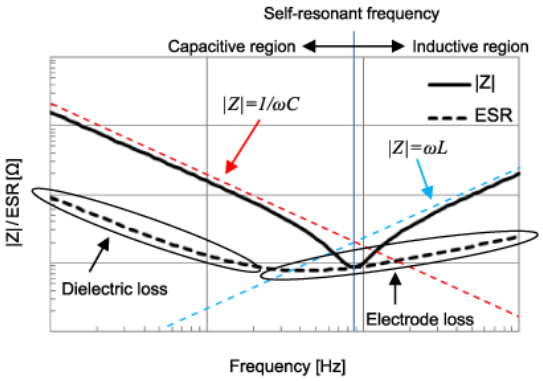


Figure 4.13: Capacitive and inductive regions of a non-ideal capacitor [19].

Bypass capacitors are added at the the DC supplies in the gate and drain bias networks. Bypass capacitors are usually used to form a low impedance path to high frequency signals while not interfering with the lower frequency signals, especially DC. The bypass capacitors in the design have two main functions. As a power supply bypass, the capacitor is used to stabilise the DC supply by providing a low impedance path to ground to all the disturbances on the DC signal. The PCB and interconnect in the circuit introduce all sorts of parasitic impedances (resistances and inductances). These parasitic impedances prevent current flowing from the supply into the devices and as such the bypass capacitors are used as temporary power supplies to maintain the voltage until the current is high enough to overcome the parasitic impedances [20]. In choosing a value for the power supply bypass capacitor, as 4.4 suggests, a larger value is desirable in order to keep the voltage ripple as low as possible. A value of 1 uF was chosen.

$$\Delta V = \frac{I \cdot \Delta t}{C} \tag{4.4}$$

The second use of the bypass capacitors in the drain bias networks is to bypass desirable signals to ground. As the main signals present at the DC power supply are that of the second harmonics due to the quarter wave transmission line, a bypass capacitor is added to resonate at the frequency of 200 MHz. A slight mismatch in the ESL may drive the capacitor to resonate at a different frequency and as such the value of the component here is critical to ensure the circuit works properly. Where normally these bypass capacitors would be chosen experimentally, we do not have the luxury as testing time is limited. A rule of thumb that was kept throughout the design was that components of size 0805 usually have an equivalent series inductance of 1 nH. Using this value and the fact that the resonant frequency should lie at 200 MHz, a capacitor of 630 pF is needed at the drain bias network according to equation 4.5. As the most dominant frequency in the gate bias network is the operating frequency of 100 MHz, the resonant frequency of the capacitor there should lie at 100 MHz. Thus a capacitor value of 2.53 nF is needed.

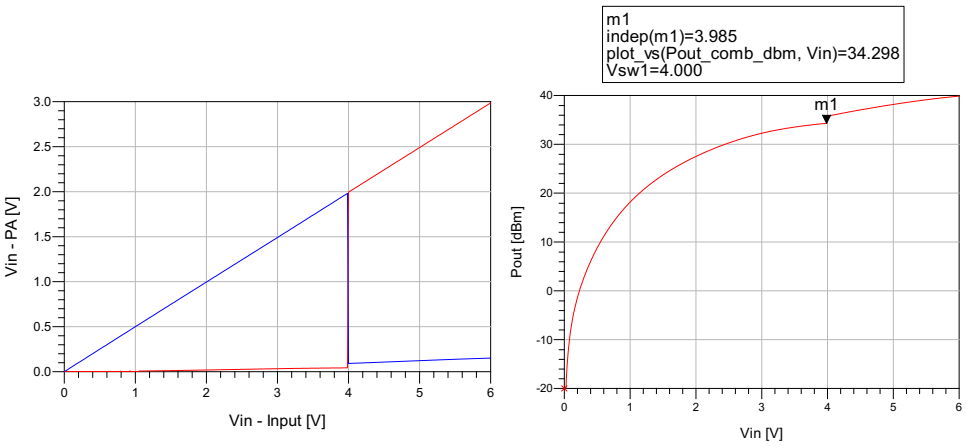
$$C = \frac{1}{(2\pi f_{res})^2 \cdot L} \tag{4.5}$$

4.2.5 Switching

The most important property of this PA that will be the trademark of this PA is the fact this it switching between two different stages to compose its output signal. This switching behavior is digitally controlled through setting the input signals of one of the two stages off when it's not needed. The point where this switching where this switching will be done, trivially called the *switching point*, is the point where the voltage of the input signal has reached a certain magnitude. Before this switching point, the main transistor stage will be used and after this switching point, the peak transistor stage will be used. This can be expressed with the following simple condition:

$$V_{in,main} = \begin{cases} V_{in} & \text{If } V_{in} < V_{sw} \\ 0 & \text{Else} \end{cases}$$
$$V_{in,peak} = \begin{cases} 0 & \text{If } V_{in} < V_{sw} \\ V_{in} & \text{Else} \end{cases} \tag{4.6}$$

Please note that Equation 4.6 can easily be expressed in terms of power if needed so. The drain voltages of the main and peak transistor stage has been designed in such a way that the peak transistor stage can deliver signals up to 40 dBm power and the main transistor stage until 34 dBm power. Therefore the switching point should be at 34 dBm output power which has the advantages that it will have the longest use of efficiency for the main transistor stage and that linearity is not too bad since the gain of the main transistor will drop after 34 dBm because it will turn into compression. Through optimization simulations, the input voltage where the output power equals 34 dBm is around at 4 V. Therefore the switching point is settled at 4 V. In Figure 4.14 the so called *switching curves* can be seen. The efficiency profile that will identify this PA can be seen in Figure 4.15.



(a) The input signal for both stages is digitally controlled. The blue curve resembles the main transistor stage, the red curve resembles the peak transistor stage.

(b) The output power that where around 34 dBm the input signal is switched.

Figure 4.14: Switching profiles for a switching point of 4 V.

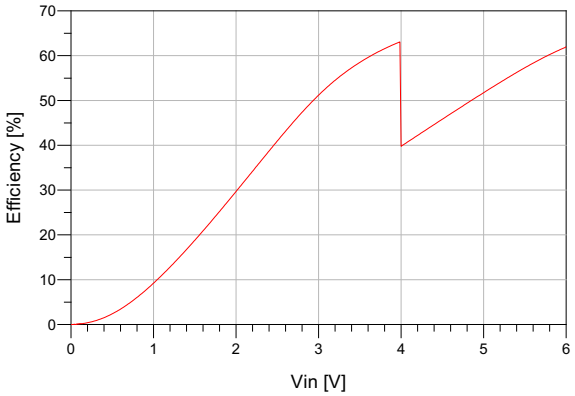


Figure 4.15: The efficiency profile when using direct switching.

Beside the basic switching equation that is denoted in Equation 4.6, a more complex linear switching curve has been worked out. The equation for this linear curve is denoted in Equatino 4.7.

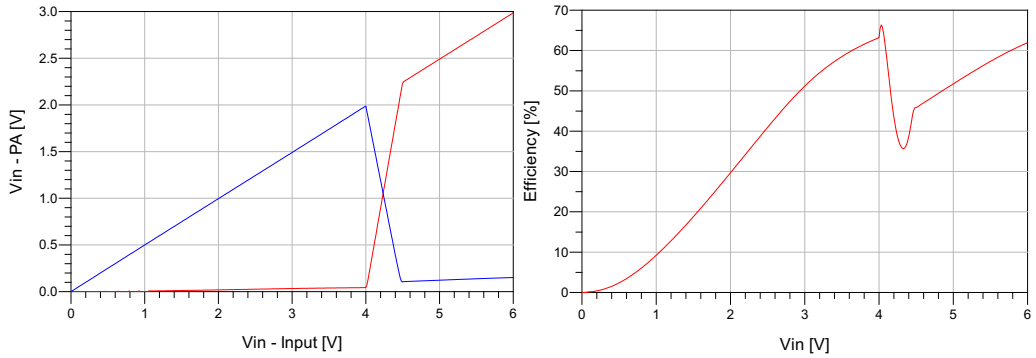
$$V_{in,main} = \begin{cases} V_{in} & \text{If } V_{in} < V_{sw1} \\ V_{sw1} - a(V_{in} - V_{sw2}) & \text{If } V_{in} < V_{sw2} \\ 0 & \text{Else} \end{cases}$$

$$V_{in,peak} = \begin{cases} 0 & \text{If } V_{in} < V_{sw1} \\ b(V_{in} - Vsw2) & \text{If } V_{in} < V_{sw2} \\ V_{in} & \text{Else} \end{cases} \tag{4.7}$$

The parameters a and b determine the gradient of the curves and are set successively by $\frac{V_{sw1}}{V_{sw2}-V_{sw1}}$ and $\frac{V_{sw2}}{V_{sw2}-V_{sw1}}$ where V_{sw1} and V_{sw2} determine the switching domain, e.g. the domain of input voltages in which the switching behavior occurs. V_{sw1} has the same value as the switching point that has been used for Equation 4.6 e.g. 4 V. The second switching point, V_{sw2} can set to different values to obtain different switching characteristics. In Figure 4.16 the characteristics of this linear switching can be seen when setting V_{sw2} to a test value of 4.5 V. From Figure 4.16b it can be concluded that the efficiency shows different behavior than the efficiency profile that Figure 4.15 resembles. The linear switching method is however such complex that it would require a complete new study to investigate in the possible implementations that can be done. Therefore the simple switching method from Figure 4.14 is used in this design.

4.3 Combining Network

The PA that is designed consists of two transistor stages (or even more when future improvements will be done) that will be responsible for building a stable output signal. As has been explained the problem of reverse conduction is a major issue with respect to the efficiency and therefore a good combining network can be critical for the performance of the PA. As have been explained, a solution to the problem of reverse conduction is biasing the transistor deep in class B. However, a combining network that is capable of isolating both stages in a loss-less way would also be a proper solution that would gradually improve the efficiency.



(a) Implementation of linear switching rather than hard switching. The blue curve resembles the main transistor stage, the red curve resembles the peak transistor stage.

(b) The effect on the efficiency when using linear switching. The first switching point is at 4 V and the second switching point is at 4.5V

Figure 4.16: Characteristics of linear switching

A combining network that has been researched is the Wilkinson Power Combiner (WPC) [21] which can be seen in Figure 4.17. The values for $Z0$ and $Z1$ are $\sqrt{2}R_{out}$ and $R = 2R_{out}$. It can be shown that these values will lead to perfect matching of the input and output impedance. The two line impedances are both $\lambda/4$ impedance transformers which will shift the signal 90° in phase. The working principle is as follows: Assume that on port S1 a signal is present. There are two paths that the signal can traverse to arrive at terminal S2:

1. Directly to S2 via the resistor R. This signal will be called $V1$.
2. Via the path $Z0 \rightarrow Z1$. The two $\lambda/4$ impedance transformers will shift the signal 90° which result in a 180° shifted signal at S2. This signal will be called $V2$.

At port two, both $V1$ and $V2$ are present now. Signal $V2$ is a copy of signal $V1$, but 180° shifted in phase.Therefor both signals will cancel out, ideally letting no current flow to terminal S2. The same principle holds for any signal that is present at terminal S2. In this way both terminals can ideally be isolated from each other, while still delivering their power to R_{out}

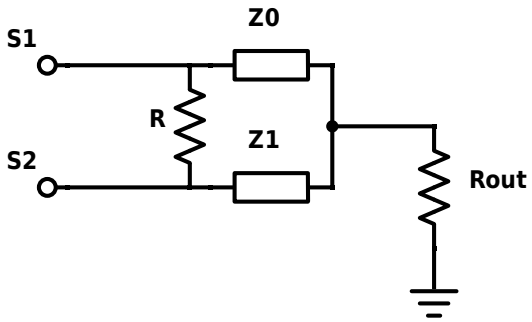
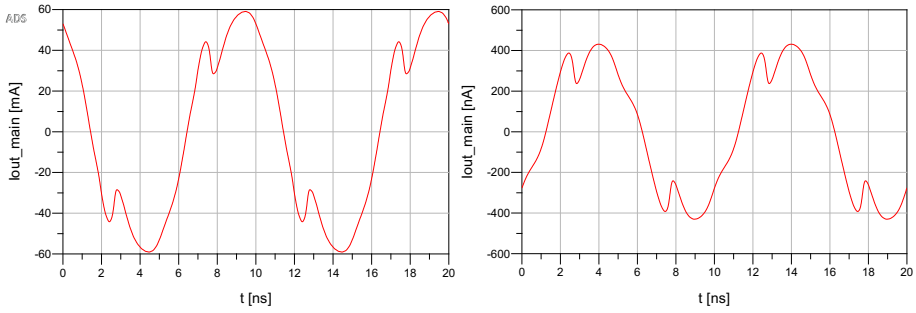


Figure 4.17: Simple configuration of a Wilkinson Power Combiner

The WPD has been simulated in the circuit by applying a signal with 18 dBm power on the peak transistor stage and measuring the output current that will flow at the main transistor stage. Results from these simulations show however that it results in a lower efficiency profile which can be seen in Figure 4.19. As Figure 4.18 shows, the isolating functionality of the WPD does work correctly since almost no current is flowing through the output of the main transistor stage. The lower efficiency is however an effect

of the load impedance of the WPD since this load must dissipate power. This is not desired and therefore the Wilkinson Power Divider is excluded from the final design.



(a) The main output current when using no WPD network

(b) The main output current when using a WPD network

Figure 4.18: The different output current profiles. Be aware of the difference in magnitude.

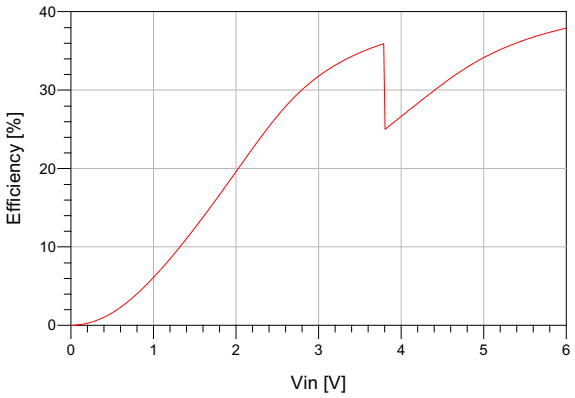


Figure 4.19: Drain efficiency when using a Wilkinson Power Combiner

4.4 Stability Analysis

A further important Figure of merit to power amplifiers is stability. When a portion of a circuit has gain, the circuit may oscillate [22]. As such passive devices that prohibit the injection of extra energy into the applied signal are not able to oscillate while active devices where an external energy source is contributing to the magnitude of the response of the circuit can start to oscillate, be it a wanted or unwanted type of oscillation. The concept of unwanted and unexpected oscillations within the circuit is seen as circuit instability. As a result of the circuit oscillating certain ”impossible” DC voltages may be detected or the resulting waveforms may be extremely noisy. In the worst case, instability of an amplifier circuit may cause the network to break down. Even a brief period of oscillations within the network may permanently damage the active device due to large voltages and power levels that could be generated as a result.

A number of measures exist to verify whether a circuit is unconditionally stable such as the Rollet factor K [23], μ [24], B_1 and B_2 [23]. Unconditional stability conditions allow any source or load impedances with their respective reflection coefficients Γ_S and Γ_L ($0 < \Gamma < 1$) at the terminations of the amplifier without the possibility of any oscillations occurring. As a measure for unconditional stability within the circuit we will limit ourselves to the Rollet stability factor K as it is the easiest one to use while it provides a clear conclusion to the stability of the network. The stability factor K is defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{4.8}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.9}$$

Equations 4.8 and 4.9 show that the stability factor K is defined through the use of S-parameters and as such design and analysis of the stability network will have to be done with S-parameter simulations in ADS. To have a better understanding of the simulation results we felt it was necessary to shortly mention the objects in the S-matrix and their generic descriptions.

- S_{11} is the input port voltage reflection coefficient
- S_{12} is the reverse voltage gain
- S_{21} is the forward voltage gain
- S_{22} is the output port voltage reflection coefficient.

In order for the system to be proven to be unconditionally stable the following conditions apply to the stability factor K:

$$K > 1 \quad |\Delta| < 1 \tag{4.10}$$

In addition to looking at the conditions stated above, a number of things should be taken into account when designing the stability network. Since the stability factor K is only defined for SISO 2-port networks whereas the amplifier designed is a system with 2 inputs and 1 output, we decided to design the two different stages of the amplifier separately such that each stage will be unconditionally stable. From this point we felt it was acceptable to conclude the two stages combined will be unconditionally stable as well. In addition, it should be noted that unconditional stability in the amplifiers should not only apply to the operating frequency of 100 MHz, but for a wide range of frequencies. Special care should be given to the lower frequency bands since oscillations occur much easier due to the higher gain available at these frequencies. Furthermore the input impedance at the operating frequency should be matched to 50Ω as much as possible.

In order to ensure stability at lower frequencies a RC network is added and using the Optimize and Tune functions of ADS by incorporating the conditions set in Equation 4.10 as goals, suitable values for the ideal components as well as the RC network can be chosen such that the system is unconditionally stable as well as matched to a 50Ω input impedance. In Figure 4.20 the designed stability network can be found. Note that the inductor of 400 nH is placed in series with the bias voltage source. This will prevent any AC signal to be present at the DC voltage source. The stability network integrated in the final PA, with the tuned parameters, is shown in Figure A.1 in Appendix A. Note that since analysis of the same network at both $V_{DD,peak}$ and $V_{DD,main}$ resulted in an unconditionally stable network, it was decided that the stability networks for both peaking and main amplifier would be held the same to ease the process of finding components.

Figures 4.21 and 4.22 show the simulation results for the S-parameter simulations from 0 Hz to 3 GHz. Figures 4.21a and 4.21b show clearly how the conditions for unconditional stability are reached. The markers show the minimum value of K which are verified to be larger than unity while Δ is kept below unity. K is exceptionally high for the lower frequencies as was the purpose of the RC network. A clear list of values for K and Δ can be found in Appendix A Furthermore, figures 4.22a and 4.22b show how the input and output impedances are matched to Z_0 = 50Ω. We can see that the input is closely matched to 50Ω while the output impedance is not. Since one of the requirements stated in Section 1.4 for the project was that no impedance transformations had to be done to the output, it is beyond the scope of this project to deal with.

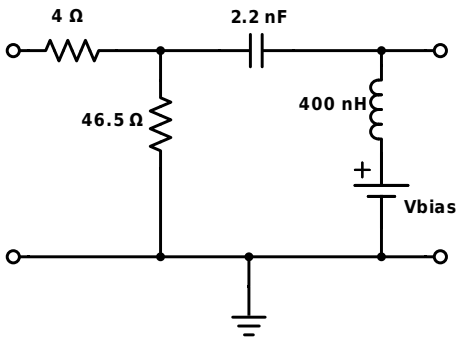
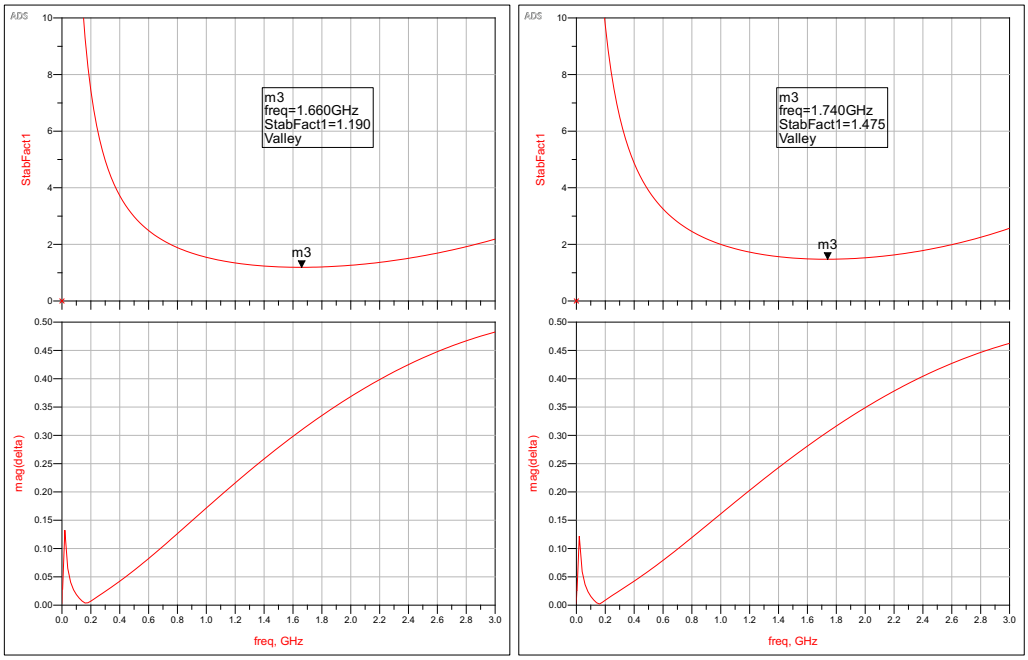


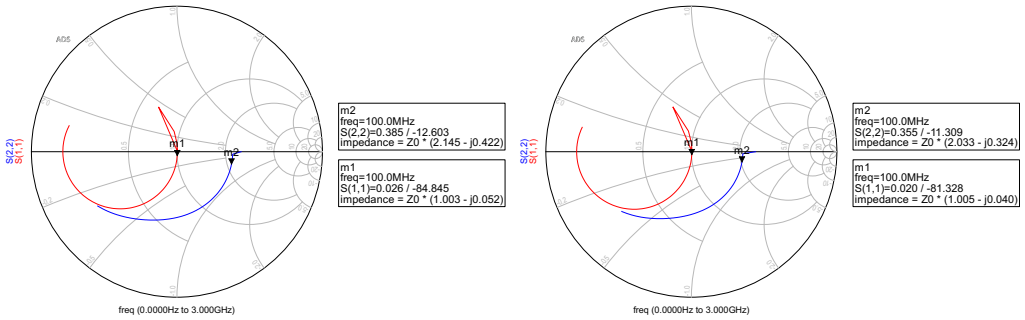
Figure 4.20: The circuit that has been designed to improve stability



(a) Rollet factor and Δ for V_{DD} = 14 V

(b) Rollet factor and Δ for V_{DD} = 28 V

Figure 4.21: S-parameter simulations from 0 Hz to 3 GHz to extract the Rollet factor and Δ



(a) Input and output reflection coefficients for V_{DD} = 14 V

(b) Input and output reflection coefficients for V_{DD} = 28 V

Figure 4.22: S-parameter simulations from 0 Hz to 3 GHz to extract the input and output reflection coefficients

4.5 System Evaluation

This section will try to evaluate all the simulations done on the final design of the variable gain interpolating supply amplifier and relate them back to the design requirements as stated in Section 1.4. The final circuit under test is shown in Figure 4.23 with all values of components and bias points shown. These values serve as reference to the outcome of the simulations.

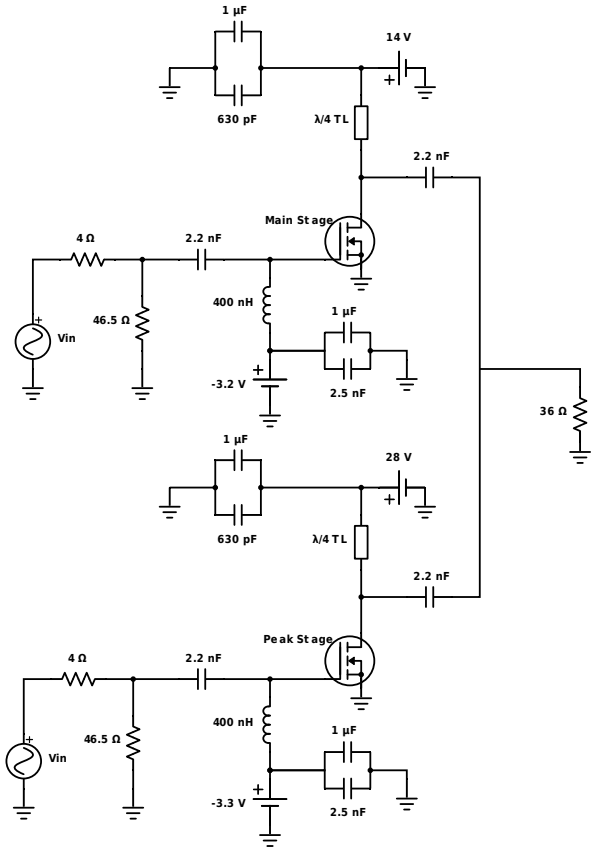
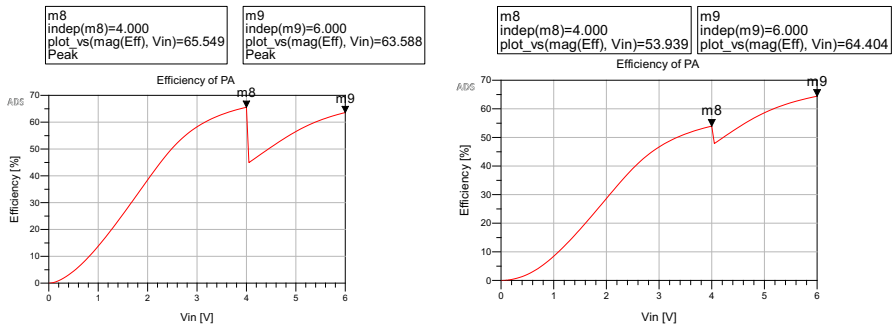


Figure 4.23: PA circuit that is designed for RF Application

4.5.1 Drain Efficiency and Gain

The main Figure of merit being efficiency, it would be necessary to evaluate the efficiency of the total system first. Figure 4.24 shows the peak drain efficiency of the variable gain PA at a $V_{GS,peak}$ of -3.2V and -3.3V and $V_{GS,main}$ of -3.2V. As discussed earlier a suitable DC bias value to ensure the transistors are operating in class B while maintaining a relatively linear gain is -3.2 V. Due to the problem of the peak transistor acting as a load when the main transistor is turned on and vice versa, efficiency is degraded. By biasing the peak transistor to -3.2 V, an even lower quiescent is applied to the peak transistor and thus it dissipates less power when the main transistor is conducting. Figure 4.24 shows that the peak efficiency of the main transistor is raised by 12% when changing the gate bias of the peak transistor to -3.2V. As the markers in Figure 4.24a highlight, the main and peak transistor reach peak efficiencies of 65.5% and 63.5% respectively. As such the the requirement that the system have a peak efficiency higher than 60% has been reached.



(a) $V_{GS,main}$ = -3.2V and $V_{GS,peak}$ = -3.3V. (b) $V_{GS,main}$ = -3.2V and $V_{GS,peak}$ = -3.2V.

Figure 4.24: Efficiency curves of the final design.

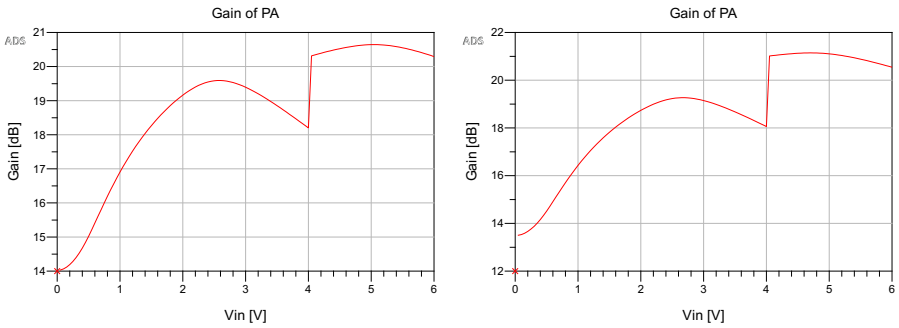
Changing the gate bias to an even lower value to ensure a low quiescent drain current, does however have a negative influence on the linearity of the gain of the system. Figure 4.25 shows the effect of this change on the linearity of the gain. It also shows why the choice of only lowering the bias value of the peak transistor was made instead of lowering the bias of both transistors to -3.2V. As the swing of the gain in the peak transistor is much lower than that of the main transistor, we deemed it affordable to further degrade the gain linearity of the peak transistor where the impact on the gain linearity of the main transistor would be too high. As is shown in Figure 4.26. Figure 4.25a shows that the maximum ripple in gain is equal to 6.5 dB which is way higher than the specified ripple of 2 dB in Section 1.4. To solve this a more preferable gate bias could be chosen such that the transistors operate in deep class AB. Due to the problem of not being able to change the bias when the transistor is supposed to be turned off however, a bias point near V_{TH} is the only way to ensure high peak efficiency, the main objective of the project.

4.5.2 Input Impedance

Figure 4.27 shows how the input impedances $Z_{in,main}$ and $Z_{in,peak}$ vary as a signal is applied to the input. As stated in Section 4.4, care was taken in the design of the stability network to match the input to 50Ω. The result clearly shows that the input is properly matched to 50 Ω at 100 MHz, like Figures 4.22a and 4.22b suggested.

4.5.3 Peak Output Power

As part of one of the design requirements, the main amplifier and peak amplifier should be able to output 34 dBm and 40 dBm peak output power respectively. Markers m7 and m12 in Figure 4.28a show that the main transistor can provide a peak output power of 34.2 dBm while the peak transistor provides a peak output power 39.9 dBm. In ensuring that the variable gain supply interpolating amplifier could provide an



(a) $V_{GS,main}$ = -3.2V and $V_{GS,peak}$ = -3.3V. (b) $V_{GS,main}$ = -3.2V and $V_{GS,peak}$ = -3.2V.

Figure 4.25: Gain curves of the final design.

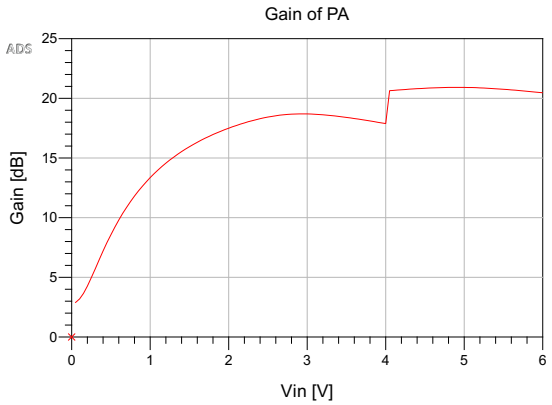


Figure 4.26: Effect on the Gain by lowering $V_{GS,main}$.

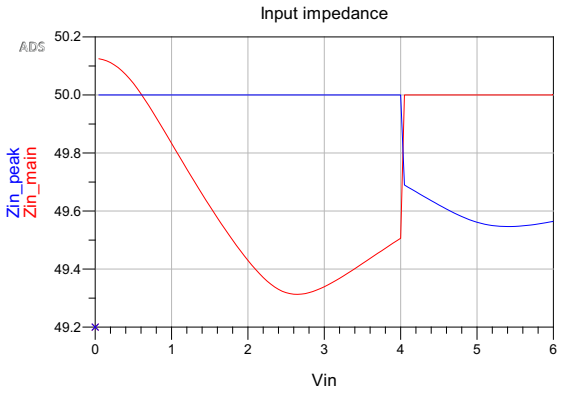
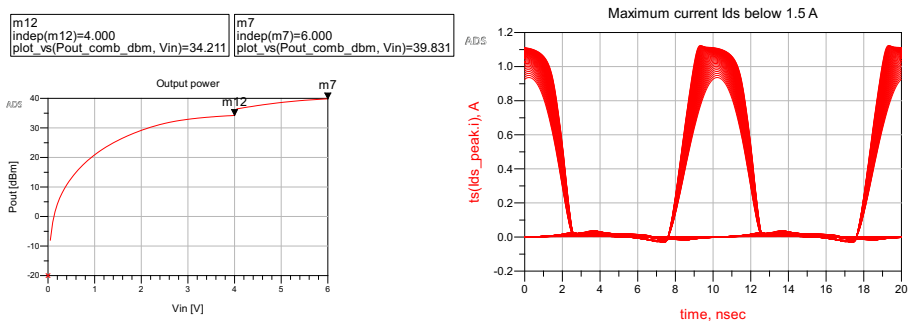


Figure 4.27: Input impedances of the main and peak amplifiers.

output power of 40 dBm at a supply rail of 28V before entering saturation, the load was lowered to 36Ω. This however meant that the current at the drain of the devices would increase. The datasheet states that the active devices used, tolerate a maximum drain current of 1.5A. Figure 4.28b shows that the drain current stays below the maximum value of 1.5A. It also shows the expected half-sinusoidal drain current that is expected of devices operating in class B.



(a) Output power curve of final implementation. (b) Maximum drain current

Figure 4.28: Efficiency curves of the final design.

4.5.4 Linearity

As stated in chapter 1.4, the examining and reduction of the influence of harmonics were deemed secondary objectives throughout the project. A widely used figure of merit when it comes to quantifying the linearity of a system is THD. The THD is defined as the ratio of the sum of the output powers of all harmonics against the output power of the fundamental:

$$THD = \frac{\sum_{n=2}^{\infty} P_n}{P_1} \tag{4.11}$$

A lower THD will thus mean that there is less harmonic distortion in the system. Figure 4.29 shows the THD of the system over its input power sweep. In order to comply with the limits of the measurement devices used, we limited ourselves to the 10^{th} harmonic in the output signal in examining the THD. The figure shows that the total harmonic distortion in the system is exceptionally low throughout the whole input power range reaching a maximum of only -18 dB. The absence of harmonic distortion in the output signal, like shown in chapter 4.2.2, is mainly due to the addition of the quarter wave line. Though its functionality is mainly as a DC feed to the drain of the transistor, it helps greatly in filtering the even order harmonics from the output signal, shown by the low THD of the system.

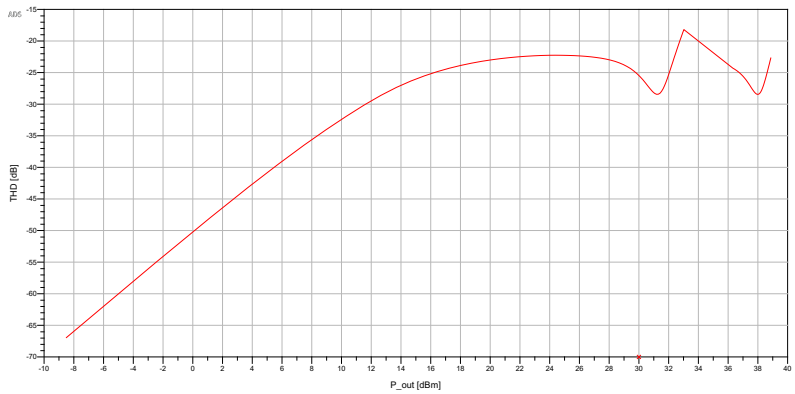


Figure 4.29: Total Harmonic Distortion of the system.

4.6 Layout Design

As part of the requirements of producing a working prototype, a PCB layout had to be designed in order to be able to fit the components and test the eventual two stage power amplifier. In order to minimise the possibility of any complications occurring with the design of the PCB we limited ourselves to a number of design constraints.

- Due to potentially high currents in the system, especially at the output, traces will be kept to a standard width of 60 mils.
- Traces will only be used at 45° angles.
- A standard convention of GND-SIGNAL-GND is used with a spacing of 30 mils.
- For stability purposes, component placement will be done as close to the gate of the active device as possible. This aids in further ensuring no unwanted oscillations occur within the system.
- To ease the measurement of voltages and currents within the circuit, the PCB will have as many grounding planes as possible
- For simplicity, the PCB will only consist of two layers of which the bottom layer functions as GND.
- The PCB's physical dimensions will be in the same order as that of the cooling element.
- In order to comply with the physical thickness of the transistor, the thickness of the PCB is chosen to be 1 millimeter.
- Pads for the components will be in 0805 size. To ease the process of choosing components, the spacing between the pads will be smaller such that 0603 components will fit as well.
- A footprint for the transistor has to be made according to the transistor dimensions in [16].

The initial PCB layout is shown in Figure 4.30. To further ease the process of production, it was decided to maintain a single layout for both the variable gain and variable bias amplifiers. The final PCB layout is shown in Figure 4.31. The footprints used for the component pads, SMA connectors and transistors can be found in Appendix B. The final layout shows the RC networks in the main lines that are used for the stabilising the network over a broad frequency range. In addition to that, capacitors are included at the gate bias to form an RF ground at the bias point while coupling capacitors in the main line ensure that no DC current flows into the source. At the drain connections for the $\lambda/4$ transmission line are made while decoupling capacitors and bypass capacitors are added to ensure ripple in the voltage supply and inductances introduced with the traces do not interfere with the integrity of the power supply.

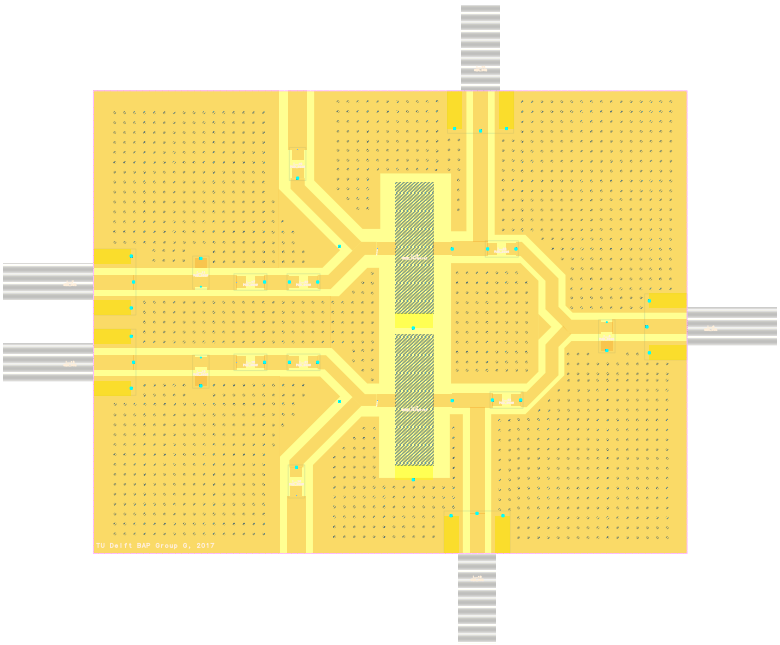


Figure 4.30: Initial PCB layout.

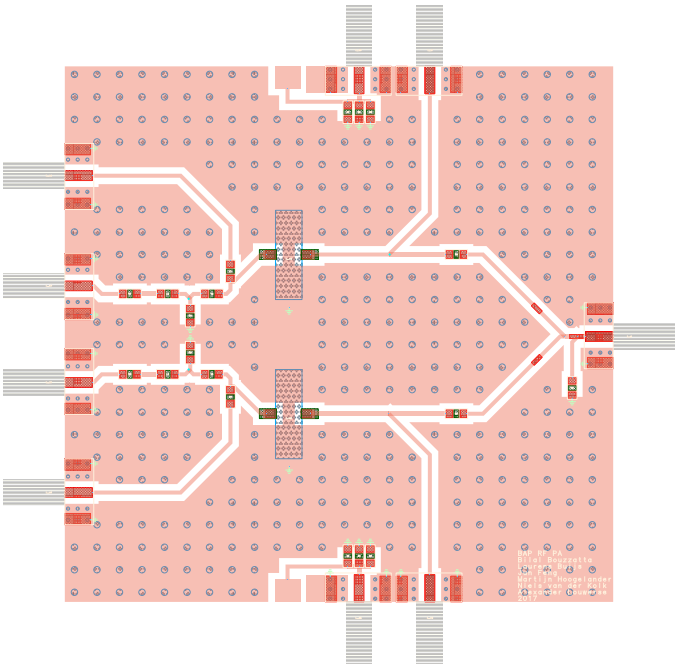


Figure 4.31: Final PCB layout.

Chapter 5

Measurements and Simulations

This section will try to relate all the measurements done on the prototype to the simulations done in ADS and shown in Chapter 4.5 in order to verify whether the design meets the required design specifications. As explained in Chapter 1.2, the measurements on the prototype are done by the measurement group. The testing of the prototype is done according to the setup shown in Figure 5.1.

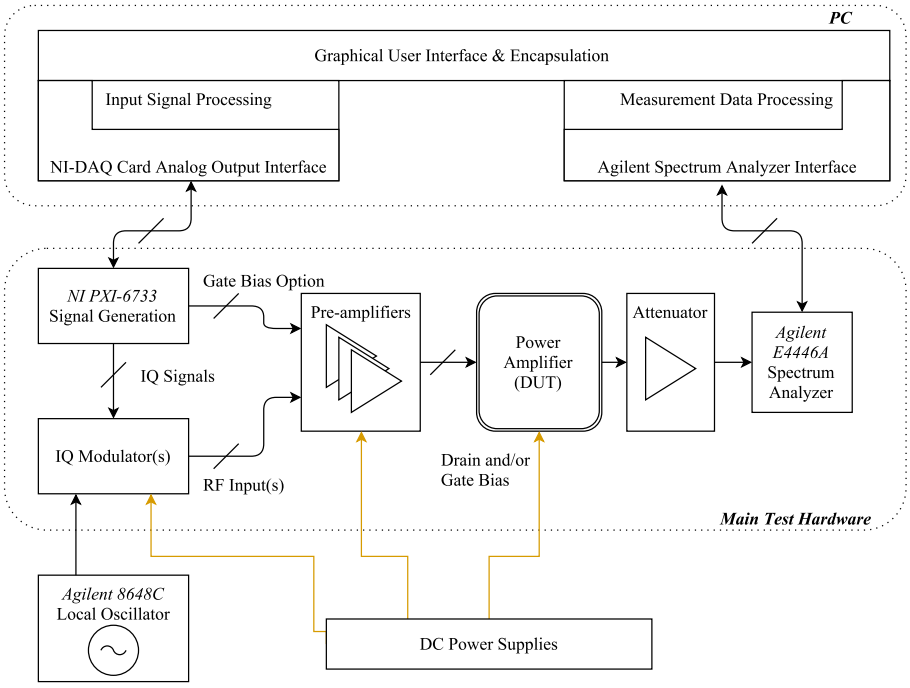


Figure 5.1: Test setup used throughout the measurement phase of the project.

In order to ensure testing of the prototype is done as accurately as possible, care had to be taken of a number of points before testing. First of all, as shown in Figure 5.1, the measurement system uses an attenuator at the input of the spectrum analyser as the specified peak output power of 40 dBm surpasses the maximum specified input power of 30 dBm tot the spectrum analyser. This means that it should be kept in mind at all times that the data acquired from the spectrum analyser is attenuated by 42.9 dBm. Secondly, the datasheet suggests that the threshold voltage V_{th} of the active devices may fluctuate between -3.8V and -2.3V. Thus the biasing the main and peak of the prototype at the specified V_{GS} of -3.2V and -3.3V may force the transistors to act according to simulated behaviour as discrepancies exist between the transistor model and the device itself. To prevent the differences in the threshold voltage between devices from influencing the device's behaviour, biasing of the prototype should be done according to the quiescent

applied current instead of the applied gate voltage. Figure 5.2 suggests that the prototype should be biased to a drain current of 3 mA and 7 mA for the peak and main amplifier respectively. Lastly, as it is not possible to dynamically switch the input signal the testing of the different amplifier stages has to be done separately, as denoted in the simulations by main and peak.

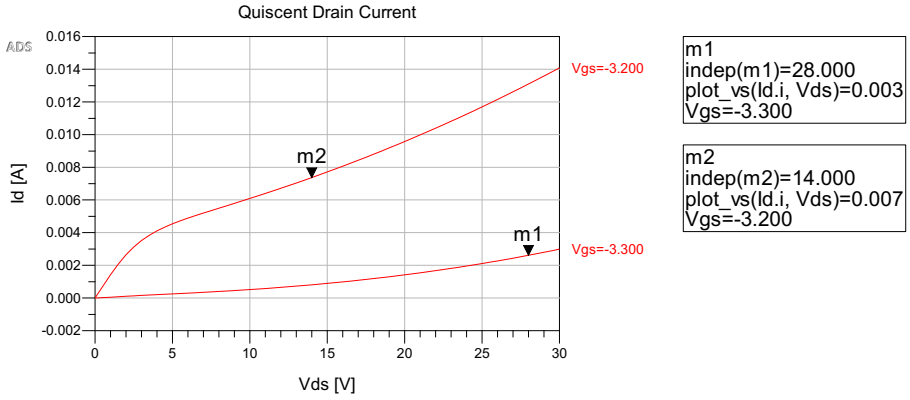
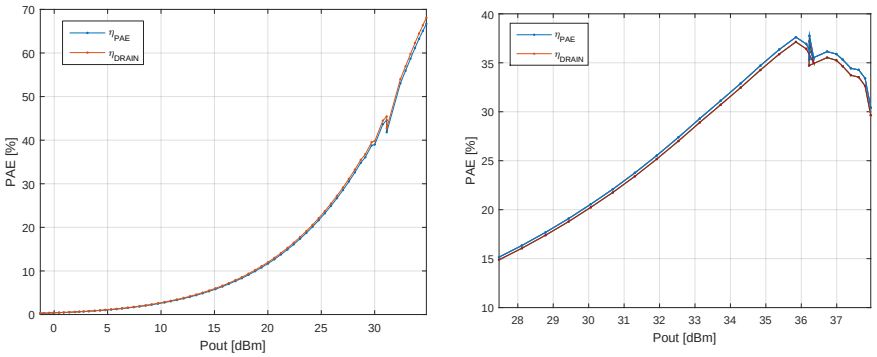


Figure 5.2: Quiescent drain current bias in the variable gain interpolating supply amplifier.

5.1 Drain Efficiency and Gain

Figure 5.3 shows the measured drain efficiency and PAE of the main and peaking amplifier. The main amplifier is measured to have a a drain efficiency of 59% at a peak output power of 34 dBm. This is in close agreement to the simulated value of 65.5%, especially considering that the interconnect in the simulations are regarded as loss less while in practice they pose as some kind of impedance to power supply thereby dissipating power. The fact that the measured results are in close agreement to the simulated ones for the main amplifier stage was however very much expected due to the low biasing point of the peaking amplifier. This means that the DC power dissipated in the peaking transistor is relatively low compared to the DC power supplied to the main transistor. Figure 5.3b shows the peak amplifier reaches a measured peak drain efficiency of 37% at an output power of 35.8 dBm before the efficiency degrades. This implies that the peak amplifier enters saturation after it reaches an output power of 35.8 dBm. Comparing the simulated peak drain efficiency of 63.5% to the measured drain efficiency, we see that the peak amplifier is greatly lacking in performance compared to the main amplifier. This was expected to a degree because of the higher drain current in the main amplifier that leads to an overall higher DC consumption. This hypotheses can be confirmed by looking at the actual DC power consumption in the main amplifier when only the peak amplifier is supposed to be conducting as shown in Figure 5.4. Figure 5.4 clearly shows how the DC power consumption in the main transistor directly contributes to the degrading of the efficiency of the peak amplifier. At high output powers, the power dissipation in the main amplifier increases rapidly which might be an explanation for the drop in efficiency before the amplifier reaches an output of 40 dBm rather than entering saturation as was previously thought.

The design specifications of the interpolating supply amplifier specified a minimum peak efficiency of 60% for both the main and peak amplifier at peak output powers of 34 dBm of 40 dBm. Looking at the measurements done it can be concluded that the main amplifier largely conforms to the simulations and design requirements. The peaking amplifier however did not meet the specified drain efficiency of at least 60%. Note that measurements of peak output for the peak amplifier could not be done as the measurement setup provided a limit of 18 dBm input power. Under the assumption that the above mentioned drop in efficiency is due to a higher power consumption in the main amplifier rather than the amplifier entering saturation, we do believe the peak amplifier should be able to output a power level of 40 dBm.



(a) Measured efficiency of the main amplifier. (b) Measured efficiency of the peak amplifier.

Figure 5.3: Measured efficiency curves.

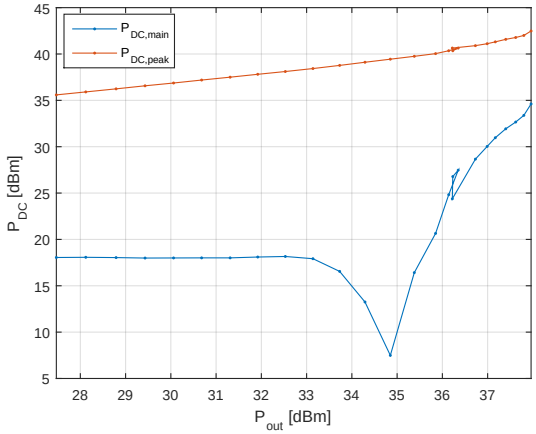
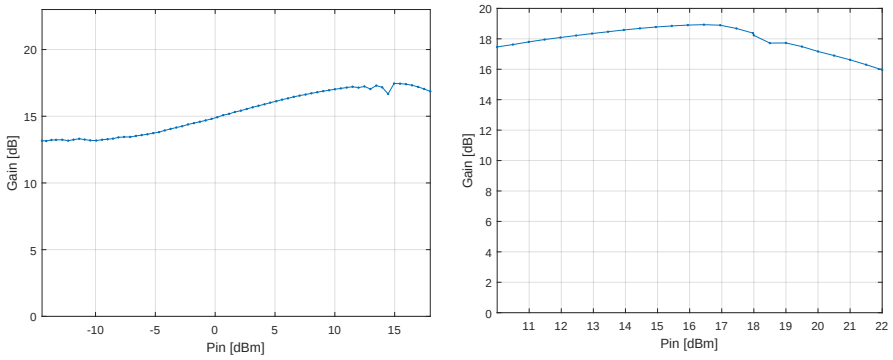


Figure 5.4: DC power consumption in the peak amplifier stage.

In assessing to what extent the gain of the prototype resembled that of the simulations and whether it reached the design specifications, measurements on the gain of the main and peak amplifier were done. The results are shown in Figure 5.5. Simulations of the gain of the system shown in Chapter 4.5 show that the main amplifier has a maximum gain ripple of 5.5 dB. The measurements in Figure 5.5a show that the prototype displays a gain ripple of about 4.5 dB. The average gain of the main amplifier is also degraded by 1 dB. This loss of gain in the measurements compared to simulations was however already estimated as the interconnect in the simulation is regarded to be loss less while in reality it dissipates power much like any impedance. The peak amplifier shows an average gain of 18 dB where the simulations suggested an average gain of 20.5 dB for the peak amplifier. This loss of gain could again be the cause of interconnect dissipating energy thereby introducing losses into the system.

The design specifications required an average gain of the system of 20 dB with a maximum ripple of 2 dB to ensure the gain profile is linear. From the simulations done in Chapter 4.5 it was already seen that both requirements individually could not be met when biasing the transistor so close to its threshold voltage. The linearity in the gain of the system was traded in for higher peak efficiency values.



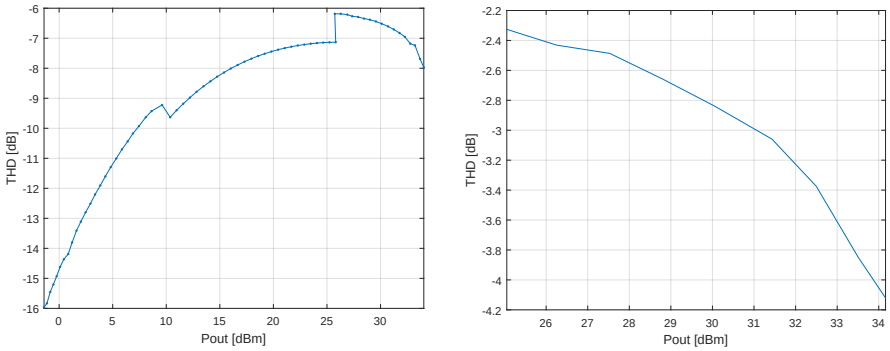
(a) Measured gain of the main amplifier.

(b) Measured gain of the peak amplifier.

Figure 5.5: Measured gain curves.

5.2 Linearity

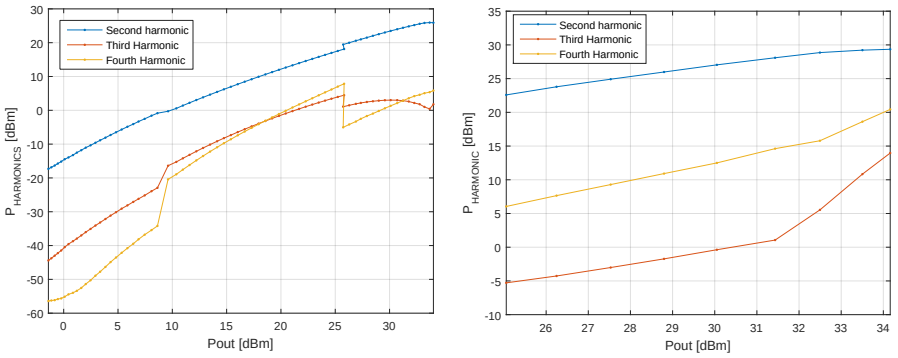
Figure 5.6 shows the measured THD over the fundamental output power as a measure for non-linearity for the main and peak amplifier. When comparing the measured THD against the simulated values shown in Figure 4.29, it becomes clear that the real output signal is much more harmonically distorted than the simulations showed. The maximum THD is 16 dB higher than was expected from looking at the simulations. As the figure of THD is merely a measure for quantifying the amount of distortion in the output signal, it does not provide us with a way of analysing where the distortion in the output comes from and at which frequencies it dominates. To that end we decided to measure the power of the individual harmonics and plot them against the fundamental output power. In order to keep a clear overview of the measurements, only the 2^{nd}, 3^{rd} and 4^{th} harmonic signals are viewed as the measurements showed they were the most dominating. The measurements are shown in Figure 5.7 for both the main and the peak amplifier. As can be seen in the figure, the largest contribution to the high measure THD values is due to the presence of the second harmonic. The negative influence of the compared to the fundamental component can especially be seen in the peak amplifier where P_2 is only degraded by 2.5 dB compared to the carrier frequency at a fundamental output power of 27.5 dB. This is however not in line with the expectations we had regarding linearity of the output signal. As explained and shown in Chapter 4.2.2, the addition of the $\lambda/4$ transmission line should have aided in filtering out all even-order harmonics. The apparent presence and dominance of even-order harmonics in the output signal is most likely due to a mismatch in the length of the transmission line. As explained before, the tuning of the transmission line needs to be very precise as it only works as intended to frequencies whose half-wavelength or quarter wave-length matches that of the length of the transmission line.



(a) Measured THD of the main amplifier.

(b) Measured THD of the peak amplifier.

Figure 5.6: Measured Total Harmonic Distortion.



(a) Harmonic power levels for the main amplifier.

(b) Harmonic power levels for the peak amplifier.

Figure 5.7: Harmonic power levels of the 2^{nd}, 3^{rd} and 4^{th} order.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis a RF Power Amplifier has been designed that has improved efficiency in the power back-off region to support newer modulation schemes that need a high PAPR. The PA consists of two stages were one is optimized for supporting the nominal power region of the output signal and the other is optimized for supporting the peak power region of the output signal which can be at maximum be 10 W. The input signals of the PA are digitally controlled to control which stage is used.

Several steps have been taken during this project to accomplish the desired behaviour that the final circuit should have. The most critical part with respect to the efficiency of the PA is to choose proper values for drain voltage V_{DD} and bias voltage V_{GS}. The amplifier has been designed to operate in class B which is the most suitable class for RF Amplifiers. However when biasing the transistor just above V_{TH}, both stages were always conducting which reduced the efficiency of the PA. One could lower V_{GS} to even lower values but this will give such a horrific gain profile that a trade-off had to be made between linearity and efficiency. Therefore for V_{GS} for the main stage has been set to -3.2 V and V_{GS} for the peak stage has been set to -3.3 V.

There has been brainstormed about finding a solution that can solve the problem of *reverse conduction*. One of these solutions that has been worked out was the Wilkinson Power Divider. This solution did manage to isolate both stages very well when they weren't needed. The problem of this network was that it however absorbed power and therefore reduced the efficiency even more than the problem of *reverse conduction* did. Therefore the WPD has not been implemented in the circuit. The problem of *reverse conduction* is still a problem, although its impact has been reduced as has been explained by properly choosing the bias voltages.

Also a stability network has been developed to improve the stability of the PA. Without a stability network the circuit can be become unstable which can lead to unwanted oscillations in the circuit. This can even cause the circuit to breakdown which is far from desired. Analysis and simulations on stability metrics such as the Rollet stability Factor have lead to a stability network that has improved the stability of the PA greatly. This circuit has been designed in such a way that it resonates at the carrier frequency of the input signal which greatly improves it performance at this frequency.

When comparing the result of the final PA design from Figure 4.23 with the design requirements that were listed in Section 1.4 we can conclude that the PA meets the following design requirements:

- **Desired Efficiency Profile**: The desired efficiency profile that should characterize this PA can be seen in Figure 4.24. The amplifier has two efficiency peaks: η_{main} = 65.5% and η_{peak} = 63.5%. Especially the first peak, η_{main}, is the desired peak that will support the energy-efficiency for high-PAPR modulation schemes.
- **Power Constraints**: The amplifier can deliver up to 10 W. Furthermore at 6 dB back-off e.g. P_{out} = 34 dBm the amplifier has its nominal efficiency peak.
- **Stable Frequency Behaviour**: The stability of the circuit is well ensured by inserting a RC network at each transistor input. The stability factor K is also exceptionally high for the lower frequencies (around 100 MHz) the PA has been designed for.

The gain profile of the PA that can be seen in Figure 4.25 shows that an input signal with a high power level will have a gain of more than 20 dB. However the gain ripple of the PA does not meet the 2-dB requirement that was set in Section 1.4. This is due to the trade-off that had to be made between efficiency and linearity. The initial goal when designing this PA was to have a better efficiency profile at power back-off than classical RF Amplifiers. The linearity of the PA had to suffer however to accomplish this efficiency profile. In Section 6.2.2 possible implementations are given to improve the linearity profile of the PA.

Furthermore, a PCB of the circuit has been developed so real measurements can be done on this circuit to see how it works out in practice. The results of these measurements can be seen in Chapter 5. The transistors though that were implemented on the PCB that has been manufactured deviated from the transistor model that has been used in simulations. The threshold voltage V_{TH} was higher several hundreds of millivolts higher than the simulated model which increased the inaccuracy of the operation point and therefore the efficiency profile. A solution to this inaccuracy was biasing the transistors of the PCB according to the applied quiescent current instead of the applied gate voltage.

The main transistor stage did perform very well at the measurements. Results of the efficiency measurements show that $\eta_{PAE} \approx 63\%$ which is a little higher than the efficiency that was aimed for (60%). Measurements on the gain profile of the main transistor stage showed that the PA was actually more linear than was simulated. The overall gain level was several dB lower than expected, but the reason behind this is that the simulations don't take all losses or any mismatches into account. The peak transistor stage did perform not as good as the main transistor stage. Results of the efficiency measurements show that $\eta_{PAE} \approx 37\%$ which is not even close to the required efficiency. Also the profile of the efficiency deviated from the expected efficiency profile e.g. high efficiency when the transistor is close to saturation. Measurements showed that the power supply of the main stage was delivering unnecessary much power which reduced the efficiency heavily. A possible cause for this problem can be bad suppression of unwanted harmonics. Figure 5.7b shows that the second harmonic was still present at the output of the PA at great magnitude.

6.2 Future Work

While this thesis has provided a fundamental theory for the development of an interpolating amplifier, there's still are lot of area's where improvement or investigation can be done.

6.2.1 Scaling the Frequency

This PA has been designed for 100 MHz, the reason being that at this frequency no complex behavior due to frequency has to be taken into account. However at microwave frequency bands frequencies range from 300 MHz up to 300 GHz, and these are the frequencies that are used for practical wireless communication systems. Especially 5G will use so called millimeter waves which have a frequency higher than 30 GHz. At these frequencies the simple lumped-element model is inaccurate because the wavelength of signals has the same dimension as elements in the circuit. Therefore distributed circuit theory must be used to make the circuit still use full at these frequencies.

6.2.2 Improving Distortion

The intention of this project was to enhance the efficiency for RF Power Amplifiers, especially in the power back-off region. In the steps that have been taken for designing the amplifier, a trade-off between linearity and efficiency had to be taken in order to make the amplifier not an extremely non-linear device. Choosing to improve linearity is however most of the times at the cost of efficiency, hence the linearity of the designed PA is not optimized at all.

There are however techniques that can improve the linearity of the PA. One of these techniques is called Digital Predistortion (DPD). This technique inversely models the gain and gain and phase profile of the amplifier and produces. When combined with the original amplifier, a linear model comes out that reduces the distortion that originally was introduced by the amplifier. DPD is a technique that can be done with a relative low budget since it's implemented digitally. Also another advantage of DPD is that it can be designed, orthogonal to the efficiency optimization of the amplifier since it won't change the PA circuit metrics at all; only the input signal of the PA is changed.

6.2.3 Optimal Efficiency for Different Power Regions

While the design of this PA has led to two different efficiency peaks at two specific power regions, it could be optimized for different power regions. The following two method can accomplish this:

Switching Behavior
In Section 4.2.5 linear switching curves have been investigated. These curves introduced such complex behavior that it was to complex for the scope of this project. However, smart use of these curves can result into a power region where the efficiency remains relatively high while still maintaining linearity.

Multiple Stages
Instead of two stages, multiple stages could be used to have multiple efficiency peaks. Furthermore these stages can have drain voltages that are designed to have their peak efficiency at a certain power level. When implementing these stages, one should take care of the problem of *reverse conduction*, since this can be problematic when utsing multiple stages.

Appendices

Appendix A

Stability Analysis

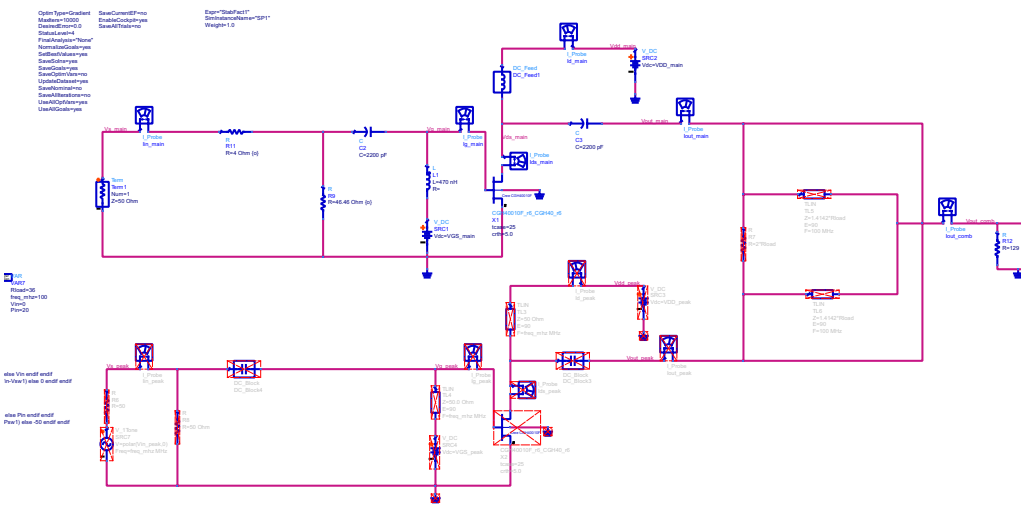


Figure A.1: Final network for both peaking and main amplifier.

freq	StabFact1		mag(delta)	
	...D_main=14.000	...D_main=28.000	...D_main=14.000	...D_main=28.000
0.0000 Hz	<invalid>	<invalid>	0.002	0.002
20.00 MHz	69.247	90.725	0.132	0.122
40.00 MHz	36.550	47.885	0.065	0.059
60.00 MHz	24.616	32.249	0.041	0.036
80.00 MHz	18.527	24.273	0.027	0.024
100.0 MHz	14.846	19.449	0.019	0.015
120.0 MHz	12.382	16.221	0.012	0.009
140.0 MHz	10.618	13.911	0.007	0.004
160.0 MHz	9.294	12.175	0.004	0.002
180.0 MHz	8.263	10.824	0.004	0.005
200.0 MHz	7.437	9.743	0.007	0.009
220.0 MHz	6.762	8.857	0.011	0.012
240.0 MHz	6.198	8.119	0.014	0.016
260.0 MHz	5.722	7.494	0.017	0.019
280.0 MHz	5.313	6.959	0.021	0.022
300.0 MHz	4.959	6.495	0.024	0.026
320.0 MHz	4.649	6.089	0.028	0.029
340.0 MHz	4.376	5.730	0.031	0.032
360.0 MHz	4.133	5.412	0.035	0.036
380.0 MHz	3.915	5.127	0.039	0.039
400.0 MHz	3.720	4.870	0.042	0.042
420.0 MHz	3.543	4.638	0.046	0.046
440.0 MHz	3.382	4.428	0.050	0.049
460.0 MHz	3.236	4.235	0.054	0.053
480.0 MHz	3.102	4.059	0.058	0.057
500.0 MHz	2.978	3.897	0.062	0.060
520.0 MHz	2.865	3.748	0.066	0.064
540.0 MHz	2.759	3.610	0.070	0.068
560.0 MHz	2.662	3.481	0.074	0.071
580.0 MHz	2.571	3.362	0.078	0.075
600.0 MHz	2.487	3.251	0.082	0.079
620.0 MHz	2.408	3.148	0.087	0.083
640.0 MHz	2.334	3.051	0.091	0.087
660.0 MHz	2.265	2.960	0.095	0.091
680.0 MHz	2.201	2.874	0.100	0.095
700.0 MHz	2.140	2.794	0.104	0.099
720.0 MHz	2.083	2.718	0.109	0.103
740.0 MHz	2.029	2.647	0.113	0.107
760.0 MHz	1.978	2.580	0.117	0.111
780.0 MHz	1.930	2.516	0.122	0.115
800.0 MHz	1.885	2.456	0.126	0.119
820.0 MHz	1.842	2.399	0.131	0.124
840.0 MHz	1.801	2.345	0.135	0.128
860.0 MHz	1.763	2.294	0.140	0.132
880.0 MHz	1.726	2.245	0.144	0.136
900.0 MHz	1.692	2.199	0.149	0.140
920.0 MHz	1.659	2.155	0.154	0.145
940.0 MHz	1.628	2.114	0.158	0.149
960.0 MHz	1.598	2.074	0.163	0.153
980.0 MHz	1.570	2.036	0.167	0.157
1.000 GHz	1.544	2.000	0.172	0.161
1.020 GHz	1.519	1.966	0.176	0.165
1.040 GHz	1.495	1.934	0.181	0.170
1.060 GHz	1.472	1.903	0.185	0.174
1.080 GHz	1.451	1.874	0.190	0.178
1.100 GHz	1.430	1.846	0.194	0.182
1.120 GHz	1.411	1.819	0.198	0.186
1.140 GHz	1.393	1.794	0.203	0.191
1.160 GHz	1.376	1.770	0.207	0.195
1.180 GHz	1.359	1.747	0.212	0.199
1.200 GHz	1.344	1.726	0.216	0.203
1.220 GHz	1.330	1.705	0.220	0.207
1.240 GHz	1.316	1.686	0.225	0.211
1.260 GHz	1.303	1.668	0.229	0.215
1.280 GHz	1.291	1.650	0.233	0.219
1.300 GHz	1.280	1.634	0.238	0.223
1.320 GHz	1.269	1.618	0.242	0.227
1.340 GHz	1.260	1.604	0.246	0.231
1.360 GHz	1.251	1.590	0.250	0.235
1.380 GHz	1.242	1.577	0.254	0.239
1.400 GHz	1.235	1.566	0.258	0.243
1.420 GHz	1.228	1.554	0.263	0.247
1.440 GHz	1.221	1.544	0.267	0.251
1.460 GHz	1.216	1.535	0.271	0.255
1.480 GHz	1.210	1.526	0.275	0.259
1.500 GHz	1.206	1.518	0.279	0.262
1.520 GHz	1.202	1.511	0.283	0.266
1.540 GHz	1.199	1.504	0.287	0.270
1.560 GHz	1.196	1.498	0.291	0.274
1.580 GHz	1.193	1.493	0.294	0.277
1.600 GHz	1.192	1.488	0.298	0.281
1.620 GHz	1.191	1.485	0.302	0.285
1.640 GHz	1.190	1.481	0.306	0.288
1.660 GHz	1.190	1.479	0.310	0.292
1.680 GHz	1.190	1.477	0.313	0.296
1.700 GHz	1.191	1.476	0.317	0.299
1.720 GHz	1.192	1.475	0.321	0.303
1.740 GHz	1.194	1.475	0.324	0.306
1.760 GHz	1.197	1.475	0.328	0.310
1.780 GHz	1.200	1.476	0.331	0.313
1.800 GHz	1.203	1.478	0.335	0.316
1.820 GHz	1.207	1.480	0.339	0.320
1.840 GHz	1.211	1.483	0.342	0.323
1.860 GHz	1.216	1.487	0.345	0.326
1.880 GHz	1.221	1.491	0.349	0.330
1.900 GHz	1.227	1.495	0.352	0.333
1.920 GHz	1.233	1.500	0.356	0.336
1.940 GHz	1.239	1.506	0.359	0.339
1.960 GHz	1.246	1.512	0.362	0.343
1.980 GHz	1.254	1.519	0.365	0.346
2.000 GHz	1.261	1.526	0.368	0.349
2.020 GHz	1.270	1.534	0.372	0.352
2.040 GHz	1.278	1.542	0.375	0.355
2.060 GHz	1.288	1.551	0.378	0.358
2.080 GHz	1.297	1.561	0.381	0.361
2.100 GHz	1.307	1.571	0.384	0.364
2.120 GHz	1.318	1.581	0.387	0.367
2.140 GHz	1.329	1.592	0.390	0.370
2.160 GHz	1.340	1.604	0.393	0.373
2.180 GHz	1.352	1.616	0.396	0.375
2.200 GHz	1.364	1.629	0.398	0.378
2.220 GHz	1.376	1.642	0.401	0.381
2.240 GHz	1.389	1.655	0.404	0.384
2.260 GHz	1.402	1.669	0.407	0.386
2.280 GHz	1.416	1.684	0.410	0.389
2.300 GHz	1.430	1.699	0.412	0.392
2.320 GHz	1.445	1.715	0.415	0.394
2.340 GHz	1.460	1.731	0.417	0.397
2.360 GHz	1.475	1.748	0.420	0.399
2.380 GHz	1.491	1.765	0.422	0.402
2.400 GHz	1.508	1.783	0.425	0.404
2.420 GHz	1.524	1.801	0.427	0.407
2.440 GHz	1.541	1.820	0.430	0.409
2.460 GHz	1.559	1.840	0.432	0.411
2.480 GHz	1.577	1.860	0.435	0.414
2.500 GHz	1.595	1.880	0.437	0.416
2.520 GHz	1.614	1.901	0.439	0.418
2.540 GHz	1.633	1.923	0.441	0.421
2.560 GHz	1.652	1.945	0.443	0.423
2.580 GHz	1.672	1.967	0.446	0.425
2.600 GHz	1.692	1.990	0.448	0.427
2.620 GHz	1.713	2.014	0.450	0.429
2.640 GHz	1.734	2.038	0.452	0.431
2.660 GHz	1.756	2.063	0.454	0.433
2.680 GHz	1.778	2.088	0.456	0.435
2.700 GHz	1.800	2.114	0.458	0.437
2.720 GHz	1.823	2.140	0.460	0.439
2.740 GHz	1.846	2.167	0.462	0.441
2.760 GHz	1.870	2.194	0.463	0.443
2.780 GHz	1.894	2.222	0.465	0.445
2.800 GHz	1.918	2.251	0.467	0.446
2.820 GHz	1.943	2.280	0.469	0.448
2.840 GHz	1.968	2.310	0.470	0.450
2.860 GHz	1.994	2.340	0.472	0.452
2.880 GHz	2.020	2.371	0.474	0.453
2.900 GHz	2.047	2.402	0.475	0.455
2.920 GHz	2.074	2.434	0.477	0.456
2.940 GHz	2.101	2.467	0.478	0.458
2.960 GHz	2.129	2.500	0.480	0.460
2.980 GHz	2.157	2.534	0.481	0.461
3.000 GHz	2.186	2.568	0.482	0.462

Figure A.2: Values of the stability factor K at V_{DS} = 28V and V_{DS} = 14V.

Appendix B

Layout Design

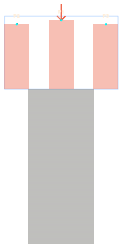


Figure B.1: Footprint of the SMA connector.

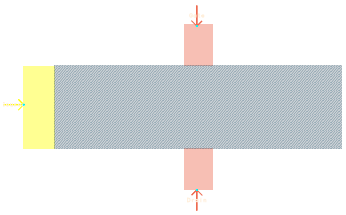


Figure B.2: Footprint of the CGH40010F transistor.

Figure B.3: Footprint of 0805/0603 pad.

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