Low-Power High Time Resolution Charge Detection ROIC in 40nm CMOS Technology

Zaki, Alireza Mohammad; Du, Yutong; Nihtianov, Stoyan

DOI
10.1109/I2MTC60896.2024.10560791

Publication date
2024

Document Version
Final published version

Published in
I2MTC 2024 - Instrumentation and Measurement Technology Conference

Low-Power High Time Resolution Charge Detection ROIC in 40nm CMOS Technology

Alireza Mohammad Zaki
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
A.R.Mohammadzaki@tudelft.nl

Yutong Du
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
Y.Du-10@student.tudelft.nl

Stoyan Nihtianov
Department of Microelectronics
Delft University of Technology
Delft, The Netherlands
S.Nihtianov@tudelft.nl

2024 IEEE International Instrumentation and Measurement Technology Conference (I2MTC) | 979-8-3503-8090-3/24/$31.00 ©2024 IEEE | DOI: 10.1109/I2MTC60896.2024.10560791

***Abstract*— State-of-the-art readout integrated circuits (ROICs) operating in particle-counting mode are tending toward high time resolution in the nanosecond range, low-noise for accurate detection of lower-energy particles, and low-power consumption allowing the use of multiple channels on a single die. In previous reports we have presented a particle counting ROIC comprising: a charge-sensitive amplifier (CSA), an active shaping filter, and a discriminator. The use of an active shaping filter provides additional gain for the signal, which relaxes the requirements for the discriminator and makes it more power-efficient. At the same time, the active shaping filter itself consumes a considerable amount of power to operate properly. In this paper we present an alternative solution, based on the same architecture, in which the active shaping filter is replaced by a passive high-pass RC filter with no static power consumption. The price to pay is increased power consumption of a more advanced discriminator with periodic offset compensation. Nevertheless, we report a comparable performance of the two solutions with a 32 % overall power reduction with the passive RC filter. The design is made for TSMC 40 nm MS/RF CMOS technology.**

Keywords*— *readout integrated circuit ROIC, charge-sensitive amplifier, signal shaping filter, discriminator, low-offset, low-noise, low-power, high time resolution

I. Introduction

Reliable detection of small charges generated in a PIN silicon detector, as a result of the impingement of energetic particles, has a variety of applications. One such application is in scanning electron microscopes (SEMs). An SEM is a device that produces an image of a specimen surface with nanometer resolution by scanning the surface with a focused beam of electrons (primary current). This results in the generation of secondary and backscattered electrons (secondary current) due to scattering reactions [1] – [3]. The secondary current is sensed by a highly segmented PIN detector, with each segment/pixel occupying a very small area. This is done in order to reduce the capacitance of the segments resulting in a better signal-to-noise ratio (SNR) of the readout integrated circuit (ROIC) assigned to each pixel [4]. The combination of a weak primary current (to improve the resolution of the surface topography), high scanning speed (to increase productivity), and large number of segments, results in the counting of individual electrons landing on the surface of the pixels, every few nanoseconds [5]. The challenge for ROIC operation is a combination of a few requirements: detection of weak charge signals, precise counting of the signals (to minimize the false and missed counts), accurate registration of the arrival time of an electron (leading to very high bandwidth), and low power consumption (due to the large number of pixels on one die).

In previous publications we have reported a solution for the ROIC with the architecture shown in Fig. 1. It consists of: a charge-to-voltage converter (charge-sensitive amplifier); a signal shaping filter; and a discriminator [6] – [9]. The charge-sensitive amplifier (CSA) provides the necessary interface to the detector and converts its charge signals to voltage signals. Details concerning the CSA design are reported in [6] and [7]. The CSA is usually designed with a lower bandwidth than required to minimize the noise level and improve the SNR. This leads to pileup of voltage signals at the CSA output, known as inter-symbol interference (ISI) [10]. Also, the drift of the DC level (offset) at the CSA output is not sufficiently controlled, which can deteriorate the detection accuracy [8]. To overcome this problem, an active shaping filter is introduced to compensate the ISI-induced errors and the associated offset. This is realized by shortening the signal time width by wiping out its tail [8]. Furthermore, the active shaping filter amplifies the signal and relaxes the requirements for the threshold discriminator, which has to distinguish the signal and digitize the data [9].

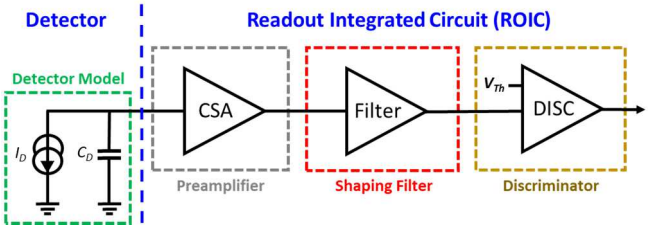

Fig. 1. Architecture of the charge detection ROIC.

Although the CSA is designed with a lower bandwidth than required, aimed at noise reduction, it consumes a significant portion of the pixel power budget. It is very difficult to further reduce the power consumption of the CSA without deteriorating the performance of the ROIC. The same is valid for the active shaping filter, due to its wide bandwidth. Therefore, despite the low power consumption of the discriminator, the reported overall power consumption is 370 µW.

This paper provides the design methodology and the post-layout simulation results of a ROIC using the architecture shown in Fig. 1 along with reduced power consumption. In the newly proposed design, the active shaping filter is replaced with a passive high-pass RC filter with negligible power consumption. The main challenges with this approach are: the stability of the CSA with an additional capacitive load; the design of a low-noise, low-power, low-offset, fast discriminator, operating with input signals more than twenty times lower than those in the previously reported solution.

Section II elaborates on the desired transfer function of the passive high-pass RC filter as well as the design considerations and characterization. In Section III, the requirements concerning the operation of the threshold discriminator leveraging the autozeroing offset reduction technique are discussed and the design methodology is presented. Section IV provides the overall performance results obtained through post-layout simulations as well as the assessment of the operational accuracy. The paper ends with the conclusions.

II. Passive High-Pass RC Filter

Similar to the active shaping filter presented in [8], a passive high-pass RC filter enhances ROIC detection accuracy by eliminating the ISI-induced errors and the offset, while consuming negligible power. The circuit diagram and the transfer function of the passive high-pass RC filter are illustrated in Fig. 2.

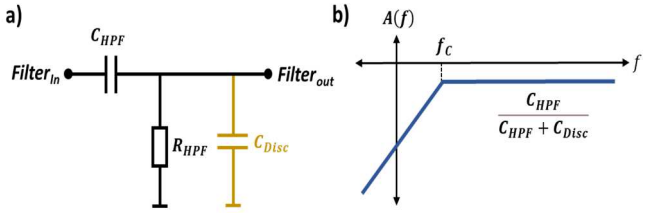

Fig. 2. Circuit diagram (a) and the transfer function (b) of a passive high-pass shaping filter.

The passive high-pass RC filter is a first-order network with a transfer function which can be expressed as:

$$T_{HPF}(S) = \frac{SR_{HPF}C_{HPF}}{1+SR_{HPF}(C_{HPF}+C_{Disc})} \quad (1)$$

where C_{HPF} and R_{HPF} are the main components of the RC network, and C_{Disc} represents the total capacitance seen at the input of the next block: the discriminator. This passive RC filter passes signal frequency contributions that are higher than a certain cut-off frequency f_C, which can be expressed as:

$$f_C = \frac{1}{2\pi\tau_{HPF}} \quad (2)$$

where $\tau_{HPF} = R_{HPF}(C_{HPF} + C_{Disc})$ is the filter time constant which must be carefully set to maximize the SNR at the filter output and limit the signal time-width to fit in a time frame of 2.5 ns after discrimination. Regarding the rise time of the CSA voltage signal [7] and considering a margin of 80 MHz for the passband [8], the cut-off frequency f_C of the filter should be below 300 MHz.

The passive RC filter, unlike the active shaping filter, does not amplify the CSA output signal; in fact, it attenuates the signal amplitude by a factor of $C_{HPF}/(C_{HPF} + C_{Disc})$. The attenuation comes from a non-ideal gain of the passive filter in the passband due to the loading effect of the discriminator block which is modeled by capacitor C_{Disc}. Thus, to minimize the attenuation factor, the capacitor C_{HPF} should be relatively larger than C_{Disc}. On the other hand, C_{HPF} cannot be very large in order not to influence the CSA stability due to the loading effect. For the $C_{Disc} = 1.8$ fF obtained from the simulation, the filter capacitor is set to $C_{HPF} = 35$ fF. Figure 3 illustrates, through simulation, the signal after the passive high-pass RC filter for different filter time constants τ_{HPF}. The input signal is provided by the CSA block with an amplitude of $V_{Amp} = 29.45$ mV, a short rise time of $t_r = 2.56$ ns, a relatively long time-width of $t_{width} = 286.91$ ns, and an output-referred offset of $V_{Offset} = 2.7$ mV [6], [7].

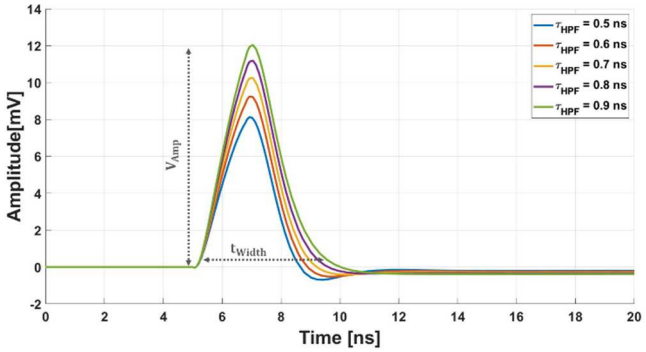

Fig. 3. Signal after the passive high-pass shaping filter with different filter time constants T_{HPF} for an input signal provided by the CSA.

Although the design of the passive RC filter is quite straightforward, the process and temperature variations alter the filter transfer characteristics causing degradation of the ROIC detection accuracy. Moreover, the capacitor C_{Disc}, modeling the discriminator input capacitance, is also susceptible to process variations and does not have a fixed definite value. Therefore, the signal amplitude, time-width, and SNR after the RC filter are altered. Table I presents the amplitude, time-width, and SNR of the signal after the passive high-pass RC filter for different time constants τ_{HPF}. Concerning the presented simulation results, the passive high-pass filter can fulfill the desired requirements with a time constant of $\tau_{HPF} = 0.7$ ns.

TABLE I.

τ_{HPF} [ns]	V_{Amp} [mV]	t_{Width} [ns]	σ_{Noise} [mV_{rms}]	SNR
0.5	8.1	2.8	0.57	14.2
0.6	9.3	3.1	0.63	14.6
0.7	10.4	3.3	0.68	15.3
0.8	11.2	3.6	0.71	15.8
0.9	12	3.9	0.74	16.2

The amplitude of the signal after the passive RC filter is approximately twenty times smaller than that of the signal after the active shaping filter. Thus, to achieve the same detection accuracy, as with the active shaper, the discriminator input-referred noise and offset must be reduced, which inevitably gives rise to its power consumption.

Another potential downside of the passive high-pass RC filter is that it gives rise to a certain extent of signal undershoot at the filter output. The undershoot stands for the drop in the output signal below the DC baseline at its falling phase, which requires a relatively long recovery time. Figure 4 illustrates, through simulations, the amplitude of the signal undershoot at the RC filter output as a function of the filter resistor R_{HPF} for several values of the filter capacitor C_{HPF}. As is evident, for the $C_{HPF} = 35$ fF and $R_{HPF} = 20$ KΩ, the undershoot amplitude enters a plateau region with an almost constant value.

The undershoot can degrade the detection accuracy when a cascade of electrons hit one detector pixel in consecutive time frames. Figure 5 illustrates the signal after the passive RC

filter for the case that three cascading electrons are hitting the detector surface in three consecutive time frames. The results are shown for a fixed filter capacitor value of $C_{HPF} = 35$ fF and different values of the filter resistor R_{HPF}. As is denoted, the peak of filter output signal drops due to the filter undershoot issue. This gives rise to a lower detection accuracy due to the drop in the SNR. In the worst case, the filter output signal is unable to exceed the discriminator threshold level and the electron is missed.

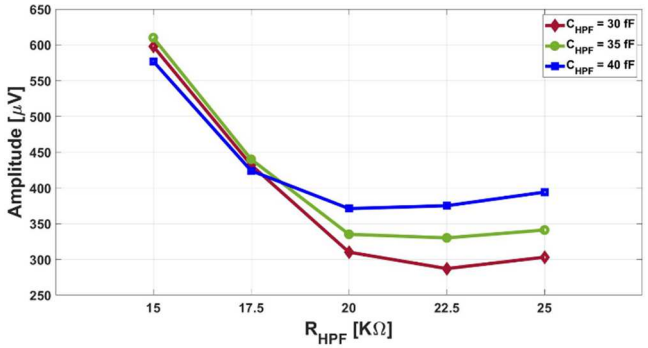

Fig. 4. Amplitude of the signal undershoot at the RC filter output as a function of the filter resistor R_{HPF} for several values of the filter capacitor C_{HPF}.

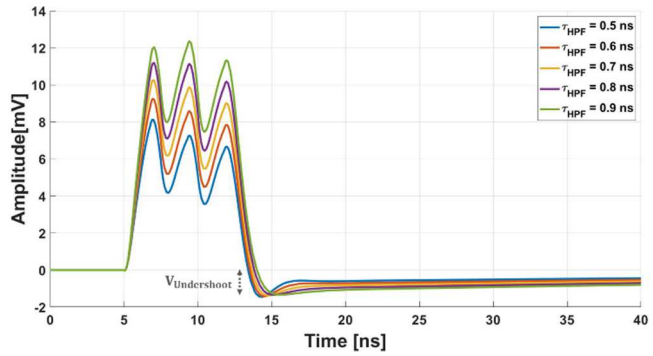

Fig. 5. RC filter output signal for three cascading electrons hitting the detector in three consecutive time frames.

III. Low-Offset Threshold Discriminator

The discriminator block compares the signal after the passive high-pass RC filter with a reference level (the threshold voltage V_{Th}) to digitize the analog signal. The discriminator comprises a differential preamplifier stage followed by a few cascading inverters to both consolidate the logic levels at the output and minimize the delay time [9].

The signal to be discriminated has a minimum amplitude of 9 mV, which is comparable to the input-referred noise and offset of the discriminator designed for the active shaping filter [9]. Therefore, for a corresponding threshold level, there is a risk of triggering the discriminator by the noise, or even saturating the discriminator output as a consequence of the offset. In this regard, the noise and offset of the discriminator play a more significant role in degradation of the detection accuracy due to devaluation of the SNR at the discriminator input node.

To mitigate this issue, the input-referred noise and offset of the discriminator should not exceed the noise at the filter output node. Concerning the results presented in Table I, to guarantee a sufficient SNR and, in turn, the desired detection accuracy, the discriminator must have an input-referred noise of $\sigma_{Noise} < 0.6$ mV and offset of $V_{Offset} < 2$ mV. These require a more conservative approach for designing the discriminator sub-blocks which gives rise to larger power consumption. The offset is the drift of the DC operating points of a stage from their nominal values, due to the mismatch of the transistors dimensions, and threshold voltages as a result of uncertainties and errors during the fabrication process. The offset can be evaluated by means of a Monte-Carlo simulation in the design tools.

The selection of the threshold level V_{Th} is another critical factor involved in the detection accuracy [11]. For a threshold level V_{Th} set in the range of 6 to 8 times the total noise power at the discriminator input node σ_{tot}, at least 99.99 % of the noise samples are below the threshold level. This necessitates an SNR in the range of 12 to 16 at the discriminator input node to obtain the desired detection accuracy [9].

A. Preamplifier

For a proper digitization of the signal, the preamplifier stage needs to provide a sufficient gain as well as a large bandwidth. As the signal after the RC filter is approximately twenty times smaller than the one after the active shaping filter, the preamplifier stage of the discriminator presented in [9] must be modified to improve the gain and shrink the input-referred noise. For this purpose, a two-stage amplifier topology (Fig. 6) is chosen. The first stage comprises a fully differential amplifier with a common-mode control loop. The second stage is a differential amplifier with single-ended output to drive the cascading inverters. The common-mode feedback is an essential auxiliary stage for fully differential amplifiers to maintain the DC level of the output nodes at the desired common mode voltage V_{CM}. This is done through continuous comparison of the output nodes with a reference voltage level $V_{CM,ref}$ and, subsequently, fine-tuning the current of the tail generator I_1.

The simulation results indicate that the preamplifier provides a total gain of 49.2 dB, with a maximum tolerance of 4.7 dB across the process corners, and a 181 MHz bandwidth, while consuming 104 μW of power. The preamplifier has an input-referred noise of 0.326 mV and offset of 15.3 mV [12]. While the input-referred noise of the preamplifier is below the target limit, the offset is still much larger than in the design spec. This calls for the utilization of offset reduction techniques which are addressed in the next subsection.

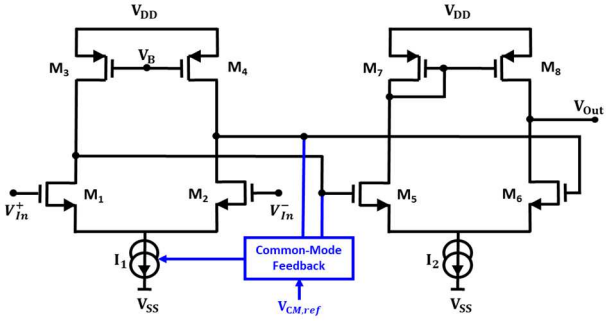

Fig. 6. Circuit diagram of a two-stage preamplifier with a common-mode control loop.

B. Offset Reduction Network

Large offset of the preamplifier can degrade the ROIC detection accuracy by devaluating the effective SNR at the discriminator input node. Although passive solutions, such as increasing the size of the input pairs, are already applied during the design and layout of the proposed preamplifier, its

offset is still larger than in the design spec. To mitigate the large offset issue and retain a high detection accuracy, an active offset reduction technique needs to be applied. Unfortunately, the active solutions give rise to larger power consumption in the discriminator block.

Two commonly used active offset reduction techniques are preamplifier autozeroing and signal chopping [13] – [15]. Due to the high electron rate in the target application, the signal chopping technique is not applicable as it requires an ultra-high chopping frequency. On the other hand, the preamplifier autozeroing technique is possible to apply at much lower frequencies. In this technique, by means of a few auxiliary switches, the preamplifier offset is periodically sampled in a memory capacitor C_{az} (offset storage phase) and then, in the next step, it is subtracted from the input signal (offset subtraction phase) [13]. Figure 7 illustrates the two phases of the autozeroing technique for preamplifier offset reduction.

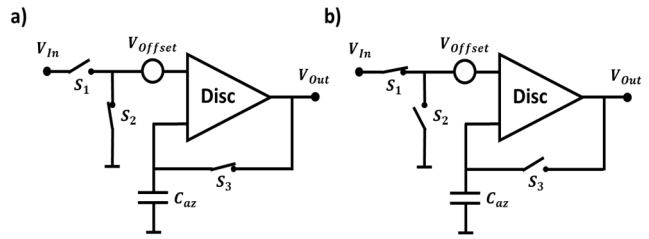

Fig. 7. Two phases of the autozeroing technique for preamplifier offset reduction: (a) offset storage phase, and (b) offset subtration phase.

During the offset storage phase, the discriminator is blind to the incoming events as it is disconnected from the preceding blocks of the ROIC. The offset storage phase is considered to be the deadtime of the ROIC since, in this period, the electrons landing on the detector surface are missed. The duration of the offset storage phase is directly proportional to the ROIC detection accuracy. To reduce the number of possible missed events during this phase, the time duration of the offset storage phase t_1 should be as short as possible.

The duration of the offset storage phase t_1 depends on the value of the autozeroing capacitor C_{az} and the preamplifier time constant τ_{preamp}. Figure 8 illustrates, through simulations, the voltage across the autozeroing capacitor C_{az} (normalized with V_{Offset}) as a function of the duration of the offset storage phase t_1 for different values of autozeroing capacitor C_{az}. For $t_1 = 5 \times \tau_{preamp}$, more than 99.33% offset is stored in the autozeroing capacitor C_{az}; therefore, it could be considered as complete offset storage.

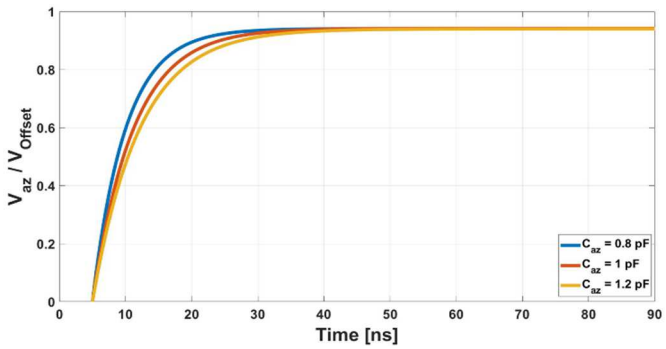

Fig. 8. Voltage across the autozeroing capacitor C_{az} (normalized with V_{Offset}) as a function of the duration of the offset storage phase t_1 for different values of the autozeroing capacitor C_{az}.

During the offset subtraction phase, the voltage across the autozeroing capacitor C_{az} gradually drops and, as a consequence, the offset cannot be effectively attenuated anymore and therefore returns to its initial value. The autozeroing capacitor C_{az} is discharged by the leakage gate currents of the preamplifier input pairs as well as the auxiliary switches, leading to offset degradation with time. The larger the size of C_{az} and the lower the leakage currents, the slower the offset degradation is due to the discharging. [12]. Figure 9 illustrates the simulated voltage across the autozeroing capacitor C_{az}(normalized with V_{Offset}) as a function of the duration of the offset subtraction phase t_2 for different values of the autozeroing capacitor C_{az}. The total leakage current discharging the autozeroing capacitor C_{az} is 18 pA.

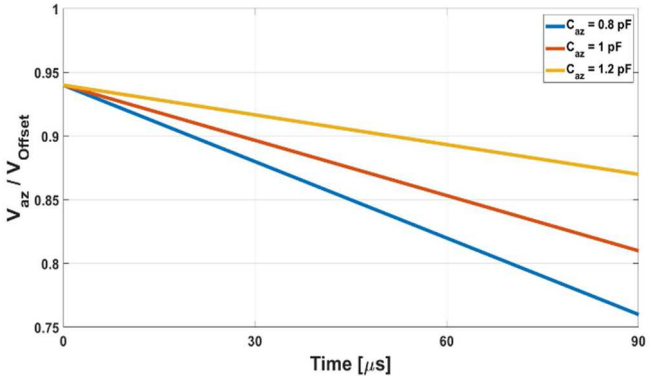

Fig. 9. Voltage across the autozeroing capacitor C_{az} (normalized with V_{Offset}) as a function of the duration of the offset subtraction phase t_2 for different values of the autozeroing capacitor C_{az}.

On the other hand, a large autozeroing capacitor C_{az} requires a longer offset storage phase t_1 period to completely store the offset value, which gives rise to a longer deadtime and, as a result, a larger detection error rate. Concerning the presented post-layout simulation results, the autozeroing capacitor is set to $C_{az} = 1$ pF, while the period of the offset storage and subtraction phases are set at $t_1 = 10$ ns and $t_2 = 90$ µs, respectively. In this regard, the initial offset of the preamplifier stage after autozeroing is shrunk to 70 µV.

IV. Overall Performance Results

The prototype of the passive high-pass RC filter followed by the low-offset threshold discriminator is designed in the TSMC 40 nm CMOS process. Figure 10 illustrates the layout mask view of the designed circuit. The passive RC filter and the discriminator occupy an area of 12 µm × 14 µm and 23 µm × 29 µm, respectively. As verified through post-layout simulations, the voltage signal after the passive high-pass RC filter has an amplitude of $V_{Amp} = 10.4$ mV with a time-width of $t_{Width} = 3.3$ ns for $R_{HPF} = 20$ KΩ, $C_{HPF} = 35$ fF, and $C_{Disc} = 1.8$ fF. Moreover, with $t_1 = 10$ ns, $t_2 = 90$ µs, and $C_{az} = 1$ pF, the discriminator has input-referred noise and an offset of 0.326 mV and 70 µV, respectively.

In the post-layout simulations and through this work, to characterize the performance and operational accuracy of the proposed passive RC filter and the discriminator, the CSA is triggered by several patterns of charge signals (equivalent to 1000 e^-) [7]. Figure 11 shows the transient signals of the ROIC after the CSA, the passive RC filter, and the low-offset discriminator for input-charge signals triggering the CSA with a Poisson distribution.

Proper selection of the threshold voltage V_{Th} is a critical point in the assessment of the detection error rate. As described in [9], the target level of the detection accuracy can be obtained by setting the threshold voltage V_{Th} in a range of 6 to 8 times that of the total noise power. The ROIC detection error rate is assessed by leveraging the technique presented in [11]. Figure 12 presents the ROIC detection error rate as a function of the threshold voltage once the CSA is triggered with 5000 charge pulses distributed with a Poisson distribution in 10^6 time frames (2.5 ms simulation period). Results indicate that the best detection accuracy is obtained for a threshold voltage V_{Th} equivalent to 7 times the noise level. This result is sensible as the overall SNR at the input node of the discriminator block is 15.3 and the threshold level is at its half. Moreover, as the input-charge signals have a random arrival moment, some of them might trigger the ROIC during the offset storage phase in the offset reduction network. Hence, they are missed by the discriminator to be digitized since, in this phase, the discriminator is blind to the input signals.

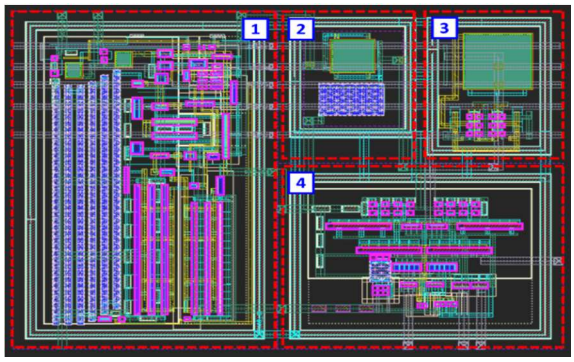

Fig. 10. Layout mask view of the passsive RC filter and the discriminator. (1) CSA, (2) Passive RC Filter, (3) Offset Reduction Network, and (4) Discriminator.

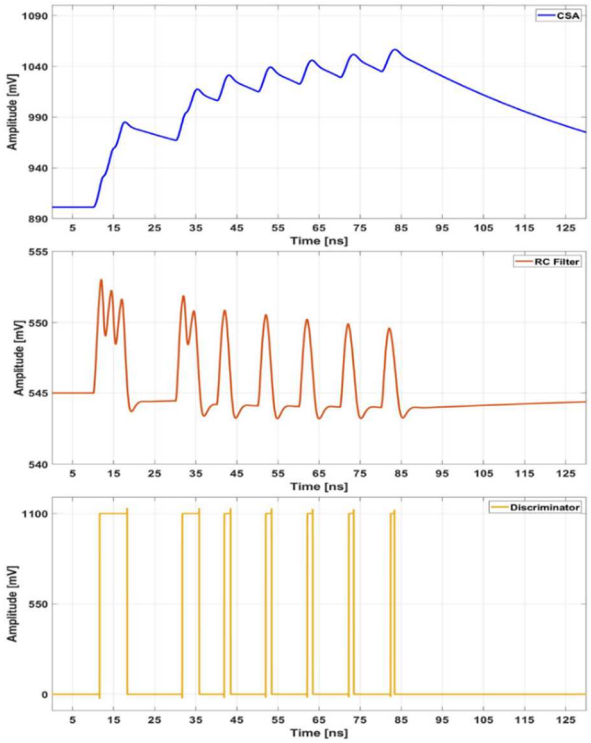

Fig. 11. Transient signals of the ROIC after the CSA, the passive RC filter, and the low-offset discriminator for input-charge signals with a Poisson distribution.

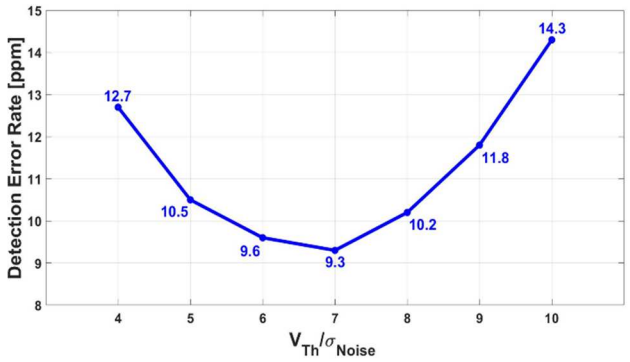

Fig. 12. ROIC detection error rate as function of the threshold voltage V_{Th} of the discriminator.

Figure 13 shows the power consumption breakdown of the ROIC including the CSA, passive high-pass RC filter, and low-offset discriminator. The ROIC has a total power consumption of 250 µW, which is 68 % of the power budget required for the ROIC with an active shaping block [7] – [9]. The discriminator with an offset reduction network takes 42 % of the total ROIC power; hence, the CSA is the only remaining power-hungry block of the ROIC. Further efficiency in power consumption could be obtained by changing the ROIC architecture and leveraging a brand-new readout technique, which will be presented in the next publications.

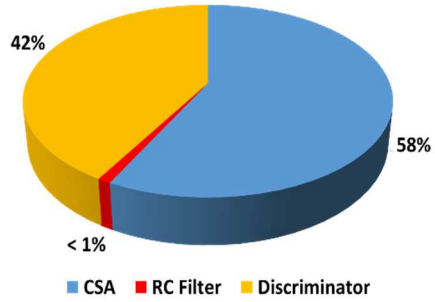

Fig. 13. Power consumption breakdown of the ROIC including the CSA, passive high-pass RC filter, and low-offset discriminator.

To classify the operational accuracy of the proposed ROIC including the passive RC filter and low-offset discriminator, the performance needs to be compared with an ROIC with an active shaping block. This is assessed by comparing the detection error rate and the total power consumption of both. Although the experimental qualification of the ROIC with an active shaping block is a work in progress, the preliminary qualification tests of the ROIC indicate that, under the above-mentioned testing conditions, it is able to continuously process the detector charge signal with a detection error rate of 5.7 ppm at its optimum threshold level with a total power consumption of 0.37 mW. This indicates that the ROIC proposed in this paper provides a higher level of power efficiency while the relatively higher detection error rate still fits within the target range of the application. As mentioned before, the ROIC deadtime due to the periodic offset reduction phase of the discriminator gives rise to this higher detection error rate. Nonetheless, in some SEM applications, the scanning principle includes periodic intermediate breaks which can be used for an offset reduction phase. Hence, a lower detection error rate, comparable to that of the active-shaper solution, could be obtained.

V. Conclusions

This paper presented the design and post-layout simulation results of a low-power high time resolution charge detection ROIC in 40 nm CMOS technology. The ROIC comprises a charge-sensitive amplifier (CSA), a signal shaping filter, and a discriminator. To minimize to ROIC power consumption, the active shaping block proposed in [8] is substituted with a passive high-pass RC filter. Generating an analog voltage signal with a relatively lower amplitude, the discriminator has been redesigned to minimize its input-referred noise through an offset leveraging autozeroing offset attenuation technique. The proposed ROIC with the passive RC filter and the low-offset discriminator detects charge signals with lower power consumption, while the ROIC detection accuracy is lower due to the periodical deadtime imposed by the autozeroing for offset reduction in the discriminator block. In some SEM applications, the scanning principle includes periodic intermediate breaks which can be used for offset reduction to retrieve the higher detection accuracy.

Acknowledgment

This work is supported by the Dutch Top Consortium for Knowledge and Innovation (TKI) HTSM.

References

[1] I. Fleck, M. Titov, C. Grupen, and I. Buvat, Handbook of Particle Detection and Imaging, 2nd ed., Cham: Springer, 2021.

[2] I. S. McLean, Electronic Imaging in Astronomy, Detectors and Instrumentation, 2nd ed., Berlin: Springer Praxis Books, 2008.

[3] K. Iniewski, Medical Imaging, Principles, Detectors, and Electronics, John Wiley & Sons, 2009.

[4] M. Nakhostin, “Pulses from Ionization Detectors,” in Signal Processing for Radiation Detectors, New York: John Wiley & Sons, 2017.

[5] Y. Wang, Z. Dong, R. L. Lai, and K. Kanai, “Semiconductor charged particle detector for microscopy,” US Patent Application 2023/0123152 A1, April 20, 2023.

[6] A. Mohammad Zaki and S. Nihtianov, "High Time Resolution, Low-Noise, Power-Efficient, Charge-Sensitive Amplifier in 40 nm Technology," 2022 XXXI International Scientific Conference Electronics (ET), pp. 1-6, 2022.

[7] A. Mohammad Zaki and S. Nihtianov, “Experimental Qualification of a Low-Noise Charge-Sensitive ROIC with Very High Time Resolution,” 2023 IEEE 32st International Symposium on Industrial Electronics (ISIE), Helsinki-Espoo, Finland, 2023.

[8] A. Mohammad Zaki and S. Nihtianov, "Low-Offset Band-Pass Signal Shaper with High Time Resolution in 40 nm CMOS Technology," IECON 2023 - 49th Annual Conference of the IEEE Industrial Electronics Society, Singapore, Singapore, 2023.

[9] A. Mohammad Zaki, Y. Du and S. Nihtianov, "Design and Qualification of a High-Speed Low-Power Comparator in 40 nm CMOS Technology," 2023 XXXII International Scientific Conference Electronics (ET), Sozopol, Bulgaria, 2023.

[10] M. A. Disi, A. Mohammad Zaki, Q. Fan and S. Nihtianov, “High-Count Rate, Low Power and Low Noise Single Electron Readout ASIC in 65nm CMOS Technology,” 2021 XXX International Scientific Conference Electronics (ET), 2021.

[11] A. Mohammad Zaki and S. Nihtianov, “Characterization Challenges of a Low Noise Charge Detection ROIC,” in IEEE Transactions on Instrumentation and Measurement, vol. 71, pp. 1-8, 2022.

[12] Y. Du, “Power-efficient, Precise Discriminator for a High Time Resolution, Low-Noise Charge Detection ROIC,” M.S. thesis, Dept. Microelectronics, TU Delft, Delft, the Netherlands, 2023.

[13] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators," in IEEE Journal of Solid-State Circuits, vol. 27, no. 12, pp. 1916-1926, Dec. 1992.

[14] R. Wu, J.H. Huijsing, and K. A. A. Makinwa, Precision Instrumentation Amplifiers and Read-Out Integrated Circuits, Springer, 2013.

[15] M. Safiallah, A. R. Danesh, H. Pu and P. Heydari, "A Current-Adjusting Auto-Zeroing Technique for DC-Offset and Flicker-Noise Cancellation," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 12, pp. 1950-1959, Dec. 2023.