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A Pitch-Matched High-Frame-Rate Ultrasound Imaging ASIC for Catheter-Based 3-D Probes

Yannick M. Hopf, *Graduate Student Member, IEEE*, Djalma Simoes dos Santos, *Graduate Student Member, IEEE*, Boudewine W. Ossenkoppele, *Graduate Student Member, IEEE*, Mehdi Soozande, *Student Member, IEEE*, Emile Noothout, Zu-Yao Chang, Chao Chen, *Member, IEEE*, Hendrik J. Vos, *Member, IEEE*, Johan G. Bosch, *Member, IEEE*, Martin D. Verweij, *Member, IEEE*, Nico de Jong, *Member, IEEE*, and Michiel A. P. Pertijs, *Senior Member, IEEE*

***Abstract*— This article presents an application-specific integrated circuit (ASIC) for catheter-based 3-D ultrasound imaging probes. The pitch-matched design implements a comprehensive architecture with high-voltage (HV) transmitters, analog front ends, hybrid beamforming analog-to-digital converters (ADCs), and data transmission to the imaging system. To reduce the number of cables in the catheter while maintaining a small footprint per element, transmission (TX) beamforming is realized on the chip with a combination of a shift register (SR) and a row/column (R/C) approach. To explore an additional cable-count reduction in the receiver part of the design, a channel with a combination of time-division multiplexing (TDM), subarray beamforming, and multi-level pulse amplitude modulation (PAM) data transmission is also included. This achieves an 18-fold cable-count reduction and minimizes the power consumption in the catheter by a load modulation (LM) cable driver. It is further explored how common-mode interference can limit beamforming gain and a strategy to reduce its impact with local regulators is discussed. The chip was fabricated in TSMC 0.18-μm HV BCD technology and a 2-D PZT transducer matrix of 16 × 18 elements with a pitch of 160 μm and a center frequency of 6 MHz was manufactured on the chip. The system can generate all required TX patterns at up to 30 V, provides quick settling after the TX phase, and has an reception (RX) power consumption of only 1.12 mW/element. The functionality and operation of up to 1000 volumes/s have been demonstrated in electrical and acoustic imaging experiments.**

***Index Terms*— 3-D ultrasound, analog front end (AFE), common-mode interference suppression, high frame rate, intracardiac echocardiography (ICE), load-modulation datalink, PAM-4, transmit beamformer, transmit/receive (T/R) switching, ultrasound application-specific integrated circuit (ASIC).**

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Yannick M. Hopf, Zu-Yao Chang, Chao Chen, and Michiel A. P. Pertijs are with the Electronic Instrumentation Laboratory, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: y.m.hopf@tudelft.nl).

Djalma Simoes dos Santos, Boudewine W. Ossenkoppele, and Emile Noothout are with the Laboratory of Medical Imaging, Delft University of Technology, 2628 CD Delft, The Netherlands.

Mehdi Soozande and Johan G. Bosch are with the Department of Biomedical Engineering, Thoraxcenter, Erasmus Medical Center, 3015 GD Rotterdam, The Netherlands.

Hendrik J. Vos, Martin D. Verweij, and Nico de Jong are with the Laboratory of Medical Imaging, Delft University of Technology, 2628 CD Delft, The Netherlands, and also with the Department of Biomedical Engineering, Thoraxcenter, Erasmus Medical Center, 3015 GD Rotterdam, The Netherlands.

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I. Introduction

ULTRASOUND imaging is a popular tool in medical treatments due to its relatively safe nature, cost-effectiveness, and compatibility with minimally invasive interventions [1], [2]. A special class of imaging devices used for the latter are catheter-based probes. These enable high-resolution images taken directly next to the area of interest in the body. The probes are disposable and purpose-built for their application in procedures such as intravascular ultrasound (IVUS) [3] or intracardiac echocardiography (ICE) [4], [5]. While IVUS is commonly used in procedures such as plaque detection in the vascular system and can typically work with a smaller imaging array [6], [7], [8], ICE is applied in a variety of cardiovascular interventions with more demanding requirements on the imaging depth and resolution [9], [10].

Particularly in upcoming 3-D probes with 2-D transducer arrays, these requirements lead to significant challenges in the design of ICE catheters. While 2-D imagers with 1-D transducer arrays commonly apply passive probes with direct element connection to the imaging system [11], [12], the higher cable count, crosstalk, and attenuation across thinner cables for 2-D transducer matrices lead to the application of application-specific integrated circuits (ASICs) in ultrasound imaging catheters [9], [13]. The basic functionality of the electronics includes ultrasound transmission (TX) and reception (RX) on each array element to maximize the imaging aperture in the limited space of the catheter, amplification of the received echoes for robust signal transmission, and communication with an imaging system outside the body [14], [15]. For 3-D imaging, the transducer pitch in the azimuthal and elevation direction has to be designed for low impact on image quality [10]. As a result, there is little space for circuitry that is matched to the pitch of the transducer. A pitch-matched design is a requirement for scalability to the about 1000 elements of a full 3-D ICE design [9], [10] but leads to a high requirement on the integration density of the circuits. Prior 3-D ICE designs have thus been limited to a subset of the desirable functionality as they could not integrate transmit

beamforming [15], only low-voltage (LV) transmission [16], no transmit functionality at all [17], [18], or had to strongly limit the achievable volume acquisition rate [9].

High-frame-rate imaging is required in order to accommodate imaging modes such as blood flow Doppler or electromechanical wave imaging [19]. However, with the pulse repetition frequency (PRF) being limited by the imaging depth, a high frame rate implies fewer acquisitions per reconstructed volume and additional requirements on the circuit design [10].

One of the main challenges in the transition to high-frame-rate 3-D probes is posed by the communication with the imaging system. Catheters with a diameter of around 3 mm have to accommodate all TX and RX signals next to common connections such as power and additional controls [9]. To reduce the number of TX cables, pulses are often generated on the ASIC. The configuration data can be provided via a serial link into local registers [20], [21], [22] or an efficient shift register (SR) [14], [23] before the next TX phase and delays for TX beamforming (TX BF) can be generated with local counters. However, this leads to large registers and counter cells for a dense array with a large number of delay steps. An alternative is to implement TX control in a row/column (R/C) approach [24], [25], [26], [27]. This minimizes the amount of associated circuitry underneath the element but, in turn, limits the amount of possible TX patterns for application in a 3-D ICE probe. A similar challenge is faced when externally generated pulses are only passed or blocked on the chip instead of local pulse generation [8], [26], [28].

Reduction of RX cables in the catheter has previously been achieved by multiplexing of transducer signals on fewer connections over multiple transmit/receive (T/R) cycles [28], [29]. To avoid the associated loss in frame rate, other designs have made use of the wider bandwidth of the channel compared to the imaging frequency. In these, several RX signals are multiplexed on a single connection within one T/R cycle [30], [31], [32]. When applied for sensitive analog signals, crosstalk can become an issue [33]. Digital signaling, on the other hand, has been shown to be possible with a low impact on signal integrity [15]. Nevertheless, the achievable channel count reduction by both analog and digital multiplexing methods is limited by the small bandwidth across the thin cables in the catheter.

Another approach is to apply subarray beamforming, also known as micro-beamforming (μBF) [34]. This shifts part of the RX beamforming into the catheter by delaying and summing the received signals of a subarray of elements. However, it comes at the cost of less raw data being available in the final image reconstruction and reduced frame rate as multiple acquisitions are required per reconstructed volume [35]. Both disadvantages can be mitigated while achieving significant cable-count reduction by a combination of subarray beamforming and digital time-division multiplexing (TDM). This has been shown with element-level digitization with subsequent digital beamforming [36], [37], digitization of the output of analog beamformers [15], [18], [38], and mixed schemes [39]. However, even more can be gained from the digital transmission as ultrasound imaging can tolerate higher bit error rates (BERs) than most communication links [40]. While current digital probe designs commonly rely on conventional LV differential signaling (LVDS) [15], [17], [18], [41] with relatively low BER, BER could potentially be traded to reduce the circuit area and power consumption. Moreover, it could allow for a lower cable count by dividing the total output data bandwidth across fewer channels with a higher transmission rate.

An additional aspect to consider in the design of ASICs for arrays with a large number of elements, particularly for high-frame-rate designs with little opportunity for averaging, is the common-mode interference across the channels. With decreasing size, the noise level of the transducer increases [42], [43]. The noise of each front-end amplifier can thus generally be higher before limiting the global performance. The uncorrelated noise can then still reveal weaker signals after beamforming in the imaging system with an SNR gain of $\sqrt{N}$ for N combined signals [44]. As more elements are summed for a smaller pitch, the final signal-to-noise ratio is, to first order, equal for different element sizes in a transducer array of a given size [45]. However, correlated noise between channels effectively reduces the maximum gain achievable through beamforming, meaning that it should remain well below the noise floor despite the larger number of channels.

In this article, a pitch-matched ASIC with a co-integrated transducer array with a pitch of 160 $\times$ 160 μm is presented. This article builds on our previous work [15], extending it with an integrated TX beamformer and a novel low-power load-modulation datalink, implemented in a prototype with a 4$\times$ larger transducer array, scalable to a full 3-D ICE probe. On-chip TX control is implemented by a compact combination of an R/C and an SR approach that offers all required beam patterns. Additional area savings are achieved by encoding the delay of the TX beamformer as the difference from its neighbor, similar to [22], and re-using the shift-register cells as counters for delay generation. Local biasing schemes for the transducer and analog front-end (AFE) amplifiers enable quick settling of the input after the TX phase and a lower impact of correlated noise on the final image. In addition, a multi-level pulse amplitude modulation (PAM) channel combined with TDM and μBF achieves an RX cable-count reduction of 18 while still enabling a high frame rate of 1000 volumes/s. To reduce the heating of tissue in the patient, the driver is implemented as a load modulation (LM) architecture.

This article is organized as follows. The architecture and system design considerations are described in Section II. Section III provides circuit implementation details on the TX beamformer, AFE, and LM data transmission. The fabricated prototype, measurement setup, and results are discussed in Section IV. This article concludes with a comparison to the prior art and a conclusion.

II. System Design

A. Overview

Fig. 1(b) shows an overview of the developed system. A matrix of 16 $\times$ 18 transducer elements is designed for

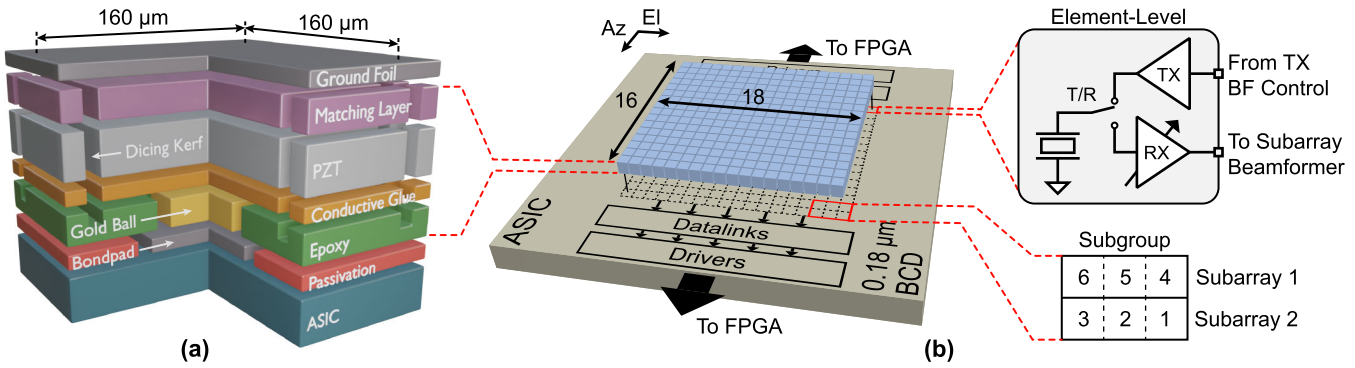


Fig. 1. (a) Conceptual drawing of transducer stack. (b) Overview of chip assembly with details on the matrix organization.

directly interfacing the presented ASIC, as shown in Fig. 1(a). The 160-μm-pitch transducer stack is a revised version of the concept shown in [46]. The circuitry interfaces with the PZT elements through individual connections made with a gold contact on the bottom side and a common aluminum ground foil on the top.

On the side of the chip, implementation in a 0.18-μm BCD technology offers a tradeoff between the ability to integrate high-voltage (HV) TX-related structures and LV logic as well as RX-related structures. Each element is connected to individual TX and RX paths to efficiently use the space inside the catheter. An isolating T/R switch between the two paths protects the receiver from HV breakdown during transmission. The receiver also implements time gain compensation (TGC) to manage the dynamic range (DR) requirement of ICE. While imaging is often done with a range of only 40 dB, ultrasound attenuation inside the human body can lead to a total DR in the order of 100 dB within one T/R cycle [15]. However, as the attenuation is time-dependent, TGC can still reduce the DR to the following components by complementing it with a time-varying gain [13]. The matrix is further grouped into subarrays of three elements each and subgroups of two subarrays each. To enable a front-end layout matched to the pitch of the transducer element, all backend circuitries, such as the datalinks and data output drivers, are pushed to the periphery. This enables the design of subgroups as unit cells that can be replicated to create a larger aperture. The periphery-level circuitry is designed in units as well and only occupies two sides, the top serving the upper and the bottom serving the lower half of the matrix, to allow scaling along one direction.

This design serves as a prototype to evaluate the architecture and shows techniques for application in a full ICE probe. While all of the functionality required for the realization of the 64 $\times$ 18-element imaging scheme presented in [10] is included, only one-fourth of the aperture in the azimuth direction is accommodated in this step. To characterize the performance of the 1-D subarray beamformer in the elevation direction and the imaging approach, the full aperture is implemented along that axis. The beamformer of just three elements enables a high frame rate as only a few acquisitions are required per volume. The full probe targets a 10-cm imaging depth and thus operates at a PRF of 7.7 kHz considering the speed of sound in human tissue. Being able to image with just seven fan-shaped beams per frame, this results in a total frame rate of up to 1000 volumes/s. The seven steps employ a TX beam with 10.7° divergence in the elevation and 70° divergence in the azimuth direction and steer the subarray beamformer in a $\pm$30° window in the elevation direction accordingly to achieve a field of view of 70° $\times$ 70° $\times$ 10 cm [10].

B. Architecture

Fig. 2 shows the architecture implemented in the presented design. The topology is building on what has been discussed in [15] and the TX part is based on the unipolar pulser with embedded T/R switch introduced in [47]. Compared to [47], the TX voltage was reduced from 65 to 30 V to allow for additional guard rings in the layout. Higher TX voltages could be achieved with the same architecture by adopting a silicon-on-insulator technology with deep-trench isolation. In this design, the control of the TX BF is realized with per-element digital delay cells that are configured in a mixed scheme. While global steering information is provided on the level of rows or columns of elements to save area, individual control is supplied by an SR spanning the whole matrix. To minimize the number of connections inside the catheter, the SR is also used to load the row and column data as well as all global configuration settings. The entire SR content of about 1.5 kb can be loaded in around 15 μs at a clock frequency of 100 MHz. The SR is updated during the RX period and thus forms an upper limit to the PRF at about 66 kHz, irrespective of the imaging depth.

On the receiver side, each element is individually connected to a low-noise amplifier (LNA), followed by a second-stage programmable gain amplifier (PGA) that also acts as a single-ended-to-differential converter. The LNA can be discretely switched in steps of 18 dB from $-$12 to 24 dB and the second stage can be configured in steps of 6 dB from 6 to 24 dB. The global step size of 6 dB enables TGC with a range of 54 dB in ten steps from $-$6 to 48 dB with a compact implementation. The LNA architecture is a modified version of the design in [48] and was employed in [15] to enable operation with HV transmitters and seamless gain switching during echo reception in a single T/R cycle. As the received signal is most sensitive at

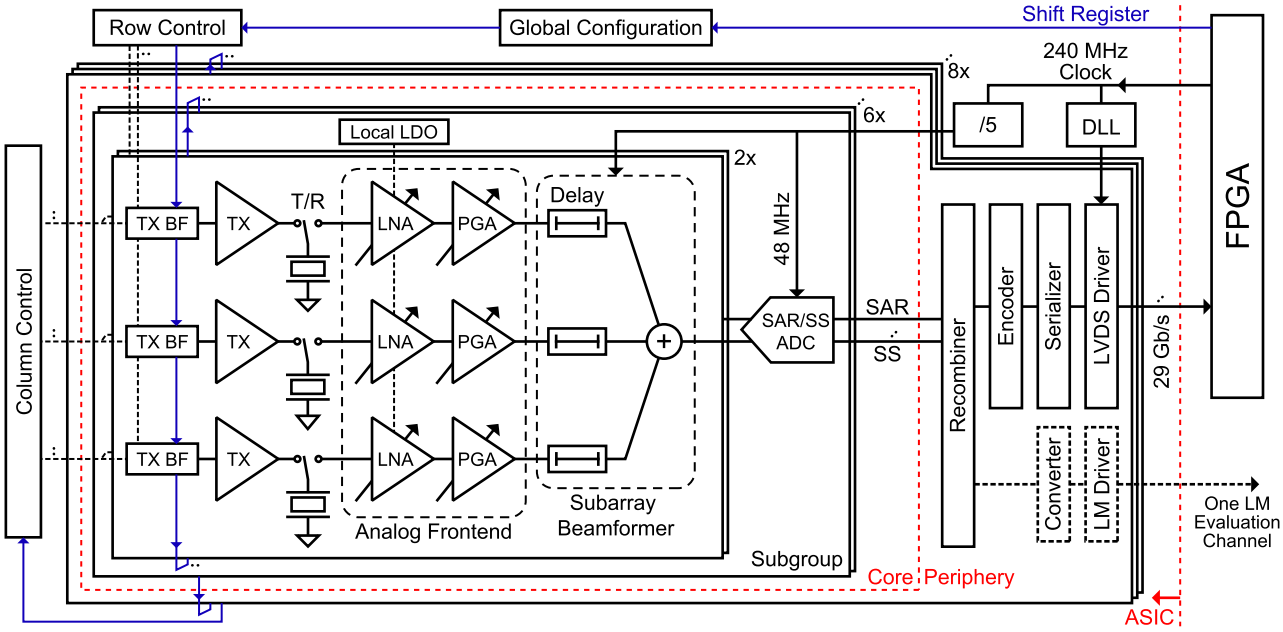
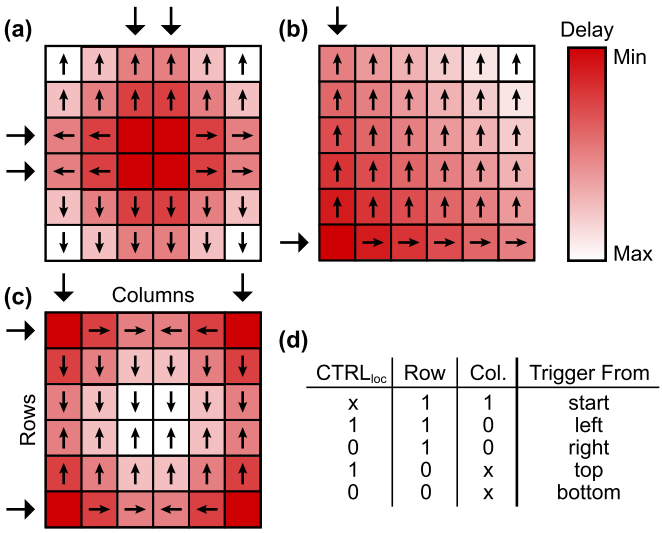


Fig. 2. Architecture overview showing how element-level circuitry, subarray beamformers, and a shared ADC structure per subgroup are combined. The arrangement of the SR and R/C approach is sketched and a global view of the data management and clocking is provided.

this point, a local regulator for the LNA supplies is installed on the subgroup level here as well to reduce the effect of common interference across the whole array. The PGA is based on [18] and [49], was employed in [15], and is again adapted to get full TGC range within one T/R cycle and thus full frame rate.

The digitization from [15] is adopted with the same parameters in this design since both implementations target the same application. Three elements are combined in the elevation direction for analog subarray beamforming in the charge domain. Two neighboring subarrays are combined for layout with a shared hybrid beamforming analog-to-digital converter (ADC) in a subgroup. The ADC combines a successive approximation register (SAR) first stage and single-slope (SS) second stage and operates at 24 MS/s per channel with a resolution of 10 bits. To allocate all hardware in the core, the SAR and SS outputs are individually transferred to the periphery.

On the periphery, two datalink configurations have been included. The regular one features recombination of the SAR and SS output to 10-bit words, 8b10b encoding [50], and serialization to conventional LVDS drivers. In the process, fourfold TDM is applied, leading to a rate of 1.2 Gb/s per channel and, together with threefold subarray beamforming and considering the differential nature of the signals, a total cable-count reduction factor of 6. The second setup only serves one channel and provides a parallel path from the recombination to a multi-level encoder and an LM driver. This enables conventional access via field-programmable gate arrays (FPGAs) [51] to the whole array for convenient imaging while providing an evaluation platform for the novel datalinks discussed in Section III-D. The periphery and core are timed by shared dividers and delay-locked loops (DLLs) working on a 240-MHz clock provided by the FPGA.



$CTRL_{loc}$	Row	Col.	Trigger From
x	1	1	start
1	1	0	left
0	1	0	right
1	0	x	top
0	0	x	bottom

Fig. 3. Examples of TX beamformer delay patterns with arrows indicating the delay propagation for a 6 × 6 array. (a) Centered diverging wave. (b) Diagonal plane wave. (c) Focused wave. (d) Decision table for the delay propagation based on SR and R/C input.

III. Circuit Implementation

A. TX Beamformer

To achieve a compact TX BF implementation, the system operates by passing a single trigger signal through the entire array based on relative delays between neighboring elements. This reduces the required delay depth per element and associated counting steps. For further area savings while still enabling the creation of all required beam patterns, the control of the propagation direction is done from the R/C level but also with one local bit from the SR, $CTRL_{loc}$. Fig. 3 shows the examples of TX patterns that can be generated with the

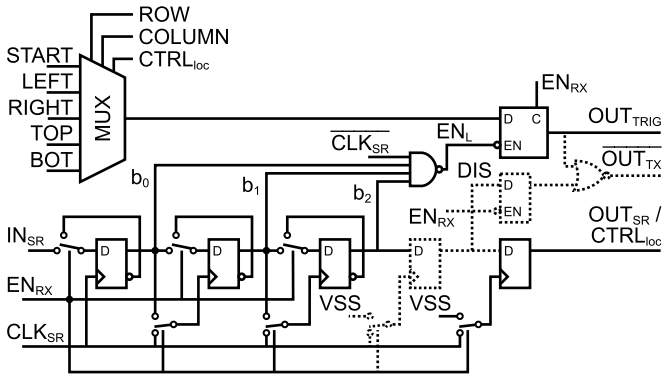


Fig. 4. Circuit details of a TX beamformer cell with additional local pulse disabling in dashed lines.

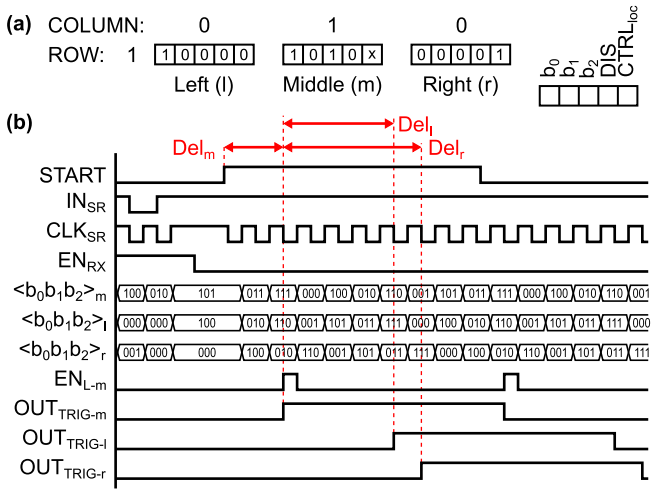


Fig. 5. (a) Example of the status of three neighboring cells at the start of the TX period. (b) Timing diagram showing the SR loading of the TX beamformer cell, subsequent pulsing based on the delay from the START trigger, and further propagation to neighboring cells. Edit: added (a) and reworked the timing diagram.

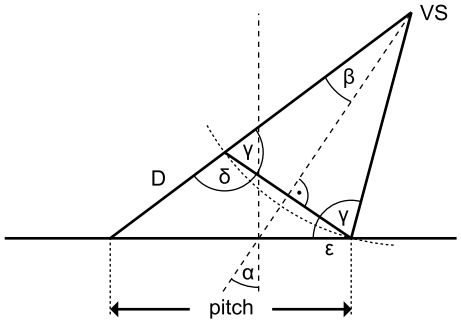


Fig. 6. Drawing showing the difference D in excitation of two elements with a certain pitch in order to create a steered diverging wave.

presented method. The targeted imaging scheme [10] relies on diverging waves that are generated by propagating a delay from the center outwards as shown in Fig. 3(a). However, it is also possible to create other common patterns, such as the angled plane waves in Fig. 3(b) or focused waves in Fig. 3(c). The graphs also demonstrate how these patterns are created by indicating the starting position and R/C control with arrows along the side of the matrix. Arrows in the matrix are pointing from the element that the trigger signal was received from and Fig. 3(d) presents the complete element-level logic table.

The circuit of an SR BF cell is shown in Fig. 4. The local relative delay value is loaded into three flip-flops (FFs) as part of the SR with the SR input, $\mathrm{IN_{SR}}$, and clock, $\mathrm{CLK_{SR}}$. As the delay information is only required during the TX phase, loading of the delay cells in the SR is done during RX without additional hold cells. Moreover, an area-efficient implementation is reached by repurposing the unused SR cells to counters during TX based on the T/R control signal, $\mathrm{EN_{RX}}$. The reconfiguration is achieved by switching the FF data inputs to an inverting feedback loop around the cell and using the data output of lower order bits as the clock input of higher order bits, leading to only a few switches as overhead instead of more FFs. The number of delay steps equals 2^N, N being the number of counter cells, and the actual delay is determined by the frequency of $\mathrm{CLK_{SR}}$ during TX as it remains connected to the least-significant bit (LSB), $\mathrm{b_0}$. In this design, the 100-MHz SR clock is maintained during TX and there are three counter cells per element, leading to a total of eight steps from 0 to 70 ns.

The counter rotation is converted to an enable signal for a latch, $\mathrm{EN_L}$, by detecting its highest value with a negative-AND (NAND) gate. All counters are continuously active during TX, but only when the dedicated neighbor has previously received the external trigger, it is copied further with the relative delay. Including an inverted version of $\mathrm{CLK_{SR}}$ can block any glitches in the asynchronous counter and clearing the latch during RX with $\mathrm{EN_{RX}}$ prevents any TX triggers in the wrong phase. Selection of the latch input is made with a multiplexer (MUX) controlled by the R/C signals and the output of the last element-level SR cell that serves as $\mathrm{CTRL_{loc}}$ but also as the output to the SR of the next element, $\mathrm{OUT_{SR}}$. Five different input triggers can be selected, LEFT to BOT indicating the output triggers, $\mathrm{OUT_{TRIG}}$, of all neighboring elements and START being the initial external trigger. Fig. 5 shows, as an example, the operation of three neighboring elements in a row. In Fig. 5(a), the state at the beginning of the TX cycle is shown. The middle element is configured as a starting point. The left and right elements are configured to receive their trigger from the middle element (i.e., their right and left neighbors, respectively). The timing diagram of the whole procedure from the end of the SR operation in RX to the actual output triggers is shown in Fig. 5(b). The output triggers are directly used to control the pulsers and a diverging wave, steered to the left, is created.

The dashed circuitry in Fig. 4 is optional and has been included to support additional debugging by excluding single elements from the entire imaging operation. The implementation adds 1 bit in the local SR to receive a disable signal, DIS, and latches it such that it is also available during the RX phase. By not directly using $\mathrm{OUT_{TRIG}}$ to control the pulser but manipulating it with a negative-OR (NOR) gate to $\mathrm{OUT_{TX}}$, elements can be permanently connected to the HV supply. At the same time, the rest of the array can function as usual as the trigger is still being passed.

Next to a compact design, TX BF by shifting an LV trigger signal through the system also has the benefit of being

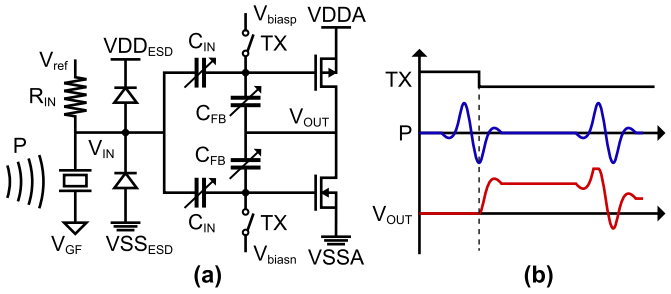


Fig. 7. (a) Simplified schematic of an inverter-based amplifier with split capacitor feedback and dynamic biasing. (b) Illustration of how the initial transducer state and forward biasing diodes due to large inputs can lead to offset issues with dynamic biasing.

able to dynamically change the number of pulses and even pulse frequency if required. One potential drawback for some applications is that only delays smaller than the pulsewidth can be generated as EN_L needs to latch during the active interval. However, this is commonly no issue for ultrasound imaging as is analyzed in the following. Typical ultrasound imager arrays remain at a pitch of half of the center transmit wavelength, λ, as that moves grating lobes out of the picture [52]. As the relative difference in distance, D, from a virtual source (VS) between neighboring elements can at most be equal to the element pitch, it can be shown that the maximum possible delay for these devices is half of the pulse period and thus in the coverable range

$$t_d = \frac{D}{c} = \frac{\frac{\lambda}{2}}{\lambda \cdot f} = \frac{T}{2} \tag{1}$$

where t_d is the required delay between elements, c is the speed of sound, f is the center frequency, and T is the pulse period. A way to determine the delay between neighbors for any pitch is shown using the diagram in Fig. 6. The relative distance from the VS can be calculated with

$$D = \frac{\sin(\alpha)}{\cos(\beta)} \cdot \text{pitch} \tag{2}$$

where α is a known angle determining beam steering and β is a known angle determining beam divergence. The equation is found by applying the law of sines on the lower triangle based on angles δ and ε, found with trigonometric equations, and can be used to derive the required delay by $\text{DEL} = D/c$. Although the pitch is slightly above half of λ, this results in maximum delays in the order of 70% of the 80-ns pulsewidth for the shown design with the intended 10° divergence and maximum steering angle of 30° [10].

B. Low-Noise Amplifier

The LNA architecture is based on the design presented in [35] but has been extended to enable co-integration with TX and high-frame-rate operation. Fig. 7(a) shows a simplified schematic of the prior design with a direct connection of the input node, V_{IN}, to the transducer element and input biasing to V_{ref} through a high-impedance path, R_{IN}. A compact implementation is reached by a split capacitor feedback network [53], an efficient inverter-based amplifier core, and dynamic biasing to potentials V_{biasx}. Discrete TGC is achieved by reconfiguration of the capacitor network comprised of C_{IN} and C_{FB} between receive cycles.

While the shown techniques have led to a receiver with state-of-the-art power and area efficiency, there are several concerns in the transition to a high-frame-rate imaging system with TX and RX on each element. To illustrate this, Fig. 7(b) shows two common problems that can be experienced in a transducer front end with incoming pressure waves, P, and dynamic biasing. To achieve quick settling following TX, the dynamic biasing is synchronized to the T/R cycle and active until shortly after TX is completed. The first issue is that, since echoes start returning immediately after the ultrasound transmission, the switching can never be guaranteed to take place at a moment in which no signal is present. As pulsing and dynamic biasing in a short-time window require a reference with a relatively low impedance, the final direct current (dc) operating point will be signal-dependent and can lead to a large offset. The second issue is that strong incoming signals, which often occur shortly after TX due to low initial attenuation in the medium, can lead to clipping due to the electrostatic discharge (ESD) protection diodes or the internal rails. This would change the dc operating point even during active RX, with no possibility to recover in a pure dynamic biasing implementation.

Irrespective of these external effects, the limitation to biasing in a short-time interval before reception also leads to issues if one would switch through all gain levels of the discrete TGC scheme due to non-ideal switching procedures. Finally, the transducer needs to be biased to a reference, V_{ref}, being, e.g., just the dc level of a bipolar pulser [14] or a mid-rail reference if the pulsing goes all the way to the negative rail [54]. Since this would need to happen in a short-time interval after TX, it cannot be covered by the high-impedance connection with R_{IN} for a design with TX and RX on the same element.

Fig. 8 shows the implemented design with the proposed changes. The LNA is still applying dynamic biasing to quickly settle all critical nodes in a short-time window after the possibly high disturbance of HV TX. To target the issues discussed above, this is assisted by the connection of the transducer to a mid-rail potential, V_{CM}, via resistors. The switches are controlled with RST_{LNA} and $RST_{LNA\text{-}DEL}$ to always close at the beginning of an RX period. $R1$ is used to raise the transducer top plate from its initial state of 0 V after pulsing to V_{CM}. The resistance is in the order of 50 kΩ to allow settling in 100 s of ns, not losing too much RX time but also not causing a second transmission. $R2$ is around 1 MΩ and connected longer, in the order of microseconds, to settle any offset due to large inputs received shortly after TX but then also disconnected as it is a potential source of noise and interference from other channels.

Next to the added resistive components, the biasing has also been modified compared to [35] by adjusting the way in which the inverter transistors are operated. During initial dynamic biasing, the upper transistor is still directly connected to a biasing voltage, V_{biasp}, and the lower transistor is still driven by an amplifier in a feedback loop to force the LNA output voltage, V_{OUT}, to a local mid-rail potential, V_{MID}.

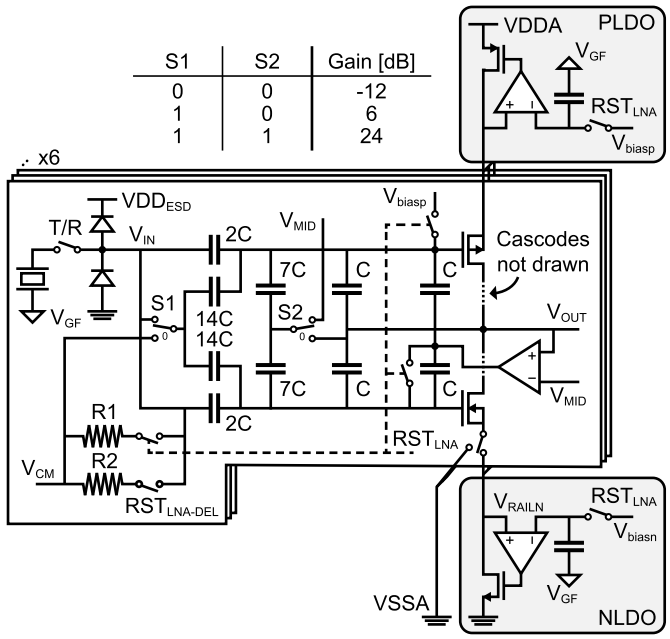


Fig. 8. Conceptual schematic of the inverter-based LNA showing gain switching, transducer biasing, and supply regulators.

However, this amplifier is not switched out and shorted after that but instead connected to two capacitors in parallel with the feedback capacitors of the LNA. This gives the structure a low-frequency path to correct for effects such as disturbances from gain switching or residual issues in the transducer biasing. Due to the low bandwidth of the additional amplifier and the capacitive attenuation toward the output, its noise contribution in the signal bandwidth as well as the power and area are negligible compared to the entire LNA.

The capacitor ratios and unit cells, C, of 45 fF are the same as in [35]. The input capacitors are held at the same potential the transducer is biased to, V_{CM}, before being switched in to minimize introduced disturbance in the RX period. Similarly, the feedback capacitors are connected to the same potential V_{out} that is driven to via the low-bandwidth loop after being switched out. After these capacitors are settled, there is also the option of removing them from V_{MID} in order to remove the noise from that source.

To mitigate the low power supply rejection ratio (PSRR) of the inverter-based topology [55], the LNA employs the local regulators [56] as in [35] and [48]. In this design, they are shared on the subgroup level and it can be chosen to switch to the analog ground, VSSA, instead of the negative low-dropout regulator (LDO) to investigate differences. In addition, the dynamically set references of both LDOs are capacitively coupled to the ground foil node of the transducer, V_{GF}. This enables the architecture to also reject variations of the ground foil node that would otherwise be amplified with the signal. Combined with the improved PSRR, this aims to reduce the common-mode interference across channels and thus maximize the possible gain from RX beamforming.

C. Programmable Gain Amplifier

The circuit implementation of the PGA is based on the compact architecture shown in [18] but modified as the original

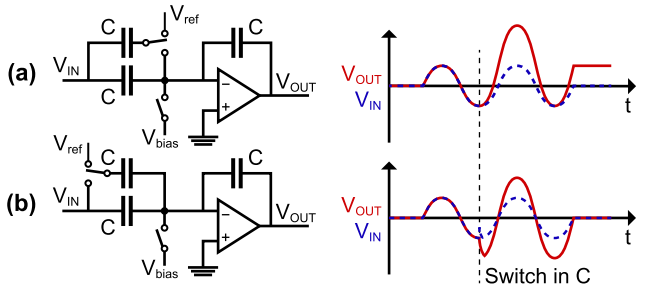
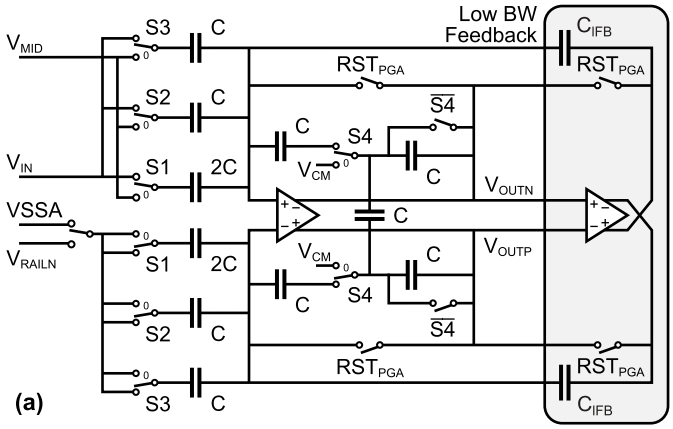


Fig. 9. Impact of switching the gain of an amplifier in a dynamically biased capacitive feedback in active operation from (a) back and (b) front.



S1	S2	S3	S4	Gain [dB]
0	1	1	0	6
0	1	0	1	12
0	1	1	1	18
1	1	1	1	24

(b)

Fig. 10. (a) Sketch of the PGA displaying gain switching and the implementation of a low-bandwidth feedback amplifier. (b) Logic table to determine the gain.

structure cannot support high-frame-rate operation and has a limited output swing. The main issue with volume acquisition at a high rate is presented in Fig. 9. The prior design is similar to Fig. 9(a) and achieves gain switching by adding a capacitor to the virtual ground of an amplifier in a capacitive feedback configuration. While the constant load presented to the driving stage of this setup is beneficial, this switching alters the operating point of the setup and leads to an offset if done during active operation. As the system is dynamically biased with V_{bias}, it cannot recover over time and even with a low-bandwidth correction path, and the possibly large step could lead to a significant loss of image information.

With the approach shown in Fig. 9(b), on the other hand, this can be avoided since the virtual ground node is not affected when the capacitor is switched from the input. The input experiences a short settling depending on the driver but then continues operation without an offset. In the proposed design, the configuration of Fig. 9(b) is adopted to enable gain switching during echo reception. This enables full TGC in one T/R cycle, rather than having to combine repeated T/R cycles with different gain settings, thus facilitating high-frame-rate operation. Fig. 10(a) shows the schematic implementation with compact T-type feedback [49] and Fig. 10(b) presents the associated logic table to determine the gain depending

on the switch settings. During one RX phase, the PGA will cycle through the settings three times to complement the three LNA gain switches to the full TGC range. To minimize the disturbance from gain switching, the input capacitors are connected to the output dc level of the LNA and the feedback capacitors are connected to a mid-rail potential, V_{CM}, when not in the loop. The LNA has sufficient phase margin and bandwidth to operate with the switching capacitance at its output and achieve quick settling.

Similar to [18], the structure is held in reset during TX to enable quick settling of the operating point after HV pulsing, but in addition to that, a low-bandwidth feedback path has been introduced. This enables the correction of any remaining disturbance caused by switching during one T/R cycle while adding little area and power consumption compared to that of the entire PGA. As they are not part of determining the signal gain, the capacitors of the low-bandwidth path can be adjusted in a tradeoff between attenuation of additional noise and achievable correction range. In this design, the unit capacitance, C, is 33 fF and the additional capacitors, C_{lFB}, are 9 fF. Combined with the low bandwidth of the feedback amplifier, the noise contribution to the signal path is negligible. Similarly, the mismatch between C and C_{lFB} will have a low impact on the overall noise performance of the PGA.

The configuration as a single-ended-to-differential converter from the prior design is kept to enable differential operation of the ADC and dummy switches are placed in the bottom branch of the feedback network as well to balance the design. However, instead of connecting to a mid-rail supply, the bottom branch is driven relative to the reference of the single-ended input. This ensures that no interferers are unintentionally amplified with the received signal and is realized by mirroring the negative rail connection of the LNA. The telescopic amplifier has moreover been replaced by a two-stage miller-compensated differential amplifier with an auxiliary amplifier to provide common-mode feedback [57]. The division in a first gain stage and a high-swing output stage can show bandwidth and power consumption similar to [18] while providing a larger output swing for the ADC and not leading to gain deviation.

D. Datalink

To explore possibilities to reduce the RX-related cables in the catheter, this design leverages the relatively relaxed BER requirement of ultrasound imaging [40]. By applying a multi-level PAM driver, several bits are transmitted in one symbol, allowing for a higher throughput without increasing the symbol rate that would cause limitations due to the low bandwidth of the thin cables [58] and applied process node. To reduce the power consumption associated with data transmission at the tip of the catheter, where heating must be limited to ensure safe operation in the human body [59], the driver has moreover been implemented based on LM [28]. Instead of direct driving, this only switches a variable load impedance, Z_{var}, on the chip with a driver on the other end of the cable, as shown in Fig. 11(a). This enables measurements at an evaluation point outside the body with part of the power consumption shifted to the system side where heating is not an issue.

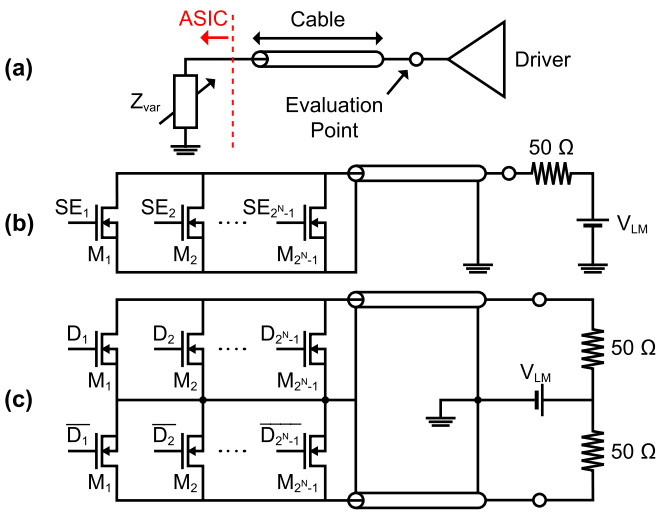


Fig. 11. (a) Block diagram summarizing the idea of LM. (b) Example of a single-ended LM implementation. (c) Example of a differential LM implementation.

In this design, single-ended and differential multi-level LM implementations are investigated. Fig. 11(b) gives an overview of the single-ended setup with the variable load being implemented by $2^N - 1$ transistors with scaled widths M_X, where N is the number of bits per symbol. The array is controlled with a thermometer code in SE_X and forms a divider with the termination resistance to a power supply, V_{LM}, on the system side. The differential configuration in Fig. 11(c) relies on the same mechanism but introduces a second, inverted path with the same scaling via a second cable. For 2 bits/symbol, the switches are designed from about 15 to 130 Ω, and for 4 bits/symbol, they are designed from about 10 to 850 Ω. While a differential channel takes an additional cable, more power consumption, and circuit area, the gained rejection of common interference compared to the single-ended structure can be beneficial in a narrow catheter with multiple parallel connections. In addition, the shared return current in the ASIC will be constant to the first order, reducing possible crosstalk between channels, and the differential signal swing is twice as high for the same supply. This potentially enables a higher bandwidth per channel at the same BER as the single-ended setup and makes differential signaling an interesting part of this study.

Fig. 12(a) gives an overview of the realized test setups in this design and their control. The 60 recombined data bits from six ADC pairs operating at 48 MHz are multiplexed into 12-bit words at 240 MHz. Based on this input, three different configurations are being analyzed in parallel: a differential driver with 2 bits/symbol at 1.44 GS/s (D-2b), a differential driver with 4 bits/symbol at 0.72 GS/s (D-4b), and two single-ended drivers with 2 bits/symbol at 0.72 GS/s that share the total data input (SE-2b). All of these achieve the targeted RX data cable reduction of 18 to ultimately arrive at a total of 64 data connections for the full probe [10] and enable the direct comparison of all schemes. The timing is provided

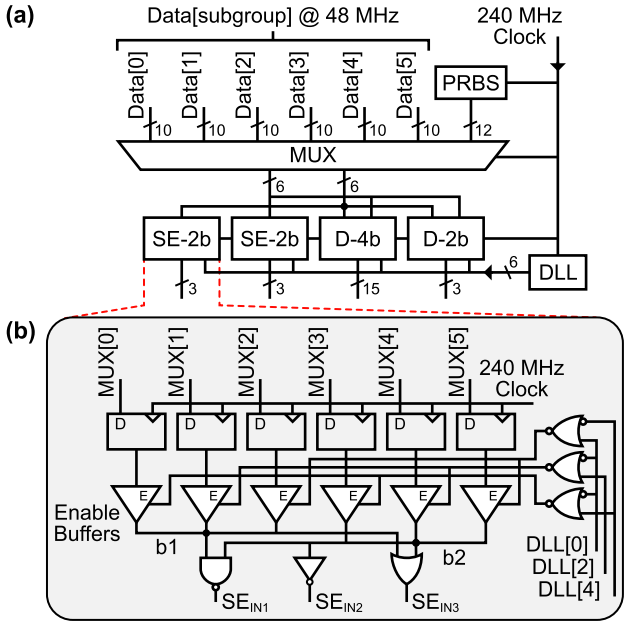


Fig. 12. (a) Overview of the data and control configuration for the multi-level signaling. (b) Details of a single-ended implementation with 2 bits/symbol.

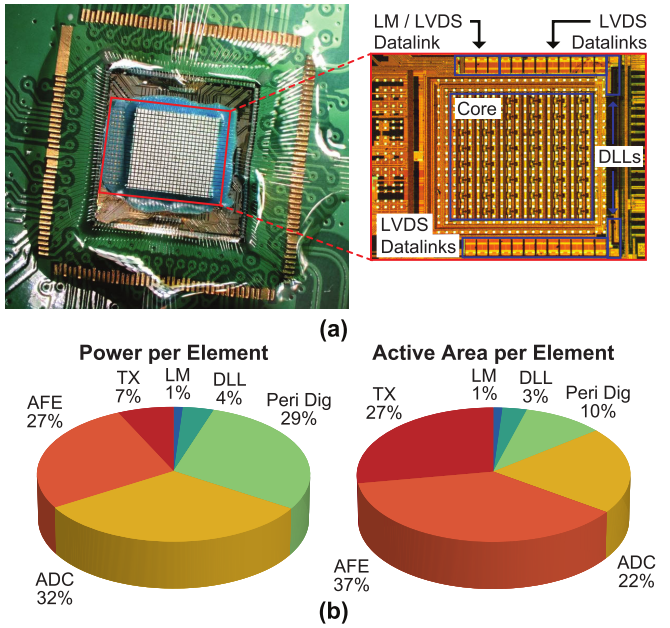


Fig. 13. (a) Micrograph of a chip with transducer stack on its surface and an inset showing the global floorplan below. (b) Power and active area per element divided among major contributors.

by a DLL that creates six phases out of the input clock to accommodate the highest transmit frequency.

The internal structure of the control blocks is shown by the example of a single-ended cell in Fig. 12(b). After synchronization of the recombined and multiplexed ADC outputs to the input clock, an array of buffers is used to drive two outputs, b1 and b2. The buffers can be disabled to have a high output impedance and effectively multiplex onto one output based on the overlap of phases from the DLL. Local generation of the overlap avoids the need for distributing a high-frequency clock and is done with one layer of logic gates. For the single-ended setup, only every second DLL output phase is required to realize the 0.72-GS/s output stream. In the last stage, the binary signal is converted to a thermometer representation for the LM driver based on logic gates.

The system also provides a second path with a pseudorandom bit sequence (PRBS) generator to be able to investigate the BER. It is implemented as a linear-feedback SR (LFSR) of 20 cells with 12-bit parallel output [60].

IV. Experimental Results

An overview of the manufactured device is given in Fig. 13(a). The ASIC has been fabricated in a 180-nm HV BCD technology and a transducer stack with a 160-μm pitch, 6-MHz center frequency, and 50% bandwidth has been manufactured on its surface. The 16 $\times$ 18 element matrix is complemented by two rows of dummy transducer elements to reduce edge effects and the ASIC measures a total of 7 $\times$ 7 mm in order to ease manufacturing of the prototype transducer. In the inset, the global floorplan shows a separation in two halves with datalinks on the top and bottom, enabling further scaling of the unit-cell-based structure along the horizontal axis. On the TX side, the circuit operates on a 30-V supply for the pulsers, a 5-V supply for driving the pulsers, and a 1.8-V supply for digital operations. The receiver is powered from a separate analog 1.8-V supply with an additional 1.2-V supply for the DLL delay cells and a 2.3-V supply for parts of the ADC [15].

Fig. 13(b) presents the system-wide power and active area distribution per element. All displayed power consumption is based on measured supplies during active operation and labeled with the most dominant contributor of the relevant segment. The total power consumption of 1.2 mW per element is dominated by the RX path with 27% being primarily associated with the AFE including LDOs, 32% to the ADC, and 29% to the digital periphery blocks realizing recombination and conversion for LM signaling. The DLLs just account for about 4% of the total power as they are heavily shared across the array and the LM driver can achieve a share of only approximately 1% per element. The TX power consumption is highly dependent on the imaging mode but is generally a minor contributor due to the duty-cycled nature of ultrasound imaging. The displayed values are obtained with a three-pulse excitation of all elements at the maximum transmit voltage and 10-cm imaging depth, such as used for the creation of the b-mode images shown in this article. In the total active area of 0.03 mm^2 per element, the TX-related structures take a larger share of 27% due to area-intense HV isolation in the BCD technology. On the RX side, the AFE is the main contributor with 37%, while the remainder is shared between about 22% for ADC-related structures, 10% for the digital periphery blocks, 3% for the DLLs, and 1% for the LM driver.

To evaluate the effectiveness of the implemented techniques, electrical and acoustic experiments have been conducted. The two configurations are each assembled with an individual daughter board to facilitate their specific requirements. Electrical test boards offer direct wire bonding to element-level

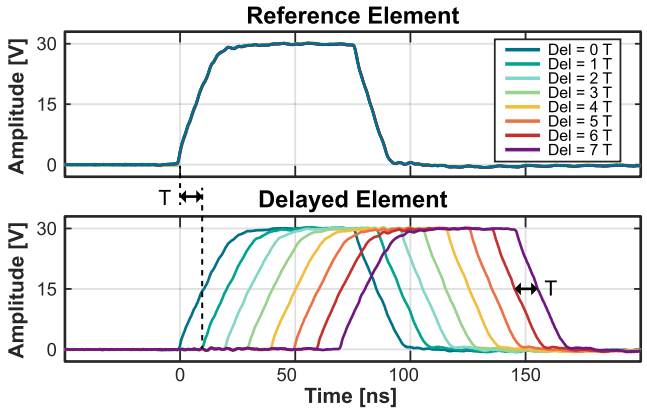


Fig. 14. Measurement of the transmit delay between two neighboring elements with configurations from the minimum to the maximum setting.

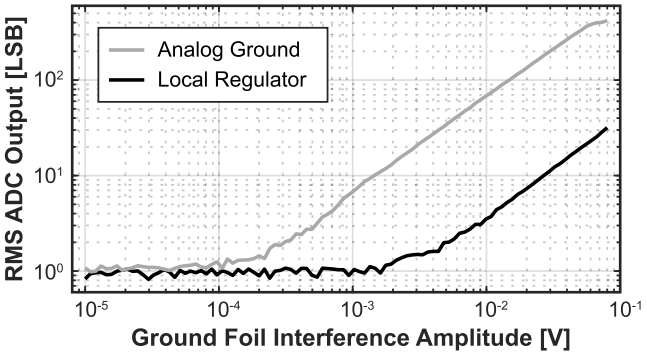


Fig. 15. Measured ADC output relative to the amplitude of an interfering signal applied to the ground foil node in the case of LNA connection to the shared analog ground or local negative supply regulator.

bondpads, while acoustic samples are assembled with a prototype transducer matrix. A custom mother board is designed to be compatible with both and interfaces with a computer for data processing through commercial FPGAs [51].

A. Electrical Measurements

Fig. 14 shows the electrical characterization of the transmit beamformer. Two neighboring elements are each connected with a capacitor to mimic the capacitive load of a single transducer element of about 2 pF. The delay between them is swept through all the configurations from zero to seven unit time periods, T. The interval is determined by the clock frequency of the time reference and is in this case approximately 10 ns. The waveforms exhibit the targeted slewing and extend to the maximum transmit amplitude of 30 V.

To investigate the implemented scheme for common-mode interference rejection around the first-stage amplifier, an experiment with an intentionally injected interferer is carried out. Fig. 15 shows the root-mean-square (rms) ADC output caused by an amplitude sweep of a 6-MHz sinusoidal signal driven onto the ground foil node with the LNA input being connected to it in the highest gain setting. To study the effects, the two configurations of the negative supply connection of the LNA, either to the shared analog ground node or the local negative supply regulator, are compared. The larger ground foil interference required to elevate the output code from the

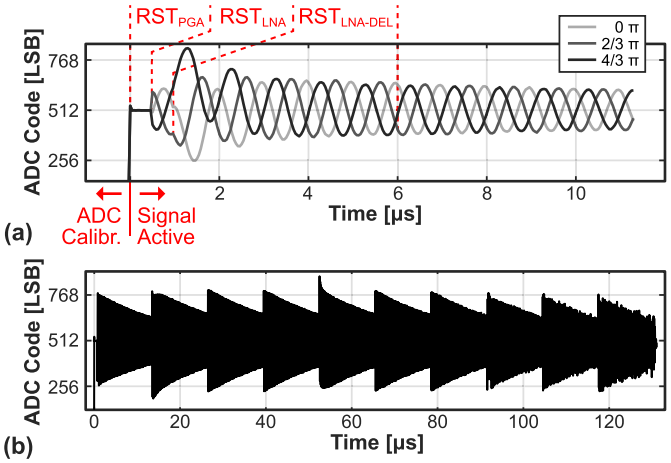


Fig. 16. (a) Initial converter output settling for an exponentially decaying sinusoidal input with three different phases and indicated amplifier biasing times. (b) Converter output showing settling during a full T/R cycle with TGC and an exponentially decaying sinusoidal input.

noise floor in the case of LNA connection to the local regulator shows the effectiveness of the suppression.

The settling of biasing points in the presence of input signals is studied with a 2-pF capacitor, modeling the capacitive component of the transducer element, in series with an arbitrary waveform generator (AWG). Fig. 16(a) shows the ADC output at the beginning of a receive phase with three different phases of an exponentially decaying 1-MHz sinusoidal input in the lowest gain setting. The signal is active before the dynamic biasing is completed and shows the response to different initial states of the high-impedance input node when actual reception is started. Typically, $\mathrm{RST_{PGA}}$ would be asserted longer than $\mathrm{RST_{LNA}}$ to optimize settling, but it is in this case disabled earlier as it would otherwise mask the output signals needed to study the behavior. In this example, $\mathrm{RST_{PGA}}$ is active 500 ns after the start of input signaling with $\mathrm{RST_{LNA}}$ and $\mathrm{RST_{LNA\text{-}DEL}}$ being asserted 500 ns and 5 μs longer, respectively. The recorded outputs show a signal-dependent offset introduced after the completion of dynamic biasing and subsequent recovery provided by the resistive input biasing and the low-bandwidth amplifier feedback paths. Fig. 16(b) additionally shows the ADC output during a full T/R cycle with an exponentially decaying 6-MHz input from an AWG. TGC is used from the lowest to the highest gain setting to maintain the output code level and it can be observed how non-ideal steps in the gain are compensated by the implemented biasing techniques.

To evaluate potential power savings from the implementation of a multi-level LM driver, Fig. 17 shows a measurement of the obtained BER for a sweep of the LM supply voltage, V_{LM}, for all investigated configurations. All results are obtained using the PRBS generated on the chip and with an assembly of 42-AWG micro-coaxial cables with a 50-Ω characteristic impedance and a length of 1 m. The transmitted sequence is directly obtained by an oscilloscope and compared to the expected pattern after a decision feedback equalization step to determine the error rate. Due to the maximum memory depth of the oscilloscope, there is a minimum measurable

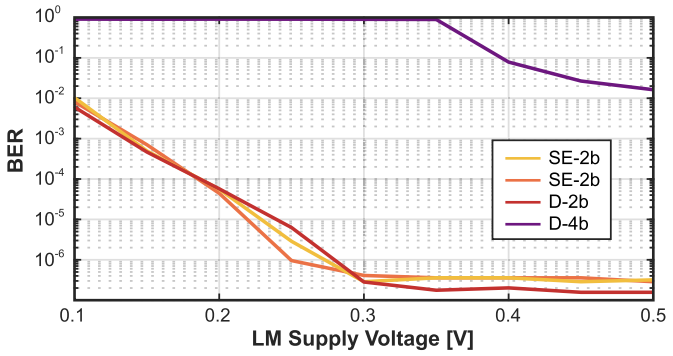


Fig. 17. BER measured for all implemented multi-level datalinks in a sweep of the LM supply voltage.

BER at about $3e^{-7}$ for the SE-2b and D-4b configuration as well as half of that for the D-2b configuration. The acquired results show that even for an LM supply of about 0.27 V, all datalinks with 2 bits/symbol can achieve the targeted BER of $1e^{-6}$ to have negligible degradation of ultrasound images [40]. The significantly worse performance of the PAM-16 approach is attributed to the higher sensitivity to non-idealities in the transmitter circuit design, receiver, and equalizer when the spacing between signal levels reduces.

Out of all implemented setups, the differential transmitter with 2 bits/symbol is considered the most attractive option out of this experiment. It has a competitive performance compared to its single-ended counterparts with the same number of cables while offering more resistance to common interference. Further improvements are expected when replacing the two micro-coaxial cables for differential signaling with a differential cable. The total power spent in the D-2b setup for V_{LM} of 0.27 V is 1.2 mW, of which about 52% is spent on the chip and the rest in the 50-Ω termination and 9 Ω of the cable. Given the resulting 17-μW on-chip power consumption per element of the multi-level LM approach compared to the 260 μW per element for the implemented LVDS scheme, the designed topology shows great potential to trade surplus BER for lower power and cable count.

B. Acoustic Measurements

The characterization of the TX BF functionality is shown in Fig. 18, following the example patterns shown in Fig. 3. The measurements are obtained with the chip assembly being submerged in water and facing a commercial hydrophone [61]. By translation of the hydrophone with an xyz-stage during repeated transmission from the prototype, C-planes in parallel to the transducer surface are captured. These evaluate the maximum peak pressure at each position and are compared to simulations [62] based on the same set of delays. Fig. 18(a) shows the simulated pressure profile at a 5-cm distance from the array for the transmission of a diverging wave on the left and the corresponding hydrophone measurement on the right. Fig. 18(b) similarly shows the results for a plane wave angled at 10° to the northeast at a distance of 5 cm from the array and Fig. 18(c) shows a plane 2 cm from the array with the TX BF focusing at its center. Good agreement between

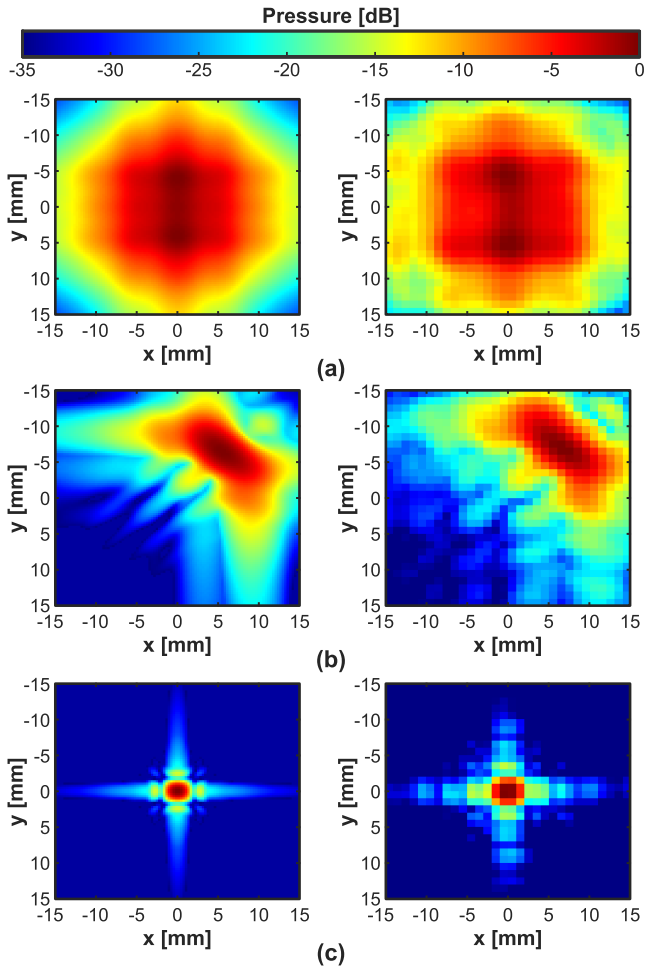


Fig. 18. Comparison of simulated C-planes on the left and corresponding measured C-planes on the right for (a) diverging beam at 5 cm from the array, (b) plane wave steered to the northeast at 5 cm from the array, and (c) focused beam at 2 cm from the array.

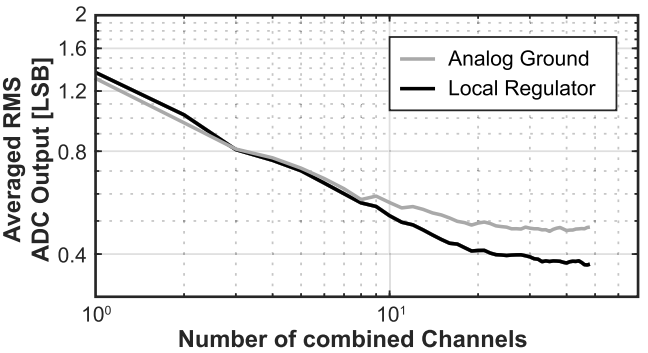


Fig. 19. Investigation of the noise output of the array as a function of the number of combined channels with the LNAs being connected to the shared analog ground or local negative supply regulators.

the measured and simulated profiles in all cases verifies the capability of creating the most common transmit-beamforming patterns applied in ultrasound imaging.

An experiment investigating the noise behavior of the array is presented in Fig. 19. In this experiment, a varying number of output channels of the chip were averaged to mimic the averaging operation associated with beamforming and the

TABLE I
COMPARISON WITH THE PRIOR ART IN CATHETER-BASED ULTRASOUND IMAGERS

	This work	JSSC'22 [15]	JSSC'21 [16]	VLSI'19 [17]	JSSC'18 [18]	TUFFC'16 [9]
Technology	**180 nm BCD**	180 nm BCD	180 nm	180 nm	180 nm	N/A
Transducer	**2D PZT**	2D PZT	2D PMUT	2D PZT	2D PZT	2D PZT
Array Size	**16 x 18**	8 x 9	6 x 6	4 x 4	6 x 24	60 x 14
Center Frequency	**6 MHz**	6 MHz	5 MHz	5 MHz	5 MHz	5.6 MHz
Pitch-matched	✓	✓	✗†	✓	✓	✓
Element Pitch	**160 µm x 160 µm**	160 µm x 160 µm	250 µm x 250 µm	150 µm x 150 µm	150 µm x 150 µm	110 µm x 180 µm
Included TX	**30 V**	65 V	13.2 V	✗	✗	40 V
TX Beamforming	**integrated**	external	integrated	✗	✗	integrated
Digitization	✓	✓	✓	✓	✓	✗
RX architecture	**AFE + µBF + ADC + Datalink**	AFE + µBF + ADC + Datalink	AFE + ADC	AFE + ADC	AFE + µBF + ADC + Datalink	AFE + µBF
El. / RX Cable	**18** §	6	0.5	0.5	18	15 to 20
Data transmission	**PAM-4 LM** §	LVDS	N/A	LVDS	LVDS	analog
Supported Frame-Rate	**1000 vol/s**	1000 vol/s	N/A	N/A	200 vol/s	50 vol/s
Active Area / El.	**0.030 mm²** §	0.032 mm² §	0.063 mm²	0.023 mm²	0.026 mm² §	N/A
RX power / El.	**1.12 mW** §	1.23 mW §	1.14 mW	1.54 mW	0.91 mW §	< 0.12 mW
Peak SNR	**52.2 dB**	52.3 dB	57.8 dB ‡	49.8 dB	52.8 dB	N/A

† Scalability limited by a non-integrated transducer array and its connection outside of the pitch.
§ With the proposed Datalink and drivers. ‡ ADC only, excluding AFE.

associated expected noise reduction. The measurements were done on a sample with transducer elements loaded with water and were recorded in the highest gain setting without an input signal. To study the effect on the noise floor, the experiment is conducted with the negative rail of the LNA being connected to the shared analog ground or local supply regulators. Fig. 19 shows the rms value of the averaged outputs, as a function of the number of channels being combined. For both connections of the negative rail, there first is an exponential reduction in the amplitude before the two curves flatten off at different effective array sizes. The initial decline is close to the anticipated $\sqrt{N}$ improvement of uncorrelated noise for N combined signals [44] but gets limited by the presence of correlated interference between channels. The reduction in common interference and, thus, improvement of potential beamforming gain for the LNA connection to the local regulator compared to the direct analog ground connection can be explained with an enhanced PSRR. Noise on the shared power rails appears common to all elements and can, even in this reduced-size prototype and without active input, pose a limit to the beamforming gain.

To verify imaging functionality, a commercial 3-D wire test phantom [63] has been studied with the setup shown in Fig. 20(a). The ASIC is mounted on a custom daughterboard that faces the surface of the phantom. The daughterboard provides local decoupling and connects to a motherboard with active components for supply regulation and signal conditioning via 1-m cables. The acquired receive data from the 24 LVDS channels is captured and stored by commercially available FPGA boards [51] in real time. Each FPGA board offers eight high-speed transceivers and three boards are thus used in parallel, while one of them additionally acts as a control host for the ASIC configuration per T/R cycle. The acquired data are downloaded to a computer that initiates measurement routines and performs image processing.

Fig. 20(b) shows a reconstructed image with the wires aligned in the azimuthal direction of the array so that they show up as point scatterers in the elevation plane. The upper seven gain settings of the TGC have been applied in each T/R cycle to maintain a suitable DR in the signal path across the attenuating phantom. A switching artifact can be observed when the LNA transitions to its highest gain setting while the PGA gain steps are barely noticeable. The artifact is caused by non-ideal switching resulting in a step in the RX signal and appears at a 0° azimuth and elevation angle after RX beamforming as the entire array is switching simultaneously. Given its deterministic nature, the artifact does not inherently harm the imaging and can potentially be compensated for during data processing.

As off-axis reflections do not propagate back to the transducer, the wire targets appear almost as points rather than lines in the 3-D plot. The behavior along the other dimension is thus evaluated by rotating the chip to align with the azimuth direction, as shown in Fig. 20(c). The lower opening angle in the azimuth render is caused by the application of the imaging scheme described in [10]. This scans a volume of 70° × 70° × 10 cm at 1000 volumes/s with seven fan-shaped beams with little divergence in the elevation direction and large divergence in the azimuth direction. As this prototype implements the full intended aperture in the elevation direction, the functionality of the 1-D subarray beamformer and TX BF can be fully verified. By choosing to realize a beamwidth in the

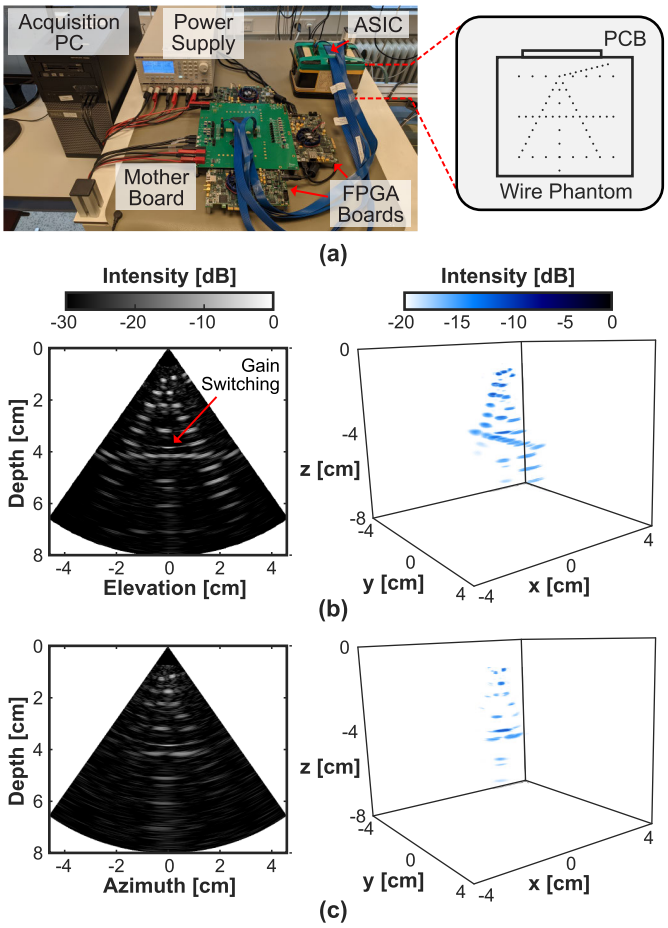


Fig. 20. (a) Measurement setup used for imaging verification with details of the 3-D wire phantom. (b) Reconstructed image plane in the elevation direction with 3-D render. (c) Reconstructed image plane in the azimuth direction with 3-D render.

elevation direction that is the same as in the intended imaging scheme while having an aperture that is 4× smaller than the intended final size in the azimuth direction, the resulting azimuthal opening angle is approximately equal to the 20° opening angle in the elevation direction, for this approximately square array.

Table I summarizes the system and gives a comparison to the prior art in catheter-based ultrasound imagers. The system complements our earlier design described in [15] with an integrated TX beamformer and a novel multi-level LM while still providing the highest reported frame rate. This completes the architecture and shows a similar peak SNR in a 4× larger array.

V. Conclusion

A transceiver ASIC implementing a comprehensive architecture for catheter-based high-frame-rate 3-D ultrasound imaging probes has been presented. A compact on-chip transmit beamformer design that can provide all required beam patterns is achieved by the combination of an area-efficient R/C architecture and a flexible SR approach. The impact of common interference and settling in the AFE have been investigated, and mitigation methods have been presented. The application of TDM, subarray beamforming, and an LM, multi-level data transmission channel, has led to a high cable-count reduction while reducing the power consumed on the chip and still offering a high frame rate. A prototype chip has been manufactured and successfully applied in a high-frame-rate, 3-D imaging experiment to verify the functionality.

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Yannick M. Hopf (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees (cum laude) in electrical engineering from the Technical University of Darmstadt, Darmstadt, Germany, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, in 2023, with a focus on application-specific integrated circuit (ASIC) design for 3-D high-frame-rate medical ultrasound imaging.

He is currently working with Sonosilicon, Delft, The Netherlands, as a Senior Analog Design Engineer to provide ASIC solutions for the next generation of medical ultrasound devices.

Dr. Hopf was a recipient of the Eckelmann AG Price for best M.Sc. degree in his year, the ProRISC 2022 Best Presentation Award, and the 2023 SSCS Predoctoral Achievement Award. His current research interests include analog and mixed-signal integrated circuits for ultrasound imaging, high-voltage electronics, and low-power analog-to-digital converters.

Djalma Simoes dos Santos (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Federal Institute of São Paulo, São Paulo, Brazil, in 2014, and the M.Sc. degree in biomedical engineering from the University of São Paulo, São Paulo, in 2018. He is currently pursuing the Ph.D. degree with the Laboratory of Medical Imaging, Department of Imaging Physics, Delft University of Technology, Delft, The Netherlands, with a focus on transducer design for high-frame-rate 3-D ultrasound imaging.

Outside of academia, he has worked as an engineer in industry for over five years. His current research interests include the design, modeling, and fabrication of ultrasound transducers for medical applications.

Boudewine W. Ossenkoppele (Graduate Student Member, IEEE) received the B.Sc. degree in aerospace engineering and the M.Sc. degree in mechanical engineering from the Delft University of Technology, Delft, The Netherlands, in 2015 and 2018, respectively, where she is currently pursuing the Ph.D. degree with the Laboratory of Medical Imaging, Department of Imaging Physics.

Her current research interests include high-frame-rate 3-D ultrasound imaging, beamforming algorithms, ultrasound transducer design, and deep learning for ultrasound signal processing.

Mehdi Soozande (Student Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Sistan and Baluchestan, Zahedan, Iran, in 2011, and the M.Sc. degree in biomedical engineering from the Tehran University of Medical Sciences, Tehran, Iran, in 2015.

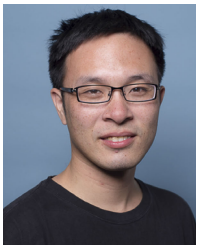
He worked as a Researcher with the Department of Biomedical Engineering, Erasmus Medical Center, Rotterdam, The Netherlands, from 2017 to 2021. In 2021, he joined Nearfield Instruments, Rotterdam, as an Ultrasound/Acoustic Researcher. His current research interests include gigahertz (GHz) ultrasound imaging for non-destructive testing (NDT) in semiconductor industry, advanced beamforming techniques, and atomic force microscopy.

Emile Noothout received the bachelor's degree from the Intermediate Technical School for Mechanics, Dordrecht, The Netherlands, in 2004.

From 2004 to 2006, he was with the Leidse Instrumentmaker School, Leiden, The Netherlands, where he studied for Research Instrument Maker. From 2007 to 2013, he was a Research Instrument Maker with TNO, Delft, The Netherlands. Since 2013, he has been with the Delft University of Technology, Delft, where he is involved in the development of medical ultrasound transducers and research assistance.

Zu-Yao Chang received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2003.

Since 2003, he has been a Staff Member with the Electronic Instrumentation Laboratory, Delft University of Technology, focusing on impedance measurement systems and smart sensor systems.



Chao Chen (Member, IEEE) received the B.Sc. degree in micro-electronics from Tsinghua University, Beijing, China, in 2010, and the M.Sc. (cum laude) and Ph.D. degrees in micro-electronics from the Delft University of Technology, Delft, The Netherlands, in 2012 and 2018, respectively.

Since 2017, he has been a Senior Analog IC Designer with Butterfly Network, Inc., Guilford, CT, USA, where he is currently a Consultant. Since 2021, he has also been with the Delft University of Technology, as a Post-Doctoral Researcher. His current research interests include integrated circuits for medical ultrasound and data converters.

Dr. Chen was a recipient of the 2017 IEEE IUS Best Student Paper Award and the 2019 Else Kooi Award. He was a co-recipient of the 2021 ISSCC Anantha P. Chandrakasan Distinguished-Technical-Paper Award and Demonstration Award, the 2020 ISSCC Technology Innovation Award, and the 2017 A-SSCC Best Student Paper Award.

Hendrik J. Vos (Member, IEEE) received the M.Sc. degree in applied physics from the Delft University of Technology, Delft, The Netherlands, in 2004, and the Ph.D. degree from the Department of Biomedical Engineering, Erasmus Medical Center, Rotterdam, The Netherlands, in 2010.

He worked as a Postmaster Researcher with the University of Florence, Florence, Italy, and a Contract Researcher for the petrochemical industry on cutting-edge ultrasonic solutions. He is currently an Associate Professor with the Erasmus Medical Center and the Delft University of Technology. His research interests include acoustical array technology for biomedical imaging in all its aspects: transducers, 2-D and 3-D beamforming, cardiac shear waves, ultrafast Doppler, contrast imaging, and related preclinical and clinical studies.

Dr. Vos received the Dutch NWOTTW VIDI Personal Grant in 2018.

Johan G. Bosch (Member, IEEE) received the M.Sc. degree in electrical engineering from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 1985, and the Ph.D. degree from Leiden University, Leiden, The Netherlands, in 2006.

He is currently an Associate Professor with the Department of Biomedical Engineering, Thoraxcenter, Erasmus Medical Center, Rotterdam, The Netherlands. He is a (Co-) Principal Investigator of projects on 3-D ultrasound image formation, transducer development, 2-D and 3-D cardiovascular imaging, and flow and tissue stiffness assessment using novel ultrasound approaches. His research interests include echocardiographic image processing, transducer development, and novel ultrasound techniques for image formation and functional imaging.

Martin D. Verweij (Member, IEEE) received the M.Sc. (cum laude) and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1988 and 1992, respectively.

In 1998, he became an Associate Professor with the Laboratory of Electromagnetic Research, Delft University of Technology, where he joined the Laboratory of Acoustical Wavefield Imaging in 2011. Since 2021, he has been heading the Ultrasound Group, Department of Imaging Physics, Delft University of Technology. His current research interests include dedicated transducer designs, beamforming algorithms, and the theoretical modeling and numerical simulation of medical ultrasounds.

Dr. Verweij is an Associate Editor of the *Journal of the Acoustical Society of America*.

Nico de Jong (Member, IEEE) graduated from the Delft University of Technology, The Netherlands, in 1978. He received the M.Sc. degree in applied physics in the field of pattern recognition and the Ph.D. degree in 1993 with a focus on acoustic properties of ultrasound contrast agents.

He has been the Vice Head of Biomedical Engineering with the Thoraxcenter, Erasmus Medical Center, Rotterdam, The Netherlands, headed by Prof. Ton van der Steen. He has been the Head of the Medical Imaging Group, Delft University of Technology, until 2021. From 2003 to 2011, he was a part-time Professor with the University of Twente, Enschede, The Netherlands, in the Physics of Fluids Group headed by Prof. Detlef Lohse, He is the Founder and a Co-Organizer of the annual European Symposium (this year for the 28th time, see www.echocontrast.nl) on Ultrasound Contrast Imaging, held in Rotterdam and attended by approximately 175 scientists from universities and industries all over the world. Now, he has partly retired and still doing research at the Delft University of Technology and the Erasmus Medical Center. He has graduated 51 Ph.D. students and is currently supervising seven Ph.D. students.

Dr. de Jong has been an Associate Editor of *Ultrasound in Medicine and Biology* and has been a guest editor for special issues of several journals.

Michiel A. P. Pertijs (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees (cum laude) in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2000 and 2005, respectively.

From 2005 to 2008, he was with National Semiconductor, Delft, where he designed precision operational amplifiers and instrumentation amplifiers. From 2008 to 2009, he was a Senior Researcher with imec/Holst Centre, Eindhoven, The Netherlands. In 2009, he joined the Electronic Instrumentation Laboratory, Delft University of Technology, where he is currently an Associate Professor. He heads a research group focusing on integrated circuits for medical ultrasound applications. He has authored or coauthored two books, four book chapters, 15 patents, and over 160 technical articles.

Dr. Pertijs is a member of the Technical Program Committee of the European Solid-State Circuits Conference (ESSCIRC) and the IEEE International Ultrasonics Symposium (IUS). He received the ISSCC 2005 Jack Kilby Award and the JSSC 2005 Best Paper Award. For his Ph.D. research on high-accuracy CMOS smart temperature sensors, he received the 2006 Simon Stevin Gezel Award from the Dutch Technology Foundation STW. In 2014 and 2023, he was elected Best Teacher of the EE Program at the Delft University of Technology. He served on the Program Committee of the International Solid-State Circuits Conference (ISSCC) and the IEEE Sensors Conference. He served as an Associate Editor for the IEEE OPEN JOURNAL OF SOLID-STATE CIRCUITS (O-JSSC) and the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC).