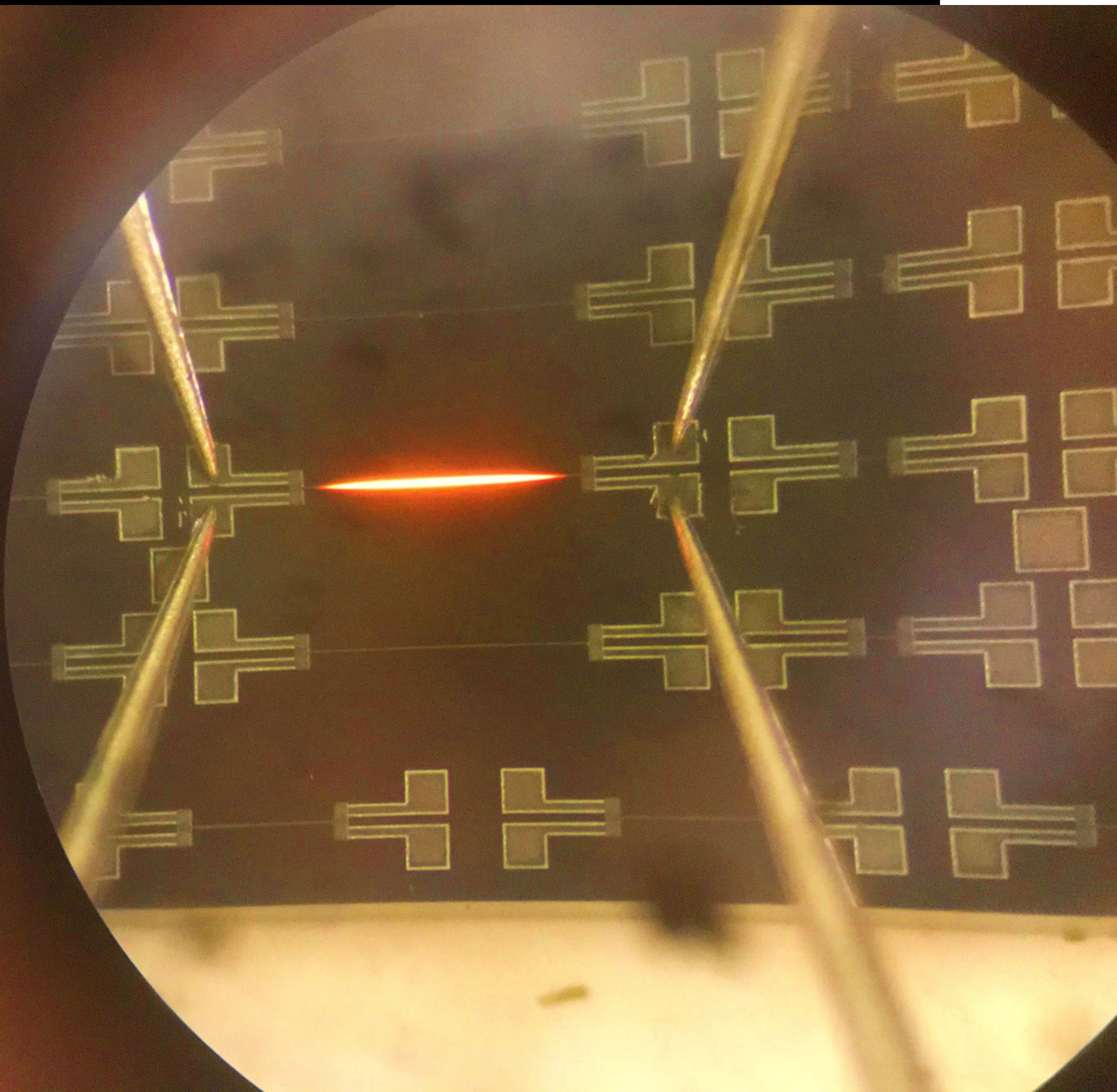
Modelling, Design, and Fabrication of High-temperature Compatible Vacuum Gauges in Silicon Carbide

J. Mo

Master of Science Thesis



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MODELLING, DESIGN, AND FABRICATION OF HIGH-TEMPERATURE COMPATIBLE VACUUM GAUGES IN SILICON CARBIDE

by

Jiarui Mo

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ABSTRACT

The demand for monitoring vacuum level at a high temperature is growing rapidly. For instance, in the semiconductor industry, the deposition process of many thin films is conducted in a high-temperature environment where the vacuum needs to be precisely monitored and controlled. Although a number of micro-fabricated vacuum gauges which show great performances have been implemented by silicon technology, they are not dedicated for high-temperature applications. The traditional Si-based sensor will lose its functionality when it is exposed to high temperature because of the degradation of the silicon.

This research work focuses on the implementation of a high-temperature compatible vacuum gauge, and the aim is to achieve an operation temperature (i.e. 500 °C) compatible with current high-temperature compatible electronics reported in the literature. The combination of poly-SiC and micro-bridge based vacuum gauge is proposed as a feasible solution. The fabrication of the vacuum gauge is conducted at the EKL cleanroom, and Pirani gauges with various geometries are fabricated by employing thin-film technologies for deposition and lithography for defining patterns. The gauge with a length up 1000 μm and a gap size down to 500 nm is achieved without any buckling. The fabrication process is a four-mask step, and it provides the potential for mass production and integration with readout electronics.

The micro-fabricated Pirani gauge showed good measurement results. Empirical Pirani gauge design rules were confirmed by experiments. It is confirmed that a longer beam and a smaller gap size will bring a larger dynamic range. At room temperature, the nominal gauge (length = 250 μm, width = 8 μm, thickness = 2 μm and gap distance = 500 nm) shows a maximum resistance change of 17.8 % from around 10 Pa to 100000 Pa, with a maximum sensitivity of 0.44 Ω/Pa. The vacuum gauge also showed a successful operation up to 750 °C, with a maximum sensitivity of 0.787 mV/Pa (1.097 Ω/Pa). Although the high-temperature compatible gauge is successfully fabricated, some issues, such as the rectifying behavior of Ti/SiC junctions and the non-uniformity of poly-SiC deposition, are still unsolved. The integration with high-temperature readout electronics could be the direction of future work.

Keywords: High temperature, vacuum gauge, SiC, micro-bridge

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ACRONYMS

MEMS micro-electro-mechanical systems 1

IC integrated circuit 1

SiC silicon carbide 2

atm standard atmosphere 3

FEA finite element analysis 5

TCR temperature coefficient of resistance 10

CMOS complementary metal oxide semiconductor 13

Pt platinum 13

Au gold 13

ppt parts-per-trillion 13

CNT carbon nanotube 17

EKL Else Kooi Lab 23

LPCVD low pressure chemical vapour deposition 23

PECVD plasma enhanced chemical vapour deposition 24

TEOS tetraethyl orthosilicate 24

ICP inductive coupled plasma 25

ELM electrical linewidth measurement 27

PVD physical vapour deposition 47

HMDS hexamethyldisilazane 54

MPS micro probe station 59

1 INTRODUCTION

Micro-systems, also known as micro-electro-mechanical systems (MEMS), is a technology to create sensors on a micro-scale ranging from 20 μm to 1 mm with integrated mechanical and/or electrical components. Great effort has been invested in this field since the first concept of MEMS was proposed in the 1960s. Up to now, various commercially successful MEMS devices can be found on the market with diverse applications in automotive, medical and electronics industries. In the broadest sense, the composition of micro-system includes the micro-fabricated transducer and readout electronics [1]. Thanks to the planar technology, the micro-fabricated transducer and integrated readout circuit can be integrated on one single chip, which is the so-called "smart sensor". By taking advantages of the batch production method utilized in the semiconductor industry, the micro-system is able to achieve a smaller size, more power efficiency and lower price [2]. At present most of the smart sensor systems are based on silicon, due to its excellent mechanical and electrical properties. The mature silicon processing technology leveraging from the integrated circuit (IC) processing also gives silicon-based MEMS many advantages from an economic perspective.

Nowadays, many applications need micro-systems that are designed to operate in a harsh environment. The harshness can come from various sources, such as high temperature, shock, moisture and harsh chemicals. Among these, the high-temperature environment is the most common situation in industrial applications. For example, in the semiconductor industry, deposition of various materials can require a high-temperature environment where temperature can easily reach up to one thousand degree Celsius in a vacuum condition. Apart from this, monitoring the performance of systems at an elevated temperature is also an important task in the aerospace and automotive industries. However, the silicon-based micro-system has a maximum working temperature of 125 °C. At this temperature, minority carrier generation rate dramatically increases, so the degradation brought by leakage current in the p-n junction becomes significant [3, 4]. Furthermore, as the temperature goes higher, the intrinsic carrier concentration will keep increasing and gradually reach the doping concentration, leaving a limited capability of conducting current. When the temperature is above 500 °C, the mechanical properties of silicon starts to degrade, and it becomes plastically deformable under mechanical stress. Above 800 °C, Si will react with water and/or oxygen, forming an oxidation layer on the surface. These facts

make the traditional silicon-based devices not suitable for high-temperature applications.

In order to meet the demand for high-temperature monitoring, traditionally, when electronics need to be used in a high-temperature environment, active or passive cooling devices are used to keep the device operating at an acceptable temperature. Alternatively, people also transfer the measurand from the hot zone to a place with a lower temperature and measure it [4]. For example, for some pressure sensors used at a high temperature, the pressure pipe is used to guide the flow to the sensor, which is put in a cooler environment. However, these solutions do not fundamentally solve the problem. In some cases, the sensing system must be placed in a high-temperature environment entirely. For instance, during the space mission to the Mercury, the whole system has to operate at 420 °C, which is the surface temperature of the planet. On the other hand, adding extra cooling parts will make the system more bulky and expensive.

Another strategy of designing high-temperature compatible devices is to build the micro-system out of new material systems. Such material includes silicon on insulator (SOI), gallium nitride (GaN), synthetic diamond and silicon carbide (SiC), which are leading candidates for harsh environment system. A comparison of temperature limitation of different semiconductor technologies is presented in Table 1.1. From the table, these semiconductor technologies allow corresponding transistors to work at a higher temperature than conventional silicon transistors. All of the listed materials have wider band gaps (3.4 eV, 3.26 eV and 5.5 eV for GaN, 4H-SiC and diamond respectively) than Si (1.14 eV), and this is the main reason why they are able to work at an elevated temperature. In the literature, there are already successful electrical components (such as transistors and p-n junction diodes) reported for each listed material[5, 6, 7, 8], which proves the feasibility to realize the high-temperature compatible IC with other materials. Compared to other materials, SiC is more well-developed in terms of making electronics. The possibility of making SiC-based power electronics had been intensively investigated, and mature power electronics devices based on the SiC have already appeared on the market [1, 9]. Considerable effort has also been made to develop the SiC-based IC [10, 11, 12, 13, 14]. For example, Spry et al. reported that their SiC-based IC operated at 500 °C successfully for more than 5000 hours [11].

SiC is not only an ideal candidate for high-temperature compatible ICs but also a promising sensing material. Compared to traditional material Si, SiC has a number of advantageous properties, as shown in Table 1.2. Firstly, SiC has a critical electric field higher than silicon, and a thermal conductivity around three times greater than silicon. In terms of mechanical properties, SiC has Young's modulus 2.4 to 4.3 times larger than silicon depending on the polytype, and it is one of the hardest materials ever known to man. More importantly, SiC retains

Table 1.1: Maximum operation temperature of different semiconductor materials

Material	Tech maturity	Temperature Limit (°C)
Si	Very high	125 [3, 4]
SOI	Medium	300 [5]
GaN	Low	400 [6]
SiC	Medium	650 [7]
Diamond	Very low	700 [8]

its excellent mechanical property even at a high temperature. Unlike Si, it does not experience plastic deformation. Besides, the SiC-based sensor is able to cope with corrosive environments due to its chemical inertness. It has a high etch resistance to most of the commonly used etchants. Unlike making SiC circuitry, many SiC sensors are not necessarily needed to be made from single-crystal carbide and can be fabricated from poly-crystalline SiC, which is much cheaper [9]. Therefore, SiC-based sensor is an economical choice even it is not intended for high-temperature applications. From the literature, SiC has been used as the construction material for some gas sensors and pressure sensor operating at an elevated temperature[9, 15, 16, 17, 18]. However, compared to the widely used SiC power electronics for high-temperature applications, the SiC sensor is still in the research phase.

Table 1.2: The main properties of silicon carbide. Adapted from [9]

Properties	SiC	Si
Band gap energy (eV)	3.26	1.14
Density (kg/m^3)	3210	2330
Young's modulus (GPa)	390-690	160
Fracture strength (GPa)	21	7
Thermal conductivity ($W/(cm \cdot K)$)	3.3-4.9	1.4-1.5

This thesis presents a full process of fabricating a micro-fabricated Pirani vacuum gauge based on poly-SiC, including the preparatory study, modelling of the device, fabrication of the device and finally the characterization of the device. This project aims to develop a vacuum gauge that is able to withstand a high-temperature operation environment.

1.1 MOTIVATION AND OBJECTIVE

Monitoring of the pressure at a very high temperature, both the over-pressure (above 1 standard atmosphere (atm)) and the under-pressure (below 1 atm), is a very important topic for industrial proposes. The MEMS sensor for over-

pressure detection at a high temperature has attracted much attention in recent years [15, 16, 17, 18, 19, 20]. One of the ways of realizing such sensors is to detect pressure by utilizing a fibre tip to sense the deformation caused by pressure change [17, 20]. Another popular method, not surprisingly, is to use the SiC as the construction material. For example, R. Okojie et al. reported a 4H-SiC piezoresistive pressure sensor which can operate up to 800 °C in 2015 [18]. However, it seems that developing a vacuum gauge operating at a high temperature is less attractive for people. There is only one vacuum gauge for the high-temperature purpose reported in 2004 [21]. Nevertheless, numerous situations where the vacuum needs to be detected at a high temperature can be found. Take the space mission to Mercury again as an example again. Mercury has a very tenuous atmosphere, and the atmosphere of the Mercury is essential data for relevant scientific research. The vacuum gauge needs to work above 400 °C to monitor the atmospheric pressure. Also, in the semiconductor industry, many processes need to be done in the vacuum environment at high temperatures, in which the degree of vacuum must be carefully measured and controlled.

The main motivation of this thesis is to explore the possibility of a high-temperature compatible vacuum gauge using the wide bandgap semiconductor, i.e. SiC. The realization of such a sensor can be seen as the first step of monolithic integration for a full-SiC smart sensor, which includes the sensor head and read-out electronics. This full-SiC platform would boost harsh environment compatibility, while reducing packaging complexity. Another motivation is that the implementation of high-temperature vacuum gauge makes it possible to realize a full-scale pressure measurement by integrating with it the current high-temperature overpressure sensor described in the literature.

According to the maximum operating temperature of SiC-based IC reported in the literature [11], the goal of the project is to design a vacuum sensor that is able to work above 500 °C for the further integration with the SiC-based IC. The thesis objective can be separated as follows:

1) Select a vacuum gauge implementation which suits high-temperature operation.

2) Investigate how design parameters will affect the performance of the vacuum gauge.

3) Develop a micro-fabrication approach for SiC-based vacuum gauge, which is compatible with high-temperature electronics.

4) Characterize the high-temperature performance of the device and examine the capability of poly-SiC at an elevated temperature.

1.2 OUTLINE

The thesis presents the implementation of the high-temperature compatible vacuum gauge, and the work is divided into six chapters. Apart from this introductory chapter, the content of the other five chapters is organized as follows:

Chapter 2 discusses the design choices of the vacuum gauge. The working principle of the vacuum gauge will be explained, and a literature review of the state of the art implementations will be shown.

Chapter 3 shows a derivation of the analytical model, which gives an early prediction of the input and output relation of the vacuum gauge. finite element analysis (FEA) simulations with COMSOL are carried out to support the mathematical calculation. In order to give accurate inputs to the model, the electrical properties and mechanical properties of poly-SiC are measured. The structure of the sensor is designed based on the model.

Chapter 4 illustrates the cleanroom realization of vacuum gauge. The flowchart and the mask design are described, and the relevant SiC processes, such as deposition and dry etching, are described in this chapter.

In Chapter 5, the characterization of the vacuum gauge is given. A measurement setup dedicated to the high-temperature characterization is built up. The vacuum gauges are calibrated in both normal and high-temperature conditions. Properties of the metal-SiC junction are also measured.

Finally, Chapter 6 draws a conclusion upon this thesis, and a recommended future work is given.

1.3 CONCLUSION

In this chapter, SiC is introduced as an excellent candidate for harsh environment application, and it has unique advantages not only for making the high-temperature electronics but also for the MEMS sensor realization. Also, the situation where a lack of research in the high-temperature compatible MEMS vacuum gauge is described. In order to meet the demand for vacuum measurement at high temperatures, combining vacuum gauge with SiC is considered as a possible solution in this thesis. The research motivation and objectives are listed in Section 1.1, and a vacuum gauge compatible with the high-temperature electronics is expected to be the outcome of the project.

2 BACKGROUND KNOWLEDGE

This chapter will discuss different implementations of the vacuum gauge. Firstly, the working principle of each type is given in Section 2.1. The pros and cons of different types of gauges will be given, and a certain configuration of vacuum gauge will be chosen for high-temperature realization. A literature review of the state of the art implementations of vacuum gauges will also be demonstrated as a reference to our design.

2.1 VACUUM GAUGE IMPLEMENTATIONS

The use of vacuum plays a significant supporting role in at least 70 general manufacturing applications. For these applications, the degree of vacuum is an essential parameter that needs to be monitored. Therefore, people have developed various types of vacuum gauges to detect the degree of vacuum. The purpose of this section is to find out a suitable type of vacuum gauge implementation which is best suited for the high-temperature condition.

In the literature, most of the vacuum gauges fall into three categories: mechanical gauges, thermal conductivity gauges and ionization vacuum gauges. Of course, there are some specialized vacuum gauges, but they are rarely seen in practical usage. The first group of vacuum sensor is the mechanical gauges, and they consist of moving parts such as cantilevers and membranes, which deform due to pressure change. For micro-fabricated implementation, the most representative mechanical vacuum gauge is based on the membrane, as shown in Figure 2.1a [22]. The silicon membrane forms a capacitor with the bottom electrode and seals a small vacuum cavity. The membrane will experience a deformation due to the pressure from the outside, thus causing a capacitive change. The fabrication of the membrane usually requires a deep etching to form the membrane, and it is not desired for SiC process since SiC is a tough material that is hard to be etched. Also, this type of gauge requires vacuum encapsulation for proper operation. A wafer bonding or a surface-micromachining process is needed to achieve a vacuum cavity, and a non-evaporable getter is required to maintain the vacuum cavity [25]. Moreover, the membrane is likely to suffer from material fatigue due to the cyclic pressure load [26], and high temperature might even accelerate this kind of failure.

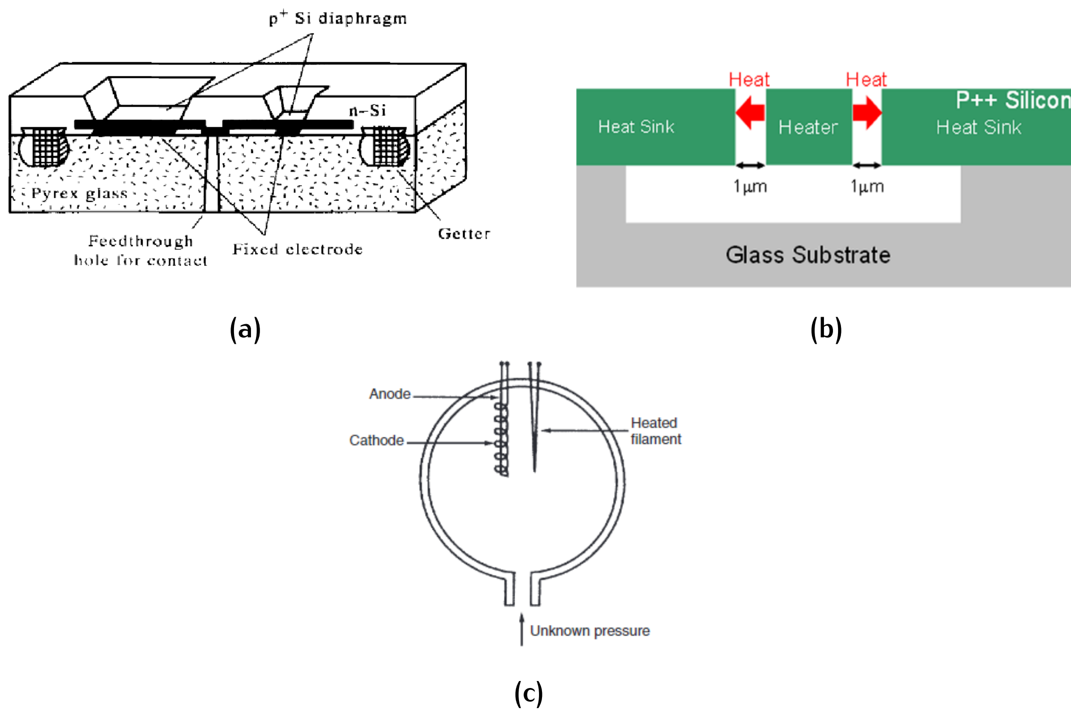


Figure 2.1: (a) Cross-section of membrane-based gauge fabricated by Esashi [22]; (b) A thermal conductivity gauge punished by Junseok [23]; (c) A sketch for the ionization gauge [24]

The second group is the thermal conductivity gauge. The basic structure is shown in Figure 2.1b. The main working principle of these gauges is the gas conductivity changes with respect to pressure. The fabrication of this kind of gauge also needs a surface-micromachining technique, but it does not rely on the differential pressure, so no vacuum cavity is needed. Therefore, the structure is simpler and more robust than mechanical gauges because it does not have any moving part.

When it comes to ionization gauges, they are mostly used for detecting a very high degree of vacuum (below 10^{-1} Pa) [27]. Figure 2.1c shows the basic structure of ionization gauges. The electrons discharge from the filament and collide with gas molecules, resulting in an ionization current between anode and cathode. This magnitude of the current is related to the number of ions in the environment, which is a measure of ambient pressure. Usually, a mass spectrometer is needed for calibration because the gauge is very sensitive to the gas composition [24]. Comparing to the mechanical gauge and the thermal conductivity gauge, the commercially available ionization gauge is still relatively large in dimension. An efficient electron source and a sufficient electron path are difficult to achieve with a reduction in dimension [25].

A comparison of the major attributes of different vacuum gauges is summarized in Table 2.1. Based on this, the thermal conductivity gauge is considered to be the most suitable type of vacuum gauge for high-temperature applications. It has a very simple structure comparing to other gauges, and it does not contain any moving part, which makes it more robust in the harsh environment. Furthermore, miniaturization of such device is confirmed by many works from the literature [28, 29, 30, 31, 23]. Although the calibration of thermal conductivity gauge is dependent on gas type, it does not cause too many problems. For most common gases, such as nitrogen, oxygen and water vapour, the calibrations are very similar.

Table 2.1: Table with major attributes of different vacuum sensor application

Attribute	Mechanical Gauge	Thermal Conductivity Gauge	Ionization Gauge
Dynamic Range	Rough/Medium vacuum	Rough/Medium vacuum	High vacuum
Moving Part	Yes	No	No
Miniaturization Potential	Good	Good	Poor
Complexity	Medium	Low	High
Gas Species Sensitive	No	Yes	Yes

2.2 PIRANI VACUUM GAUGE

The most representative thermal conductivity gauge is the Pirani gauge, and other types of thermal conductivity gauges, such as the thermistor gauge and the thermocouple gauge, are more or less the variations based on the Pirani gauge [32]. The Pirani vacuum gauge has a history of over 100 years, and it was first invented in 1906 by Marcello Pirani. The advantages of this kind of gauge include high robustness, low cost and excellent response to pressure change. Moreover, due to the useful dynamic range it covers, it is widely used for industrial purposes. The traditional Pirani gauges are physically large, making them difficult to integrate with on-chip circuitry. Similar to many traditional transducers, the miniaturization trend is also applied to the Pirani gauge. By combining with silicon planar technologies, there are quite a lot micro-fabricated Pirani gauges have been reported. Besides, more and more emerging technologies are pushing the Pirani gauge to be smaller, more power-efficient, more batch-producible and more compatible with the integrated circuit [2, 29, 31, 33, 34].

2.2.1 Working Principle

As quickly mentioned in Section 2.1, the principle behind these type of vacuum gauge is that the thermal energy dissipated by gaseous conduction (Q_{gas}) is proportional to the number of gas molecules involved in the heat transfer, which in turn is proportional to the pressure. To make use of this effect, a heated element, usually a conductive wire, is heated up in an enclosure of a stable temperature.

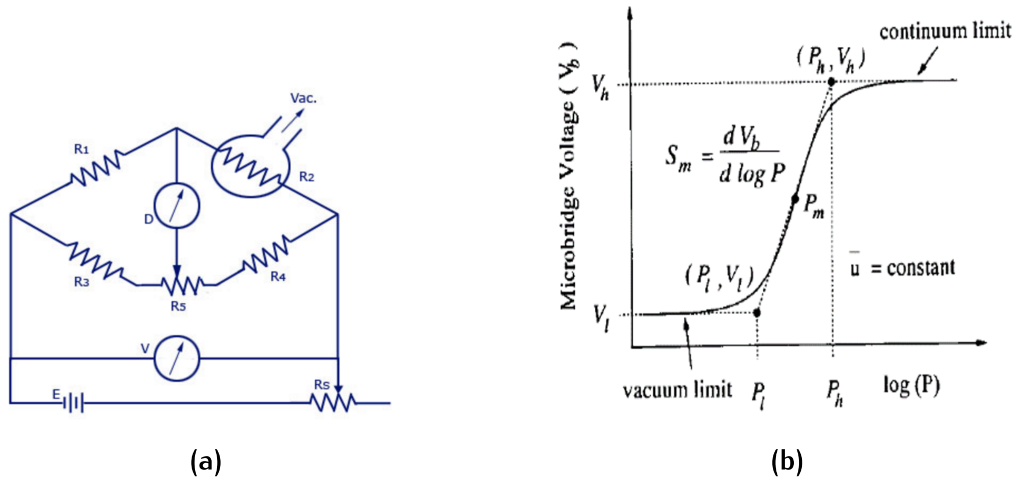


Figure 2.2: (a) A Pirani gauge implemented with Wheatstone bridge; (b) A typical input-output relation of a Pirani gauge[35].

Due to the heat loss rate difference under different pressure, the heated element will build up a corresponding temperature distribution. The overall temperature of the conductive element will affect the total resistance of the heater itself, according to the temperature coefficient of resistance (TCR) of its construction material. Eventually, pressure change can be converted into an electrical signal with a bias current. In this way, the ambient pressure is correlated to the resistance of the heater. In reality, a Pirani gauge is usually combined with a Wheatstone bridge to amplify the output signal, as shown in Figure 2.2a. One resistor is put into the vacuum to sense pressure variation of environment and the rest are put into normal condition, and a precise and amplified electrical signal can be read at voltage meter "D".

In Figure 2.2b [35], a typical relationship between pressure versus electrical output is given. As can be seen, the output is an "S" shaped curve, which shows the device is most sensitive in the middle and loses sensitivity at two ends. To understand this effect, it is important to understand that heat in the system is not only dissipated by Q_{gas}, but also is transferred through the solid connection to the heater (Q_{solid}), means of heat radiation ($Q_{radiation}$) and convection ($Q_{convection}$), as demonstrated in Figure 2.3a [23]. If the Pirani gauge is considered as an ideal isolated system, then the following equation always stands, due to conservation of energy:

$$Q_{total} = Q_{gas} + Q_{solid} + Q_{radiation} + Q_{convection} \tag{2.1}$$

Q_{solid} is the heat loss through the solid part of the sensor, and $Q_{radiation}$ is depending on the temperature of the object. Both of them are not directly related to the pressure, so they are treated as constants over the pressure. In theory, convection also exists, but it can be neglected because the Pirani vacuum gauge is usually placed inside an enclosure of rarefied gas, where almost no external

force exists. Among all the heat loss source, only Q_{gas} is pressure-dependent, the qualitative relation between Q_{gas} and absolute gas pressure is given in the Figure 2.3b [23]. The under-pressure regime can be divided into three parts according to the Knudsen number (K_n):

$$K_n = \frac{\lambda}{d} \tag{2.2}$$

where λ is the mean free path of gas molecules which increases as pressure drops, and d characteristic length of a system being studied. When $K_n > 1$, which corresponds to low pressure, it is in a molecular regime where characteristic length is comparable to mean free path of molecules, which makes the mean free path of the gas molecule is so large that statistically molecules only hit the surface but not collide with each other. In essence, Q_{gas} is a result of collisions between gas molecules and collisions between molecules to other surfaces, therefore the more collisions, the more heat exchange occurs. Impingement rate on the surface is proportional to the number of particles per volume, and the number of particles in a unit volume has a linear relation with the ambient pressure, so the amount of heat transfer is linearly related to the pressure at the molecular regime. As shown in the left part of Figure 2.3b, gaseous conduction Q_{gas} is proportional to pressure, and it is usually the range where the dynamic range of Pirani gauge is located. When the pressure goes lower ($0.01 < K_n < 1$), then Q_{gas} starts to be less dependent on the pressure. When $K_n < 0.01$, it is called the continuum regime in fluid mechanics. In this regime, gas molecules will collide with each other intensively, so Q_{gas} gets saturated and does not change with pressure. Equation 2.2 also implies that the micro-fabricated Pirani gauge will have a larger linear range than macroscopic one, because of its smaller dimension, i.e. d.

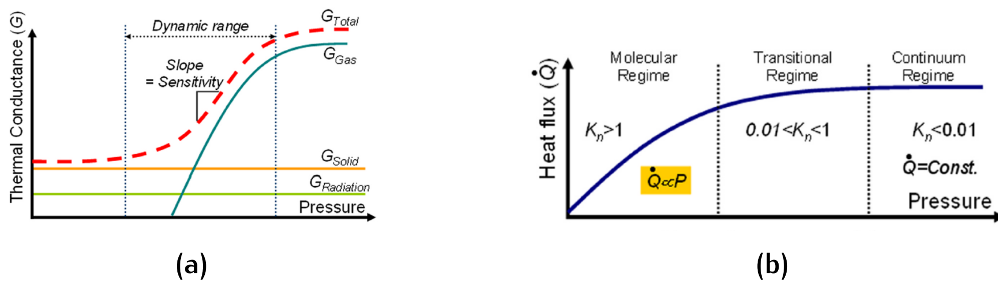


Figure 2.3: (a) Heat dissipation sources in the Pirani gauge [23]; (b) The amount of Q_{gas} with respect to the pressure [23].

2.2.2 Optimization Strategy

Based on the working principle described in Section 2.2.1, several qualitative rules to optimize the performance of Pirani gauge can be concluded. As shown in Figure 2.3a, gaseous conduction Q_{gas} decreases with a pressure drop. Once

Q_{gas} becomes smaller than other heat loss sources, i.e. Q_{solid}, $Q_{radiation}$, then the Pirani gauge will lose the detection ability, because Q_{total} will be the sum of Q_{solid} and $Q_{radiation}$, which is a constant and is not related to pressure. Therefore, the sum of Q_{solid} and $Q_{radiation}$ is a constraint for the lower detection limit of Pirani gauge. On the one hand, Q_{solid} and $Q_{radiation}$ should be suppressed, and the most common way is to design proper structures and to avoid having too much contact area between the heating element and supporting structure [36]. On the other hand, increasing Q_{gas} is another approach to expand the detection limit at low pressure. As what has been discussed in Section 2.2.1, Q_{gas} will be larger if more collisions occur on the surface. The most straightforward method is to make the heating area large to enhance the gas conduction, and this is the reason why the heating part of many Pirani gauge designs are made meandered. Last but not least, in the transduction chain, the pressure is eventually reflected by the resistive change of the heater. Therefore the TCR of heating material should be preferably large to enhance the sensitivity. These are factors which will affect the performance of the gauge, and a model will be shown in Chapter 3 to quantitatively define the impact of each parameter.

2.2.3 Sensor Structures

The micro-fabricated Pirani gauge can be grouped into two types according to differences between structures:

1) Suspended micro-bridge heater;

2) Heater on a dielectric membrane.

The first category, micro-bridge, consists of a suspended wire or coil acting as the heating element, as shown in Figure 2.4a. Two ends of the heater are clamped to the anchors, and a certain distance is left underneath the heater to obtain a high heat transfer rate. Therefore the heater is suspended and supported only at two ends. Q_{solid} is naturally minimized in this structure since solid contact only occurs at two ends, and most of the surface only contact with air. In addition, as for micro-fabricated Pirani gauge, the vertical dimension of the air gap is usually a few micrometers long, which can be treated as the representative physical length scale d (because the direction of heat flux to be investigated is vertical). According to Equation 2.2, this small d allows the vacuum gauge to enter the continuum regime at a higher pressure, which means a larger linear region. However, the drawback of this structure is also obvious. The heater structure is not well mechanically supported, and it makes the whole structure relatively fragile, especially when a longer micro-bridge is desired for lower pressure detection [28].

In the second structure, the sensor is mainly composed by a dielectric membrane and a heater patterned on top, which is usually meandered, as shown in

Figure 2.4b. The dielectric layer is used to improve the mechanical rigidity of the structure. The dielectric layer is usually composed of materials with low thermal conductivity, such as SiO_2 or Si_xN_y, to minimize the solid thermal conduction. The advantage of this configuration is that the heater is sufficiently held by the dielectric membrane, making it mechanically stable. A longer heater with more surface area is possible to be built on the membrane, and this helps to increase the amount of Q_{gas}. Although low thermal conductivity material is used, the solid conduction is still a big concern due to the large contact area between the heater and the membrane. Besides, this kind of structure usually required a bulk micromachining process to form a cavity on the substrate, which is challenging to realize in term of the SiC wafer.

In general, the heater on dielectric structure requires an in-depth etching process of SiC, which is challenging. Furthermore, it does not make use of the excellent mechanical properties of SiC. On the contrary, the Pirani gauge based on the micro-bridge is easy to fabricate, since it does not have any supporting structure. Due to the same reason, the structure is relatively more vulnerable to the thermally-induced buckling and mechanical shock. However, this can be improved by utilizing tougher material, such as SiC, as the construction material. Therefore, the realization of the vacuum gauge is decided to be based on the micro-bridge structure.

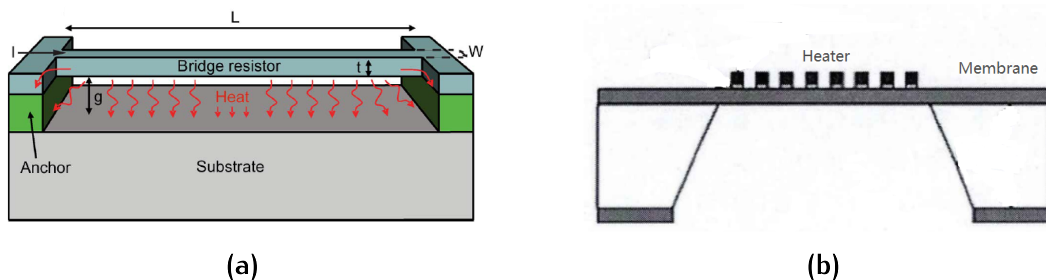


Figure 2.4: (a) Suspended heater structure [33]; (b) The resistor on the dielectric membrane structure.

2.2.4 Traditional Materials

According to current publications, existing MEMS Pirani sensors are mainly based on polycrystalline silicon [28, 29, 23, 33, 34]. However, as discussed in Chapter 1, the Si-based device can not operate properly above 200 °C. In addition, the poly-Si layer has a compressive residual stress, which makes it have a critical length for buckling [28, 33]. In some of the implementations, the platinum (Pt) or gold (Au) are used as the construction material for the Pirani gauge [30, 31, 37]. However, these metals are called red metals, which are notorious for the complementary metal oxide semiconductor (CMOS) process. They have a high diffusion rate, and even few parts-per-trillion (ppt) of Pt, Au or other

red metals will introduce large amounts of defects and eventually kill the transistors in read-out circuit. Even worse, these metal are stable and hard to remove. Therefore they might contaminate cleanroom tools and can cause an issue to other people's process. Additionally, the evaporation of Pt at a high temperature (larger than 700 °C) could be problematic [38].

In contrast, a SiC-based Pirani gauge is advantageous from following aspects. First, SiC is one of the hardest material known to the man. It has a high Young's modulus, so a beam with more stiffness can be made from SiC, making the structure more less vulnerable against the mechanical shock. Besides, SiC layers deposited on the Si substrate has a tensile stress, and the tensile stress provides a tensile pre-stress to the suspended structure. The pre-stress can compensate the thermal stress induced by the Joule heating or high-temperature environment. Also, SiC has a large TCR as reported in the literature [39, 40, 41], and this is desired not only for the implementation of Pirani gauge but also for all the other Joule-heating based sensors. The sensitivity of this type of sensors will increase with increasing power consumption, so a higher TCR of the sensing material can help to reduce applied power while still having the same output signals. Furthermore, SiC is not a material that bring contamination, which makes compatible to existing CMOS technology.

2.3 STATE OF THE ART

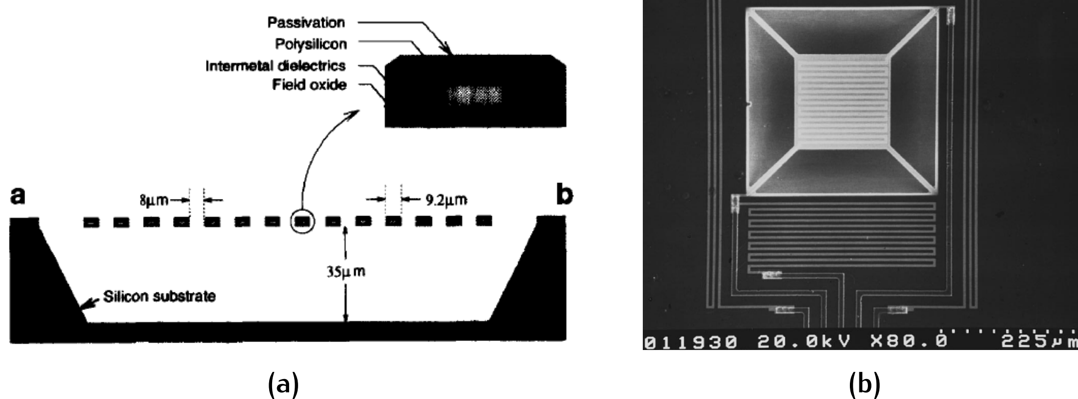
The Pirani gauge has been fabricated in a variety of forms and processes, and main focuses of these works include the choice of gauge material, innovative sensor structures and integration with traditional IC technology. Some representative work is summarized in Table 2.2.

The earliest micro-fabricated Pirani gauge can be found in the literature was in 1991, which was done by Mastrangelo et al. In this work, the Pirani gauge was based on micro-bridge structure, and was integrated with 4 μm NMOS technology on-chip circuit. The sensitivity of the device they presented was from 10 and 10^4 Pa. In addition to this, they also proposed an accurate numerical model for the single bridge Pirani gauge, which is widely used by other researchers. Right after them, Robinson et al. reported their micro-fabricated Pirani gauge fabricated with CMOS-compatible process, and they used a resistor on the dielectric membrane. The length of their heater was still relatively short, and only 340 μm was achieved. In 1994, Swart et al. proposed a suspended coil structure to improve the heat transfer efficiency, where the heat transferred by solid conduction and radiation is less than 1 %. The length of each coil is 1200 μm, and the poly-SiC bridge is sandwiched by dielectric layers, as shown in Figure 2.5a. The structure was surprisingly robust, and the operation range was from 1.33 to 1.33

Table 2.2: Summary of Pirani gauge designs in the past thirty years and their performance

Researcher	Year	Configuration	Material	Pressure Range	Reference
Mastrangelo et al.	1991	Micro-bridge (400 μm long)	Poly-Si	10 - 10^4 Pa	[35]
Robinson et al.	1992	Resistor on membrane (340 μm long)	Poly-Si	1.33 - 1.33 $\times 10^4$ Pa	[42]
Swart et al.	1994	Micro-bridge (1200 μm long)	Poly-Si	1.33 - 1.33 $\times 10^5$ Pa	[43]
O. Paul et al.	1994	Resistor on membrane	Poly-Si	10^2 - 10^6 Pa	[44]
Shie et al.	1995	Resistor on membrane	Pt	1.33 $\times 10^{-4}$ - 1.33 Pa	[36]
Stark et al.	2003	Resistor on membrane	Pt	0.13 - 1.33 $\times 10^3$ Pa	[31]
Baar et al.	2004	Micro-bridge	Pt	3.5 - 10^6 Pa	[45]
Stark et al.	2005	Micro-bridge with dual heat sinks	Cr/Pt or poly-Si	2.67 - 2.67 $\times 10^2$ Pa	[23]
Doms et al.	2005	Micro-bridge (100 μm long)	Pt	100 - 10^6 Pa	[30]
J. Mitchell et al.	2008	Ladder structure bridge (1000 μm long)	Poly-Si	0.13 - 10^3 Pa	[28]
Kaul et al.	2009	Micro-bridge (5 - 10 μm long)	Carbon nanotube	1.33 $\times 10^{-4}$ - 10^6 Pa	[46]
Santagata et al.	2011	Tube-shaped bridge (3000 μm long)	Poly-Si	0.1 - 10^5 Pa	[47]
Fangzhou et al.	2013	Micro-bridge	Carbon nanotube	0.8 - 8 $\times 10^4$ Pa	[48]
Julien et al.	2016	Micro-bridge (1000 μm long)	Ni/Pt	10^3 - 1.5 $\times 10^5$ Pa	[49]
Viard et al.	2017	Micro-bridge (1000 μm long)	Pt	10^4 - 8 $\times 10^5$ Pa	[50]

$\times\ 10^5$ Pa. Shie et al. reported a Pirani gauge with an operation range from 1.33 $\times\ 10^{-4}$ to 1.33 Pa, which is one of the lowest detection limits of micro-fabricated Pirani gauge that can be seen from literature. The resistor is patterned on the membrane, and the floating membrane is supported by four thermally insulating beams, as shown in Figure 2.5b. The advantage of this structure is that the heat loss to the substrate is limited.



(a) (b)

Figure 2.5: (a) An cross-section view of the suspended poly-SiC fabricated by Swart et al. [43]; (b) SEM picture of the Pirani gauge fabricated by Shie et al.[36].

In 2003, Stark et al. from the University of Michigan designed and fabricated a doubly anchored surface micro-machined Pirani gauge. In this structure, the heating element was made in Pt, and a sandwiched layer of $SiO_2/Si_3N_4/SiO_2$

was used as a supporting structure, and the gap distance was 800 μm. This Pirani sensor can measure a pressure that ranges from 0.133 Pa to 1.33×10^3. In 2005, the same research group reported both lateral and vertical micro-fabricated Pirani sensors with dual heat sinks, as shown in Figure 2.6. The highlight of this work is to introduce a concept of using two heat sinks to obtain a broader measurement range and sensitivity compared to the traditional structure with one heat sink. Also, they successfully achieved a small gap size (less than 1 μm) between its heater and two thermal heat sinks, which further improved the performance. However, it was reported that the fabrication is quite challenging because it is difficult to have heater precisely placed in the center of two heat sinks.

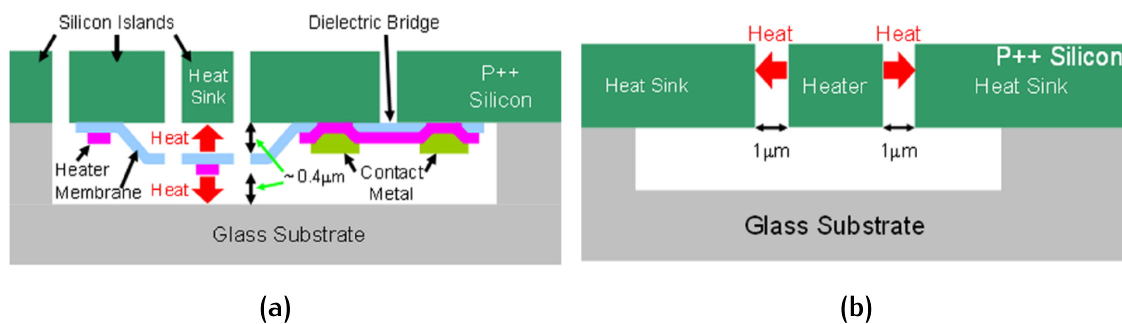


Figure 2.6: A demonstration of dual heat sinks Pirani gauge configuration proposed by Stark et al. [23] (a) Vertical configuration (b) Lateral configuration.

In recent ten years, there are still many Pirani gauges reported in the literature [28, 46, 47, 48, 49, 50]. Compared to older implementations, they are designed with more sophisticated approaches and more innovative structures. In 2008, Mitchell et al. proposed a micro-bridge based on ladder structure (as shown in Figure 2.7a) in order to prevent horizontal buckling so that longer beams can be fabricated. Also, by applying the ladder structure, the heat will spread across to the structural links. Thus more heat can be eventually conducted through the gas. In 2011, Santagata et al. reported a tube-shaped Pirani gauge, which is buried inside the Si wafer, as shown in Figure 2.7b. This structure provides a significantly larger structural stiffness (a factor of 10^4) comparing to the traditional Pirani gauge with a similar size, and they achieved 3000 μm long device. Another advantage of this design is that the hollow tube structure Pirani gauge gives a large surface area to volume ratio, which increases the gaseous conduction.

In 2013, Viard et al. designed a micro-bridge structure supported by suspended segments, as shown in Figure 2.8a. Although this design was not meant for pressure monitoring initially, it is still worth mentioning because it enlightened researchers to apply this structure to Pirani gauges. Based on this, Julien et al. and Viard et al. reported similar implementations of Pirani gauges in 2016 and 2017 respectively, as shown in Figure 2.8a and Figure 2.8b. In this kind of

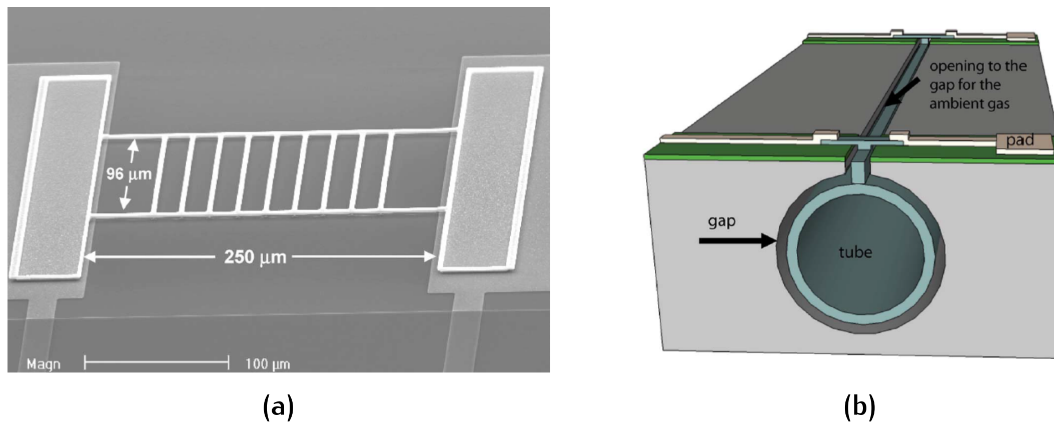


Figure 2.7: (a) Piarni gauge design based on the ladder structure [28]; (b) SEM picture of the Pirani gauge fabricated by Shie et al.[47].

structures, the Si is usually used as the sacrificial layer to form the gap, and the heater lies on the periodical SiO_2 micro-bridges. The periodical micro-bridges play a similar role comparing to the membrane in resistor on membrane structures, and they can largely enhance the stiffness of the structure and prevent the Pirani gauge from collapsing to the substrate, but with less heat draining from the dielectric material to Si substrate. With the help of SiO_2 mechanical supports, Viard et al. reported a Pirani gauge with only 169 nm gap size, achieving a dynamic range from 10^4 to 8×10^5 Pa.

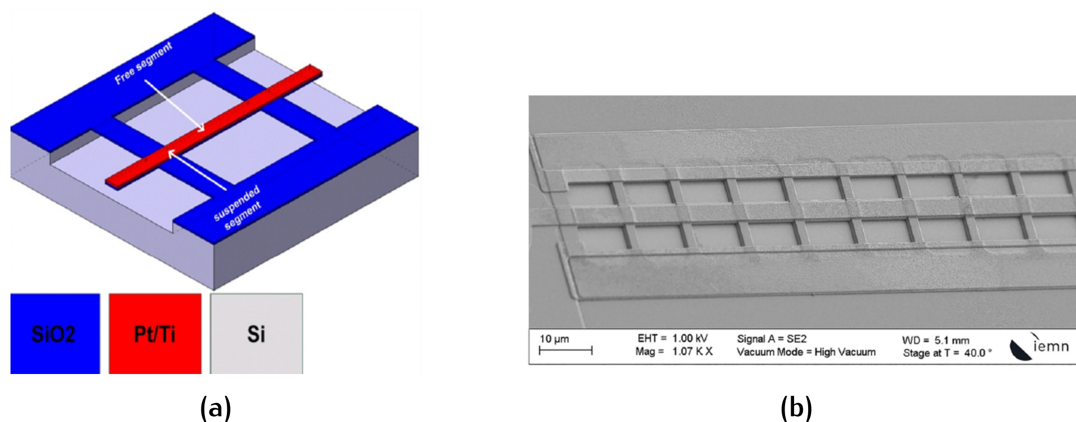


Figure 2.8: (a) A method proposed by Viard et al. to achieve long suspended beam with high robustness [51]; (b) The Pirani guage filament is well supported by SiO_2 micro-bridges [50].

Innovative materials, such as carbon nanotube (CNT), are also applied to the fabrication of micro-fabricated Pirani gauge [46, 48]. The advantage of using single-wall carbon nanotube is that the cylinder shape of carbon nanotubes makes the contact area between electrodes and CNTs very tiny. In addition, the TCR of CNTs is very large so that the CNT-based heating element will bring more resistance change with the same amount of temperature change. For example, Kaul

et al. reported a CNTs-based Pirani gauge which has a dynamic range from 1.33 $\times$ 10^{-4} to 10^6 Pa. The process of fabricating carbon nanotube Pirani gauge is illustrated in Figure 2.9a. First of all, the electrodes were sputtered and patterned on the Si substrate. Then after the solution which contains carbon nanotube was dripped on the substrate, an AC voltage source was applied to the electrodes to form the carbon nanotube bridge. This step is called the dielectrophoretic assembly technique. Finally, the sacrificial layer beneath the bridge was removed by means of buffered HF. The device is shown in Figure 2.9b. However, this process does not guarantee the formation of the bridge structure. As shown in Figure 2.9b, the CNTs are scattered on the substrate, and only a few of them successfully formed bridges.

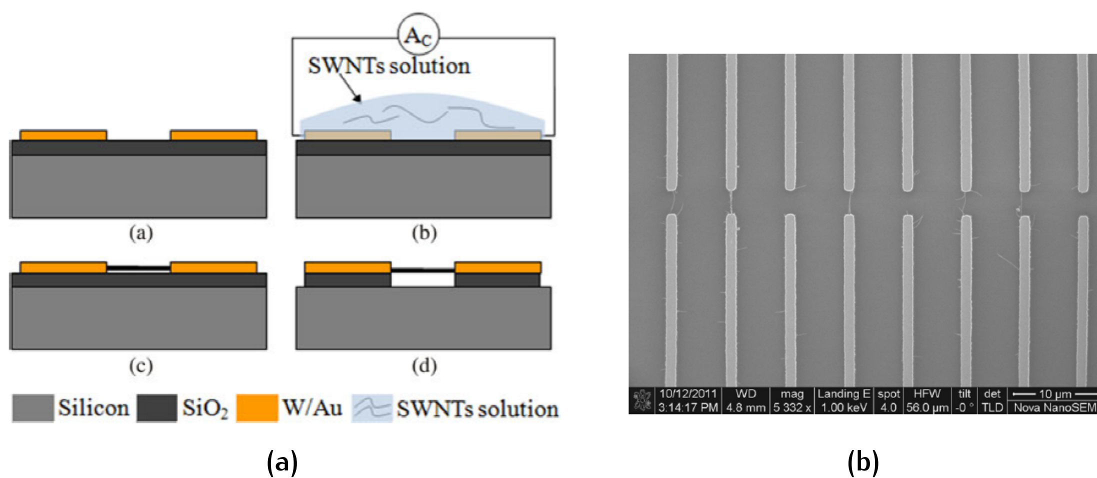


Figure 2.9: (a) Fabrication process of CNTs-based Pirani gauge; (b) The actual device of CNTs-based Pirani sensor reported by Fangzhou et al. [48]

2.4 CONCLUSION

In this chapter, the structure of the vacuum gauge is decided to be based on thermal conductivity gauge, i.e. the Pirani gauge, because of its excellent mechanical robustness and good compatibility to CMOS technology. By combining with the poly-SiC, this vacuum gauge has the potential to work in an elevated temperature environment and integrated to high-temperature compatible electronics. The basic working principle was explained, and a more detailed description of the working mechanism will be more elaborately in Chapter 3. Finally, a literature review of current Pirani gauges was shown in Section 2.3.

3 MODELLING AND DESIGN

In Chapter 2, the empirical design rules are discussed. However, an accurate model is needed to predict the actual performance of the Pirani gauge, and it can be used as a firm reference for the design of the Pirani gauge. In this chapter, some fundamental knowledge of heat transfer theory will be introduced at first. Based on that, an analytical model will be derived in Section 3.2. With the help of the model, the design parameters can be numerically investigated. Simulations with finite element analysis (FEA) software, i.e. COMSOL Multiphysics, will be carried out to verify the correctness of the theoretical model and to study the buckling of the Pirani gauge.

3.1 BASIC HEAT TRANSFER THEORY

The Pirani gauge is the thermal conductivity gauge that relies on the heat transfer between the heater and ambient environment, so it is necessary to introduce the basic heat transfer theory briefly. Heat transfer can be divided into three modes. They are thermal conduction, thermal convection and thermal radiation. Thermal conduction is induced by the collisions of particles within a body, and it takes place in all phases including solids, gases and liquids. Thermal conduction can be expressed with Fourier's law, as shown in Equation 3.2.

$$Q_{conduction} = -\lambda A \frac{dT}{dx} \tag{3.1}$$

where $Q_{conduction}$ is the amount of heat transferred per unit time. λ is the thermal conductivity of the material. A is the surface area, and dT/dx is the temperature change per unit length. From Fourier's law, it can be seen that the rate of thermal conduction through the material is proportional to the temperature gradient and the surface area.

Different from the conduction, the bulk movement of the gases or liquids is the cause of the convection. Therefore, convection does not take place in solids because molecules and atoms are fixed in certain positions. The heat transfer induced by convection can be described as follows.

$$Q_{convection} = hA(T_{fluid} - T) \tag{3.2}$$

where h is the heat transfer coefficient. A is the surface area for convection. T_{fluid} is the temperature of surrounding gases or liquids, and T is the object's temper-

ature. h is not only dependent on the properties of the fluid but also dependent on other factors, such as flow rate, the geometry of the solids and so on. It is difficult to get an accurate h by theory, so h is mainly obtained by experiments.

The third fundamental mechanism of heat transfer is thermal radiation. Any object with temperature larger than 0 K keeps emitting thermal radiation, and at the same time, they absorb thermal radiation from other objects. For a single object put in a cavity with a surface temperature of T_c, the net heat acquired can be expressed by Equation 3.3.

$$Q_{radiation} = \varepsilon_1 \sigma A (T^4 - T_c^4) \tag{3.3}$$

where ε_1 is the emissivity of the object, and σ is the Stefan-Boltzmann constant. A and T are again surface area and surface temperature of the object, respectively.

As discussed in Section 2.2.1, the most dominating heat transfer mechanism is the thermal conduction between the heater and substrate. Therefore in the next section, the effects of thermal convection and thermal radiation are not taken into account.

3.2 ANALYTICAL MODEL

The transfer function of the Pirani gauge based on a single micro-bridge was derived by Mastrangelo et al. [35], and the model is widely used for designing of Pirani gauges. The derivation of the model is shown as follows. Let us first consider a Pirani gauge with a length of l, a width of w, a thickness of z and a gap size of s, and the heater is biased with a current I_b. The resistivity of the material is ρ_0 at room temperature, and the TCR is α. The sensing ability of the Pirani gauge relies on the resistance change induced by the pressure-dependent temperature change of the heater. The resistance of the heater R_{heater} can be expressed as:

$$R_{heater} = \int_0^l \frac{\rho(x)}{wz} dx = \rho_0 \frac{l}{wz}(1 + \alpha \bar{t}) = R_0(1 + \alpha \bar{t}); \tag{3.4}$$

$$\rho(x) = \rho_0[1 + \alpha(T(x) - T_s)] \tag{3.5}$$

$$t(x) = T(x) - T_s; \quad \bar{t} = \frac{1}{l}\int_0^l u(x) dx \tag{3.6}$$

where $T(x)$ is the temperature distribution of the heater along the x-axis, $\rho(x)$ is the resistivity of the poly-SiC on the corresponding x position, R_0 is the initial

resistance. $t(x)$ and $\bar{t}$ are the temperature rise of each point and the average over-temperature respectively. From Equation 3.4, we can see the key is to find out the temperature distribution across the suspended heater so that we can obtain the resistance of the heater. In order to do this, we need to solve a differential equation based on Fourier's law and energy conservation law. Before doing this, several assumptions are made to simplify the model:

1) Two ends of the beam are anchored to the substrate with a homogeneous boundary conditions $T(0) = T(l) = T_s$ ($T(0)$ and $T(l)$ are temperatures at two ends of the heater, T_s is the temperature of the substrate), which means there is no temperature rise at the ends of the bridge resistors [33, 28, 35];

2) The Pirani gauge does not have a temperature difference in width (in Y-axis direction) and in height (in Z-axis direction).

3) The physical properties, such as thermal conductivity, resistivity and specific heat capacity, are uniform. The area of cross-section is also considered to be the same.

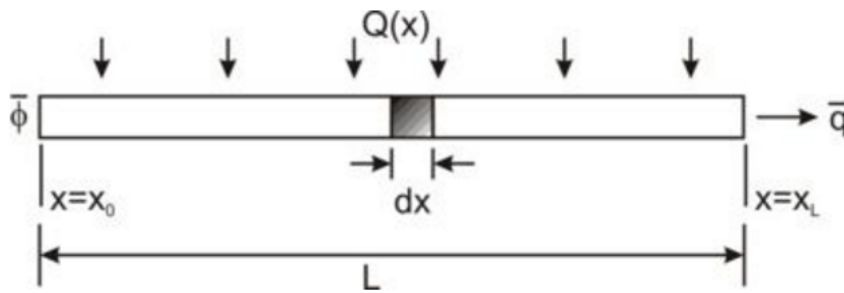


Figure 3.1: One-dimensional model of the Pirani gauge

In this way, the model is reduced to a one-dimensional heat transfer problem, as shown in Figure 3.1. From the heat transfer theory, the three-dimensional temperature field in thermal equilibrium can be described with the Poisson equation:

$$\lambda_b\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + Q_{unit} = 0 \qquad (3.7)$$

where λ_b is the thermal conductivity of the heater material, and Q_{unit} is the net heat transfer per unit volume. According to the assumption. there is no temperature change along y-axis and z-axis. Therefore the terms $\partial^2 T/\partial y^2$ and $\partial^2 T/\partial z^2$ equals to zero, and Equation 3.7 can be rewritten as:

$$\lambda_b \frac{\partial^2 T}{\partial x^2} + Q_{unit} = 0 \qquad (3.8)$$

The term Q_{unit} needs to be determined. This term only includes the ohmic power generation per unit volume Q_{ohmic} and the power dissipated through the air gap

Q_{gas} because convection and radiation are ignored. For ohmic power generation part, Q_{ohmic} on dx can be expressed as:

$$Q_{ohmic} = \frac{I_b^2 R_0}{wlz} + \frac{\rho_0 I_b^2 \alpha t(x) \frac{dx}{wz}}{wzdx} \tag{3.9}$$

Conduction through the gas Q_{gas} can be expressed according to Equation 3.2:

$$Q_{gap} = -\eta \lambda_g w \frac{t(x)}{s} \cdot dx \tag{3.10}$$

where η is a correction factor which accounts for the fringing of heat flux, and for the ideal case $\eta = 1$ [33, 35]. λ_g is the pressure-dependent thermal conductivity of the surrounding gases and the approximation of λ_g is given in Equation 3.11.

$$\lambda_g(P) = \lambda_c[\frac{P/P_0}{1+(P/P_0)}] \tag{3.11}$$

In the equation, λ_c is the thermal conductivity of air in the normal condition, which equals to 0.0262 $W \cdot m^{-1} K^{-1}$. P_0 represents transition pressure, the thermal conductivity of air can be treated as linearly increasing until reaching P_0. After that, it goes into the transitional regime [23]. P_0 can be obtained from an empirical equation:

$$P_0 \approx \frac{\eta \lambda_c w T_s}{(w+z)sv}; \quad v = \sqrt{\frac{8kT_g}{\pi m}}; \quad T_g \approx T_s \tag{3.12}$$

where v is the average velocity of gas molecules and m is the average mass of dry air, and k is Boltzmann constant in $J \cdot K^{-1}$. From the equation above, it can be seen that formula involves the gas properties such as mass of the molecules. Therefore the gauge needs to be calibrated before measuring different types of gases.

After finding out the composition of Q_{unit}, Equation 3.8 can be further expanded as follows:

$$\lambda_b \frac{\partial^2 T}{\partial x^2} + \frac{I_b^2 R_0}{wlz} + \frac{\alpha \rho_0 I_b^2 t(x) \cdot \frac{dx}{wz}}{wz \cdot dx} - \frac{\eta \lambda_b w \frac{t(x)}{s} \cdot dx}{wz \cdot dx} = 0 \tag{3.13}$$

$$\lambda_b \frac{\partial^2 T}{\partial x^2} + \frac{I_b^2 R_0}{wlz} + \frac{I_b^2 R_0 t(x)}{wlz} - \frac{\eta \lambda_b t(x)}{wz} = 0 \tag{3.14}$$

The equation is rewritten to simpler form as shown in

$$\frac{\partial^2 t}{\partial x^2} + \delta - \epsilon t = 0 \tag{3.15}$$

In which,

$$\delta = \frac{I_b^2 R_0}{\lambda_b wlz}; \quad \epsilon = \frac{\eta \lambda_g}{\lambda_g sz} - \frac{I_b^2 R_0}{\lambda_b wlz} \tag{3.16}$$

By solving the heat balance differential equation, the solution to over-temperature distribution is:

$$t(x) = \frac{\delta}{\epsilon}[1 - \frac{cosh\sqrt{\epsilon}(x - \frac{l}{2})}{cosh\sqrt{\epsilon}\frac{l}{2}}] \tag{3.17}$$

By integrating along the x-direction, the average over-temperature $\bar{t}$ can be obtained:

$$\bar{t} = \frac{1}{l}\int_0^l u(x)dx = \frac{\delta}{\epsilon}[1 - \frac{tanh(\sqrt{\epsilon}\frac{l}{2})}{\sqrt{\epsilon}\frac{l}{2}}] \tag{3.18}$$

The expression of the R_{heater} is written in the Equation 3.19

$$R_b = R_{ref}[1 + \frac{\delta\alpha}{\epsilon}(1 - \frac{tanh(\sqrt{\epsilon}\frac{l}{2})}{(\sqrt{\epsilon}\frac{l}{2})}] \tag{3.19}$$

With Ohm's law, the output voltage of the gauge with respect to pressure can also be determined, as shown in Equation 3.20

$$V_b = I_b \cdot R_{ref}[1 + \frac{\delta\alpha}{\epsilon}(1 - \frac{tanh(\sqrt{\epsilon}\frac{l}{2})}{(\sqrt{\epsilon}\frac{l}{2})}] \tag{3.20}$$

Equation 3.19 and Equation 3.20 give an analytical prediction for how output resistance and output voltage of the Pirani gauge vary with the ambient pressure. Based on the model, we can study the effect of the geometry and predict the performance of our Pirani gauge designs.

3.3 SIC LAYER CHARACTERIZATION

From the model, it is obvious that if we want to obtain the complete numerical expression of micro-bridge resistance as a function of pressure, then electrical properties of the poly-SiC, i.e. resistivity and TCR, needs to be determined. A low pressure chemical vapour deposition (LPCVD) Poly-SiC deposition recipe was developed in the Else Kooi Lab (EKL) by Bruno Morana before, and an elaborate characterization of the poly-SiC layer was described in his doctoral thesis [52]. However, some changes have been made in the cleanroom, i.e. the poly-SiC deposition tool was changed from furnace E4 to furnace F3. This can affect the deposition conditions, and it is possible to obtain poly-SiC layer which has different properties compared to Morana's work, even with the same recipe. Therefore, to avoid the uncertainty brought by equipment change, properties of poly-SiC deposited in F3 furnace were measured again, such as electrical properties and residual stress.

3.3.1 LPCVD Poly-SiC Deposition

Three poly-SiC layers deposition recipes with different doping concentrations were investigated, and they respectively used the same recipes corresponding to D1, D2 and D4 poly-SiC layers described in Morana's work [52]. By using the same deposition recipes, it is easy to compare SiC layers obtained in F3 with previous SiC layers. The process parameters of poly-SiC deposition from Morana's work are listed in Table 3.1 [52]. The precursor gases of the SiC deposition are dichlorosilane (SiH_2Cl_2) and acetylene (C_2H_2) which is diluted in hydrogen (H_2). The gas flow ratio (GFR) of SiH_2Cl_2 and C_2H_2 will strongly affect the composition of deposition product, i.e. the ratio of silicon atoms and carbon atoms. The flow rates of SiH_2Cl_2 gas and 5% C_2H_2 gas are set to 320 standard cubic centimeter per minute (sccm) and 80 sccm, so the actual GFR of SiH_2Cl_2 and C_2H_2 is 5. Under this flow rate, the deposition yields a very close concentration of Si atom and C atom, and this gives a poly-SiC layer very similar to stoichiometry. The temperature during the deposition process is also critical. For a higher deposition temperature, it is more likely to obtain amorphous SiC instead of poly-SiC. The deposition is conducted at a fixed temperature of 860 °C and an ambient pressure of 80 Pa. Ammonia (NH_3) is used as the dopant gas in order to obtain a conductive SiC layer. Ammonia will bring nitrogen doping atoms which are able to replace original carbon atoms and form four covalent bonds with Si atoms. In the meantime, each nitrogen atom will provide one free electron, so n-type doping can be obtained [53]. The doping concentration of poly-SiC was tuned by the flow rate of NH_3 gas. The deposition time was set to 2 hours, which will result in a poly-SiC layer close to 1 μm thick based on earlier experience.

Table 3.1: Process condition of LPCVD poly-SiC

Layer ID	SiH_2Cl_2 (sccm)	C_2H_2 (5% in H_2) (sccm)	NH_3 (5% in H_2) (sccm)	Total gas flow (sccm)
D_1	80	320	15	415
D_2	80	320	30	430
D_4	80	320	60	460

In order to find out the resistivity, it is necessary to measure both thickness and sheet resistance of the layer. To measure the sheet resistance, three test wafers were deposited with a certain thickness of plasma enhanced chemical vapour deposition (PECVD) tetraethyl orthosilicate (TEOS) oxide, which can be used as the electrical isolation layers in sheet resistance measurement and landing layer for later etching. After the PECVD deposition, 2-hour poly-SiC deposition with varying amount of NH_3 doping was applied to test wafers separately. The sheet resistance of D1, D2 and D4 layer were measured with CDE Resmap tool. The average sheet resistance of D1, D2 and D4 are 508.1, 106.3 and 26.8 $\Omega/\square$, and the detailed sheet resistance measurement results are shown in Table 3.2. It is worth mentioning that the sheet resistance has a deviation up to 12.7 % across

the whole wafer. According to our deposition experience, the sheet resistance will be smaller when it is close to the primary flats of wafers. This variation of sheet resistance might come from the non-uniformity of the SiC deposition rate of F3 furnace, which causes a gradient in thickness across the wafer.

Table 3.2: Raw data of Sheet resistance test SiC layers D1, D2 and D4 (unit: Ω/□)

Measurement Point	D1	D2	D4
No.1	413.0	94.0	25.3
No.2	419.1	95.2	25.7
No.3	482.9	103.0	25.7
No.4	451.3	98.6	26.6
No.5	545.4	111.5	27.4
No.6	543.7	111.5	27.5
No.7	565.6	112.5	27.6
No.8	509.2	106.7	27.0
No.9	546.9	110.8	27.1
No.10	604.1	118.0	28.0
Standard Deviation	64.64	8.15	0.94
Average R_{sheet}	508.1	106.3	26.8

In order to determine the resistivity of each poly-SiC layer, the thickness of the corresponding layer is also required for the calculation. One of the methods is utilizing optical reflectometry system, i.e. Leitz MPV-SP in cleanroom 100, the advantage of this method is that the measurement is fast and convenient. However, due to the varying optical constants of different poly-SiC layers, it is difficult to develop a measurement recipe which can obtain accurate results from the poly-SiC layer with different doping concentrations. Due to the absence of optical reflectometry recipe for poly-SiC, the measurement was carried out with Veeco DekTak 8 profilometer. In this tool, a stylus presses against the sample with a constant force and scans sample surface along a certain direction. This method provides a direct measurement of height change on the sample with respect to the location. The advantage of this approach is that it directly detects the vertical distance, so the result is accurate and gives a resolution of a few nanometers. However, compared to optical reflectometry, contact profilometry needs an additional deposition step and a lithography step to obtain accurate measurement results. In order to carry out thickness measurement with the profilometer, same test wafers were used. The SiC layers were patterned with a lithography step and dry-etched with inductive coupled plasma (ICP) tool. The remaining oxide layer beneath SiC was completely removed by wet etching. Profilometer measures the total thickness of the SiC layer and the oxide layer. The oxide thickness was measured before SiC deposition, and by subtracting oxide thickness from the total thickness, SiC thickness was obtained as shown in Table 3.3. There were five points had been measured. From the result, a non-uniformity

of thickness is indeed observed on each wafer, which explains the variation on sheet resistance. Since the deposition time is known, the deposition rate of SiC was obtained as well. Although the layer thickness is not uniform, it still can be a reference for later deposition. The deposition rate is 8.60 nm/min, 8.54 nm/min and 8.43 nm/min for D1, D2 and D4 layer respectively, and a slight decrease of deposition rate can be observed with increasing doping gas flow.

Table 3.3: Thickness of D1, D2 and D4 SiC layers with 2-hour deposition and corresponding deposition rate

Measurement Point	D1	D2	D4
No.1	991.80	972.43	987.37
No.2	1046.16	1021.51	1015.55
No.3	1009.23	1021.16	994.03
No.4	1024.44	1034.68	1017.34
No.5	1083.48	1076.26	1042.98
Average Thickness	1031.02	1025.21	1011.46
Deposition Rate (nm/min)	8.60	8.54	8.43

3.3.2 Resistivity and Stress of Poly-SiC Film

With the measurement data in Section 3.3.1, the resistivity of LPCVD poly-SiC film can be simply calculated with Equation 3.21:

$$\rho = x \times R_{sheet} \tag{3.21}$$

where x is the thickness of the film. The resistivity of poly-SiC layers is given in Table 3.4.

The stress in the SiC thin film is the summation of thermal stress and intrinsic stress. Intrinsic stress develops during the formation of the thin film, due to sources such as coalescence of grain boundaries, grain growth. Thermal stress is induced by the mismatch of thermal expansion coefficient between SiC (4×10^{-6} /K) and Si substrate (2.6×10^{-6} /K). After cooling down from the high-temperature LPCVD process, Si substrate and SiC thin film will shrink differently. The total residual stress σ can be calculated with Equation 3.22:

$$\sigma = \frac{E_s h_s}{6h\left(1 - v_s\right)} \left(\frac{1}{r} - \frac{1}{r_0}\right) \tag{3.22}$$

where E_s is Young's modulus of the Si substrate. h_s is Si wafer thickness. v_s is the Poisson's ratio of Si. r and r_0 is the wafer curvature before and after SiC film deposition. Since layer thickness was measured before, the residual stress σ in the film can be calculated with above equation. Thanks to the advanced

measurement tool in EKL cleanroom, the wafer curvature result can be obtained directly from Flexus 2320S optical measurement system, and embedded software will help to calculate the residual stress.

Table 3.4: Resistivity and residual stress measurement results of D1, D2 and D4 poly-SiC films

Layer ID	$\rho \times 10^{-3}(\Omega \cdot cm)$	$Stress(MPa)$
D1	52.39	403.9
D2	10.90	486.7
D4	2.68	557.5

Three bare silicon wafers were covered with 1000 nm thick D1, D2 and D4 poly-SiC layers respectively, after measuring their initial wafer curvature R.The LPCVD SiC on the backside of the wafers was removed by dry etching, and the film stress was measured after the etching process. The stress measurement result is also shown in Table 3.4. The residual stress in the LPCVD SiC film is tensile, and it is notable that more doping brings more tensile stress to the film.

3.3.3 TCR Measurement

The TCR of the poly-SiC α is the most important material property for the Pirani gauge because α determines the amount of resistance change according to temperature change. Equation 3.23 shows how temperature and resistance are related to TCR. With this equation, we are able to calculate α by experiments.

$$R = R_{ref}[1 + \alpha(T - T_{ref})] \tag{3.23}$$

Three test wafers used in Section 3.3.1 were patterned with electrical linewidth measurement (ELM) test structures to measure the $R - T$ relation. The experiment was done in the measurement room with Cascade probe station 33 on a gold chuck with a temperature controller. The measurement started from a reference temperature R_{ref} of 25 °C with a temperature step of 20 °C till reaching the maximum 200 °C. At each temperature set point, the measurement was held for 10 minutes so that the whole wafer could stabilize at the desired temperature.

The $R - T$ data of D1, D2 and D4 are plotted with black dots in Figure 3.2. The resistance of the heater decreases with the increase of the ambient temperature, indicating poly-SiC has a negative TCR. As known from Equation 3.23, the resistance of heater should have a linear relationship with temperature. Therefore the data was fitted in the linear equation to obtain the α. The fitted curves are shown in Figure 3.2 with red curves. The TCR results are listed in Table 3.5, and the detailed fitting expressions are given in the figures. It needs to be mentioned that the TCR obtained from the linear fitting is the average TCR across

the temperature range (25 to 200 °C). In fact, the absolute value of poly-SiC TCR decreases at a higher temperature. Take D1 layer as an example, the TCR of D1 layer at 25 °C is around -2217 ppm/°C, and it decreased to -1383 ppm/°C at 200 °C. Predictably, there will be a decrease of sensitivity when the Pirani gauge operates at a higher temperature. The TCR value obtained of D1 layer is close to what had been reported by Roya et.al. They observed a TCR of -1700 ppm/°C at room temperature and decrease to -1000 ppm/°C at 350 °C [40]. However, almost twice as big or even more TCR values can also be seen in other literature. For example, Noh et al. and Wu et al. reported TCR up to -5374.5 ppm/°C and -6900 ppm/°C respectively [41, 54]. A decrease of TCR with respect to NH_3 doping concentration can be observed, which is consistent with the work from Morana [52].

Table 3.5: TCR reults for D1, D2 and D4 layers extracted from linear fittings

Layer ID	$TCR(ppm/°C)$
D1	-1770.0
D2	-1080.0
D4	-586.4

The poly-SiC layer is supposed to work in a harsh environment of more than 200 °C, but the maximum allowable temperature of the hotplate is 200 °C due to equipment capability. Nevertheless, we obtained acceptable TCR values compared to literature, which can be used for the preliminary simulation for the first place. As for other parameters, such as resistivity and residual stress, we observed some differences compared to the previous LPCVD poly-SiC deposition. Nevertheless, these properties are still in the same order of magnitude compared with previous results.

3.4 DESIGN OF PIRANI GAUGE

From the model derived from Section 3.2, the micro-bridge resistance R_b is as a function of its geometrical parameters including length (l), width (w), thickness (z)and gap distance (s), as well as bias current. Therefore, apart from measurement results in Section 3.3, these geometrical parameters also need to be determined. However, due to the complexity of the final expressions Equation 3.19 and Equation 3.20, it is not clear to see how design parameters will affect the performance. To make things simpler, a nominal gauge is designed as a starting point. By varying a single design parameter for each time, we can compare the result with the nominal device and investigate the effect brought by a single variable.

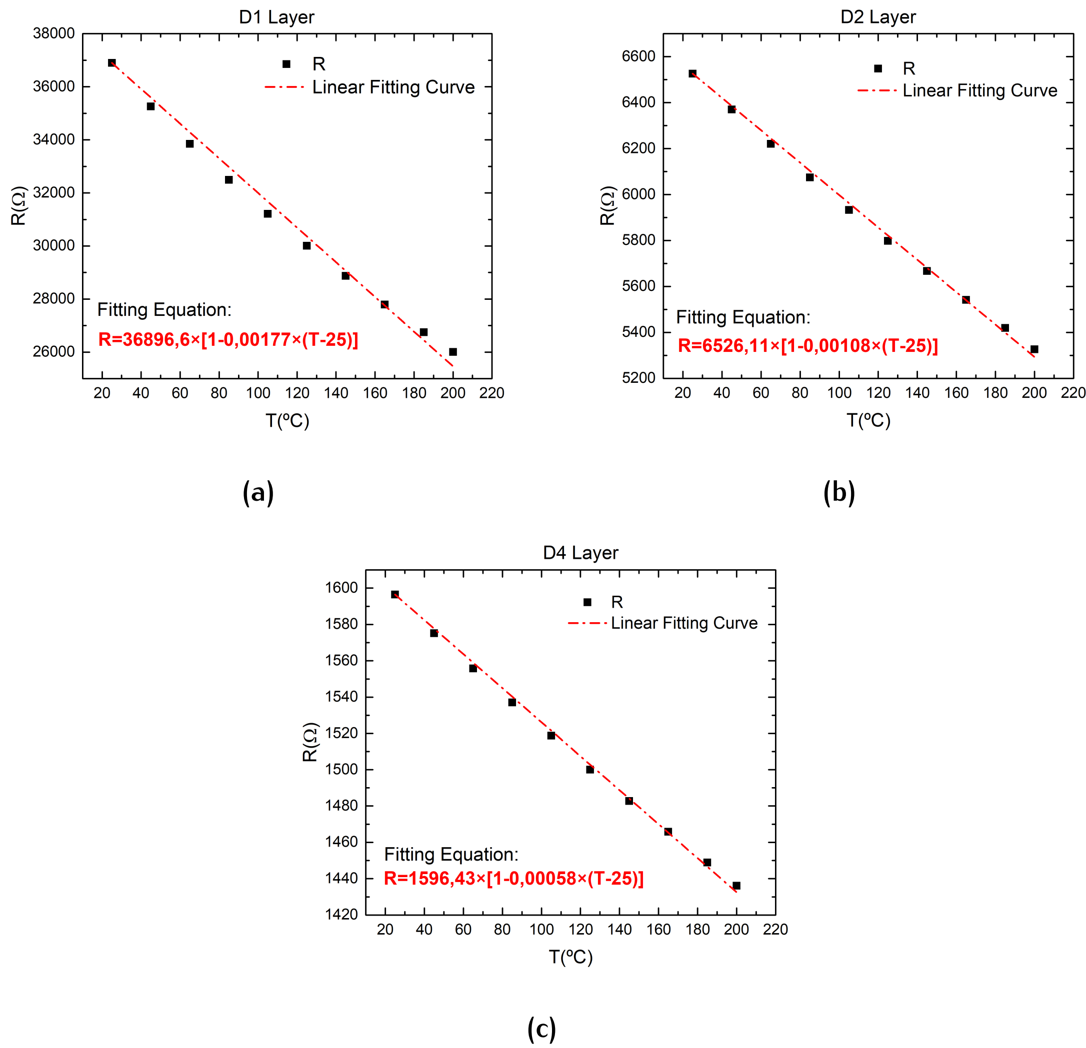


Figure 3.2: Resistance of the ELM test structure with respect to temperature for (a) D1 layer; (b) D2 layer; (c) D4 layer.

Table 3.6: Constants used in the equation

Parameters	*Values*
Boltzmann constant	$1.38 \times 10^{-23} \quad J \cdot K^{-1}$
Average molar mass of dry air	$28.96 \quad g \cdot mol^{-1}$
Average molecule diameter of air	$4 \times 10^{-10} \quad m$
Thermal conductivity of poly-SiC	$370 \quad W \cdot (m \cdot K)^{-1}$
Thermal conductivity of air at 1 atm at room temperature	$0.0262 \quad W \cdot (m \cdot K)^{-1}$

3.4.1 Nominal Pirani Guage

The dimension of the nominal Pirani gauge with a geometrical parameters of $l = 250\ \mu m$, $w = 8\ \mu m$, $z = 2\ \mu m$ and $s = 2\ \mu m$. The bias current of the nominal gauge is 600 μA. The nominal Pirani gauge is based on the D1 poly-SiC layer,

and material constants of which were measured in Section 3.3. As for other related parameters, such as thermal conductivity of air, are listed in Table 3.6. The substrate temperature is set at room temperature. The resistance of the micro-bridge with respect to the ambient pressure can be calculated by inputting all variables into Equation 3.19. The calculation was done at a pressure range from 1 Pa to 1 atmospheric pressure with a pressure step of 10 Pa. Since the Pirani bridge is working in constant current mode, the output voltage $V(P)$ can be easily calculated with the help of Ohm's law. The resistance of the micro-bridge R_b versus the pressure and output voltage versus the pressure are shown in Figure 3.3a.

As we expected from the literature review, both curves demonstrate "S" shapes, and due to the negative TCR of poly-SiC, the resistance and voltage output are decreasing with decreasing pressure. When the bias current is set to 600 μA, the maximum output voltage and minimum output voltage are 4.828 V and 4.836 V respectively. By calculating the first derivative of the output voltage, the maximal sensitivity of the nominal device is obtained when the pressure is at the lowest point. The P_H and P_L are determined not only by the geometry but also by the voltage detection limit of the readout, which is limited by the resolution of readout electronics and the noise-induced environmental disturbance and/or thermal effects. The source meter that will be used to characterize the device is Keithley 2612B. According to its datasheet, its voltage resolution is 50 μV, and this value is considered as the detection limit. From Figure 3.3b, the relations of $V_{max} - V(P)$ and $V(P) - V_{min}$ between pressure are plotted. The value of P_L can be found from the intersection between function $V(P) - V_{min}$ and horizontal line where $V = 50 \quad \mu V$, while P_L can be found from the intersection between function $V_{min} - V(P)$ and horizontal line. From the curve, P_L is approximately 40 Pa. At the high-pressure end, we consider the output voltage is saturated at 1 atm, so the maximum output voltage is 4,84 V, and the higher detection limit is around 90570 Pa.

3.4.2 COMSOL Multiphysics Verification

In order to confirm that if the calculation is correct, the analytical model is verified with FEA simulation software COMSOL Multiphysics. The basic principle of COMSOL software is to solve a set of differential equations formed by laws of physics. To do this, the structure that needs to be simulated is built and discretized by the software. Then, proper boundary conditions are applied to the discretized geometry, resulting in corresponding numerical models. The geometry used for running the simulation is shown in Figure 3.4. The functional element of Pirani gauge is the suspended micro-heater, in order to simplify the geometry, only suspended part was built and all the other things, such as supporting structures and contact pads, were ignored. The heater is made the same

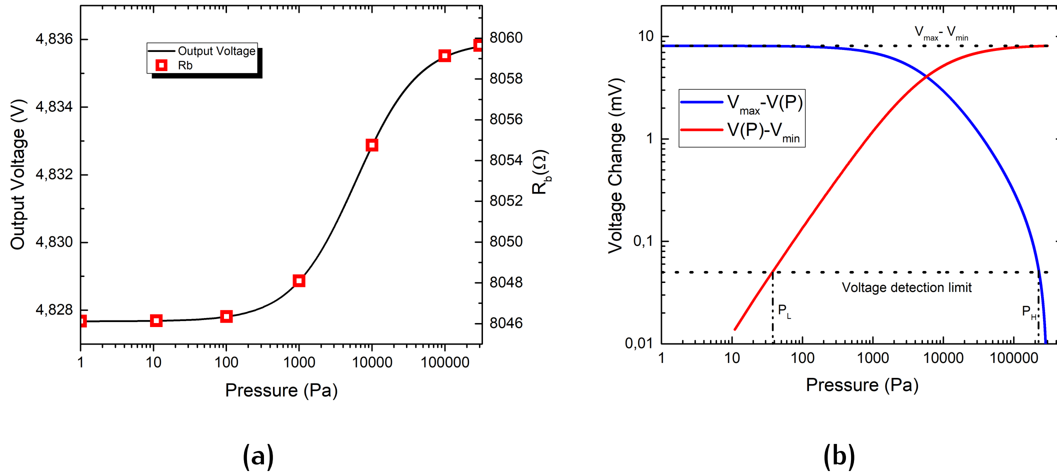


Figure 3.3: (a) Output voltage and heater resistance with respect to pressure calculated by the theoretical model; (b) Pressure range of the nominal device.

size as the nominal device and is placed 2 μm above the 525 μm thick silicon substrate. In between the suspended heater and silicon substrate, a block of air is inserted.

Setting up the physics involves in the transduction mechanism is essential, and settings should be close to what will happen in reality. In order to simulate the situation where micro-bridge heats up with a constant current and loses heat through the air gap, "AC/DC" module and "Heat Transfer" module were applied to the geometry. Under the AC/DC module, electrical current is injected to the one end of the heater, and the other end is set as grounded. The heater block is electrically isolated with other blocks. In the Heat Transfer module, the thermal conduction between the suspended heater and substrate is determined by the three-dimensional form of Fourier's law Equation 3.24.

$$\frac{Q_{gas}}{A} = -\lambda_g \cdot \nabla T \tag{3.24}$$

According to Equation 3.11, the pressure-dependent air thermal conductivity λ_g is calculated in advance and is inputted as a material property. The conduction not only takes place in the air gap but also in the heater itself, the heat generated by heater is distributed by thermally conductive poly-SiC bulk, which can also be described by Fourier's law. The model still obeys the homogeneous boundary condition made in Section 3.2. Therefore the temperature at both ends is set at a substrate temperature $T_{substrate}$. The Joule heating caused by injecting current affects the thermal conduction. Therefore a coupling between Heat Transfer module and AC/DC module was done to allow them to interact with each other. The net heat accumulated in a finite element should be zero when the system eventually reaches an equilibrium state according to the energy conservation law.

A proper element size is crucial to get a good balance between computation time and simulation accuracy. For this simulation, the model was meshed by free triangular block with an extra-fine element. The minimum element quality is 0.51, and the computation time is about 20 minutes to calculate 21 data points.

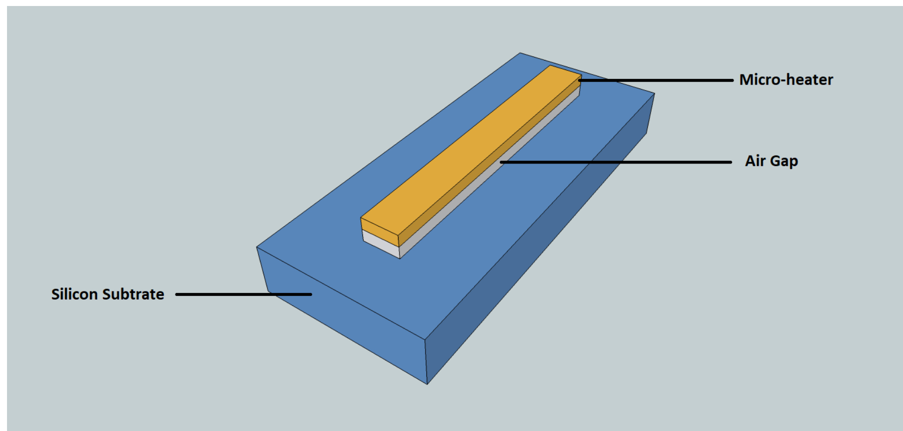


Figure 3.4: Digital model of the device

The output voltage can be obtained by deriving the maximum potential of the model. The simulation result is plotted in the Figure 3.5, in comparison with the theoretical result. From the curve, we can clearly see that at each simulated pressure data point, there is no significant difference between COMSOL model and theoretical model. This proved the correctness of the theoretical model derived in Section 3.2. With the verified numerical model, it is not necessary to carry out the simulation with COMSOL for each time, which is quite time-consuming. By inputting corresponding parameters in the theoretical model, we can easily get predicted performance same as COMSOL.

3.4.3 Length

Up to now, we obtained the performance of the nominal device, and the correctness of the theoretical model is verified by the COMSOL model. Therefore, taking the nominal device as a referential point, we can now easily investigate how a single geometrical parameter affects the performance of Pirani gauge quantitatively by controlled experiment. First of all, the effect of different length was studied. For this purpose, the length was reduced to 150 μm and was increased by a factor of two and four respectively, compared to nominal dimension. And all the other geometrical variables remained the same as the nominal device. Because of the dimensional change, the initial resistance of each device was changed. Thus, in each case, the biased current was changed accordingly to maintain the output voltage the same at the 1 atm. In such a way, we can better compare the effect brought by length changes between different devices. Figure 3.6a gives the output voltage of each simulated geometry. Compared to the

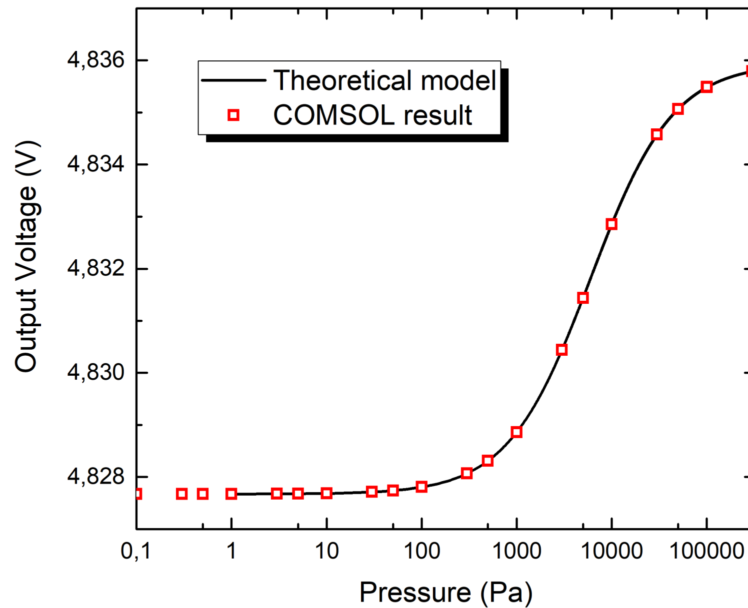


Figure 3.5: A comparison between the analytical result and COMSOL simulation.

nominal dimension, geometries which have larger length gives a larger output different. By contrast, for example, the geometry with a 150 μm length only has an output voltage change of 3.12 mV, more than twice less than that of the nominal device. Also, from the Figure 3.6b, with decreasing length, the absolute value of the fractional resistance change (relative to the initial resistance at atmospheric pressure) deceased from 1.07% to 0.51%, 0.17 % and 0.065 % respectively. These plots indicate that a longer geometry is more sensitive to pressure change, and this aligns with the qualitative prediction mentioned in Section 2.2.2. Figure 3.6c gives the result of $V(P) - V_{min}$ versus pressure in order to better illustrate how the length changes the measurement range of the Pirani gauge. The horizontal line at 50 μV represents the resolution of our readout instrument. From the figure, the lower operation limit decreased from around 100 Pa to 0.2 Pa while length increased from 150 μm to 1000 μm.

According to the calculation above, we can conclude that in order to make Pirani gauge more sensitive to at lower pressure, the length should be made as long as possible. However, a longer heater does not always bring benefits. From the mechanical point of view, a larger length makes the structure more mechanically unstable. The deflection of a clamped-clamped beam w is expressed in Equation 3.25:

$$w = -\frac{qx^2}{24EI}(l^3 - 2lx^2 + x^3) \tag{3.25}$$

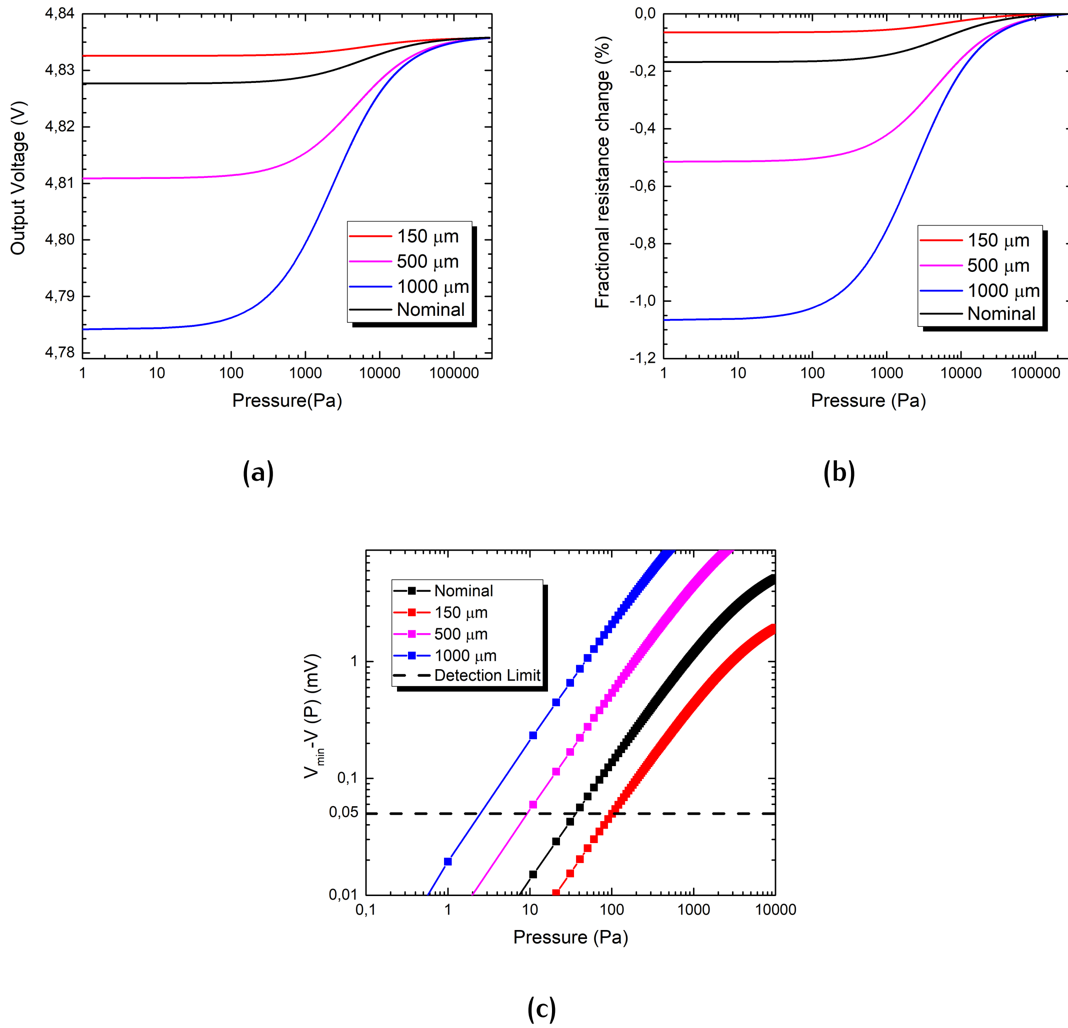


Figure 3.6: (a) Output voltage of geometries with lengths of 150 μm, 500 μm and 1000 μm versus pressure, in comparison with nominal geometry; (b) Fractional resistance change of geometry with different lengths; (c) Measurement ranges of Pirani gauges with different lengths at the low pressure end.

where q is the force applied on per unit length. EI is the product of Young's modulus and the second moment of area. The maximum value of the expression can be obtained while $x = l/2$, which is at the center of the beam, and the w_{max} can be written as:

$$w_{max} = -\frac{5ql^5}{768EI} \tag{3.26}$$

As can be seen from Equation 3.25 and Equation 3.26, the maximum deflection is proportional to the fifth power of l. Therefore, a longer suspended structure is more likely to suffer from buckling and makes it more vulnerable to an applied force. Once the suspended heater is pulled down and contact the substrate, it will create more thermal conduction through solids and affect the performance of the device.

3.4.4 Width

In order to study how the width affects the performance, geometries with a width of 6 μm, 10 μm and 12 μm are calculated. Similarly, to compensate for the resistance change brought by the geometrical change, bias current was modified accordingly. The results are shown in Figure 3.7. Among all the simulated geometries, the output voltage change is the same as that of the nominal geometry. Therefore, the fractional resistance change should also be the same for each geometry. The performance curve shifts a little bit to the right with the increasing width. This effect can be explained by Equation 3.12, where P_0 is proportional to the term $w/(w+z)$. When z is relatively small compared to w, P_0 will not increase significantly with w, and this could be the reason the curve only moves a little bit to high-pressure side with increasing width. Also, Increasing the width does not affect too much on lower detection limit. Because as the width increases, not only Q_{gas} increases, Q_{solid} also increases at the same time. It is worth noting that the wider gauge will need more power to achieve the same performance as the narrower gauge, and this might also be caused by more heat transfer rate provided by more surface area and more solid contact area.

Similar to varying length, varying width also has an impact on mechanical performance. In Equation 3.25 and Equation 3.26, the term EI is known as the flexural rigidity of the beam, where I is the second moment of area. Flexural rigidity represents the resistance of the structure while undergoing bending. The value of I depends on the cross-sectional shape of the beam. As for a rectangular shape in this case, it is equal to:

$$I = \frac{w^3 z}{12} \tag{3.27}$$

From this, we can see that narrower beams also have less mechanical stability compared to wider ones, in spite of having only a little extension of measurement range at low pressure.

3.4.5 Gap distance

When it comes to gap distance, smaller gap distance should improve the detection limit at the atmospheric side, because it compensates the decrease of mean free path of gas molecules, making the thermal conductivity saturate at higher pressure (see Equation 3.12). In order to verify this, the gap distance was reduced to 500 nm and 1000 nm. Because changing gap distance does not affect heat itself, the bias current for each case remains 600 μA.

Figure 3.8a gives the performance curve of devices with different gap sizes. At the low-pressure end, devices with different gap distance all have the same voltage output, indicating the temperature of different geometries is all the same at

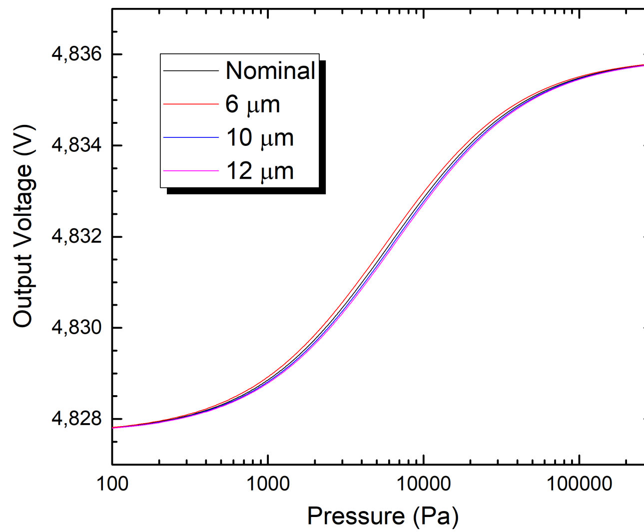


Figure 3.7: Output voltage of geometries with different widths versus pressure, in comparison with nominal geometry;

the vacuum side. This is explainable because at the lower vacuum side devices have almost no capability to transfer heat via air gap, and the heat conduction through the solid is the same for all the devices since the geometries are the same. At the high-pressure side, we observed a large output voltage with decreasing gap size as expected. Figure 3.8b gives the result of $V_{max} - V(P)$ versus pressure in order to better show how the gap size affects the higher detection limit. The maximum detection limit increased from 90570 Pa (nominal gap distance) to 97310 Pa (1000 nm) and 99500 Pa (500 nm). This proved that the structure with a smaller gap is more sensitive at higher pressure range and gives a larger detection limit near atmospheric pressure.

3.4.6 Layer Comparison

Effects of geometrical parameters have been investigated, yet it is also needed to look into which type of poly-SiC layer should be applied to the suspended heater. In Section 3.3, the properties of three different types of SiC layer were obtained. Based on that, the fractional resistance change of the heaters with those three types of SiC are calculated and plotted in Figure 3.9. In each case, the power consumption at atmospheric pressure is kept the same to make each heater has the same initial temperature.

From Figure 3.9, the device made by D1 will have the largest fractional resistance change. Considering the fact that D1 layer has the largest resistivity, the total resistance change of device with D1 layer will also be the largest, and as a result,

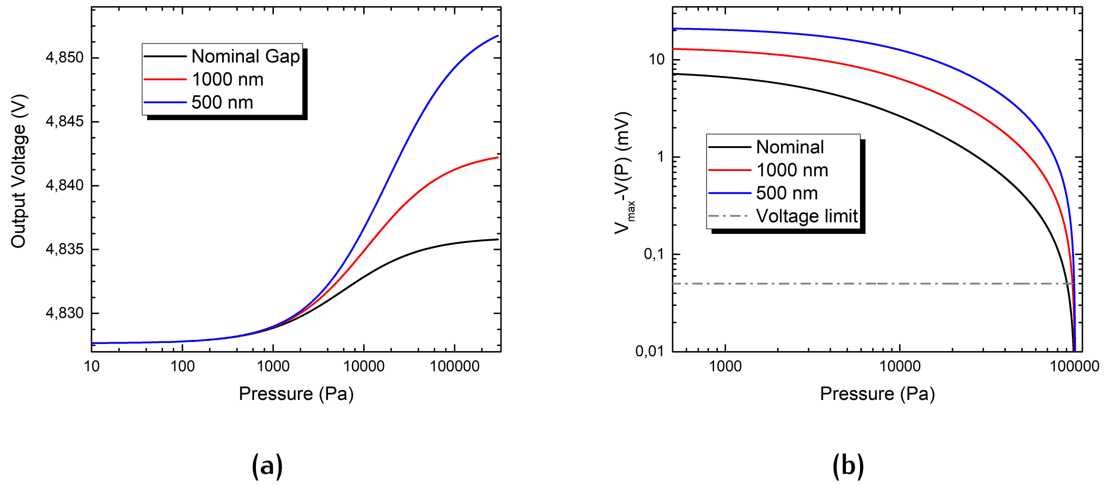


Figure 3.8: (a) Output voltage of geometries with gap size of 500 nm and 1000 nm versus pressure, in comparison with nominal gap size; (b) Fractional resistance change of geometry with different lengths.

a maximum output voltage change can be obtained. In contrast, D2 and D4 layer have lower resistivity and lower TCR. Therefore with the same amount of temperature change, the total resistance change will be less compared to the device with a D1 layer. In order to achieve the same performance, a larger bias current is required, which consumes more power. As discussed above, the D1 Poly-SiC is the best choice among three layers for fabricating Pirani gauges.

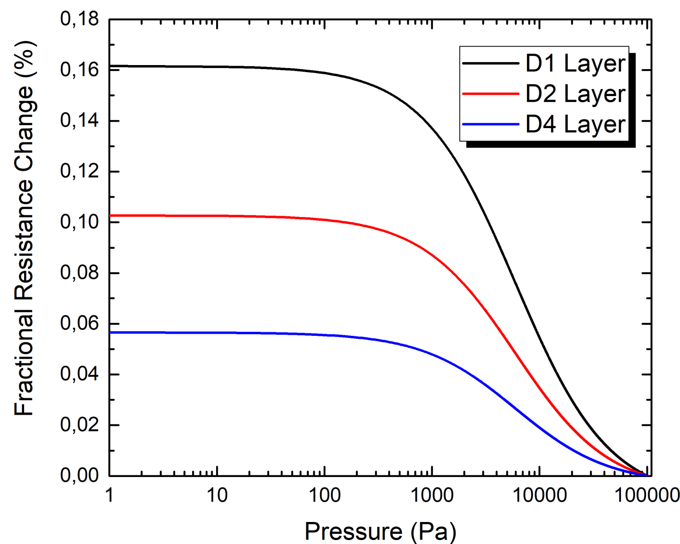


Figure 3.9: Output voltage of geometries with different SiC layers versus pressure, in comparison with the nominal geometry;

3.4.7 Pirani Gauge Dimensions

Up to now, all the design parameters have been investigated with the help of the theoretical model. From the result obtained by model, it can be concluded that in order to allow lower pressure to be measured, the ratio of Q_{gas} and Q_{solid} should be maximized. From Section 3.4.3 and Section 3.4.4, it can be seen that increasing the length is the most effective way to extend the detection limit at lower pressure. By contrast, increasing the width does not help to expand the lower detection limit as expected, because increasing the width also increases Q_{solid}. In order to expand the measurement range at high pressure, the gap distance between the suspended heater and the substrate needs to be tuned smaller. Section 3.4.5 shows that the P_H will be higher with smaller an air gap size. Increasing the width helps a bit with improving the high detection limit, but it is at the cost of more power consumption. Therefore, it can be concluded from the model that in order to achieve the largest operation range and sensitivity, and the gauge should be made long, and the air gap size should be made smaller. And in order to make the gauge more power-efficient, the gauge should be made as narrower as possible. However, as discussed in the previous content, we have already known that the length can not be infinitely large due to the decrease of the stiffness of the beam. Also, it is imaginable that less air gap makes it easier for suspended structures to contact the substrate. Therefore, possible sources that will cause deformation is studied in the following content.

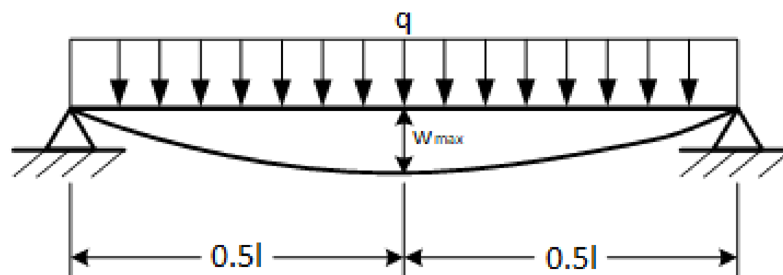


Figure 3.10: An illustration of heater bending under a uniformly applied force.

The deflection of the nominal device is first considered. During the operation, the gravity of the beam will drag the structure towards the substrate, as shown in Figure 3.10. The deflection induced by gravity w_g can be calculated from Equation 3.26. By plugging all the values needed, w_g is equal to 9.8×10^{-8} nm. As for the longest heater (1000 μm), the w_g is equal to 1.0×10^{-4} nm, which is negligible compared to the size of the air gap.

The self-buckling of the beam under the resistive heating and high-temperature environment also bring instability to the structure. To investigate this, a simulation was carried out with COMSOL, where the deflection of the nominal device

was simulated in different temperatures. The device was simulated in a environment where temperature increased from 100 °C to 600 °C with a step of 100 °C, and the coefficient of thermal expansion of poly-SiC was taken from the literature [9], The simulation results are plotted in the Figure 3.11b, it shows deflection profiles along the beam. As can be seen, the overall deflection increases with the rising temperature, and the maximum deflection is obtained at 600 °C, which is around 600 nm. The same simulation was carried out with the longer (1000 μm) beam, and the results are shown in Figure 3.11c. With longer geometry, a significant increase in the maximum deflection can be seen at each temperature. At 600°C, the w_{max} can be up to 15 μm, and this is not desirable for high-temperature compatible Pirani sensor since the heater will have physical contact with the substrate and create a thermal short-cut.

In order to achieve the largest possible dynamic range, the suspended heater should be made as long as possible, and the gap size should be minimized. However, this design rule leads to a mechanically unstable structure, making it has less resistance to thermal buckling. Therefore, the geometrical design of the Pirani gauge involves some trade-offs between sensing ability and mechanical stability. From the simulation in Figure 3.11b, the nominal device has less than 600 nm maximum deflection (less than the gap size) at an elevated temperature up to 500 °C, and it also gives an acceptable performance as described Section 3.4.1. Therefore it is considered to be one of the design choices. Longer geometries with 250 nm, 500 nm and 1000 nm lengths are also designed to pursue better performance though they are more likely to suffer from buckling. And the device with shorter length (150 nm) is designed for more robust structure. For each length, the width increases from 6 μm to 12 μm with a step of 2 μm for more mechanical strength. And for each heater, there will be three gap sizes, i.e. 500 nm, 1000 nm and 2000 nm. Totally there will be 48 devices with various geometries, longer Pirani gauge designs will have better sensing ability and short ones are meant for working in higher temperature environments. Different designs are made on a single die, and this makes it possible to integrate multiple Pirani gauges to achieve a large dynamic range. Also, multiple designs help to verify the effect of length, width and gap size in the future measurement.

3.4.8 Metal Layer

Many studies have stressed the importance of metallurgy used in SiC applications [39, 55, 56, 57]. An inappropriate metal-semiconductor junction can bring reliability issues. In order to have a negligible contact resistance at the metal-semiconductor interface with a non-rectifying behaviour, an ohmic contact to poly-SiC is desired, and a proper ohmic contact is a great challenge for high-temperature SiC-based sensor and power electronics. The metal-semiconductor junction property depends on the Schottky barrier height, which is equal to the work of function of the metal minus the electron affinity of the semiconductor.

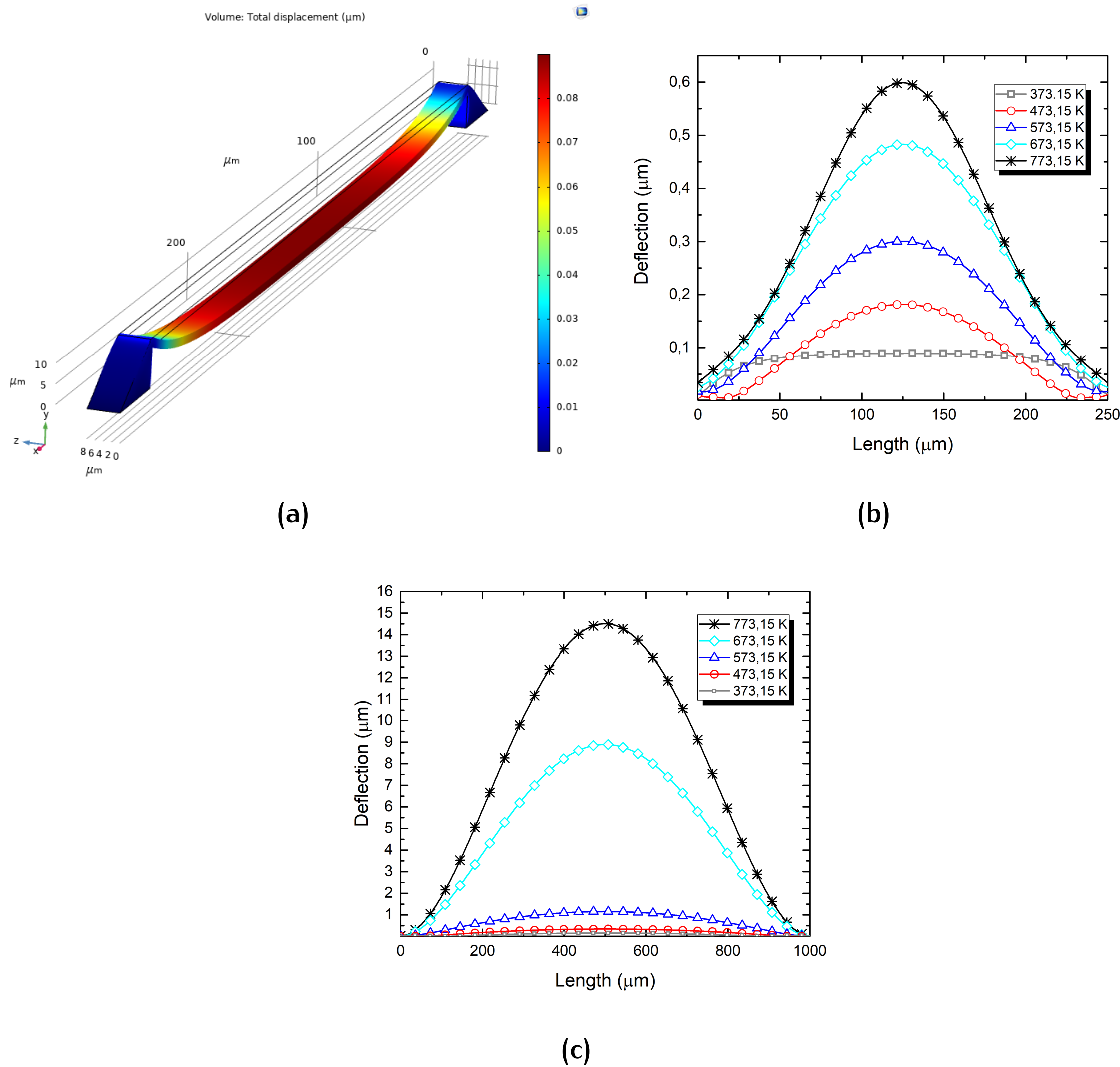


Figure 3.11: (a) The COMSOL simulation for thermally induced deflection of the nominal device at 100 °C; (b) Simulation results for the nominal device at different temperatures; (c) Simulation results for the 1000 μm long beam at different temperatures.

The lower the Schottky barrier is, then the more electrons on both sides, i.e. metal side and semiconductor side, can tunnel through the junction more easily under an electric field. A summary of recent progress on ohmic contact to SiC has done by Wang et al. [58]. Conventionally, Al is able to form an ohmic contact with SiC. Al has a work function of 4.28 eV, and SiC has an electron affinity of around 4.17 eV, so the barrier height is 0.11 eV, which means there is no effective barrier. However, aluminium is not suitable for high-temperature applications because aluminium is reactive, and the contact will suffer from reliability issues brought by long term operation at the high temperature [9, 57]. As reported in the literature [39, 59], titanium (Ti) and nickel (Ni) are able to achieve good ohmic contacts with SiC. Compared to the aluminium, titanium and nickel have similar work functions (4.33 eV and 5.15 eV), but they are less reactive in high

temperature than Al which causes less degradation at the SiC/metal interface. However, nickel is considered as contaminated metal which will bring some restriction during the process, so Ti and Al are chosen to be the metal layer in our design.

3.5 CONCLUSION

In this chapter, the derivation of the Pirani gauge's analytical model was demonstrated, and the correctness was verified with FEA software. The theoretical result showed a nice match with the COMSOL result. In order to get the accurate theoretical result from the model, the parameters of poly-SiC needed for estimating the performance of the Pirani gauge were obtained by experiments, and the D1 poly-SiC layer with the largest TCR was chosen as the construction material for micro-bridge. The performance of devices with different geometries was calculated with the analytical model derived by Mastrangelo et al., and this can be a reference for further measurement procedure. The impacts of different geometrical parameters, e.g. length, width and gap size, on the performance of the Pirani gauge were investigated by calculation. In general, the trend performance that varies with geometries matches qualitative conclusion mentioned in Chapter 2. Apart from sensing ability, the thermal buckling was simulated. From the simulation, we know that shorter structures give better mechanical stability when operating at a high temperature, but it has less dynamic range, By the contrary, longer structures are less robust but will have better sensing ability. Therefore, multiple combinations of geometrical parameters are designed for the Pirani gauge.

4 PROCESSING

This chapter will discuss the fabrication of the Pirani gauge. The fabrication process is based on the existing technologies in EKL, and the detailed process flowchart for the device fabrication is given in the Appendix E. The issues encountered during the fabrication will be presented, and the corresponding solutions will be discussed.

4.1 STRUCTURE OVERVIEW

In our fabrication, not only the Pirani gauge will be fabricated, but also test structures for sheet resistance measurement and contact resistance. In this section, we will briefly demonstrate the structures of the devices which will appear on a single die.

4.1.1 Pirani Gauge

Based on the conventional micro-bridge structure, the Pirani gauge structure designed in this work is shown in Figure 4.1. The structure consists of the suspended heater, anchors and metal pads. To make the heater to be suspended above the substrate, two SiC islands at both sides of the heater act as anchors, providing sufficient mechanical supporting for the micro-bridge. The area of SiC island can be neither too large nor too small. If it is too large, more heat will be conducted through the solid, and the performance of the device will be affected. If it is too small, the structure will be gone after the releasing process. From Section 3.4.7, the widest suspended structure has a width of 12 μm. Considering this, each of the SiC islands covers an area of 130 × 50 μm^2. The metal wire is put on top of the SiC mesa, connecting to be metal pads on the isolation layer (SiO_2). The metal pad is designed to be 150 × 150 μm^2 to have a proper landing during measurement. During the release step, there will be an unavoidable under-etching of SiO_2, because an anisotropic etching process is used. This might cause physical contact between the metal and substrate, as shown in Figure A.1. Therefore, an additional Si_3N_4 isolation layer is patterned under SiO_2 isolation layer to ensure good electrical isolation after releasing of the heater. The process flow of the Pirani gauge will be presented in Section 4.2.2.

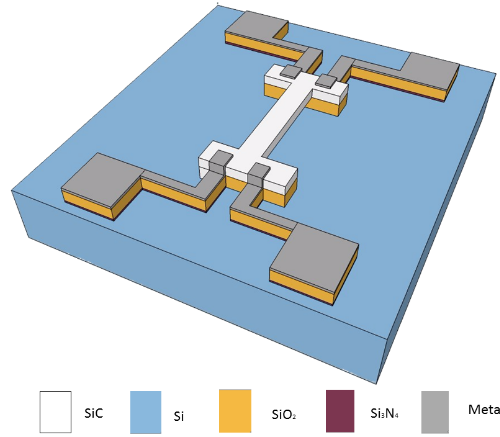


Figure 4.1: The structure of the Pirani gague in this work.

4.1.2 Test Structure

In Section 3.4.8, we chose aluminium and titanium as interconnections and pads for our devices. However, it is difficult to model the contact resistance analytically. In contrast, a direct measurement of contact resistance is relatively easy to achieve, so a special test structure needs to be prepared. In the design, we include a most widely used structure, i.e. Kelvin test structure, to measure the contact resistance. The structure of Kelvin test structure is shown in Figure 4.2a. As shown in the figure, a SiO_2 layer serves as the isolation layer, isolating most of the area between the poly-SiC layer and the metal layer and leaving only a small contact window. In this way, we can obtain the contact resistance (R_c) simply by Ohm's law. Given the area of the contact window (A), the contact resistivity (ρ_c) can be calculated by:

$$\rho_c = R_c \times A \tag{4.1}$$

Apart from test structures for contact resistance measurement, the test structures for layer sheet resistance measurement are included in each die. Although the overall sheet resistance can be measured with Resmap tool, it is still necessary to have test structures to measure the local sheet resistance of the layer for each die. The Greek cross van der Pauw test structure (shown in Figure 4.2b) will be used to measure the layer sheet resistance.

4.1.3 Supporting Structure

The thermally-induced buckling of the heater is a potential threat during the operation of the Pirani gauge. In order to prevent this, a back-up structure (shown in Figure 4.3) is designed in case the Pirani gauge has a significant out-of-plane buckling. The structure is similar to structure which has been presented in the work carried out by Julien et al. and Viard et al. [50, 51]. The idea is to divide

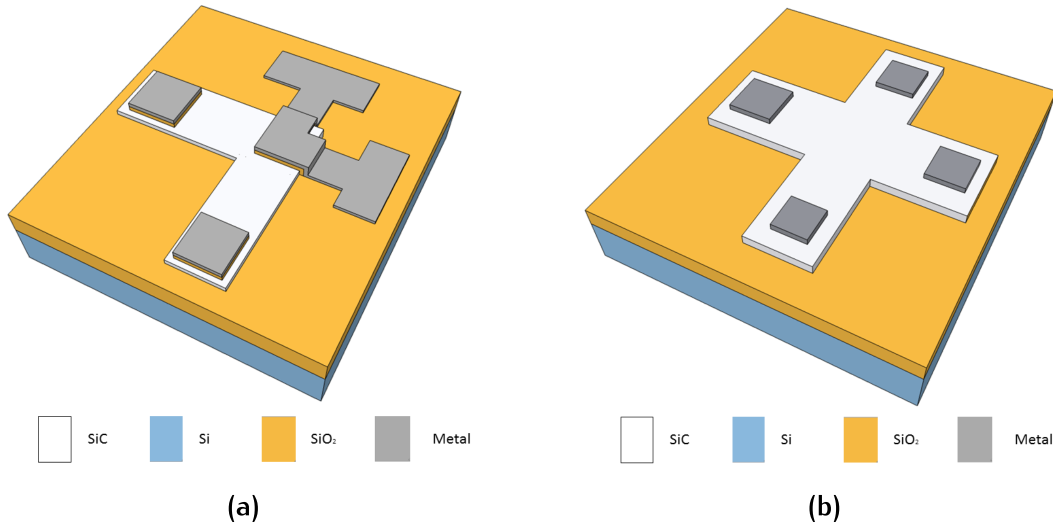


Figure 4.2: (a) Cross Kelvin resistor test structure; (b) Greek cross van der Pauw test structure.

the suspended heater into shorter segments because shorter beams will have smaller maximum deflection. Each segment is held by the transverse SiO_2 supporting structures beneath, which can prevent the beam from deflecting towards the substrate. The heater also has an equal chance to bend upwards, so a silicon nitride layer is patterned on top of the heater to prevent the upward deflection. Another purpose of the Si_3N_4 layer is that it can serve as the masking layer of SiO_2 supporting structures so that the SiO_2 still remains after releasing process.

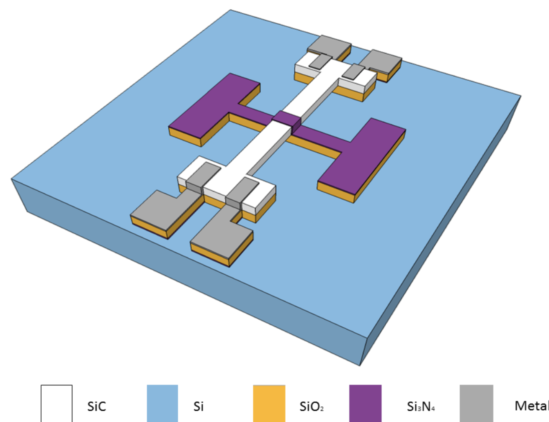


Figure 4.3: Pirani gauge with the supporting structure to prevent buckling.

4.2 FABRICATION

The fabrication of Pirani gauge is a 3-mask process, and the fabrication of Kelvin test structure need an additional mask layer for contact openings. Therefore, the whole process requires a 4-mask step in total. Challenges encountered during the fabrication and the solutions will be discussed in the following contents.

4.2.1 Fundamental Fabrication Techniques

MEMS processing is based on the mature manufacturing technologies used in the semiconductor industry. A brief overview of techniques that will be used in the fabrication is given below.

1) Photolithography

   Lithography is a process to pattered the thin film or the substrate and is the most crucial step for any micro-fabrication process. During the lithography, a light-sensitive organic material, i.e. photoresist, will be applied to the surface. After a certain dose of exposure, the information on the photomask will be transferred to the photoresist. The desired image will be patterned on the photoresist after a developing process. In this project, the equipment for coating and developing process are EVG120 and Brewer Science Manual Spinner, and ASML PAS 5500/80 is used for exposure step. The mask that will be used during the lithography step is attached in Appendix C.

2) Chemical vapour deposition (CVD)

   Chemical vapour deposition is a thin film growth technique, where one or more precursor gases react or decompose in a vacuum furnace. The resultant non-volatile product will be deposited on the wafer. The CVD techniques that will be used in this project are LPCVD and PECVD. LPCVD produces thin films with good quality, but it requires high thermal energy to activate the reaction, this LPCVD process usually has a high thermal budget. By contrast, the deposition temperature of PECVD can be lower by introducing plasma. However, the step coverage of PECVD film is a challenge.

3) Etching

   In order to transfer the pattern on the photoresist to the thin film, the material which is not masked by photoresist must be etched away. Wet etching is the most common etching technique, and it uses a specific chemical to etch the desired material without affecting other material. This process is anisotropic, so the masked material is also likely to be attacked by the chemical. Compared to wet etching, dry etching (also known as reactive ion etching) is an isotropic process. It utilizes reactive ions to bombard the

exposed surface. In this work, Trikon Omega and Drytek384 Triode will be used for this purpose.

4) Sputtering

Sputtering, also known as physical vapour deposition (PVD), is another thin film growth technique, and it is mainly used for metal growth. In the sputtering tool, the gaseous ions (typically Argon) are biased by an electric field and keep attacking the metal target. The target material is first transferred into vapour phase and is eventually deposited on the wafer.

5) Vapour HF etching

Vapour HF etching is a special form of etching that will be used in this work. The working principle is similar to wet etching, but the difference is that the etchant is not in a liquid phase but a vapour phase. The advantage of the using vapour HF is that it can prevent the suspended beam from being pulled down to the substrate by the capillary force during drying [60].

4.2.2 Process Flow

The main processing step of the Pirani gauge is given in Figure 4.4. The starting material is a 525 μm thick single-side polished silicon wafer. First, a 300 nm Si_3N_4 is deposited by LPCVD with a mixture of $SiCl_2H_2$ and NH_3 at a temperature of 850 °C at 20 Pa. As shown in Figure 4.4a, Si_3N_4 is patterned with the same mask used for the metal layer so that it can serve as an additional isolation layer between the substrate and the metal layer. The wafer is then coated with PECVD TEOS oxide, and the TEOS layer is not only the sacrificial layer for the releasing the micro-bridge, but also the electric isolation layer. Depending on the gap size, the TEOS oxide is deposited on separate wafers with different thickness (500 nm, 1000 nm and 2000 nm). After the oxide deposition, a 2000 nm poly-SiC is deposited with SiH_2Cl_2, C_2H_2 and NH_3 as precursor gases at a temperature of 860 °C at 80 Pa. A patterning step is used after SiC deposition to define the micro-bridge structure and anchor regions, as shown in Figure 4.4b. This patterning step involves the etching process of SiC, which will be discussed in detail in Section 4.3. If a supporting structure is desired, then a nitride layer should be deposited and patterned at this after SiC patterning. In Figure A.3c, the metal layer for interconnections and pads are fabricated. The metal deposition is done by sputtering at 350 °C, 500 nm of Ti and 675 nm of Al are deposited on different wafers to get SiC/Al and SiC/Ti contacts. As shown in Figure A.2, the metal film has a good step coverage on SiC mesa. A 400 °C annealing step in a nitrogen environment is followed. The post-deposition annealing helps to relieve the strain and improve the surface quality of the film. Additionally, it can induce reactions between the metal and the semiconductor, which can enhance the bonding between two material at the interface. After annealing, the wafer is

diced into $6 \times 6\ \mu m^2$ chip. Finally, dies are put on a carrier wafer to release the suspended micro-bridge structures with the aid of vapour HF tool. One of the final devices is shown in Figure 4.5.

Because test structures for contact resistance, i.e. Kelvin test structure, will be fabricated together with Pirani gauges on the same die, a SiO_2 isolation layer will be deposited and patterned in between Figure 4.4b and Figure A.3c, which is not presented in Figure 4.4. The process of Kelvin test structure is shown in Figure A.3.

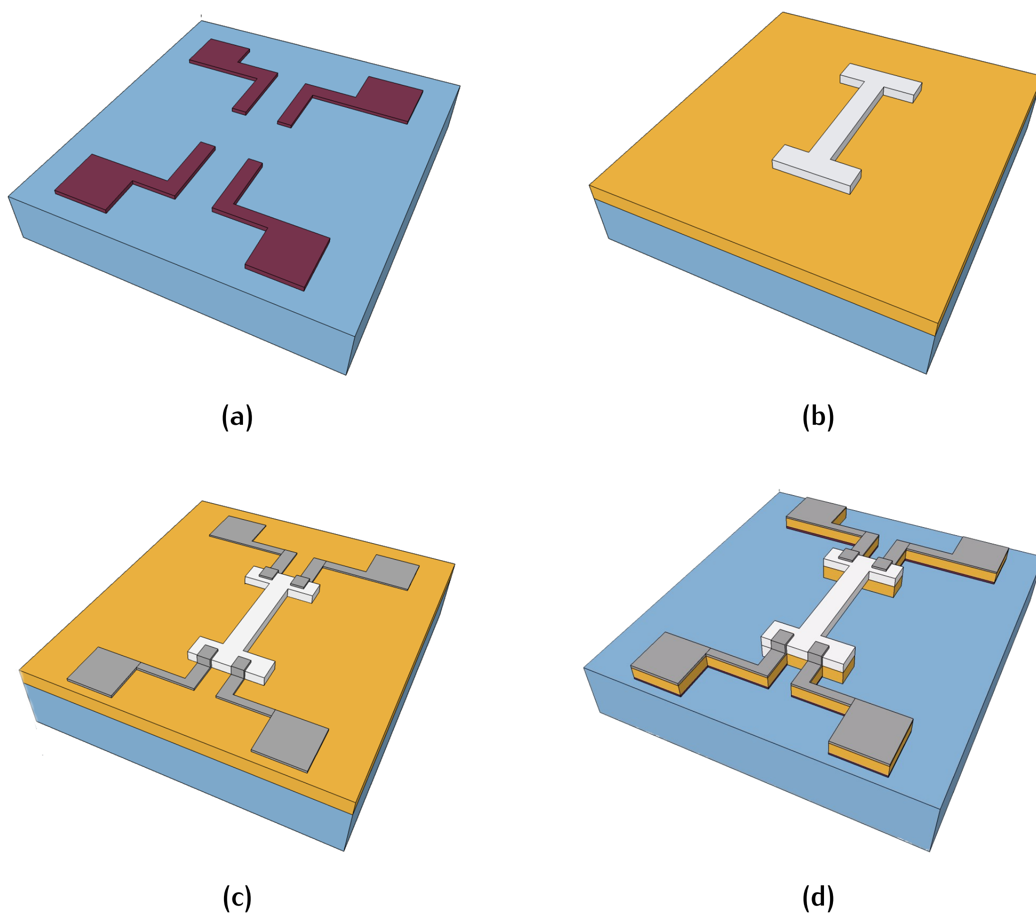


Figure 4.4: (a) The LPCVD Si_3N_4 layer on top of the silicon substrate serves as an additional isolation layer; (b) The PECVD TEOS oxide is deposited as the sacrificial layer which defines the gap, and then the D1 poly-SiC layer is deposited and patterned as the sensing element; (c) Metal layer deposition and patterning; (d) The micro-bridge structure is released by vapour HF.

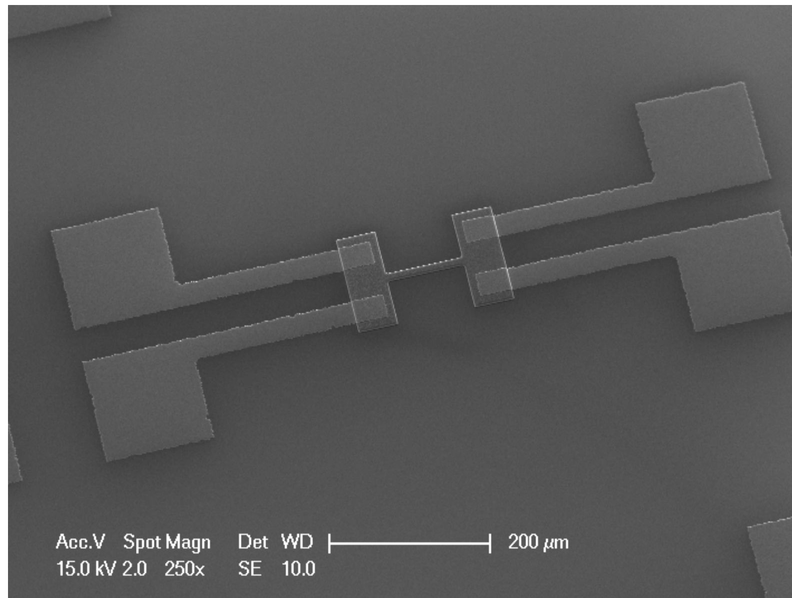


Figure 4.5: SEM image of a micro-fabricated Pirani gauge. The dimension of this Pirani is 150 μm long and 10 μm wide. The gap size is 2 μm.

4.3 CRITICAL PROCESS STEPS

The last section demonstrated the process flow of fabricating the Pirani gauge and the test structure. In this section, the critical process steps, including SiC deposition, SiC etching and surface micro-machining process, will be investigated.

4.3.1 SiC Deposition

In Table 3.1, we have already discussed the poly-SiC deposition recipe that will be used for this project. The layer D1 with the largest TCR is chosen as the construction material. In our fabrication, we used the recipe for D1 with a 4-hour deposition to obtain 2 μm poly-SiC layer for heating elements. The average layer properties are concluded in Table 4.1, and the raw data of the sheet resistance are attached in Table B.1. The TCR of each deposited layer was not measured after the deposition because TCR measurement will bring contamination to the process wafers.

From the table, we can clearly see a difference compared to the D1 layer obtained in Section 3.3.2. In general, all layers show a decrease in resistivity, and resistivity of one the layers is more than two times lower than the resistivity obtained in the previous experiment. Similar results have also been reported in the literature [52]. As suggested by the author, the possible reason could be that depositing a thicker layer requires a longer deposition time in the high-temperature furnace and this process will better activate doping atoms in the lattice, which enhances

the electrical conductivity of SiC layer.

Table 4.1: The D1 poly-SiC layer properties deposited on each processing wafer.

Wafer Number	Sheet Resistance ($\Omega/\square$)	Thickness (nm)	$\rho \times 10^{-3}(\Omega \cdot cm)$
No.1	112.6	2000.0	22.5
No.2	138.5	2050.0	28.4
No.3	168.6	2106.3	35.5
No.4	246.4	2065.7	50.1
No.5	203.9	1915.6	39.1
No.6	201.4	2126.2	43.4

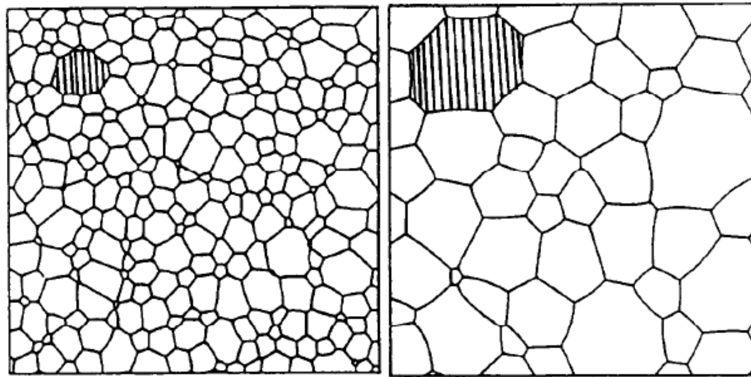


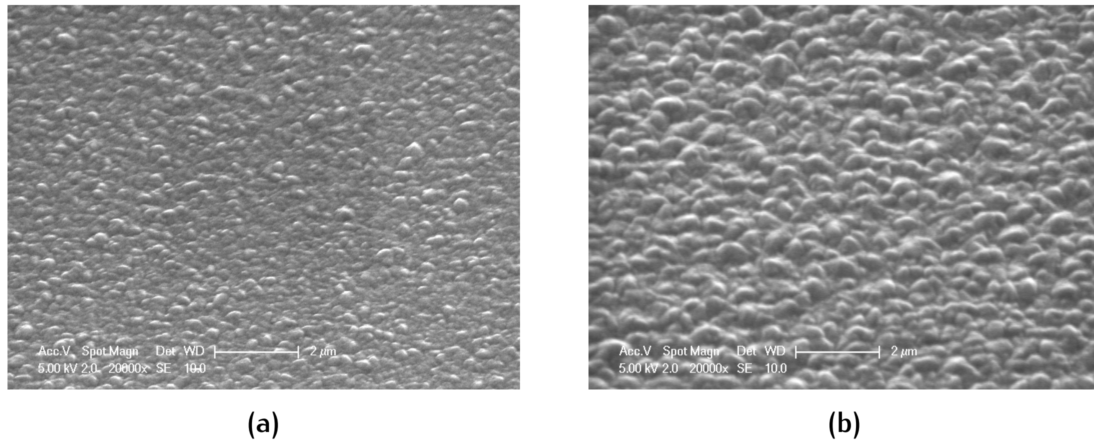
Figure 4.6: An illustration of normal grain growth process. The increase in average grain size with respect to time leads to a reduction in area of grain boundary [61].

Another possible reason is that a spending longer time in the high-temperature environment could induce an increase in the size of SiC grains, which will cause a reduction of the grain boundary. The normal grain growth process is time-dependent (t) and temperature-dependent (T), which can be described by the following equation:

$$d^2 - d_0^2 = c_0 t e^{-Q/kT} \tag{4.2}$$

where d is the grain size and d_0 is the grain size at $t = 0$. c_0 and Q are constant. From the equation, it can be seen that the grain size increases with time, and a higher temperature will accelerate the grain growth process. The reduction in grain boundaries can enhance the conductivity of the material because the grain boundaries are considered as lattice defects and can impede the motion of free charge carriers. SEM pictures (Figure 4.7) were taken to verify the time-dependent grain growth effect. Figure 4.7 shows surfaces of a 1 μm SiC layer and a 2 μm SiC layer, which were deposited by 2 hours and 4 hours approximately. The 1 μm SiC layer has a smaller granular aggregate on the surface than

the thicker layer, and this indicates the grain size increases over time. A similar experiment result was reported by Fu et al. [62].



(a) (b)

Figure 4.7: A 45° tilted view of surfaces of (a) 1 μm and (b) 2 μm D1 poly-SiC layers in a same magnification.

We also observed that the layer resistivity and thickness are strongly dependent on the location where wafers are put inside the furnace. According to our experience, the wafer located closer to the furnace door will get thicker poly-SiC layer. Also, the wafer located closer to the furnace door might be easier to get doped by ammonia due to the layer resistivity results. The non-uniformity of the deposition brings a difficulty to predict film properties, so a more repeatable LPCVD SiC deposition recipe needs to be created in the future work.

4.3.2 SiC Etching

Since poly-SiC has an excellent chemical inertness, it has a high etch resistance to commonly used etchants, which makes it difficult to conduct a conventional wet etching to poly-SiC. A number of approaches have been employed to obtain a high-quality carbide etching recipe [63]. These methods include using molten corrosive chemicals [64], electrochemical etching [65], laser ablation [66, 67] and plasma etching [68, 69]. SiC cannot be attacked by any acid or alkali at room temperature, but when etchant is heated up, it will start attacking SiC. However, molten alkali is extremely aggressive, and it is at a high temperature (usually above 350 °C). Therefore, handling molten etchant becomes an issue [64]. Usually, this kind of chemical needs a Pt container and tools to handle it. Also, not many mask materials are able to survive from corrosion of molten alkali. The electrochemical method makes use of anodization process in low concentration HF solution to form a porous SiC layer which is easy to be oxidized compared to normal poly-SiC layer. After the oxidation, the anodized part can be easily removed by wet etching. This method needs electroplating equipment to ob-

tain porous SiC. Finally, due to the availability of equipment, laser ablation and plasma etching methods are chosen to be candidates for our SiC etching process.

The principle of laser ablation is straight-forward. It uses a high energy laser beam to interact with a small area of the target material. The material which is illuminated will experience a photo-chemical and photo-thermal process and will be heated up instantaneously [66]. Because of these two effects, the material under exposure sublimates or melts, and therefore is etched away. Laser micromachining technique is extremely suitable for material which is hard to be removed by a conventional process, such as glass, piezo-ceramics and SiC. Another important advantage of laser etching is that it is a maskless process. Unlike conventional etching processes where etching takes place on the entire wafer, the laser ablation only takes place at the user-defined area, and the rest of the area remains intact. This makes laser ablation especially helpful for an in-depth etching process where a thick mask layer is needed, e.g. creating via holes on a wafer.

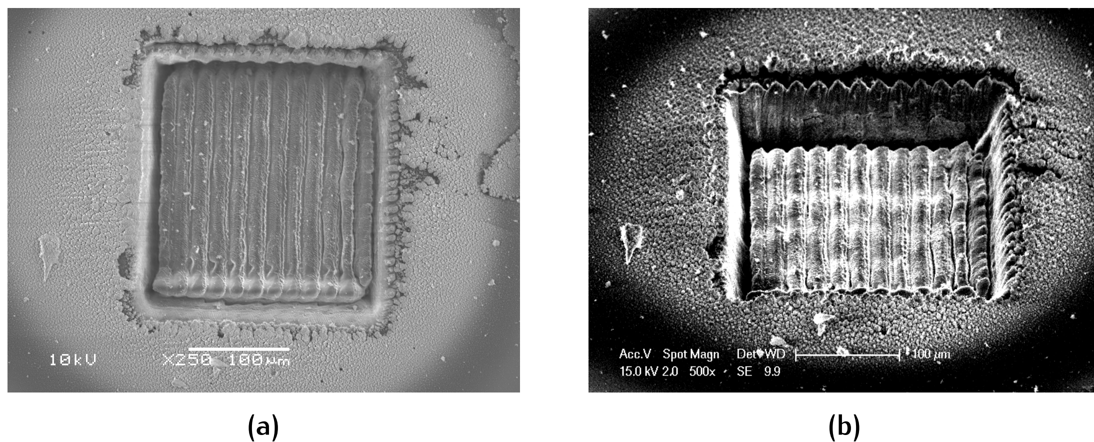


Figure 4.8: (a) Top view and (b) tilted view of the SiC etched by laser.

A test was carried out in the faculty of 3mE with the help of Dr. Hunt to examine the feasibility of laser ablation for Pirani gauge fabrication. The laser cutter employed is Talon 355-15, and it uses an ultraviolet laser source at 355 nm wavelength. A 4 inch n-type 4H-Sic was used for the etching test. The detailed parameters used in test etch are shown in Table B.5. The SEM result when laser repetition object is set to 10 is depicted in Figure 4.10, and laser ablation results with other laser settings are attached in Figure A.4 and Figure A.5.

From the SEM images, the area where SiC has been etched by the laser has a poor surface quality. This is mainly caused by the non-uniform power distribution of the laser beam. The power distribution of a single laser beam is usually considered to be Gaussian, and as a result, each laser-cut will produce a parabolic etching profile. Also, a large amount of debris caused by re-deposition can be

observed on the top surface, as shown in Figure 4.8b. The laser etches around 4 μm of SiC for each repetition, which is too fast for precise process control. As mentioned above, we can conclude that the laser ablation technique provides poor process control and is not suitable for our process. However, due to the fast etch rate, laser ablation is still an excellent method for building high-aspect ratio structures, such as through silicon carbide vias.

Compared to laser ablation, plasma etching is the most common technology in the semiconductor industry. In this work, the poly-SiC drying recipe "SiC_3mu" will be investigated. This recipe contains the main reactant HBr gas with a flow rate of 40 sccm and 30 sccm of chlorine (Cl_2) gas. The purpose of adding Cl_2 is to increase the etch rate and improve the etch profile [69]. The RF power, ICP power, plate temperature and chamber pressure are set to 40 W, 500 W, 25 °C and 5 mT, respectively.

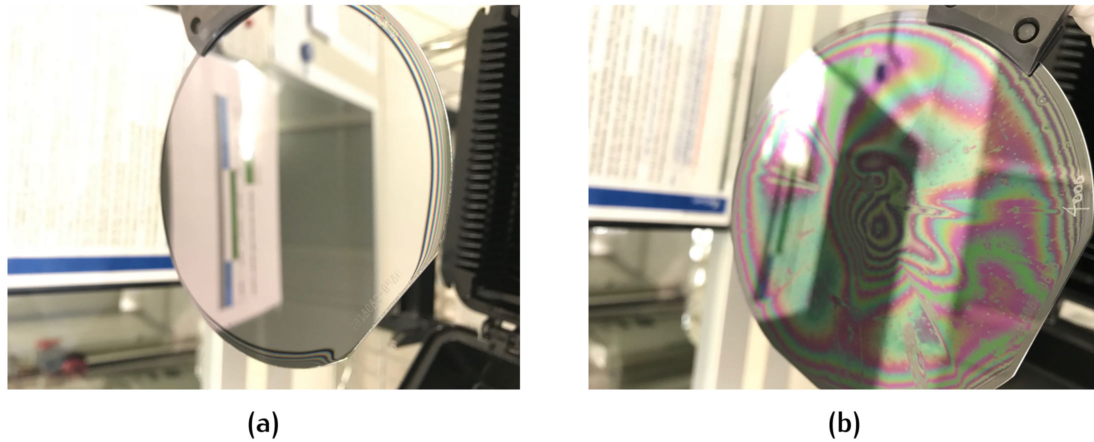
First of all, the etch rate of the recipe needs to be determined. Three blank test wafers (T1, T2 and T3) were deposited with 1 μm of D1 poly-SiC layer. The wafers were patterned with test structures to measure the depth with profile analyzer afterwards. In order to avoid to etch away the photoresist mask and/or SiC layer completely, the etching time was set to be 2 minutes only. After dry etching, the photoresist was removed, and the thickness of the removed SiC was measured. For each wafer, five points were measured on each test wafer, and average values were taken to calculate the etch rate of the recipe. From the data given in Table 4.2, the etch rate is 173.8, 151.4 and 167.0 nm/min for the corresponding test wafer. This SiC etching recipe yields an averaged etch rate of 164.1 nm/min with a maximal variation of 7.7 %.

Table 4.2: The etching depth after being etched by 2-min of "SiC_3mu"(unit: nm)

Measurement Point	T1	T2	T3
No.1	330.7	309.5	320.1
No.2	333.5	312.5	340.2
No.3	355.1	296.7	314.9
No.4	362.3	285.3	344.8
No.5	355.9	310.0	350.1
Averaged Thickness	347.5	302.8	334.0
Etch rate (nm/s)	173.8	151.4	167.0

Many studies have reported a variety of mask materials used for SiC dry etching [64, 69], such as Al, Ni, Cr, SiO_2. These mask materials are used as hard masks to obtain a high selectivity. However, it makes the patterning step more complicated than patterning with photoresist. Additionally, the usage of metal mask brings two problems. One is that it brings contamination to the etch tool and later fabrication. Another is that micromasking effect can be observed with the metal mask, where the metal redeposits to the SiC surface and form grass-like

structures [69]. In order to avoid using a hard mask, we used a thick layer of photoresist to mask our 2 μm SiC layer.

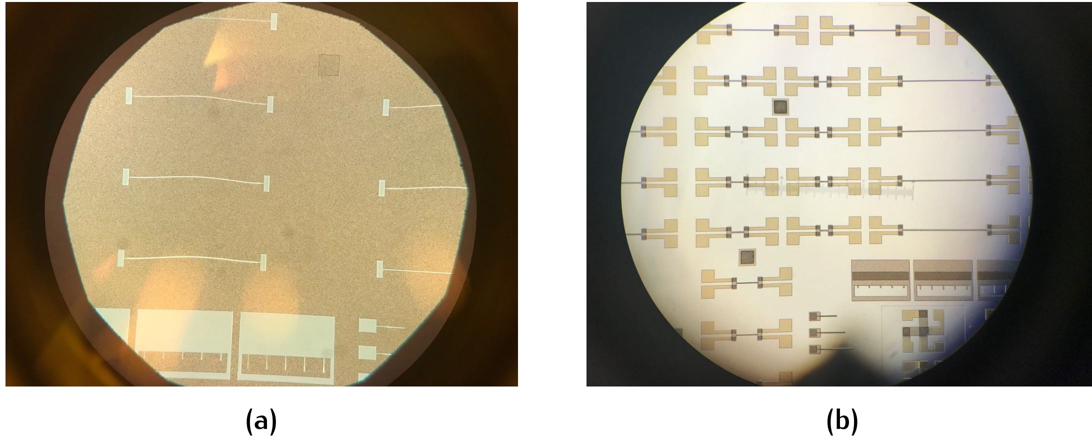


(a) (b)

Figure 4.9: (a) A 4 μm thick photoresist and (b) a 7 μm thick photoresist after 12 min 10 sec of dry etching.

In order to obtain a sufficient masking layer, the photoresist mask at least needs to withstand 12 min 10 sec of drying etching. First, the standard recipe "1 - Co - 3027 - 4 μm" in the automatic coating tool EVG 120 was tested. After 12 min 10 sec dry etching by "SiC_3mu" the photoresist was totally gone as in the Figure 4.9a, indicating that it is not a sufficient mask. However, 4 μm is the thickest mask layer we can obtain from the standard recipe, so the manual coating is used to achieve a thicker mask layer. For manual coating, AZ-12-XT-20PL-10 positive photoresist was employed. The 12-XT series photoresist features for large high-aspect ratio, and it allows a single coat thickness from 3 μm to 20 μm. The coating step was carried out with Brewer Science manual coater. With 4000 rpm spinning for 30 seconds, 7 μm photoresist was obtained. After development, the masking layer was also etched by SiC dry etch recipe for 12 min 10 sec. After etching, we can still observe a layer of photoresist, as shown in Figure 4.9b. It indicates that 7 μm 12-XT photoresist gives a sufficient mask for our etching recipe.

It is worth mentioning that an out-of-plane bending can be observed in many photoresist patterns for micro-bridge structures after development, as shown in Figure 4.10a. This might be result from the internal stress of the photoresist and/or the centrifugal force which pulls the structure outwards during the spin-dry process. This can be solved by applying a longer hexamethyldisilazane (HMDS) treatment before coating and/or a longer soft-baking time (180 sec at 110 °C) to enhance the adhesion between photoresist and the substrate. The SiC layer after patterning is given in Figure 4.10b.



(a) (b)

Figure 4.10: (a) The out-of-plane bending of the photoresist after development; (b) SiC micro-bridge structures after dry etching.

4.3.3 Structure Releasing

During the release process, the sacrificial layer below the SiC bridge, i.e. SiO_2, will be removed, making the micro-bridge suspended. It should be mentioned that the dicing of the wafer should take place before the releasing procedure. Because during dicing the wafer will be continuously flushed by water to remove particles generated. If the structure is released before dicing, then the suspended structure has a very high chance to be destroyed. After dicing, the micro-bridge is released by means of vapour HF. The drying process is not needed after the vapour HF etching, so it can prevent stiction from happening. Detailed recipes for vapour HF etching is given in Table B.6. The reaction between SiO_2 and HF is given below:

$$SiO_2 + 4HF \rightarrow SiF_4(gas) + 2H_2O \tag{4.3}$$

The poly-SiC is around 2 μm thick, so it makes the SiC not transparent. This makes it hard to find out when the sacrificial layer underneath will be etched clean. A feasible solution is to use another transparent layer to help us find out the endpoint. A 300 nm LPCVD Si_3N_4 layer was deposited on the sacrificial layer and was patterned into the bridge structure. Figure 4.11 shows the release process of a structure after a 10-minute and a 25-minute vapour HF etching. We can see that after 25 min, there is almost no SiO_2 can be observed. The total release time depends on the dimension of the Pirani gauge. In general, a wider bridge with a larger gap size takes more time than a narrower bridge with a smaller gap. The release time of a 12 μm wide beam with 2 μm gap size can be up to 50 minutes.

In order to verify if the suspended structure has an in-plane deflection towards Si substrate, the distance between the top surface of the micro-bridge and Si substrate was measured with Keyence VK-X250. The measurement results of a device with a 1000 μm length and a 6 μm width are shown in Figure 4.12. In

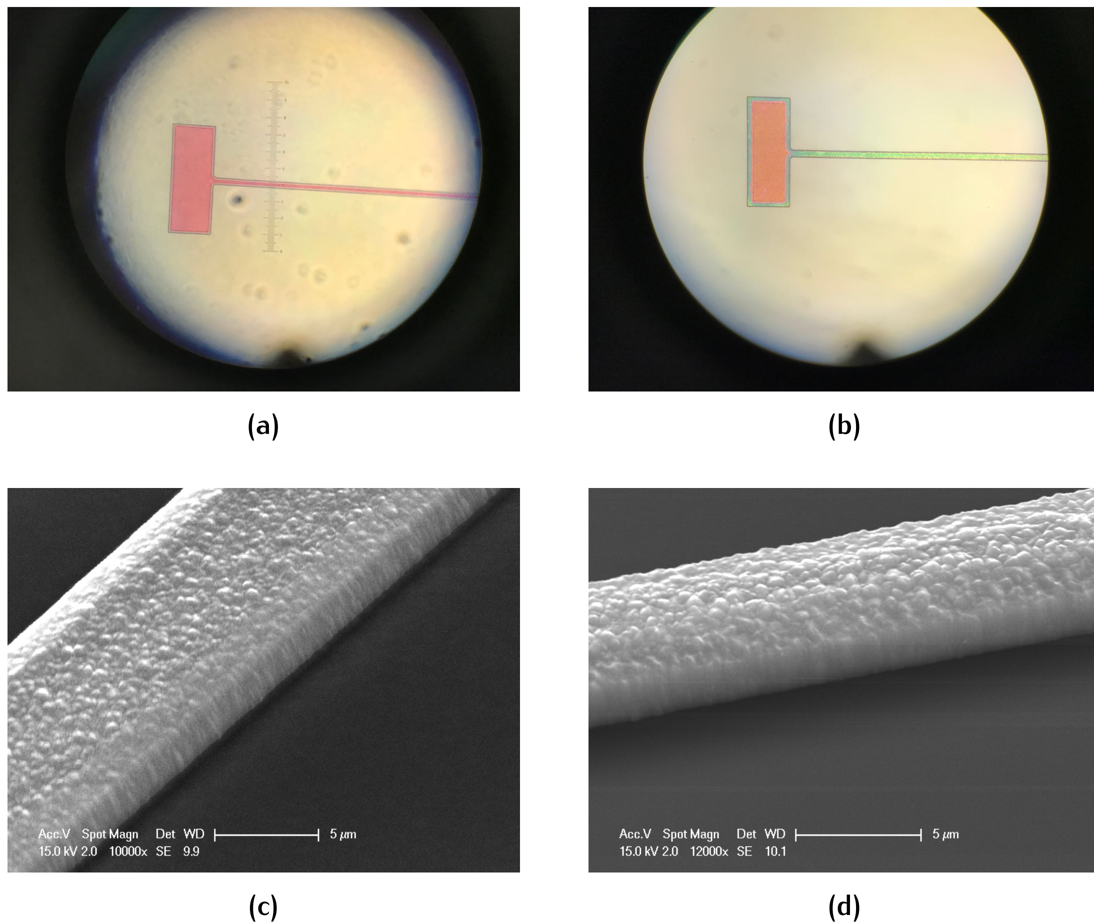


Figure 4.11: The vapour HF release process of an 8 μm wide micro-bridge at (a) 10 min; (b) at 25 min. (c) and (d) are SEM images of beams before and after experiencing a release process. Compared to (c), there is a shadow beneath the beam in the (d), indicating the structure is suspended.

theory device with such dimension is the most vulnerable to bending and will have the largest maximum deflection. The cross-sectional profile along the beam is scripted with Keyence. No obvious deflection can be seen from Figure 4.12b. The distance between the top surface of the micro-bridge and Si substrate was measured to be 3956.3 nm at the middle of the beam. By subtracting the thickness of the SiC layer, the gap size is 1956.3 nm which is approximately equal to the thickness of SiO_2 sacrificial layer.

4.4 CONCLUSION

This chapter demonstrated a successful fabrication of the MEMS Pirani gauge based on D1 poly-SiC layer. The general manufacturing procedures and the critical steps in the process, i.e. SiC deposition, SiC etching and structure releasing,

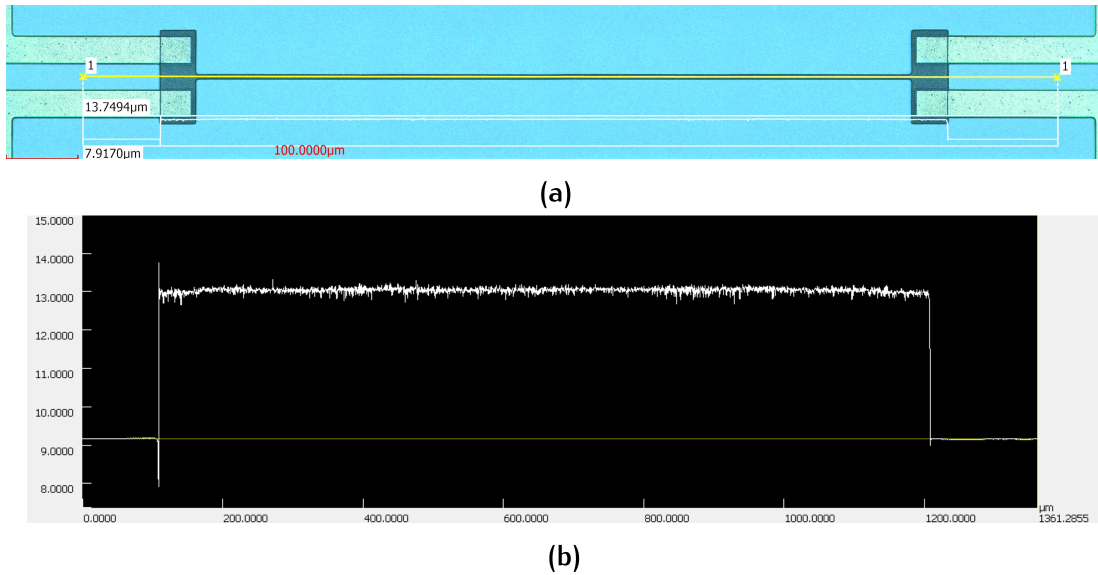


Figure 4.12: (a) Device with a 1000 μm length and a 6 μm width, the yellow line indicate the position of the cross-section; (b) Distance between the top surface of the micro-bridge and Si substrate along the beam.

are discussed in detail. By introducing vapour HF to release the micro-bridge structure, a very high yield can be obtained from the process. The micro-bridge with a length of 1000 μm is achieved. It is also possible to build a more robust structure with supporting structures or more sensitive devices with dual heat sinks based on the current process. However, there is an issue with the deposition recipe. In the future, a more repeatable SiC recipe should be created.

5 MEASUREMENT

In this chapter, a dedicated pressure measurement setup will be built up for the Pirani gauge characterization. With this setup, the device will be characterized at both room temperature elevated temperature. Finally, the contact resistivity of the metal/SiC junction will be measured.

5.1 MEASUREMENT SETUP

The micro-fabricated vacuum gauge is aimed to work at an elevated temperature, so apart from room temperature, the gauge also needs to be calibrated at a high temperature. In order to meet the measurement requirements, the measurement setup must be able to provide a pressure range from a certain vacuum level to atmospheric pressure. In addition, the Pirani gauge needs to be heated up by the setup to a desired temperature to verify its high-temperature capacity. A sketch of the measurement setup for characterizing the Pirani gauge is shown in the Figure 5.1. The measurement setup is comprised of a micro probe station (MPS), a pressure controller, a pump and a source meter for the electrical measurement. The actual setup is demonstrated in Figure A.6.

The MPS bought from NEXTRON is dedicated for the high-temperature usage. The MPS consists of a hotplate, a pressure chamber and four micro-probes. The hotplate is controlled and powered by a temperature controller via computer, and the hotplate is able to work at a temperature up to 750 °C. The pressure chamber has a small volume (less than 100 mL). Therefore only die-level measurement is possible. Both over-pressure and under-pressure environment can be created with the micro-chamber. The probe is for electrical measurement and is integrated on the micro slide rail. The MPS provides four BNC connections for interfacing with the instrument.

The back-pressure controller P-700 from the Bronkhorst is used to monitor and to control the pressure in the micro-chamber. The resolution of the pressure sensor is 10 Pa, and the control ability is ± 100 Pa. The controller is connected in between the micro-chamber and vacuum pump with Teflon hoses. The pressure controller connects to the PC with RS232 cable to monitor and control the pressure in the chamber.

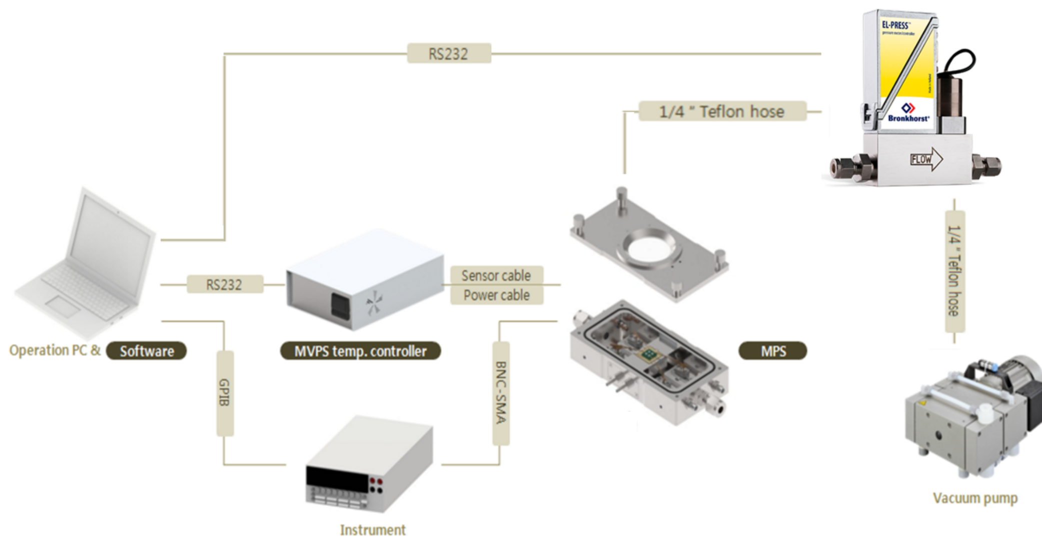


Figure 5.1: A block diagram that shows the composition of the measurement setup.

Currently, two source meters, i.e. Keithley 2612B and Agilent 4156C, are available to interface with the probe station. The probe station is originally made to interface with electrical instruments by four coaxial connectors (BNC). Keithley 2612B is able to connect to these connectors directly. When using Agilent 4146C as the source meter, adaptors from BNC to triax (SMA) are needed. The measurement can be programmed by using "Keithley Test Script Builder" (TSB) or "iccap" software. In our setup, we chose Keithley 2612B as the source meter because of its convenience. The detailed code which was used for measurement is illustrated in Appendix D.

5.2 DEVICE CHARACTERIZATION

With the measurement setup, the device can be calibrated in different temperature. In order to compare with the result from the model, we will first characterize the Pirani gauges with different geometries at room temperature. Then, the characterization of the device at high temperatures will be carried out.

5.2.1 Four Probe measurement

The MPS is equipped with four probes, and therefore it is possible to carry out four-probe measurements. Figure 5.2 demonstrates the principles of the two-probe method and four-probe method. In the two-probe method, an ohmmeter is directly used to measure the impedance of the device, which also includes the

impedance of the metal lines, the contact resistance and the probes. Depending on the value of the R_{wire}, the two-probe method can bring a certain amount of inaccuracy. To avoid this, the four-probe method is applied for obtaining more accurate measurement result compared to the two-probe method. As shown in the Figure 5.2b, it uses separated pairs of probes to measure the current and voltage across the device under measurement. Because voltmeters have a high impedance, using a separate pair of lines to measure the voltage drop on the resistor will cause a negligible voltage drop, and the current passing through the voltmeter is also negligible. Thus, the voltage drop on the wires is not added to the voltage drop of the actual device.

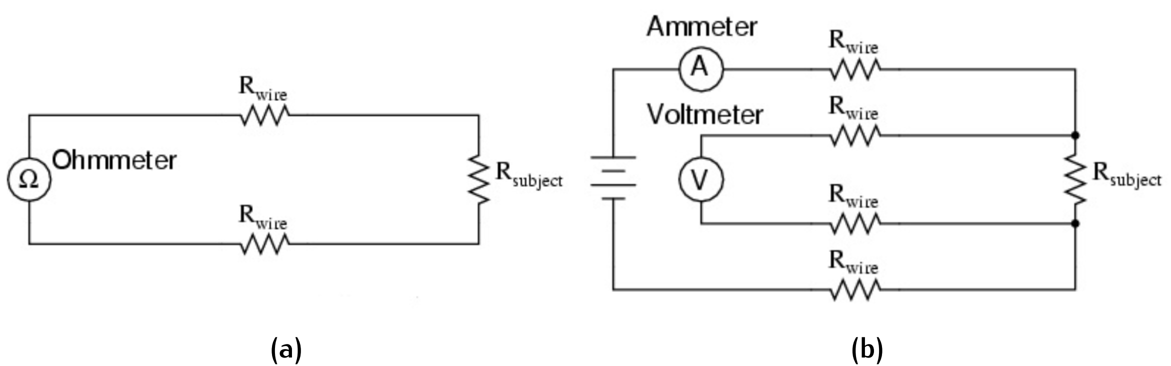


Figure 5.2: An illustration of (a) two-probe measurement; (b) four-probe measurement.

5.2.2 Room Temperature Calibration

First of all, the nominal device was calibrated to verify the functionality of the fabricated device. Same as the simulation, the nominal device was biased with a current of 600 μA. The Pirani gauge was calibrated from 0 % of 1 bar to 100 % of 1 bar. It is worth noting that the 0 % of 1 bar is not the absolute vacuum. Due to the resolution of our pressure controller, the pressure when the pressure controller indicates 0 % is considered as 10 Pa. Since most of the sensitivity of the Pirani gauge is at lower pressure range, the pressure step for the calibration was set differently across 1 atm to avoid taking to much time. The pressure step was set as 500 Pa at the lower pressure range. From 20 kPa to 30 kPa, the pressure step was set as 2000 Pa. And from 30 kPa to 100 kPa, the pressure step was set to be 5000 Pa. In total, there will be 60 pressure setpoints needs to measure, and the pressure will hold for 200 s at each pressure set point to give the device enough time for settling. In order to examine the retention ability of the gauge, the pressure increased to 1 atm and swept back to 0 %. The pressure profile for the calibration is indicated by the blue curve in Figure 5.3.

The output voltage versus pressure is shown in Figure 5.3. As shown in the figure, the output voltage ranges from 2.987 to 3.636 V when the pressure in-

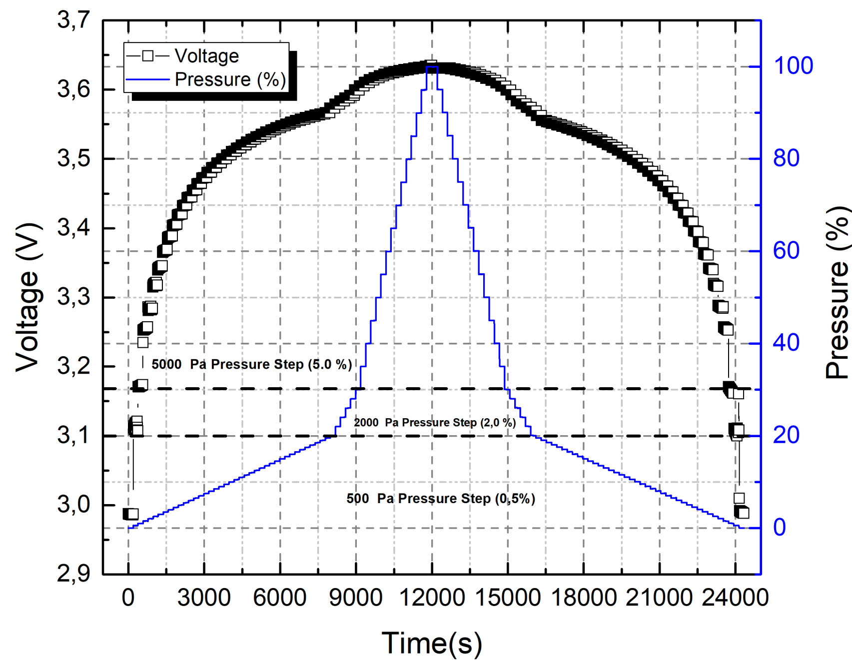


Figure 5.3: The pressure profile for the calibration (blue curve) and the output voltage of the fabricated Pirani gauge as a function of pressure (black dots).

creases from the low vacuum side to 1 bar, which means a maximum resistance change of 17.8 %. The pressure gauge has its highest sensitivity when it is at the lowest pressure setpoint, which is 0.264 mV/Pa or 0.44 Ω/Pa. The nominal gauge showed a repeatable respond to the pressure change, as indicated by the symmetrical curve in the calibration curve. The measurement range is from at least 10 Pa to 1 bar because the voltage is not saturated at both sides. We can see a significant difference between the simulation result and the actual device. The first reason is the difference between the material parameters used in simulation and fabrication. Although the values used in the simulation was obtained by experiment, the SiC deposition recipe can not guarantee a repeatable result, as mentioned in Chapter 4. The resistivity of the actual SiC layer used in the fabrication is lower than what has been measured in the Section 3.3.2. This can explain the output difference between the model and the experiment at 1 atm. Also, we can observe that the output voltage change is much larger than what we expected from the model. It indicates that the heat transfer in the lower pressure range is much less than we expected. The reason for the mismatch could also be the error in the material properties or the inaccurate assumption made in the Chapter 3. If we attribute all the discrepancy to the error in the material properties, we can obtain a quantitative match when reducing the thermal conductivity value of the SiC used in the simulation by around 20 times. Figure 5.4 shows a comparison between experimental results and theoretical results after

the model has been adjusted.

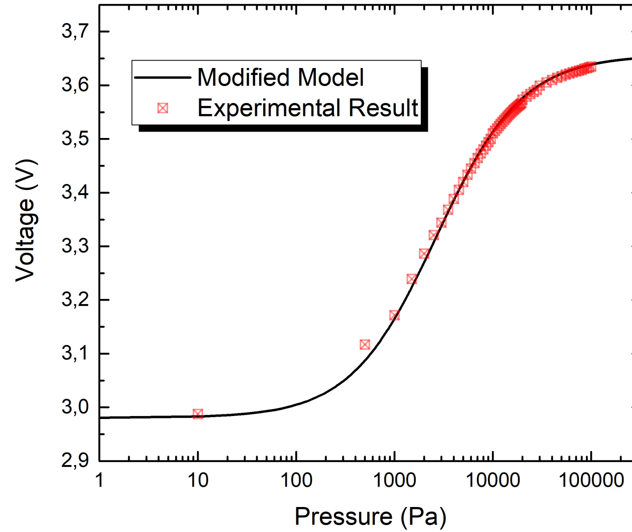


Figure 5.4: A comparison between the experimental result and the result obtained from modified model.

In order to verify the effects of dimensional parameters experimentally, the calibration of the devices with different geometries was carried out in the room temperature. First of all, the device with different length was calibrated. To make it more straightforward to compare with the nominal device, the input current was adjusted for each Pirani gauge to obtain the same voltage at 1 atm pressure. The result is shown in Figure 5.5. From the figure, we can see the most obvious effect brought by increasing the length is that the performance curve shifts towards the left, which aligns with the prediction from the analytical model. From 150 μm to 1000 μm, the maximum sensitivity increases from 0.137 mV/Pa (0.131 Ω/Pa) to 0.953 mV/Pa (6.42 Ω/Pa). Therefore, the Pirani will get more sensitivity at the low vacuum side, and lower pressure can be measured. But we can also observe that the device with 1000 μm length starts to saturate at around 10000 Pa, while the shortest device shows much larger sensitivity at 1 bar.

Figure 5.6 shows the impact of the width variation. Reducing the width of the heater caused only a little left shift of the performance curve, and this result is the same as the result we have obtained from Section 3.4.4. The power consumption of each device is 1.53 mW, 2.18 mW, 2.84 mW and 3.50 mW (6, 8, 10 and 12 μm) which means more power is needed to achieve the same performance as the narrower gauge has. This also aligns with the analytical model. Therefore, narrower Pirani gauges are more power-efficient comparing to wider gauges.

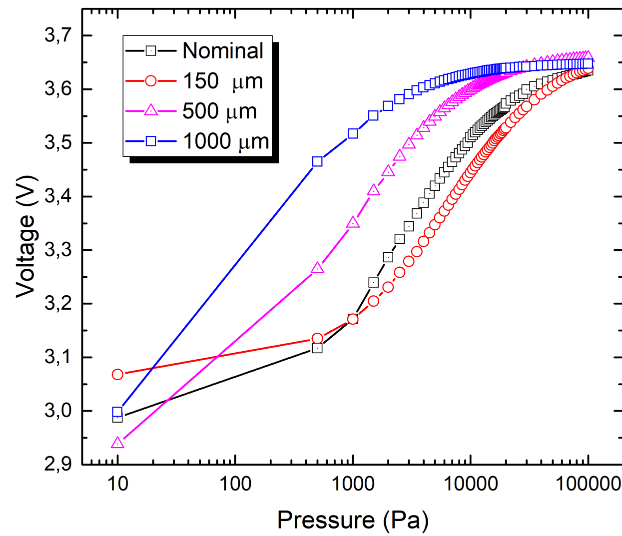


Figure 5.5: The output voltage versus pressure for devices with a length of 150 μm, 500 μm, 1000 μm and nominal length.

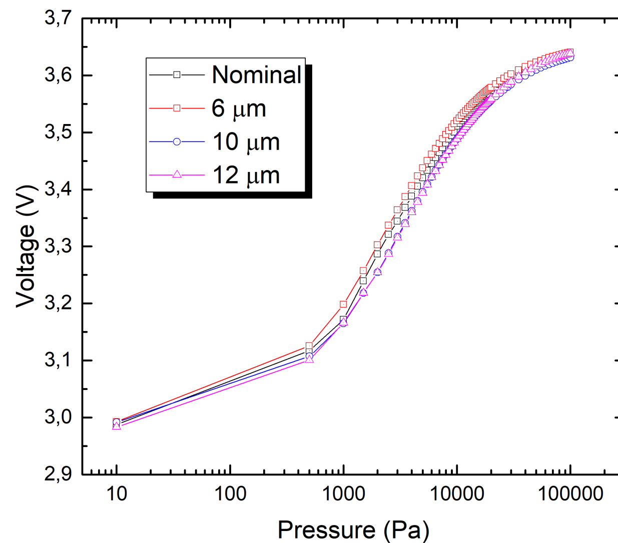


Figure 5.6: The output voltage versus pressure for devices with a width of 6 μm, 10 μm, 12 μm and a nominal width.

The Pirani gauges with 500 nm, 1000 nm and 2000 nm gap sizes were tested. Except for gap sizes, the other geometrical parameters were kept the same with the nominal device. The Pirani gauge with different gap sizes was fabricated on three different wafers. Although the SiC was deposited at the same time, the initial resistance of the heaters at the room temperature was different due

to the non-uniformity of the deposition between wafers. Therefore, unlike the simulation where input currents are the same, the bias current for each device was adjusted to acquire the same output voltage at 1 bar in the experiments. The experimental results are plotted in the Figure 5.7. From the plot, the device with a smaller gap demonstrates a slightly larger output voltage change. At the high-pressure regime, the slope of the device with a smaller gap is larger, indicating a larger sensitivity. Also, the curve of the device with a smaller gap tends to saturate at a higher pressure. The maximum sensitivity for each case is still at the lowest pressure point, which is 0.224 mV/Pa (0.5 μm), 0.271 mV/Pa (1 μm) and 0.263 mV/Pa (2 μm). As a result, the variation of gap size does not affect too much on the performance at lower vacuum side. It is proved by experiments that the gap distance will extend the higher detection limit of the Pirani gauge.

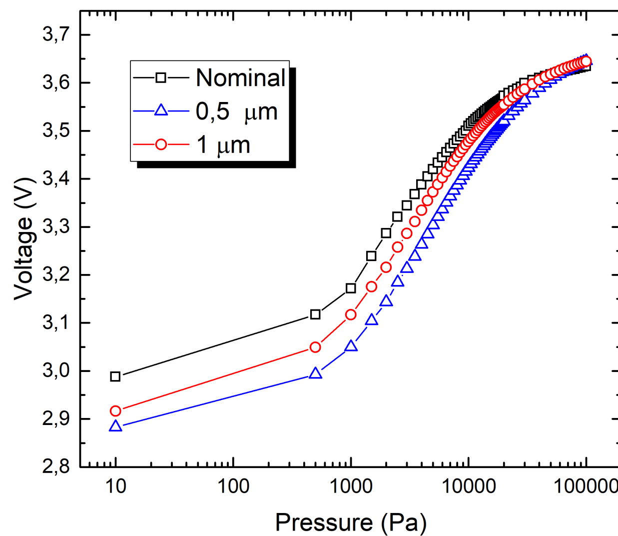


Figure 5.7: The output voltage versus pressure for devices with a gap size of 0.5 μm, 1.0 μm, 2.0 μm.

The main attributes of Pirani gauges with different dimensions are listed in Table 5.1, Table 5.2 and Table 5.3. Due to the capability of our measurement setup, we can not calibrate the gauge below 10 Pa. In spite of this, we can see that none of the gauges reaches saturation at 10 Pa. Therefore, the P_L is at least 10 Pa for all the gauges. According to the experiments, We can draw a similar conclusion as in the Section 3.4.7. First of all, increasing the length gives better sensitivity at the lower-pressure regime, but it sacrifices the sensitivity at the high-pressure regime. Width variation does not have too much impact on the performance, but wider Pirani gauges are less power efficient due to more heat loss through anchors and gas conduction. In terms of gap distance, smaller gap size makes the gauge more sensitive at the high-pressure regime, without affecting the per-

formance at the lower pressure range. Therefore, the gap distance should be made as small as possible.

Table 5.1: The main attributes of fabricated Pirani gauges with different lengths

Length	Initial Resistance (Ω)	Bias Current (μA)	Max. Sensitivity (mV/Pa)	Max. Power Dissipated (mW)	P_L (Pa)	P_H (Pa)
150 μm	3483.6	1043.5	0.137	3.80	< 10	99878
250 μm	6061.5	600.0	0.264	2.18	< 10	99816
500 μm	12508.8	290.9	0.666	1.06	< 10	99264
1000 μm	24919.6	148.4	0.953	0.54	< 10	97058

Table 5.2: The main attributes of fabricated Pirani gauges with different widths

Width	Initial Resistance (Ω)	Bias Current (μA)	Max. Sensitivity (mV/Pa)	Max. Power Dissipated (mW)	P_L (Pa)	P_H (Pa)
6 μm	8583.4	423.7	0.271	1.54	< 10	99742
8 μm	6061.5	600.0	0.264	2.18	< 10	99816
10 μm	4650.9	782.0	0.236	2.84	< 10	99788
12 μm	3769.7	964.7	0.239	3.51	< 10	99796

Table 5.3: The main attributes of fabricated Pirani gauges with different gap sizes

Gap size	Initial Resistance (Ω)	Bias Current (μA)	Max. Sensitivity (mV/Pa)	Max. Power Dissipated (mW)	P_L (Pa)	P_H (Pa)
0.5 μm	4277.6	849.9	0.224	3.10	< 10	99884
1.0 μm	6286.0	579.6	0.271	2.12	< 10	99834
2.0 μm	6061.5	600.0	0.264	2.18	< 10	99816

5.2.3 High Temperature Characterization

For high-temperature calibrations, an external heat source, i.e. the hotplate on the MPS, was used to heat the Pirani gauge. The heat source simulates the situation where the Pirani gauge works in a high-temperature environment. The longest Pirani gauge (1000 μm) was used for the high-temperature test because it is more likely to observe a reliability issue from long beams. For each measurement, the temperature increased with a step of 50 °C. The Pirani gauge with Al metal layer was tested first, and the maximum temperature of the measurement was 500 °C because the melting of Al is a concern when the temperature is higher than 500 °C.The calibration curves are plotted in Figure 5.8a. As the temperature increases, the output change decreases, which could result from the decrease of the TCR due to the rising temperature. Therefore, the maximum sensitivity reduces from 1.156 mV/Pa (5.626 Ω/Pa) at the room temperature to 0.489 mV/Pa (1.405 Ω/Pa) at 500 °C. Despite this, the Pirani gauge shows a successful operation up to 500 °C, and this working temperature is compatible with the operation temperature range of most SiC-based ICs reported in the literature [10, 11, 12, 13, 14].

In order to examine the functionality of our Pirani gauges at even higher temperatures, the Pirani gauge with Ti electrodes was calibrated at 550 °C, 650 °C and

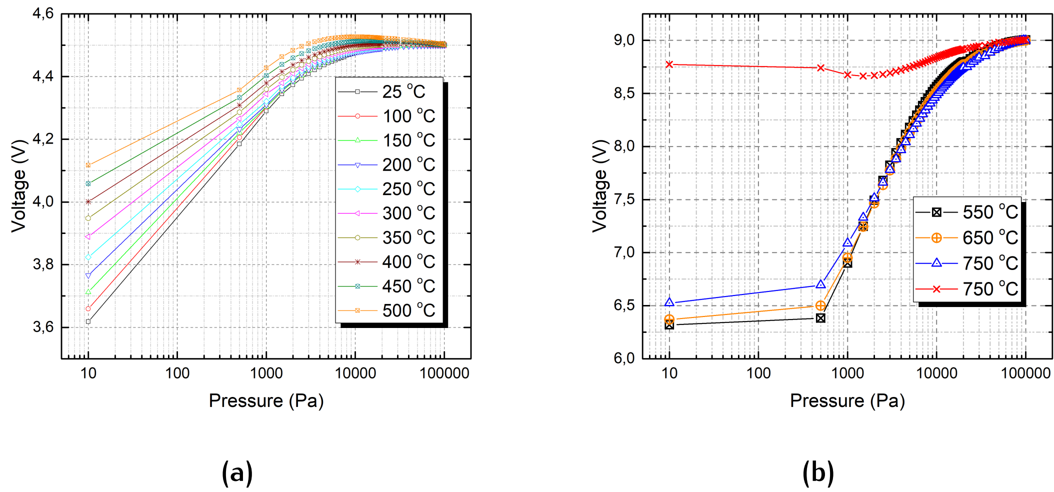


Figure 5.8: (a) Calibration curves of a 1000 μm Pirani gauge (with an Al metal layer) from the room temperature to 500 °C; (b) Calibration curves of a 1000 μm Pirani gauge (with a Ti metal layer) from 550 °C to 750°C. The red curve shows an example of resistive increase occurred at some gauges at a low pressure.

Table 5.4: The main attributes of fabricated Pirani working at different temperatures

Temperature (°C)	Initial Resistance (Ω)	Bias Current (μA)	Max. Sensitivity (mV/Pa)	Max. Power Dissipated (mW)	P_L (Pa)	P_H (Pa)
25	24589.7	183.0	1.156	0.82	< 10	68465
100	21917.8	205.5	1.116	0.93	< 10	78864
150	20410.9	220.5	1.039	0.99	< 10	87727
200	19032.2	236.4	0.951	1.06	< 10	64242
250	17788.9	253.0	0.827	1.14	< 10	53958
300	16638.9	270.4	0.769	1.22	< 10	44138
350	15601.5	288.5	0.690	1.30	< 10	32549
400	14652.9	307.1	0.637	1.38	< 10	27230
450	13763.0	327.0	0.559	1.47	< 10	13587
500	12943.8	347.7	0.490	1.57	< 10	9667
550	17082.3	527.0	1.036	4.74	< 10	94957
650	16174.7	556.7	0.900	5.01	< 10	96428
750	12556.4	717.1	0.787	6.45	< 10	99788

750 °C. The calibration curves are shown in Figure 5.8b. Under higher temperatures, the gauge shows a good response to the pressure change. The maximum sensitivity lies between 500 Pa and 1000 Pa, which is 1.035 mV/Pa (1.964 Ω/Pa) at 550 °C, 0.902 mV/Pa (1.621 Ω/Pa) at 650 °C, and 0.787 mV/Pa (1.097 Ω/Pa) at 750 °C. The overall sensitivity of the gauge has a slight decrease at a higher temperature. However, during the calibration, we found some of the gauges had a resistance increase at a very low pressure, which is indicated by the red curve in Figure 5.8b. Figure 5.9a demonstrates this behavior in a timescale. As can be seen from Figure 5.9a, when the pressure is above 1000 Pa, the resistance reduces with decreasing pressure as expected. When the pressure further decreases, the resistance will first have a rapid decrease and will then go to a larger resistance

than before.

A possible reason is that the TCR of SiC turns from negative to positive at very low pressure. In the semiconductor, two mechanisms are affecting the electrical conductivity of a semiconductor material (σ), which can be expressed as:

$$\sigma = \mu_n n + \mu_p p \tag{5.1}$$

where μ_n and μ_p are the mobility of electrons and holes. n and p are the concentration of electrons and holes. As the temperature increases, more charge carriers will be activated and are available for conduction (larger n and p), which is the reason why SiC has a negative TCR. However, a higher temperature also will cause more scattering, which impedes the movement of charge carriers (lower μ_n and μ_p). At very low pressure, the heat transfer rate from the heater to the beam is so low that the temperature increases dramatically. At a certain point, the scattering effect becomes dominating, and the TCR of the SiC turns from negative to positive. Therefore, the resistance increases along with the temperature until the system reaches a new thermal equilibrium. In order to verify if this behavior is TCR-related, the TCR of SiC was measured with test structures from the room temperature to 750 °C (maximum temperature of the setup), as shown in Figure 5.9b. But from the results, although the absolute value of TCR is decreasing (from 1533.4 ppm/°C to 740.0 ppm/°C), it remains negative until 750 °C. We can only infer that it might become positive at a higher temperature. From the TCR measurement result, we can also calculate that the average temperature of the previously calibrated gauge is around 1123.3 °C when it operates at the lowest pressure, which means the TCR is still negative at this temperature.

Another possible explanation is that a thermally-induced buckling occurs due to the rising temperature of the heater at very low pressure. The buckling makes the heater contact the Si substrate, which creates a thermal shortcut. This makes the heater lose more heat to the substrate through the thermal conduction, and the temperature of the heater will drop down. Eventually, the temperature drop will cause the increase of the output voltage. However, we can not verify this possibility because we did not find suitable equipment to observe the out-of-plane buckling.

5.2.4 Time Response

After a pressure change, the sensor output will not jump to a new value immediately. The vacuum gauge will reach a new stable state over a period of time, which is call response time. A shorter response time allows the gauge to give a reliable output when it operates in an environment where the pressure changes with a high frequency. Figure 5.10a shows the output of a gauge versus time

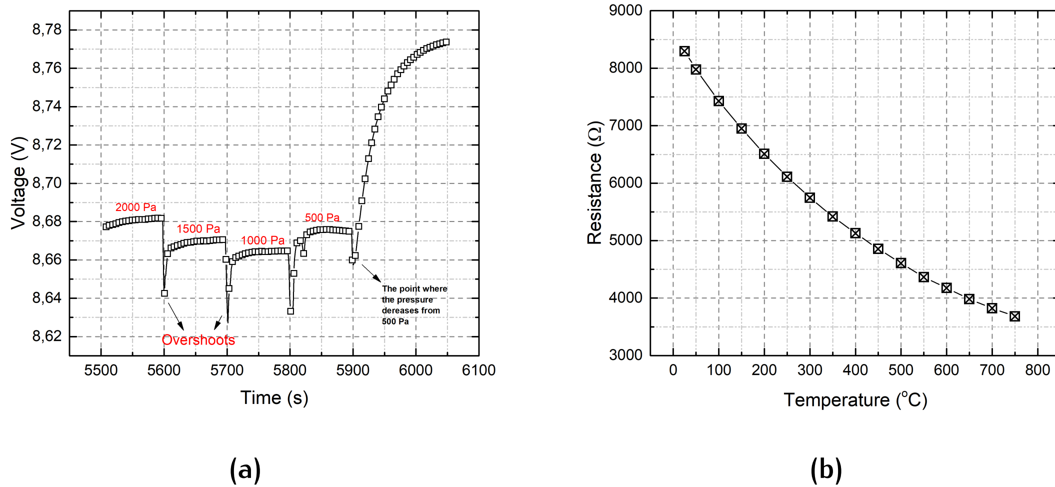


Figure 5.9: (a) The resistance increase behavior in a timescale; (b) The TCR measurement of the SiC from the room temperature to 750 °C

at different temperatures. In order to minimize the error brought by the venting process, we only increased the pressure from 5000 Pa to 20000 Pa. From the figure, the output experiences a sudden increase after the pressure change. After reaching a maximum point, it finally reduces to a settled value. The time response of the vacuum gauge does not show an obvious dependency upon the temperature. Figure 5.10b demonstrates the settling behavior of the device at 700 °C. The gauge takes around 3 seconds to change from the previous state to a tolerance band (usually ± 5 %) of the new steady state.

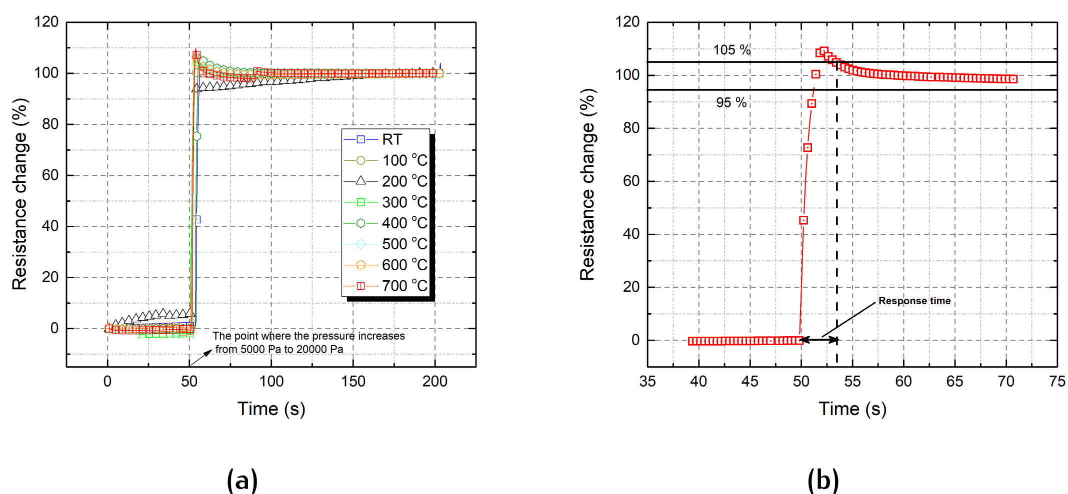


Figure 5.10: (a) Output versus time at different temperatures; (b) Response time of the vacuum gauge at 700 °C.)

5.3 METAL-SIC CONTACT PROPERTY

As we have already stated in Section 3.4.8, Ti and Al should form an ohmic contact with the SiC at the room temperature because of the low Schottky barrier height. However, as the temperature increases to a higher temperature, a reaction between the metal and SiC is more likely to happen, which will induce a formation of carbides, silicides, oxides and/or free carbon generation at the junction interface[57, 58]. Therefore, the degradation at the junction might cause a resistance increase.

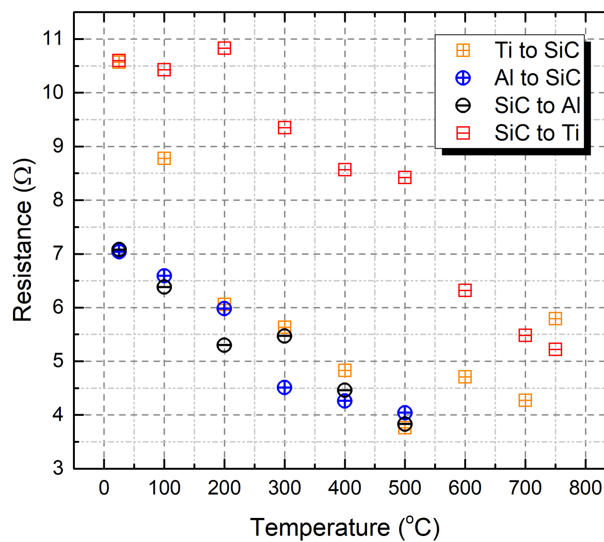


Figure 5.11: Contact resistance measurement. The test temperature for SiC/Al went to up 500 °C. As for SiC/Ti contact, the measurement was done at a temperature up to 750 °C

To investigate the electrical property of metal-SiC junction with respect to temperature, we measured the contact resistance of SiC/Al and SiC/Ti junctions by using Kelvin test structures. During the measurement, one mA constant current was injected from either SiC side or metal side to verify if the junction has a rectifying behavior. The measurement results are given in Figure 5.11. The Al/SiC contact shows relatively good ohmic behavior until 500 °C. As for the Ti/SiC contact, it does not show an idea ohmic behavior. The contact resistance shows a clear difference (except for the room temperature) when it is biased from different directions, which indicates that it has a certain extent of rectifying behavior. The annealing recipe after Ti metallization should be optimized to obtain a better ohmic contact in the future. Nevertheless, the contact resistance is almost negligible compared to the resistance of Pirani gauge. The area of contact opening in test structure is 60 $times$ 60 μm^2, so the Ti/SiC junction obtains the

maximum contact resistivity at 200 (°C) (0.0031 $\Omega/\mu m^2$). Generally, the contact resistance has a tendency to decrease at higher temperatures. Despite the fact that no significant degradation of the metal-semiconductor had occurred during the measurement, tests are still needed to examine the long-term reliability of the junction in the future.

5.4 CONCLUSION

A dedicated measurement setup was built to characterize the performance of the vacuum gauge at different temperatures. The nominal device was calibrated at room temperature to examine the basic functionality of our micro-fabricated Pirani gauge. The nominal gauge showed a maximum resistance change of 17.8 % when it is biased at a current of 600 μA. By comparing the experimental result with the analytical model, we found that the original analytical model is able to predict the trend performance of the Pirani gauge. However, the analytical model does not quantitatively match the experimental result. This could be the incorrect material properties used in model or incorrect assumption made during the derivation. A close match can be obtained through tuning the thermal conductivity of SiC used in the model. The vacuum gauge was measured at both room temperature and an elevated temperature up to 750 °C. For 1000 μm gauges with Al metal layer, it showed a successful operation at 500 °C. For temperature higher than 500 °C, devices with a Ti metal layer were used for the calibration. The Pirani gauge operated successfully at a temperature up to 750 °C, and the largest sensitivity of 0.787 mV/Pa (1.097 Ω/Pa) was obtained at this temperature. However, for some gauges, an abnormal resistance increase was observed at very low pressure. The possible reasons could be TCR change and/or thermally-induced buckling. The metal/SiC junctions were characterized by Kelvin test structures. Al/SiC junction showed an non-rectifying behavior from the room temperature to 500 °C. Ti/SiC showed a certain degree of rectifying behavior when it is higher than the room temperature. But the rectifying behavior does not have too much negative impact upon the operation of the gauge, because the contact resistance is so small that it can be neglected.

Although the gauge is able to work up to 750 °C, the long-term stability of the device under a high-temperature environment is not tested. The average time for each device put in the high-temperature environment is around 5 to 6 hours. A complete reliability test should be conducted in the future.

6 CONCLUSION AND FUTURE WORK

This chapter will quickly review the work has been done in previous chapters. Then, several recommendations for the future work will be given.

6.1 CONCLUSION

This work focused on the realization of the micro-fabricated high-temperature vacuum gauge due to the growing demand for vacuum monitoring in a high-temperature environment. As one of the leading candidates for high-temperature applications, the LPCVD poly-SiC was proposed to be the construction and sensing material for the vacuum gauge. Compared with traditional sensing material, such as Si, SiC retains its excellent properties at an elevated temperature. Furthermore, SiC-based sensor can be integrated with SiC electronics to achieve the high-temperature compatible "smart sensor". The sensor configuration was based on the micro-bridge structure. The analytical model of the micro-bridge structure was derived based on previous research. With this model, effects brought by geometrical parameters, such as length, width and gap size of the gauge, were studied by calculations. Generally speaking, the gauge should be made long enough to allow a lower pressure to be measured, and the suspended heater should be as close as possible to the substrate to obtain a good sensitivity at the high-pressure side. However, this design rule does not lead us to a mechanically stable design, especially at a high temperature. Therefore, multiple geometries were designed for the suspended heater to make trade-offs between dynamic range and mechanical stability.

The fabrication of Pirani gauges, together with test structures is a four mask process. The whole process was contamination-free and achieved the ability of mass production, which is crucial for the integration with CMOS readout electronics in the later stage. The fabrication process of the Pirani gauge involves many SiC processing techniques. The deposition of poly-SiC was conducted with F3 furnace in the Class 10000. By controlling the deposition time, 2 μm thick SiC layers were successfully deposited. However, the uniformity for the electrical property of the deposited layer is a problem. Laser ablation and plasma etching were tried to etch the SiC layer. Compared with the laser ablation, plasma etching has an advantage in term of accurate process control, because it has a much lower etching rate (164.1 nm/min) than laser ablation. In order to avoid the stiction,

the micro-bridge structure was finally released with the help of vapour HF. The longest Pirani gauge we fabricated is 1000 μm, and no in-plane and out-of-plane deflection could be observed after the releasing process.

The device characterization was carried out with a dedicated measurement setup for the pressure calibration at an elevated temperature. This setup can reach a temperature of 750 °C, and this was the maximum temperature for our measurement. First of all, devices with different dimensions were calibrated to verify the effect of different geometrical parameters by experiments. As for the nominal gauge, it showed a maximum resistance change of 17.8 % with a bias current of 600 μA. However, the result matches the theoretical model qualitatively but not quantitatively. A closer match can be obtained by tuning material inputs of SiC. The gauge was also measured in different temperatures. The gauge successfully operated at 750 °C, and it has the potential to work at an even higher temperature. For some of the gauges, a resistance increase behavior can be observed while the gauge is working at very low pressure. This effect needs to be further investigated though several possible reasons were given. Although the metal/SiC junction we fabricated is not ideally ohmic, it does not affect the operation of Pirani gauges, because the contact resistance is much lower than the resistance of heaters.

6.2 FUTURE WORK

In this thesis, there are several problems remain unsolved, which should be first addressed in future work. First of all, the LPCVD SiC deposition recipe does not give repeatable deposition results. This makes it difficult to make an accurate prediction of device performance in the design phase. Secondly, the resistance increase behavior described in Section 5.2.3 deserves to be further investigated. Thirdly, an ideal ohmic contact is still desired only for the Pirani gauge itself but also for the SiC IC to be achieved in the future. The contact resistivity we obtained is relatively large compared with the literature [9]. It is reported that Ti can form a good ohmic contact with SiC [58, 59], but we failed to obtain a Ti/SiC with an ideal ohmic behavior in our work. It is suggested to optimize the annealing recipe after metallization. In addition to a single layer, ohmic contacts with multiple layers are also worth investigating [58].

In the next stage, we also need to consider the monolithic integration between CMOS readout electronics and fabricated Pirani gauge. A proposed process flow is illustrated in Figure 6.1. After the fabrication of the CMOS circuitry part, a sacrificial layer (SiO_2) is deposited on the whole wafer. Then, SiC and metal layers are patterned to form micro-bridge structures and metal lines, respectively. Before releasing step, the circuit part should be masked to prevent the electrical

isolation layer being etched away.

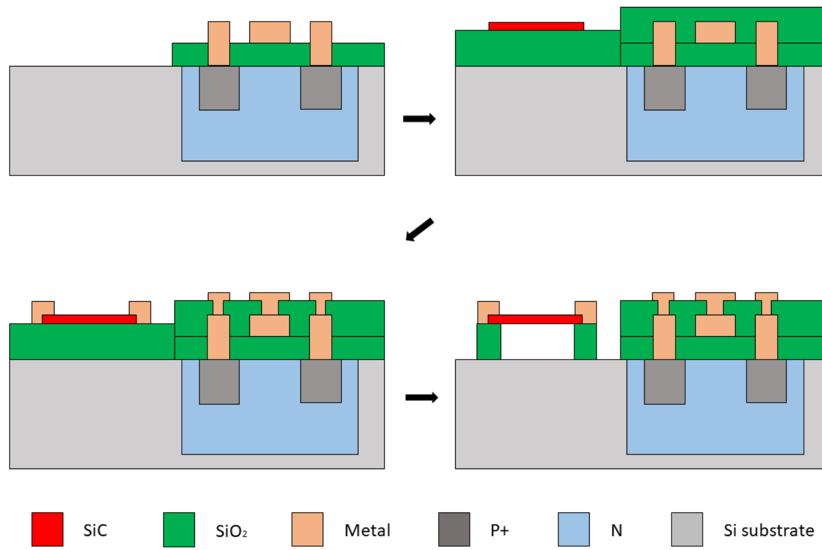


Figure 6.1: An illustration of process steps for integrating the Pirani gauge with a CMOS circuitry.

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A IMPORTANT FIGURES

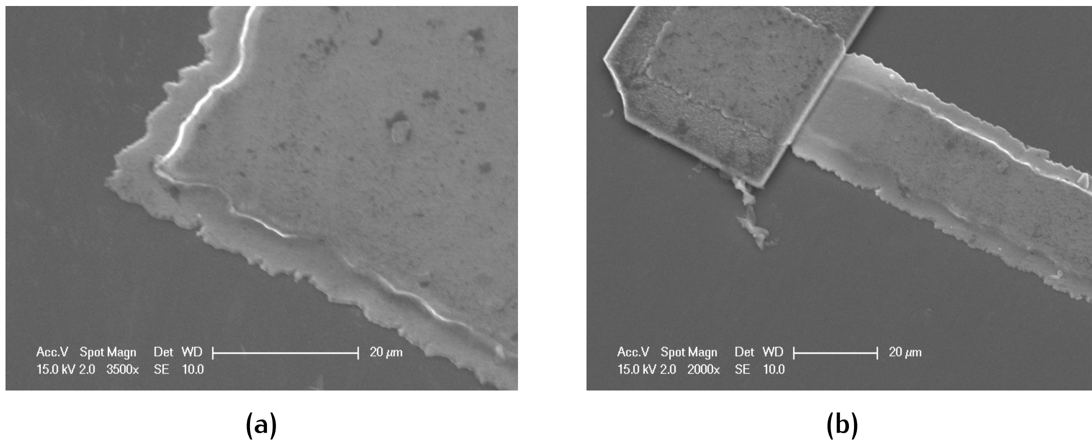


Figure A.1: The isolation layer experienced an over-etch because of the isotropic etching process. The figure shows the metal layer has a physical contact with substrate due to insufficient support from the isolation layer,

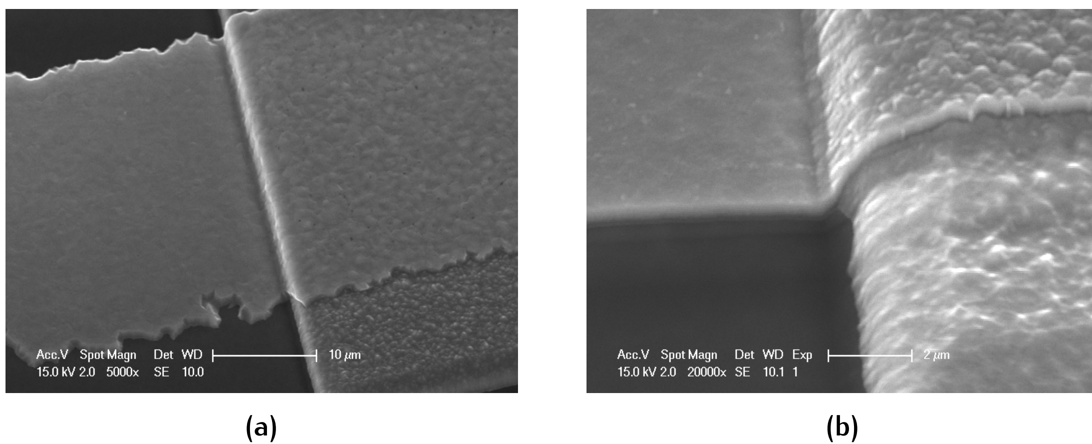


Figure A.2: Al (a) and Ti (b) shows a good step coverage to the SiC measa.

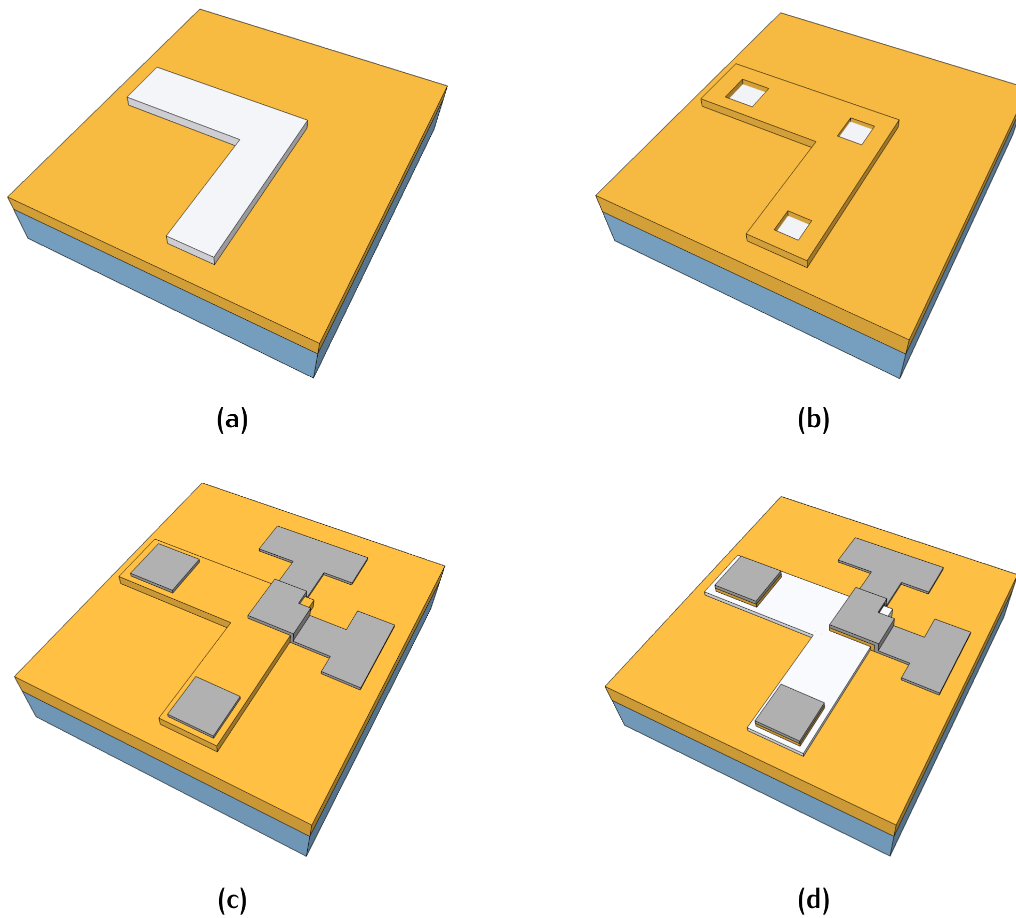


Figure A.3: First the SiC layer is deposited and patterned. Then, LPCVD TEOS oxide is conformably deposited and is then patterned to form the opening for metal-semiconductor contact. After this, metal layer is patterned by sputtering. The last step (vapor HF) is unnecessary for Kelvin test structure. However, since test structures are on the same die with Pirani gauges, test structures also have to experience a vapor HF with Pirani gauges.

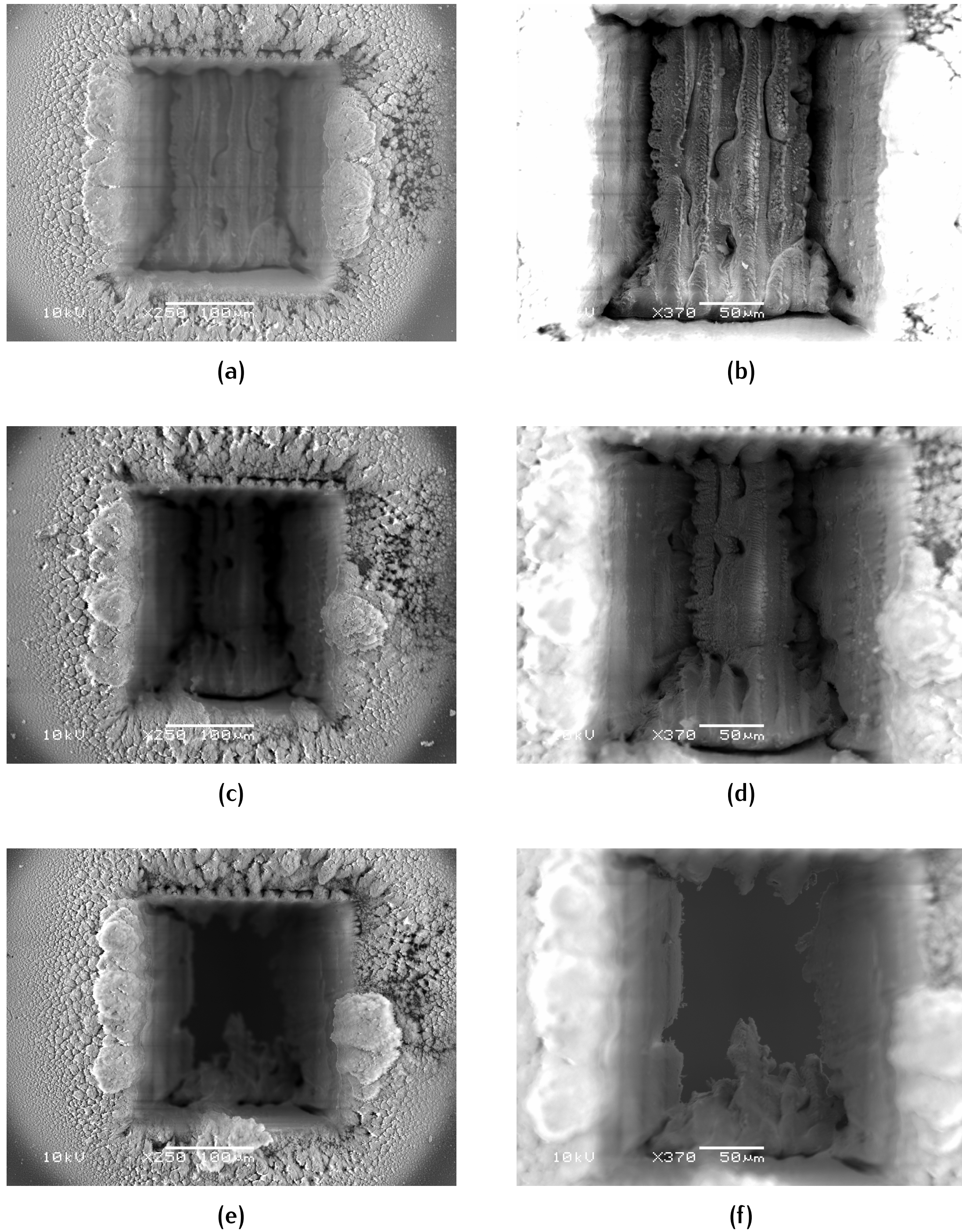
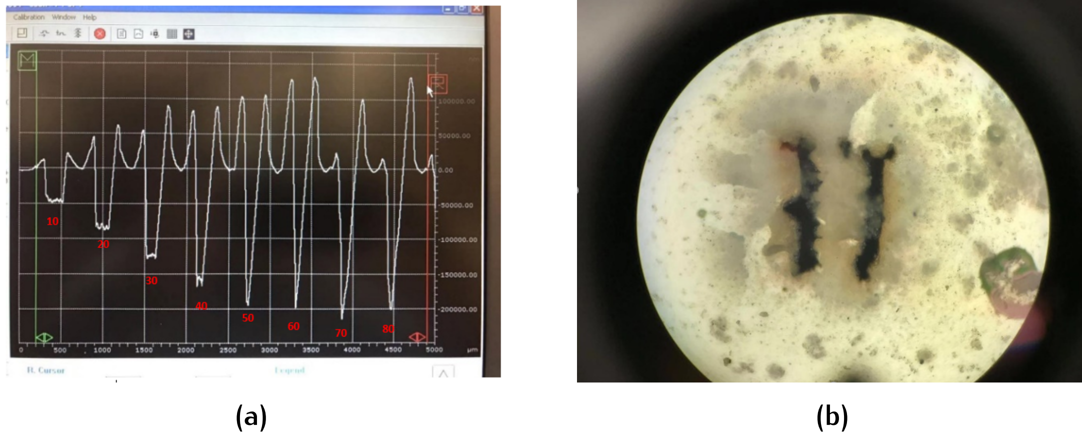


Figure A.4: Etching result of test structures with a (a) repetition objs of 50 (top surface); (b) repetition objs of 50 (bottom surface); (c) repetition objs of 70 (top surface); (d) repetition objs of 70 (bottom surface); (e) repetition objs of 100 (top surface); (f) repetition objs of 100 (bottom surface).



(a) (b)

Figure A.5: (a) The accurate depth information of each hole obtained by profile analyzer Dektak 8; (b) The backside of SiC wafer after being etched by 80 times.

Every 10 times etching will yield approximately 40 μm deep trench, and the etch rate keeps a linear relation with repetition objs up to 30 times. After that, etch rate per 10 repetition objs starts to have a slight decrease. As what can be seen from Figure A.5a, with the increasing repetition objs, the size of holes becomes smaller in the bottom region so the profile of holes becomes a sharp "V" shape eventually. Therefore the profile is too narrow for profile analyzer to obtain an accurate depth measurement. A clear evidence is that we can visually see from Figure A.5b, back side of the wafer was almost etched through when repetition ojbs is 80 times, however Dektak indicated only 200 μm is etched (SiC wafer is 360 um thick). As a result, only first five depth measurements which are considered to be accurate. The reason for "V" shape trench could be the re-deposition of substrate material. The deeper the hole, the more difficult for the debris to get out of the hole, which makes debris deposit locally on the sidewalls. This possibility is explained elaborately by Ampere A. Tseng et. al [70]. In their study, they attribute the cross-sectional difference to fluence and frequency of the laser. In their theory, the ablated material is transferred into ionized vapor or plasma and forms convection inside the hole, which helps to bring out melted material and debris. However, the lifetime of plasma or vapor state is short, therefore large energy is needed to keep them into gaseous state. As a result higher power and/or higher frequency is suggested to yield an U-shaped profile.

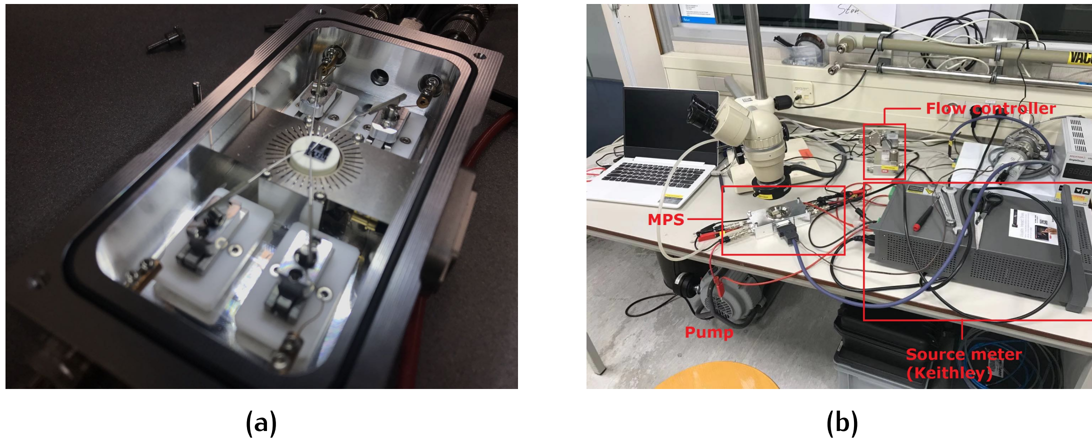


Figure A.6: Pictures of actual (a) MPS and (b) pressure setup.

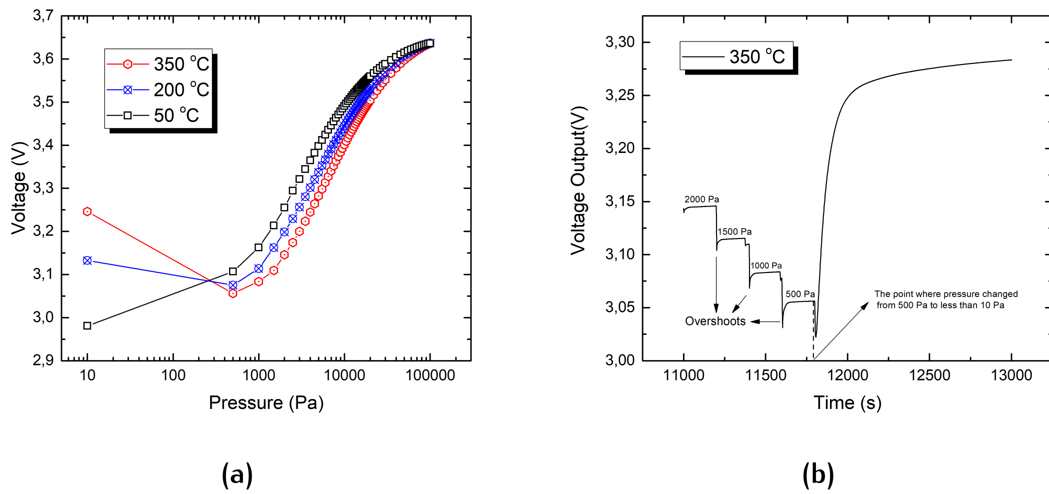
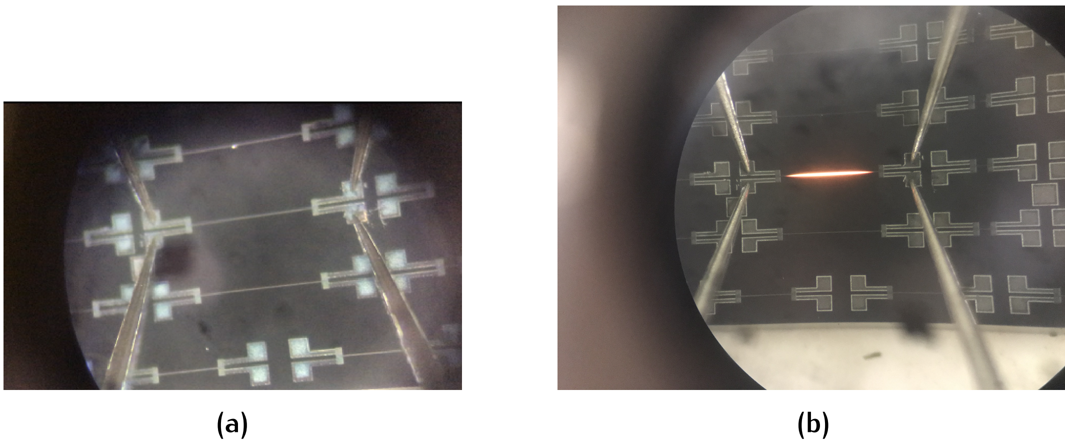


Figure A.7: (a) Calibration curves of the nominal device at 50 °C, 200 °C and 350 °C; (b) The time response of the nominal gauge when the pressure drops from 2000 Pa to less than 10 Pa.



(a) (b)

Figure A.8: Operation of a Pirani gauge at 750 °C when the pressure is at (a) 1 atm and (b) 10 Pa. At a low pressure, heat transfer rate is very low so temperature of the beam increases significantly.

B IMPORTANT TABLES

Table B.1: The raw data of sheet resistance of D1 poly-SiC layers measured during the fabrication

Measurement Point	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6
No.1	89.8	108.2	130.2	189.8	159.1	155.6
No.2	91.6	111.0	132.1	191.3	161.8	159.0
No.3	98.6	118.9	144.8	213.3	176.0	170.8
No.4	105.9	128.7	155.4	228.8	188.6	189.1
No.5	114.7	143.5	171.6	244.3	224.4	217.9
No.6	121.7	150.5	188.8	266.0	219.3	206.4
No.7	121.4	154.4	181.1	268.3	217.2	220.8
No.8	120.6	148.3	180.4	273.4	228.3	219.3
No.9	125.1	150.2	189.5	281.3	207.4	226.8
No.10	136.3	171.7	212.5	307.0	256.4	248.9
Average R_{sheet}	112.6	138.5	168.6	246.4	203.9	201.4
Standard Deviation	15.5	20.8	27.1	39.6	31.6	31.4

With the data in Table B.2, Table B.3 and Table B.4 given below, we can calculate the actual thickness of poly-SiC we have deposited, as shown in Table 4.1.

Table B.2: Thickness of TEOS layers during fabrication (unit: nm). Note: Point 5 is the nearest to the primary flat.

Measurement Point	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6
No.1	2033.72	1024.20	535.72	/	2002.63	/
No.2	2037.83	1030.39	541.11	/	2009.55	/
No.3	2055.35	1024.35	538.72	/	2028.25	/
No.4	2037.83	1031.15	543.09	/	2010.42	/
No.5	2047.31	1031.79	538.02	/	2019.93	/
Average thickness	2042.4	1030.37	539.24	1041.32	2014.16	1041.32

Table B.3: Thickness of remaining TEOS layers after SiC dry etching (unit: nm).

Measurement Point	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6
No.1	1844.39	857.95	402.14	867.52	1803.23	865.03
No.2	1877.94	896.49	442.27	906.19	1834.14	902.65
No.3	1819.55	819.09	358.69	833.46	1769.06	818.27
No.4	1851.56	852.56	405.65	867.79	1803.23	870.78
No.5	1923.65	935.03	477.40	931.53	1887.52	947.04
Average thickness	1863.42	872.22	417.23	880.9	1817.65	880.8

Table B.4: Total thickness of the poly-SiC layer and the TEOS layer that had been etched away (unit: nm).

Measurement Point	Wafer 1	Wafer 2	Wafer 3	Wafer 4	Wafer 5	Wafer 6
No.1	2124.24	2129.61	2157.57	2001.14	2204.53	2240.62
No.2	2167.24	2173.92	2218.35	2048.27	2266.91	2269.78
No.3	2172.85	2218.42	2249.55	2084.75	2290.39	2327.25
No.4	2207.64	2247.50	2242.53	2098.12	2270.97	2307.39
No.5	2221.94	2271.51	2227.71	2149.23	2278.46	2288.10
Average thickness	2179.38	2208.19	2219.14	2076.30	2253.65	2286.63

Table B.5: Laser settings for the laser ablation experiment

Laser Setting	Value
Speed	100
Jump Speed	200
Laser Firing Rate	50
Laser Power	100
Burst Power	1000
Repetitions	0
Repetitions Ojbs.	$10 \times n$

Table B.6: Detetailed vapor HF etch recipes.

Recipe	Pressure (torr)	HF (sccm)	EtOH	N_2	Regulator	Etch rate ($\dot{A}$/min)	Uniformity (%)
Recipe 1	125	190	210	1425	7.75	143	2.9%
Recipe 2	125	310	350	1250	7.75	473	5.2%
Recipe 3	125	525	400	1000	7.75	1086	3.4%
Recipe 4	125	600	400	910	7.75	1321	1.3%
Recipe 5	125	720	325	880	7.75	1599	1.3%

C MASK DESIGN

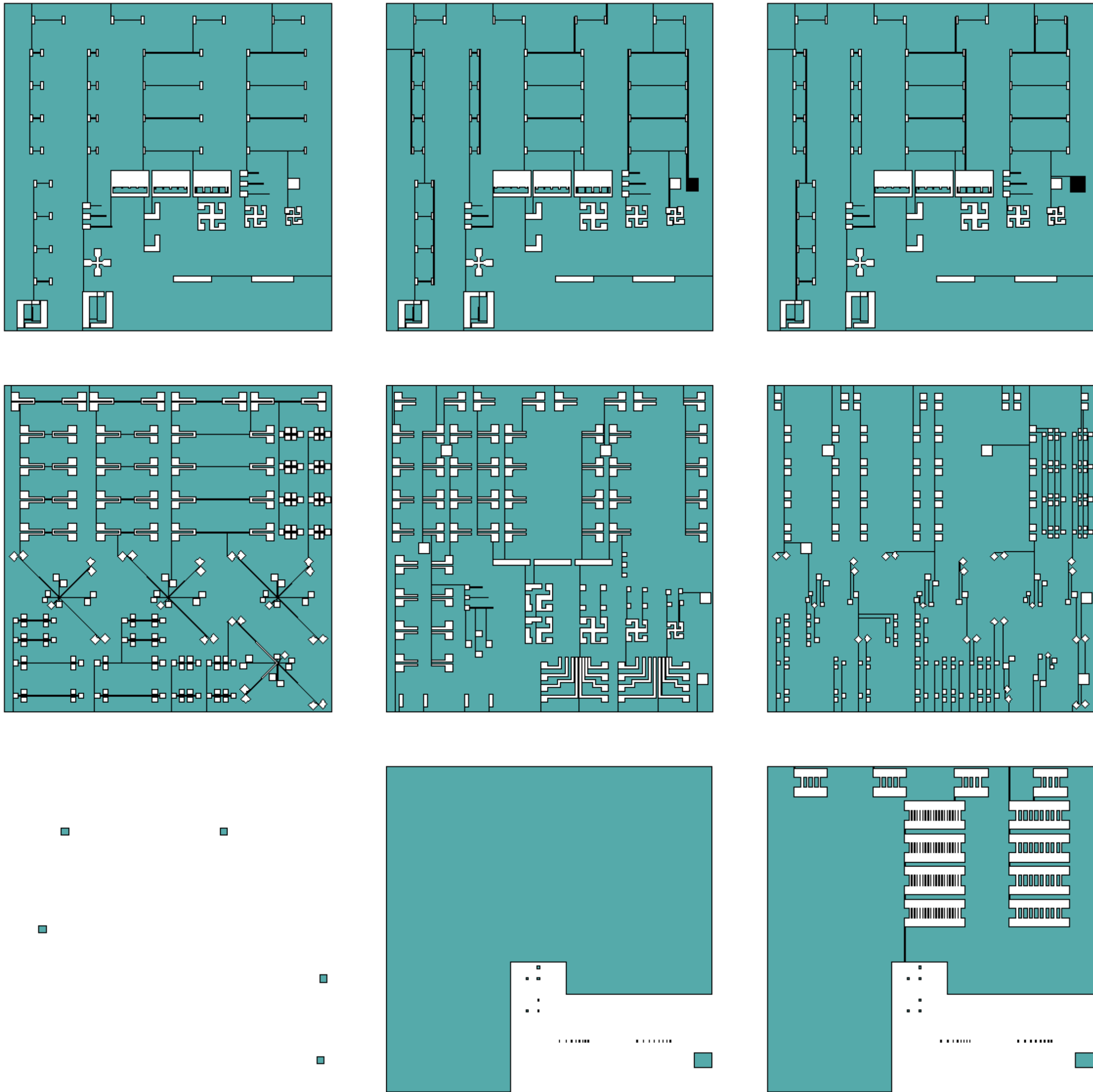


Figure C.1: A complete overview of the mask design. The colored area is bright field, and the rest is dark field.

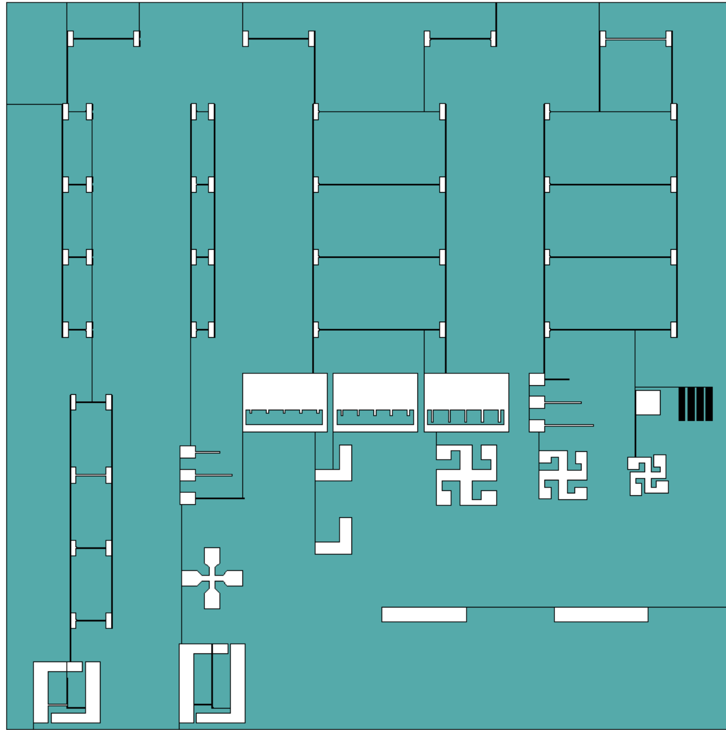


Figure C.2: Image 9: SiC layer with grayscale patterns (400 nm of pitch size). Note: The grayscale pattern is designed to overcome the potential step coverage issue during metal sputtering.

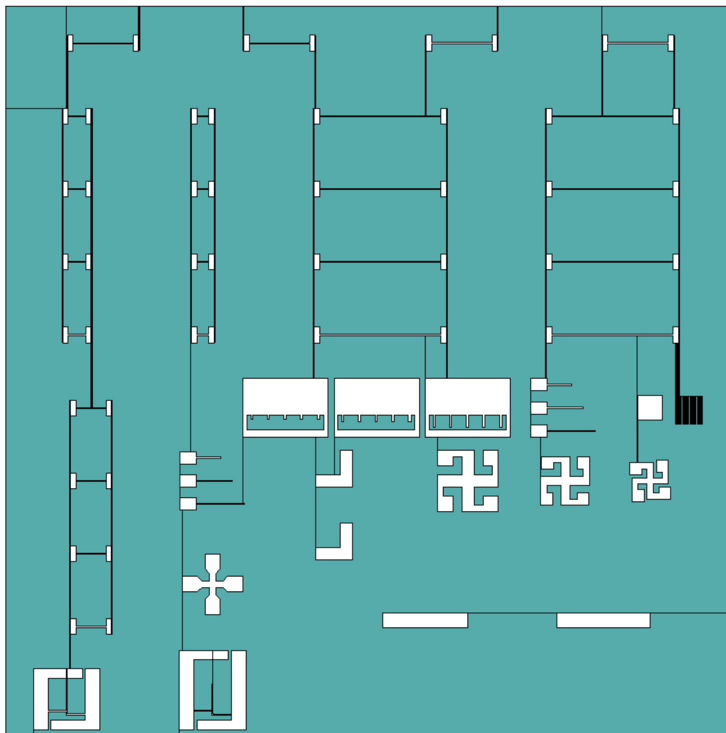


Figure C.3: Image 8: SiC layer with grayscale patterns (500 nm of pitch size).

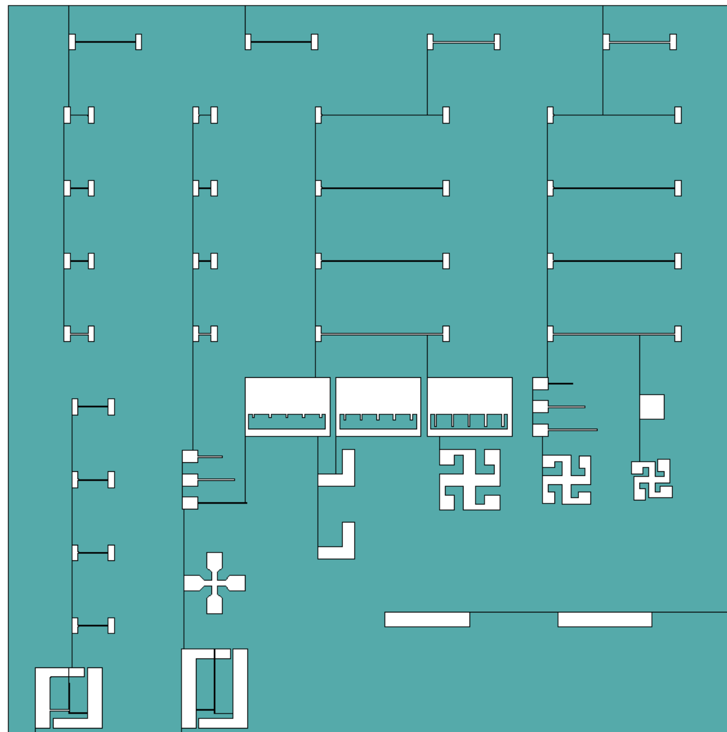


Figure C.4: Image 7: SiC layer without grayscale patterns. This image was used in our fabrication mainly.

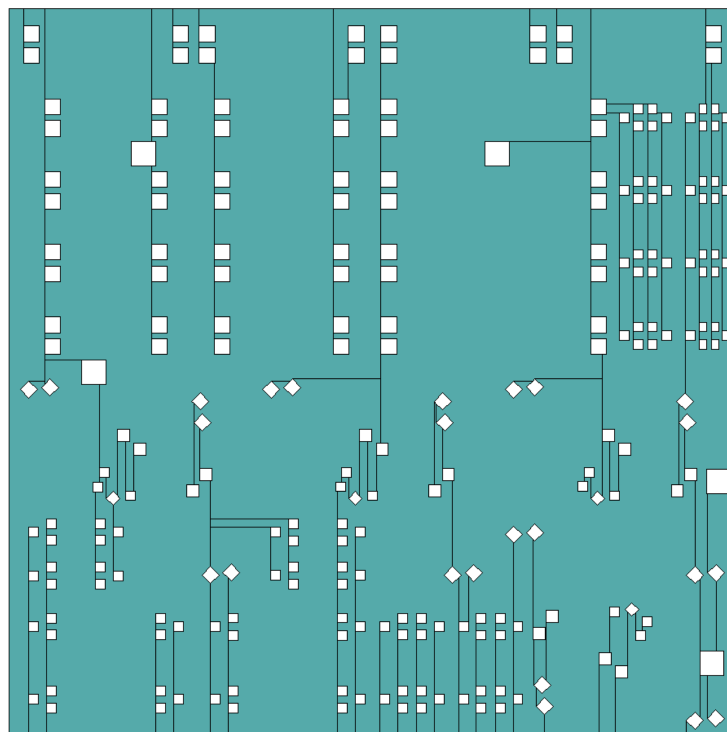


Figure C.5: Image 6: Metal layer patterns for backup designs of the Pirani gauge.

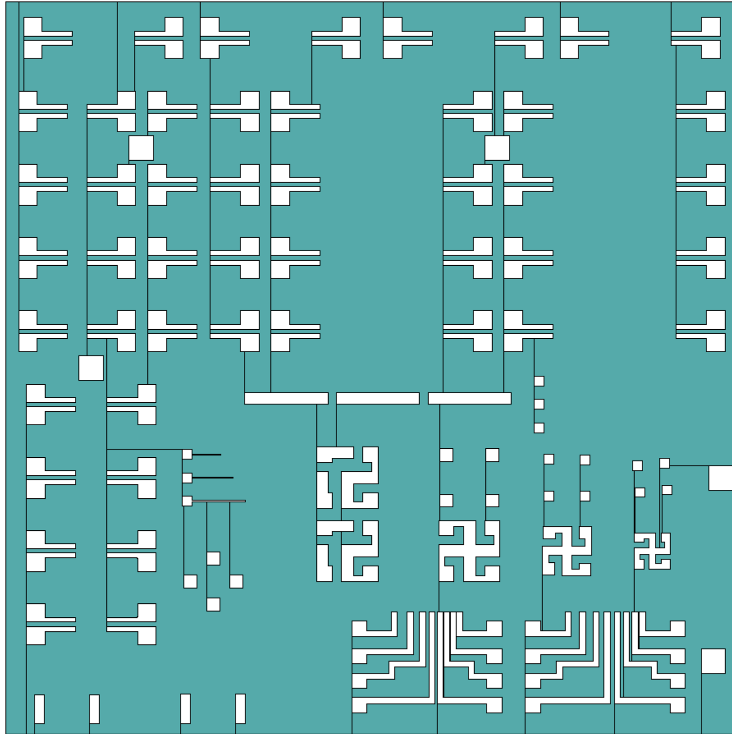


Figure C.6: Image 5: Metal layer patterns.

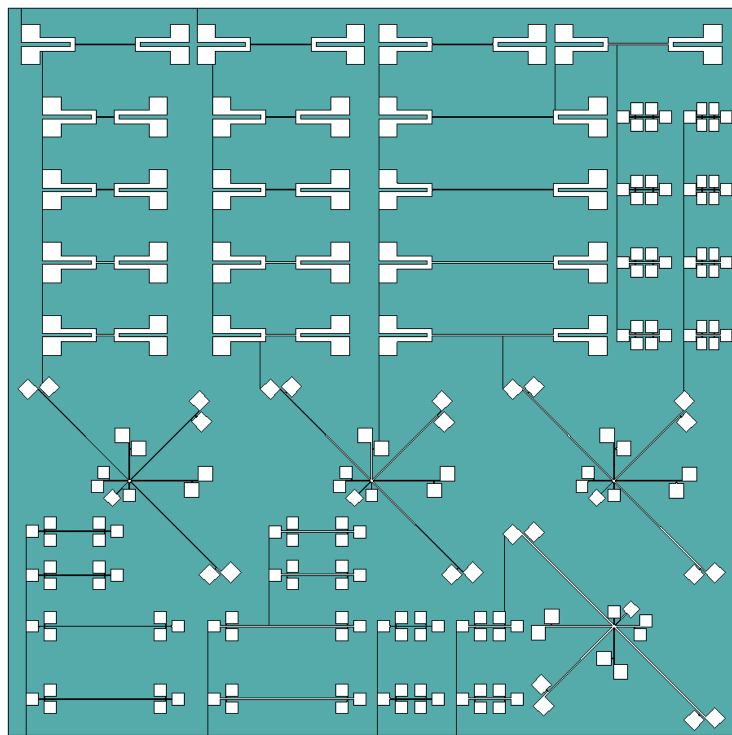


Figure C.7: Image 4: Backup designs for the Pirani gauge.

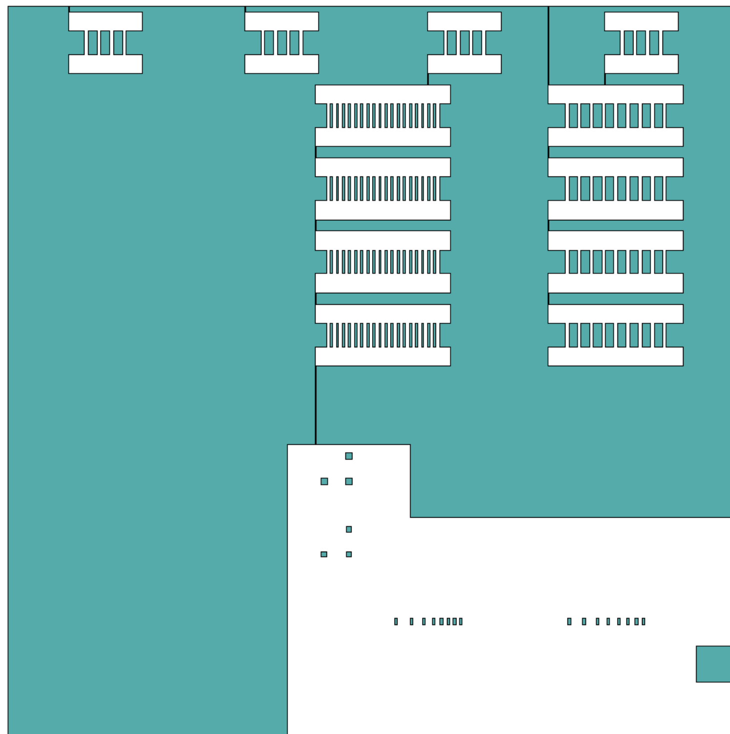


Figure C.8: Image 3: Contact openings for test structures as well as supporting structures for suspended heaters.

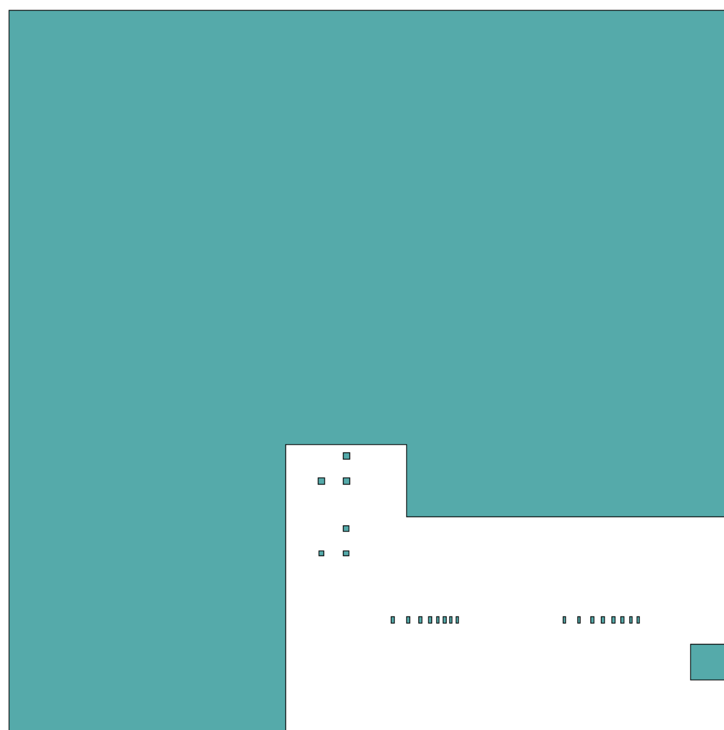


Figure C.9: Image 2: Contact openings for test structures.

Figure C.10: Image 1: Ground connections to avoid possible parasitic effects with the substrate.

D CODE

Keithley Script for the fou-probe measurement:

```
ON      = 1
OFF = 0

local v_cmpl = 20
local data_interval = 6

smua.reset()

smua.source.func = smua.OUTPUT_DCAMPS
-- smua.source.outputenableaction =
smua.measure.nplc = 10
smua.source.limitv = v_cmpl
--smua.source.rangev = v_cmpl
--smua.measure.autorangev = smua.AUTORANGE_ON
--smua.measure.autorangei = smua.AUTORANGE_ON
--smua.source.limiti = 0.5
-- smua.source.rangei = 0.1 -- *
smua.sense = smua.SENSE_REMOTE
--smua.measure.rangev = 0.1

--beeper.beep(0.5,500)

smua.source.output = ON

timer.reset()

i = 600e-6
smua.source.leveli = i
smua.source.rangei = 600E-6
NUM = data_interval
print("Time", "I1", "V1", "Res1")
repeat
        Ia, Va = smua.measure.iv()
        Res_a = Va/Ia
        if NUM == data_interval then
                        time = timer.measure.t()
                        print(time, Ia, Va, Res_a)

                        display.clear()
                        display.setcursor(1,1)
                        display.settext("R:"..string.sub(tostring(Res_a),1,9))
                        display.setcursor(2,1)
                        display.settext("Elapsed time: "..time.." s")
                        NUM = 1
        end
        NUM = NUM + 1
        keyCode = display.getlastkey()
        --until (time > 5)
until (keyCode == display.KEY_RUN)
smua.source.output      = smua.OUTPUT_OFF
```

E COMPLETE FLOWCHART

Run number: EC2358
Contamination: None

1. Cleaning

Clean 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench "HNO3 99% (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Clean 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench "HNO3 69,5% 110 °C (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

2. Coating

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas;
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump;
- a soft bake at 95 °C for 90 seconds;
- an automatic edge bead removal with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating and follow the instructions for this equipment.

Use program "Co - 3012 - zero layer". There will be a larger edge bead removal.

3. Exposure

Expose masks COMURK, with job "ZEFWAM" and the correct exposure energy 125 mJ. This results in alignment markers for the stepper and contact aligner.

4. Developing

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bakes at 115 °C for 90 seconds;
- developing with Shipley MF322 with a single puddle process;
- a hard bake at 100 °C for 90 seconds.

Use program "1 - Dev - SP".

5. Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope and check the line width and overlay. No resist residues are allowed.

6. Wafer numbering

Use quartz pen to mark developed wafers in the blank area.

7. Plasma etching: Alignment markers (URK's) in Silicon

Use the Trikon Omega 201 plasma etcher. Follow the operating instructions from the manual when using this machine. It is not allowed to change the process conditions and times from the etch recipe!

Use sequence "URK_NPD" (with a platen temperature of 20 °C to etch 120 nm deep ASM URK's into the Si.

8. Layer stripping: Photoresist

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier.

Use program 1: 1000 watts power and automatic endpoint detection + 2 min over etching.

9. Cleaning

Clean 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench "HNO3 99% (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Clean 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench "HNO3 69,5% 110 °C (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

10. LPCVD silicon nitride deposition 300 nm: Electrical isolation layer

Use the LPCVD furnace E2 to deposit silicon nitride. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!

Use recipe "4INCHST" with a proper deposition time to deposit a 300 nm thick nitride layer.

11. Measurement: Thickness of Nitride

Use the Leitz MPV-SP measurement system for layer thickness measurement.

Use program: #33

12. Dry etching: Backside nitride

Use the Drytek Triode 384T plasma etcher. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions from the etch recipe, except for the etch time!

Use recipe "StdSiN" to etch the nitride layer. Etch time is 1 min to etch 300 nm of nitride.

13. Coating

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas;
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump;
- a soft bake at 95 °C for 90 seconds;
- an automatic edge bead removal with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating and follow the instructions for this equipment.

Use program "Co - 3012 - 1.4 μm".

14. Exposure

Expose "IMGAE5" of the "PIRANI" mask, with the job "DIE6x6_9IMG" and the correct exposure energy 150 mJ This results in the pattern for the nitride isolation.

15. Developing

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bakes at 115 °C for 90 seconds;
- developing with Shipley MF322 with a single puddle process;
- a hard bake at 100 °C for 90 seconds.

Use program "1 - Dev - SP".

16. Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope and check the line width and overlay. No resist residues are allowed.

17. Dry etching: Nitride on the backside

Use the Drytek Triode 384T plasma etcher. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions from the etch recipe, except for the etch time!

Use recipe "StdSiN" to etch the nitride layer. Etch time is 1 min to etch 300 nm of nitride.

18. Layer stripping: Photoresist

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier.

Use program 1: 1000 watts power and automatic endpoint detection + 2 min over etching.

19. Cleaning

Clean 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench "HNO3 99% (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Clean 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench "HNO3 69,5% 110 °C (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

20. PECVD TEOS oxide Deposition: Sacrificial layer deposition

Use the Novellus Concept One PECVD reactor. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!

Use recipe ".xxxnmteos" to deposit a 2000/1000/500 nm thick SiO2 layer on different wafers. The used deposition time was 71.8, 35.7 and 18.0 seconds respectively.

21. Measurement: Thickness of TEOS oxide

Use the Leitz MPV-SP measurement system for layer thickness measurement.

Use program: #50

22. LPCVD SiC deposition: 2.2 μm poly-SiC layer

Use furnace F3 in Class 10000 to deposit the SiC layer. Use progaram "1_ST_SiC_". Calculate deposition time according to the logbook to obtain a desired thickness.

23. Sheet resistance measurement

24. Dry etching: SiC on the backside

Use recipe "SiC-3mu" on Omega. Use a proper time to etch away the deposited SiC on the back of the wafer.

25. HMDS treatment
Use the EVG120 system to carry out a HMDS treatment before coating. Use recipe "1 - only - HMDS - on coater".

26. Manual coating

Use the manual coater to apply AZ-12XT photoresist on the wafers. The process consists of:
- spin coating of AZ-12-XT positive resist by using recipe "x-JR-4000-RPM-ebr";
- a soft bake by using "x-0-JR-softbake-110degree-180s-contact";
- a manual edge beam removal with acetone.

Always check the relative humidity (48 ± 2 %) in the room before coating and follow the instructions for this equipment.

27. Exposure

Expose "IMGAE7" of the "PIRANI" mask, with the job "DIE6x6_9IMG" and the correct exposure energy 330 mJ This results in the pattern for the micro-bridge structure.

28. Developing

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bakes at 115 °C for 90 seconds;
- developing with Shipley MF322 with a single puddle process;
- a hard bake at 100 °C for 90 seconds.

Use program "x - Henk - DEV - 12XTxxum - PB - HB" and an additional "x - Henk - DEV - 12XTxxum - noPB - noHB".

29. Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope and check the line width and overlay. No resist residues are allowed.

30. Dry etching: Patterning of the SiC layer

Use recipe "SiC-3mu" on Omega. Adjust the etch time depending on earlier poly-SiC etch experience in order to etch the SiC layer landing exactly on the sacrificial SiO2 layer, leaving only the anchor and the bridge structure.

31. Measurement: Thickness of remaining TEOS oxide

Use the Leitz MPV-SP measurement system to measure the remaining sacrificial. The layer should be slightly thinner than the previous thickness to make sure the SiC is totally etched away.

Use program: #50

32. Layer stripping: Photoresist

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier.

Use program 1: 1000 watts power and automatic endpoint detection + 2 min over etching.

Note: After this step, the thickness of the deposited SiC and the removed oxide can be measured with Dektak 8.The actual thickness of the SiC thickness can be obtained by subtracting thickness of the removed oxide from the total thickness.

33. Cleaning

Clean 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use the wet bench "HNO3 99% (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Clean 10 minutes in concentrated nitric acid at 110 °C. This will dissolve metal particles. Use wet bench "HNO3 69,5% 110 °C (Si)" and the carrier with the white dot;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use the Semitool "rinser/dryer" with the standard program, and the white carrier with a red dot.

34. LPCVD TEOS oxide deposition 300 nm: Electrical isolation layer for test structure
Use the LPCVD furnace E1 to deposit TEOS oxide. Follow the operation instruction from the manual when using the machine. It is not allowed to change the process conditions and time from the deposition recipe!

Use recipe "NEWTEOS1" and set the deposition time to 44 minutes to deposit a 300 nm thick TEOS layer.

35. Measurement: Oxide thickness
Use the Leitz MPV-SP measurement system for layer thickness measurement. Follow the operation instructions from the manual when using this equipment.

Use program: #39

36. Coating

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:
- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas;
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump;
- a soft bake at 95 °C for 90 seconds;
- an automatic edge bead removal with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating and follow the instructions for this equipment.

Use program "Co - Topo - 3027 - 4.0 μm".

37. Exposure

Expose "IMGAE02" of the "PIRANI" mask, with the job "DIE6x6_9IMG" and the correct exposure energy 450 mJ This results in the pattern for contact openings of test structures.

38. Developing

Use the developer station of the EVG120 system to develop the wafers. The process consists of:
- a post-exposure bakes at 115 °C for 90 seconds;
- developing with Shipley MF322 with a single puddle process;
- a hard bake at 100 °C for 90 seconds.

Use program " Dev - SP - 2".

39. Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope and check the line width and overlay. No resist residues are allowed.

40. Wet etching: Contact Openings

Moisten Rinse for 1 minute in wet bench "H_2O/Triton X-100 tbv BHF 1:7". Use the carrier with the blue dot. The bath contains 1 mL Triton X-100 per 5000 mL deionized water;

Etch Use wet bench "BHF 1:7 (SiO_2-ets)" at ambient temperature, and the carrier with the blue dot. The bath contains a buffered HF solution.

Time Etch until the windows on the front side are hydrophobic, plus an extra 30 seconds. Check the manual to calculate a proper etch time;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dots.

Note: Thickness of the oxide needs to be measured after etching to make sure no residual oxide on contact openings.

41. Layer stripping: Photoresist

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier.

Use program 1: 1000 watts power and automatic endpoint detection + 2 min over etching.

42. Wet etching: Oxide dip etching

Etch Use wet bench "0.55 % HF" at ambient temperature, and the carrier with the black dot;

Time 2 minutes;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dots.

Note: Metallization must be performed immediately after drying.

43. Sputtering: Metallization

Use recipe "AlSi-675nm-350C" or "Ti-500nm-400C" to deposit a 675 thick 99% with 1% or a 500 nm thick Ti.

44. Coating

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- a treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas;
- spin coating of Shipley SPR3012 positive resist, dispensed by a pump;
- a soft bake at 95 °C for 90 seconds;
- an automatic edge bead removal with a solvent.

Always check the relative humidity (48 ± 2 %) in the room before coating and follow the instructions for this equipment.

Use program "Co - Topo - 3027 - 4.0 μm".

45. Exposure

Expose "IMGAE05" of the "PIRANI" mask, with the job "DIE6x6_9IMG" and the correct exposure energy 450 mJ This results in the pattern for metal lines and pads.

46. Developing

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- a post-exposure bakes at 115 °C for 90 seconds;
- developing with Shipley MF322 with a single puddle process;
- a hard bake at 100 °C for 90 seconds.

Use program " Dev - SP - 2".

47. Inspection: Linewidth and overlay

Visually inspect the wafers through a microscope and check the line width and overlay. No resist residues are allowed.

48. Inspection: Linewidth and overlay

Etch Use wet bench "Al etch (35 °C)" and the carrier with the yellow dot. The bath contains PES at temperature 35 °C. A typical etch rate of Al is 170 nm/min;

Time 4 minutes 30 seconds;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Etch Use wet bench "Poly-Si etch" and the carrier with the green dot to remove the 1 % silicon.

Time 4 minutes 30 seconds;

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use "Avenger Ultra-Pure 6" rinser/dryer with the standard program, and the white carrier with a black dots.

As for the Ti metallization, use the Trikon Omega 201 plasma etcher with a sequence "Ti-500nm".

49. Layer stripping: Photoresist

Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper and use the quartz carrier.

Use program 1: 1000 watts power and automatic endpoint detection + 2 min over etching.

50. Cleaning: 100% HNO_3 (metal)

Cleaning 10 minutes in fuming nitric acid (Merck: HNO3 100% selectipur) at ambient temperature. Use wet bench "HNO_3 100% and the carrier with the red dot.

Rinse Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ;

Dry Use "Avenger Ultra-Pure 6" rinser/dryer with the standard program. Always use the special orange carrier.

51. Annealing

Use C4 furnace and program "ALLOY1" for this step.

52. Dicing: MEMS lab

53. Vapor HF: Structure releasing

Use the recipe 3 in the vapor HF tool to remove the sacrificial layer. Additional time for over etch is needed to ensure there is no SiO_2 residue left underneath the bridge structure.

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