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A Low-Power Oscillatory Feature Extraction Unit for Implantable Neural Interfaces

Hoda Yassin*, Arash Akhoundi†, El-Sayed Hasaneen*, Dante G. Muratore†
* Department of Electrical Engineering, Aswan University, Egypt
† Department of Microelectronics, Delft University of Technology, The Netherlands

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***Abstract*—Power and area efficient on-chip feature extraction is needed for future closed-loop neural interfaces. This paper presents a feature extraction unit for neural oscillatory synchrony that bypasses the phase extraction step to reduce hardware complexity. Instead, the sine and cosine of the phase are directly approximated from the real and imaginary components of the signal to calculate the phase-amplitude coupling (PAC) and phase locking value (PLV). The synthesized design achieves state-of-the-art performances at 43 nW/channel and 0.006 mm^2, while maintaining sufficient accuracy for seizure detection in epileptic patients.**

I. Introduction

Future neural interfaces will enable the treatment of neurological disorders for which a cure does not exist, such as epilepsy, treatment-resistant depression, and Parkinson's disease (PD) [1]–[5]. Typically, these disorders originate from abnormal synchronization in the neural activity, e.g., hyper-synchronization in the beta band of local field potentials for PD [6]. Neuromodulation is effective at disrupting this abnormal oscillatory behavior in the target neural network. However, open-loop neuromodulation can introduce unwanted side effects, e.g., the deterioration of non-motor symptoms in PD patients treated for essential tremor with deep-brain stimulation [7].

Closed-loop neuromodulation enables precise and personalized treatment, which can reduce adverse side effects. Neural features can be extracted from recorded neural activity to drive the stimulation parameters [8]–[12]. In order to enable fully implantable closed-loop neuromodulation devices, there is a need for low-power feature extraction near the sensor. The features can be directly used to drive the stimulation [9], [10] or as a pre-processing step to reduce the complexity of the neural signal classifier driving the stimulation [12]–[14].

Measuring the oscillatory synchrony of the neural activity is an effective way to provide closed-loop neuromodulation [15]. Statistical features such as the phase locking value (PLV) or the phase-amplitude coupling (PAC) are commonly used to quantify neural oscillatory synchrony. These features require calculating trigonometric expressions of the phase and magnitude information. Typically, the raw signal is divided into different spectral bands using a bandpass filterbank. A Hilbert transform is used to extract the real and imaginary parts of the signal for each band of interest. Then, the phase and magnitude are extracted to calculate the PAC and PLV features - see Fig. 1(a). Phase and magnitude can be extracted with high accuracy using CORDIC processors at the cost of power and area efficiency, making it unsuitable for high channel count devices [9]. A light phase extractor was proposed that approximates the phase based on a first-order Lagrange interpolation to reduce hardware complexity while introducing negligible accuracy loss [10]. The amplitude is extracted using the l_∞-norm approximation to reduce hardware complexity further. However, this approach still requires trigonometric lookup tables (LUTs) to calculate the sine and cosine of the phase (or phase difference) for the calculation of PAC (or PLV). To further reduce the power and area consumption, coarse approximation methods have been proposed that directly calculate PLV without extracting any phase information, but they suffer from lower accuracy and cannot extract PAC [16], [17].

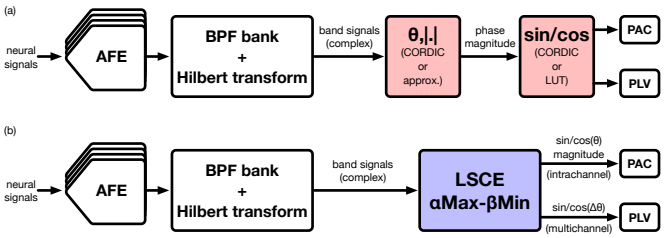

Fig. 1. System diagram of (a) a conventional PLV/PAC extraction unit and (b) the proposed PLV/PAC extraction unit with light sine and cosine extractor (LSCE) and αMax-βMin magnitude approximation.

This paper proposes a PLV/PAC unit that approximates the sine and cosine of the phase (or phase difference) directly from the complex signals, avoiding the complexity of phase extraction and trigonometric LUTs - see Fig. 1(b). The proposed light sine and cosine extractor (LSCE) and αMax-βMin magnitude approximation maintain competitive accuracy and achieve state-of-the-art power and area performance. Section II describes the proposed PLV/PAC architecture. Simulation results are presented in Section III, and conclusions are discussed in Section IV.

II. PLV/PAC Architecture

Phase locking value (PLV) and phase-amplitude coupling (PAC) are two commonly used features to quantify synchronization in neural oscillations. PLV measures the level of phase synchronization between two intra-band neural signals. PLV between two signals S_1 and S_2 is defined as:

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$$PLV = \frac{1}{N}\sqrt{\left(\sum_{i=1}^{N} sin\Delta\theta_i\right)^2 + \left(\sum_{i=1}^{N} cos\Delta\theta_i\right)^2} \quad (1)$$

$$\Delta\theta_i = \theta_{2,i} - \theta_{1,i} \quad (2)$$

where N is the number of samples of the averaging time window, and $\theta_{1,i}$ and $\theta_{2,i}$ are the instantaneous phases of S_1 and S_2 at the i^{th} sample.

Phase-amplitude coupling (PAC) is a type of cross-frequency coupling (CFC) in which the phase of a low-frequency oscillation modulates the amplitude of a high-frequency oscillation. Typically, PAC is observed with theta (3:8) Hz as the phase-modulating band and low gamma (40:70) Hz or high gamma (70:120) Hz as the amplitude-modulated band. One of the most widely used measures for PAC is the mean vector length (MVL). PAC based on the MVL is defined as:

$$PAC = \frac{1}{N}\sqrt{\left(\sum_{i=1}^{N} A_{m,i} sin\theta_{p,i}\right)^2 + \left(\sum_{i=1}^{N} A_{m,i} cos\theta_{p,i}\right)^2} \quad (3)$$

where N is the number of samples of the averaging time window, $\theta_{p,i}$ is the instantaneous phase of the low-frequency phase-modulating signal, and $A_{m,i}$ is the instantaneous magnitude of the high-frequency amplitude-modulated signal, at the i^{th} sample.

The similarity between PLV and PAC mathematical functions makes it possible to share resources and implement a single PLV/PAC extraction unit. In such a unit, the real and imaginary parts of the PLV input signals (RE_1, IM_1, RE_2, IM_2) as well as the real and imaginary parts of the PAC low-frequency phase-modulating signal (RE_p, IM_p) are applied to a shared phase extraction module to extract θ_1 and θ_2 for PLV (or θ_p for PAC). Also, the real and imaginary parts of the PAC high-frequency amplitude-modulated signal (RE_A, IM_A) are applied to a magnitude extraction module to extract A_m. Then a shared sin/cos extraction module is utilized to extract sin$\Delta\theta$/cos$\Delta\theta$ for PLV (or sinθ_p/cosθ_p for PAC). After that, shared accumulators and shifters are used to perform the averaging over a predefined time window. Finally, a magnitude extraction module is utilized to get the final value of PLV (or PAC). Typically, the sin/cos extraction module is a trigonometric look-up table (LUT) that extracts the sin/cos values of the input approximated phase. Here, we propose to approximate the sin/cos values directly from the real and imaginary inputs without having to extract the phase information first to reduce hardware complexity and improve power and area efficiency - see Fig 2. In our proposed PLV/PAC unit, the real and imaginary parts of the PAC low-frequency phase-modulating signal are applied directly to the light sine and cosine extractor (LSCE) to get sinθ_p/cosθ_p. Also, the real and imaginary parts of the PLV input signals are applied to a $\Delta\theta$ extractor module that generates the real and imaginary parts of a signal with phase equal to $\Delta\theta$.

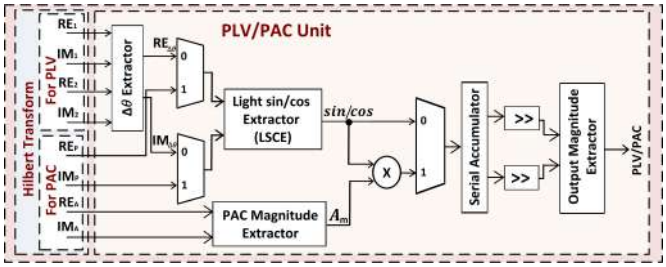

Fig. 2. Block diagram of the proposed PLV/PAC extraction unit.

This way, the output of the $\Delta\theta$ extractor module can also be applied to the LSCE to extract sin$\Delta\theta$/cos$\Delta\theta$. Since sine and cosine are generated serially from the light sine and cosine extractor (LSCE), the PAC multiplier is shared and a single serial accumulator is utilized instead of using two multipliers and accumulators. Each sub-block is described in detail below.

A. $\Delta\theta$ Extractor

Typically, the first step in PLV calculation is extracting the phase difference $\Delta\theta$ between the two input signals. Then, the sine and cosine of this phase are extracted using CORDIC or trigonometric LUT. In the proposed implementation, the PLV inputs are combined to generate a complex output signal with a phase equal to $\Delta\theta$. Then, the LSCE is utilized to extract sin$\Delta\theta$/cos$\Delta\theta$ from this complex number. For two input signals S_1 and S_2 with phases θ_1 and θ_2, the real and imaginary parts of a signal with phase $\Delta\theta = \theta_2 - \theta_1$ are given as:

$$RE_{\Delta\theta} = RE_1 \times RE_2 + IM_1 \times IM_2 \quad (4)$$

$$IM_{\Delta\theta} = IM_1 \times RE_2 - IM_2 \times IM_1 \quad (5)$$

where RE_1, IM_1 and RE_2, IM_2 are the real and imaginary parts of S_1 and S_2, respectively.

This extraction requires four multiplications and two additions, which are implemented serially with one multiplier and one adder running at four times the input sampling clock. The operating frequency matches the overall PAC/PLV unit that already operates at a clock frequency four times higher than the input sampling clock because the LSCE unit extract sine and cosine serially and it is shared among the PAC and PLV extraction. A leading zero block is used to detect small outputs of the $\Delta\theta$ extractor and multiply them by a constant to reduce truncation errors in the fixed-point hardware implementation.

B. Light Sine and Cosine Extractor

The sin/cos extraction module has the function of approximating sine and cosine of the phase directly from the real and imaginary inputs. The proposed LSCE unit implements a piece-wise approximation of the sin/cos functions directly. A trade-off between accuracy and hardware complexity exists and the optimal design can be studied based on the specific application. Here, we propose a two-step approximation that allows for resource sharing between the cosine and sine approximation blocks:

$$cos/sin = SN \times \begin{Bmatrix} CX & CX \leq 1 \\ 1 & CX > 1 \end{Bmatrix} \quad (6)$$

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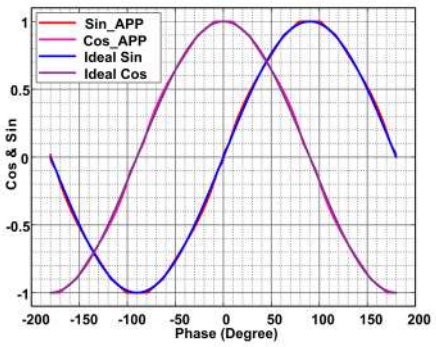

Fig. 3. Approximated sine and cosine

$$CX = \begin{cases} 0.5(X+0.1) & X & < & 0.1 \\ X & 0.1 & \leq X \leq & 0.9 \\ 0.5(X+0.9) & X & > & 0.9 \end{cases} \quad (7)$$

For the sine approximation

$$X = 1.27 - \frac{2|RE|}{2|IM| + 1.5|RE|} \quad (8)$$

$$SN = sign(IM) \quad (9)$$

For the cosine approximation

$$X = -0.1 + \frac{2|RE|}{|IM| + 1.5|RE|} \quad (10)$$

$$SN = sign(RE) \quad (11)$$

The block diagram of the proposed LSCE is shown in Fig. 4. The absolute values of the inputs RE and IM are determined using two absolute blocks. A multiplexer is used to control the sin/cos selection by determining the multiplication factor for IM in the fractional denominator. The division is calculated using a multiplier and a reciprocal lookup table (LUT). Referring to (8) and (10), if the fraction is considered without the nominator constant factor (2), the fraction is always smaller than one. In such a case, a leading zero detector associated with shifters can be used to reduce the input data range by 1 bit. The shifter for the numerator can account for the constant factor 2 in the equation. This results in the reciprocal LUT size being reduced by half. Another multiplexer is used to select the offset value of X for the sin/cos approximation. A comparator monitors X to determine the offset and the shifting factor for CX, and a second comparator monitors CX to limit the maximum output value to one. Finally, a sign detector is used to determine the output sign based on the IM (for sine approximation) or RE sign (for cosine approximation).

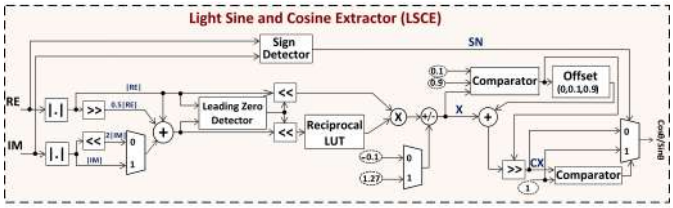

Fig. 4. LSCE schematic diagram

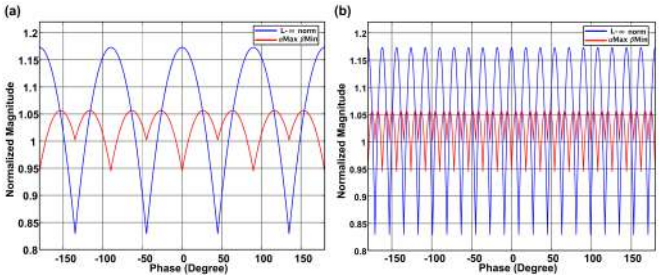

Fig. 5. Magnitude approximation error . (a) Self-phase, (b) Low frequency phase

C. αMax-βMin Magnitude Extractor

Typically, the l-∞ norm is used to approximate the magnitude of complex numbers. This approach is very efficient, but it comes at the cost of accuracy. The proposed implementation uses the αMax-βMin approximation algorithm instead [18]. In this algorithm, the magnitude is approximated as $A = 0.945(|Max| + 0.5|Min|)$, where $|Max|$ and $|Min|$ are the maximum and the minimum between the absolute values of real and imaginary parts, respectively. The constant factor 0.945 in the approximation does not introduce any necessary information for the PAC/PLV calculation and it can be omitted to reduce hardware complexity further.

Similar to the l-∞ norm, the error introduced by the αMax-βMin magnitude approximation as function of the phase of the complex number, appears as a high-frequency ripple (Fig. 5). However, the maximum error introduced by the αMax-βMin approximation (± 5.5%) is significantly lower than the one introduced by the l-∞ norm approximation (± 17%) - see Fig. 5(a). The MVL values calculated for a constant magnitude signal using its phase and approximated magnitude (for both algorithms) are approximately zero, proving that these errors do not affect the intra-band PAC state. Typically, the phase modulating signal is lower frequency than the amplitude modulating signal (e.g., the theta (3:8) Hz band is five times slower than the low gamma (40:70) Hz band). As a result, the effect of errors in the magnitude approximation on the coupling state is even less significant - see Fig. 5(b). This makes both approximation methods suitable for the magnitude extraction of the magnitude-modulated signal in the PAC extraction unit. However, for the output magnitude extractor needed for both PLV and PAC, the approximation error directly affects the overall accuracy.

A design option is to use the lower-power, lower-accuracy l-∞ norm approximation for the PAC magnitude extractor, and the higher-power, higher-accuracy αMax-βMin approximation for the output magnitude extractor. Instead, the proposed architecture shares the same αMax-βMin approximation for both magnitude extractors to reduce the overall area consumption. This improves the overall system accuracy and introduces a negligible power penalty.

III. Simulation Results

A Matlab hardware model with 10-bit input resolution is implemented to verify the functionality of the proposed PAC/PLV

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extraction unit using the CHB-MIT scalp EEG database [19]. This database is collected at the Children's Hospital Boston from pediatric subjects with intractable epileptic seizures. The database uses the international 10-20 system EEG electrode positions and a sampling frequency of 256 Hz with 16-bit resolution. The raw data is quantized to 10-bit resolution before the PAC/PLV extraction. Bandpass filters are used to split the required frequency bands. Theta (3:8) Hz is chosen as the PLV extraction band as well as the phase-modulating band for PAC. The amplitude-modulated band for PAC is set to low gamma (40:70) Hz. Then, the Hilbert transform is used to extract the real and imaginary parts of each of the signals. Finally, the real and imaginary parts are applied as inputs to the PAC/PLV unit model.

The PAC unit is evaluated on 12 hours recording of patient NO.1 using the FP1-F7 channel and a four-second time window. Over this interval, the extracted PAC has a maximum error of 3.6% and a standard deviation of 0.4% - see histogram in Fig. 6(a). For comparison, the extracted and the ideal PAC time series are plotted over a 400-second time interval with a 32-second seizure event (Fig. 6(b)). The extracted PAC feature approximates the ideal feature well, showing it can be used for seizure detection.

Similarly, the PLV unit is evaluated over the same recording with the same time window. The extracted PLV has a maximum error of 7.8% and a standard deviation of 2.25% - see histogram in Fig. 7(a). Again, a time series of the extracted and the ideal PLV over the same 400-second time interval is plotted (Fig. 7(b)), validating the suitability of the extracted feature in seizure detection.

A 16-channel VHDL implementation of the proposed

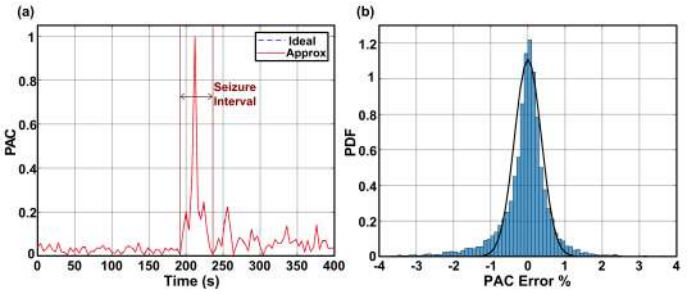

Fig. 6. PAC simulation results. (a) PAC percentage error PDF histogram. (b) Ideal and extracted PAC time series with seizure interval.

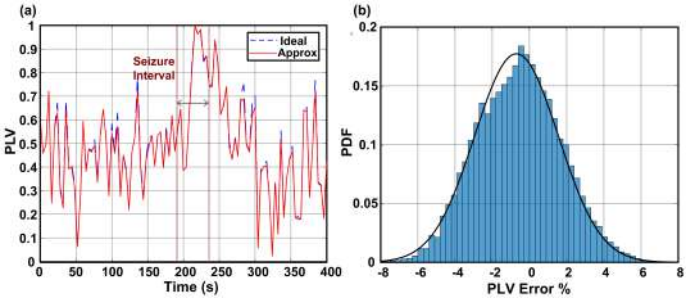

Fig. 7. PLV simulation results. (a) PLV percentage error PDF histogram. (b) Ideal and extracted PLV time series with seizure interval.

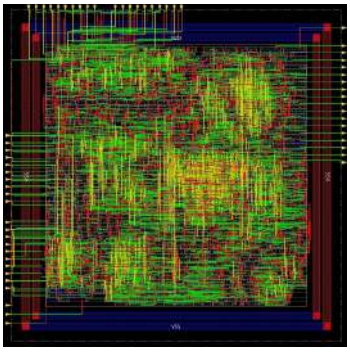

Fig. 8. Layout vie of the proposed PLV/PAC extraction unit.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART FE UNITS

Parameter	TBioCAS'19 [16]	JSSC'13 [9]	ISSCC'18 [20]	CICC'22 [10]	This Work
Process (nm)	180	130	130	65	40
Supply Voltage (V)	0.5	1.2	1.2	0.85	1.1
Area (mm^2)	0.05[a]	0.245[a]	0.632[b]	0.033[a]	0.006[c]
PLV/PAC channels	1 PLV	32 PLV	65 PAC/PLV	8 PAC/PLV	16 PAC/PLV
Total Power (μW)	0.015	400	200.4	9.7	0.689
Power/ch (μW)	0.015	12.5	3.1	1.2	0.043

[a] Estimated from reported total area and the percentage area occupied by the FE unit (without filters and memory).
[b] Estimated from reported total area and the SoC micrograph (without filters and memory).
[c] Reported after place and route.

PAC/PLV extraction unit described in the Matlab hardware model was synthesized, and placed and routed in a 40-nm CMOS technology (Fig. 8). The design operates at a frequency of 16 kHz, consumes a total power of 0.689 μW and occupies a core area of 0.006 mm^2. The design can operate at a maximum frequency of 500 MHz, which enables sharing it up to thousands of channels. The operating frequency scales linearly with the number of shared channels. As the channel sharing increases, the contribution of leakage power to the total power becomes negligible. For reference, the leakage power contributes 80% to the total power consumption in the current 16-channel implementation.

A comparison between the simulation results of the proposed PAC/PLV unit and the state of the art is given in Table I. This work achieves the best area and power performance over the PAC/PLV units, even when accounting for technology scaling. The work in [16] achieves better power per channel, but it cannot extract PAC values.

IV. Conclusion

This paper presents a feature extraction unit for neural oscillatory synchrony that bypasses the phase extraction step to reduce hardware complexity. Instead, the sine and cosine of the phase are directly approximated from the real and imaginary components of the signal to calculate the phase-amplitude coupling (PAC) and phase locking value (PLV). The proposed design achieves 43 nW/channel and a total area of 0.006 mm^2, while maintaining sufficient accuracy for seizure detection in epileptic patients. This is a power efficiency improvement of approximately 28x over the state of the art.

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